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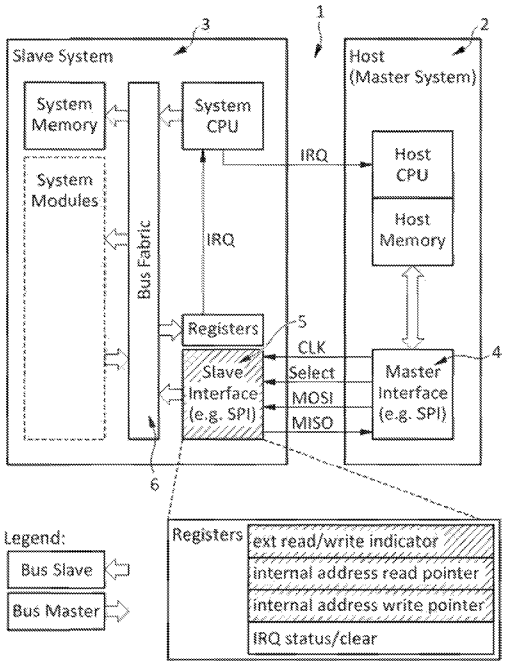

Fig. 1

(57) Abstract: The invention discloses a single communication interface between a master device and at least one slave device and a method with internal/external addressing mode using the single communication interface. The object to provide a leaner communication interface between a master and slave device which is more universal and independent from internal software changes will be solved by a single communication interface between a master device and at least one slave device, whereas the master device comprises a master interface and the slave device comprises a slave interface and a slave bus-system, whereas the slave interface is directly connected to the slave bus-system, wherein the master interface and the slave interface communicate on a packet based protocol by an internal and external addressing mode inside the slave interface, whereas the addressing mode, data direction transfer and data address location are coded by the packet based protocol inside a first 32-bit word of each transmission between the master device and slave device over the single communication interface.

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SINGLE COMMUNICATION INTERFACE AND A METHOD WITH INTERNAL/EXTERNAL ADDRESSING MODE

TECHNICAL FIELD

[0001] The invention discloses a single communication interface between a master device and at least one slave device and a method with internal/external addressing mode.

BACKGROUND

[0002] Master-Slave interfaces, like the serial peripheral interface (SPI), are communication interfaces between a master and one or more slave devices. The master device is responsible to initiate the communication. Normally, in a Master-Slave interface relation the Slave side is not able to initiate communication, or the Master side needs detailed memory location information.

[0003] If a slave device wants to transfer data, it must signalize its demand via an interrupt signal to the master and the master can initiate a transfer to read out the data from the slave device.

[0004] It is commonly known that Master-Slave interfaces can be half or full duplex.

[0005] Master-Slave interfaces are usually used for register access and data streaming.

[0006] For register access, the slave has implemented a register interface, where the master transmits the command (read or write) and the address. In case of write accesses, the master transmits the data and in case of write accesses the slave transmits the requested data.

[0007] For streaming scenarios no addressing is used and application specific packets are transmitted.

[0008] Complex slave devices, like embedded systems with integrated processors, require a combination of two different modes: In a first mode the master wants to access the internal register of the slave device (e.g. for debugging purpose). The word size is 32 bits and 32 bits wide addresses are used for byte addressing. In a second mode, the master and slave want to send application specific messages, where no addressing is needed. In both modes, the communication should be energy efficient. Thus, the integrated processor of the slave device should be involved in the communication as little as possible.

[0009] For common implementations used today, two main problems arise from these requirements: Firstly, the slave device can usually not initiate communication when it wants to send a message. As hardware protocols like SPI or I2C do usually not cater for this need, additional measures are required to give the slave device the opportunity to initiate a communication sequence. Secondly, for debug purposes the master device obviously needs to know the internals of the slave device, usually by having access to an address map. When just performing communication through messages, which often covers the practical use cases in the field, it is usually not desirable that the master device needs to know the message buffer memory locations, as they also might be changing within the available memory regions depending on software needs. It is therefore desirable to give the slave device the opportunity to configure the hardware interface in a way to automatically direct the messages to a proper location. This would make the communication interface leaner, more universal and independent from internal software changes. So the master device could still talk to the slave device but without the need to know about possible changes of the buffer locations e.g. through updates or different use cases.

SUMMARY

[0010] The object of the invention will be solved by a single communication interface between a master device and at least one slave device, whereas the master device comprises a master interface and the slave device comprises a slave interface and a slave bus-system, whereas the slave interface is directly connected to the slave bus-system, wherein the master interface and the slave interface communicate on a packet based protocol over the single communication interface by an internal and external addressing mode inside the slave interface, whereas the addressing mode, data direction transfer and data address location are coded by the packet based protocol inside a first 32-bit word of each transmission between the master device and slave device over the single communication interface.

[0011] The described interface connects two systems, where one system is the master and the other system is the slave. It is advantageous that the slave device has its own slave interface like a serial peripheral interface (SPI). Only the slave interface is directly connected to the bus system of the slave device. It can access all registers and memories of the slave device. It is no longer necessary that the master device has to know about the internals of the slave device or the message buffer memory locations inside the slave device.

[0012] The inventive single communication interface comprises registers like an IRQ

status/clear register, an external addressing read/write indicator, an internal address read pointer and an internal address write pointer. This allows that a single interface can be used for internal and external addressing mode in an energy efficient way. The external addressing mode is used for register accesses, where the master device transmits the address and the direction (read or write). The internal addressing mode is used for application data, where the master device transmits only the direction (master to slave or slave to master transfer). There is only a minimal communication overhead: Only the addressing mode, the direction and the address have to be coded in one single 32-bit word.

[0013] Hence, in a preferred embodiment of the inventive single communication interface, a first significant bit of the 32-bit word decodes the addressing mode. A second significant bit of the 32-bit word decodes the data direction transfer. Bits 29 down to 0 in the 32-bit command word represent the address for the external addressing mode access, hence the bits 31 down to 2 of the internal slave device bus. The Bits 1 down to 0 can be omitted, as only word-aligned access are permitted, hence the lower 2 bits will always be zero and do not need to be transmitted by the master device.

[0014] In another preferred embodiment, the communication interface is implemented in a fully embedded system-on-chip. So it is not bound to external communication interfaces.

[0015] The object of the invention will also be solved by a method for communicating between a master device and at least one slave device using the inventive single communication interface, wherein each communication transfer is initiated by the master device and the master interface and the slave interface communicate on a packet based protocol initiating an internal and external addressing mode, whereas the slave interface manages autonomously an addressing to a slave system memory via a slave bus-system to which the slave interface is connected to.

[0016] All communication transfers are initiated by the master device. The slave device must accept all transfers from the master device. Internally to the slave device, the slave interface has direct memory access via the bus-system. Externally the slave interface supports burst modes with an auto address incrementation for consecutive multiple word accesses. Internally, these are translated into single bus transfers, as the external interface is about 1 to 2 orders of magnitude slower than the internal bus and excessive blocking times would result from initiating the bursts also internally.

[0017] In a preferred embodiment of the inventive method, each communication transfer starts with a 32-bit command word comprising two most significant bits

representing the command of addressing mode and direction and a remaining 30-bits sequence representing a word address for external addressing mode access. This has the advantageous effect that there is only a minimal communication overhead – only the addressing mode, the direction and the address have to be coded in one single 32-bit word at the beginning of each communication transfer.

[0018] In another preferred embodiment, four communication modes are supported by the 2-bit command word part of the 32-bit command word: "01" indicates an internal addressing mode read request meaning that the slave device transmits a message to the master; "11" indicates an internal addressing mode write request meaning that the master device transmits a message to the slave device; "00" indicates external addressing mode read request meaning that the master does a read access on a slave bus-system of the slave device with a given address; "01" indicates external addressing mode write request meaning that the master does a write access on the slave bus-system of the slave device with a given address. The external addressing mode is used for register accesses, where the master device transmits the address and the direction (read or write).

[0019] The internal addressing mode is used for application data, where the master device transmits only the direction (master to slave or slave to master).

[0020] In a further preferred embodiment of the inventive method, the slave device raises an interrupt if the slave device intents to transfer data to the master device, whereas the master device starts an internal addressing mode read request. This has the positive effect that the master device will be informed about new data from the slave device and does not need to poll a status register or the "slave-to-master data channel".

[0021] In an embodiment of the inventive method, an asynchronous communication is used. This has the positive effect that no specific timing is required for the communication between the master device and slave device.

[0022] Summarizing, the inventive single communication interface between a master device and at least one slave device and the inventive method have the advantages that due to the asynchronous communication, no specific timing is required. Furthermore, there exists non-blocking, which means that another party can continue communication until a ready/request IRQ is received. For the master device or the receiver device the message storage location is irrelevant, it just requests the needed content. With the inventive single communication interface a just-in-time handling can be realized, because no busy waiting/polling for readiness/requests is necessary. Another advantage is that any overlay protocol can be implemented in the packets, so no fixed length is needed. For the

communication a very compact command structure is used, two bits for command and 30 bit for the word address. And last but not least, only a minimal control overhead exists if direct memory access (DMA) like incremental bursts are supported.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] The invention will be described in more detail using exemplary embodiments shown in the drawings.

[0024] Fig. 1 System Example with SPI master slave interface;

[0025] Fig. 2 Command word structure.

LIST OF REFERENCE SIGNS

1 single communication interface
2 master device
3 slave device
4 master interface
5 slave interface
6 slave bus-system

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0026] Fig. 1 shows the inventive single communication interface 1 which connects two systems, where one system is the master 2 and the other is the slave 3. The slave device 3 has its own slave interface 5 like a serial peripheral interface (SPI). Only the slave interface 5 is directly connected to the bus system 6 of the slave device 3. It can access all registers and memories of the slave device 3. It is no longer necessary that the master device 2 has to know about the internals of the slave device 3 or the message buffer memory locations inside the slave device 3.

[0027] The inventive single communication interface 1 comprises registers like an IRQ status/clear register, an external addressing read/write indicator, an internal address read pointer and an internal address write pointer. This allows that a single interface 1 can be used for internal and external addressing mode in an energy efficient way. The external addressing mode is used for register accesses, where the master device transmits the address and the direction (read or write). The internal addressing mode is used for application data,

where the master device 2 transmits only the direction (master to slave or slave to master transfer). There is only a minimal communication overhead: Only the addressing mode, the direction and the address have to be coded in one single 32-bit word.

[0028] Each communication transfer starts with a 32-bit command word comprising two most significant bits representing the command of addressing mode and direction and a remaining 30-bits sequence representing a word address for external addressing mode access, this is shown in Fig. 2. This has the advantageous effect that there is only a minimal communication overhead – only the addressing mode, the direction and the address have to be coded in one single 32-bit word at the beginning of each communication transfer.

[0029] Four communication modes are supported by the 2-bit command word part of the 32-bit command word: “01” indicates an internal addressing mode read request meaning that the slave device 3 transmits a message to the master 2; “11” indicates an internal addressing mode write request meaning that the master device 2 transmits a message to the slave device 3; “00” indicates external addressing mode read request meaning that the master 2 does a read access on a slave bus-system 6 of the slave device 3 with a given address; “01” indicates external addressing mode write request meaning that the master 2 does a write access on the slave bus-system 6 of the slave device 3 with a given address. The external addressing mode is used for register accesses, where the master device 2 transmits the address and the direction (read or write).

CLAIMS

1. A single communication interface between a master device and at least one slave device, whereas the master device comprises a master interface and the slave device comprises a slave interface and a slave bus-system, whereas the slave interface is directly connected to the slave bus-system, wherein the master interface and the slave interface communicate on a packet based protocol with an internal and external addressing mode inside the slave interface, whereas the addressing mode, data direction transfer and data address location are coded by the packet based protocol inside a first 32-bit word of each transmission between master device and slave device.

2. The single communication interface between a master device and at least one slave device according to claim 1, wherein a first significant bit of the 32-bit word decodes the addressing mode.

3. The single communication interface between a master device and at least one slave device according to claim 1, wherein a second significant bit of the 32-bit word decodes the data direction transfer.

4. The single communication interface between a master device and at least one slave device according to any one of claims 1 to 3, wherein bits 29 down to 0 of the 32-bit command word represents the address for the external addressing mode access.

5. The single communication interface between a master device and at least one slave device according to any one of claims 1 to 4, wherein the communication interface is implemented in a fully embedded system-on-chip.

6. A method for communicating between a master device and at least one slave device using the single communication interface according to any one of claims 1 to 5, wherein each communication transfer is initiated by the master device and the master interface and the slave interface communicate on a packet based protocol initiating an internal and external addressing mode, whereas the slave interface manages autonomously an addressing to a slave system memory via a slave bus-system to which the slave interface is connected to.

7. The method for communicating between a master device and at least one slave device according to claim 6, wherein each communication transfer starts with a 32-bit command word comprising two most significant bits representing the command of addressing mode and direction and remaining 30-bits representing a word address for external addressing mode access.

8. The method for communicating between a master device and at least one slave device according to claim 7, wherein four communication modes are supported by the 2-bit command word part: “01” internal addressing mode read request meaning the slave device transmits a message to the master; “11” internal addressing mode write request meaning the master device transmits a message to the slave device; “00” external addressing mode read request meaning the master does a read access on a slave bus-system of the slave device with a given address; “01” external addressing mode write request meaning the master does a write access on the slave bus-system of the slave device with a given address.

9. The method for communicating between a master device and at least one slave device according to claim 8, wherein the slave device raises an interrupt if the slave device intents to transfer data to the master device, whereas the master device starts an internal addressing mode read request.

10. The method for communicating between a master device and at least one slave device according to any one of claims 6 to 9, wherein an asynchronous communication is used.

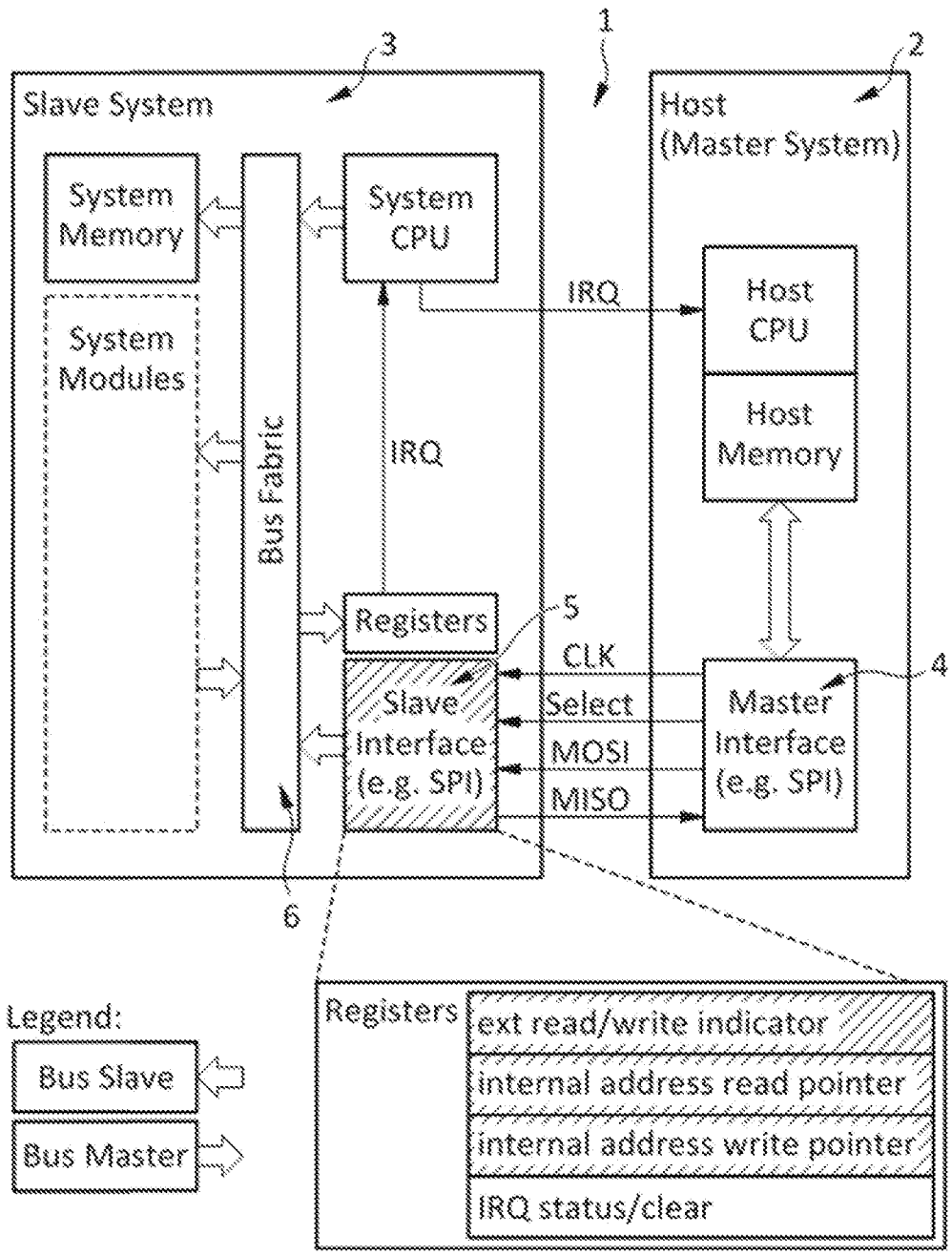

Fig. 1

int_addr	wr	addr[31]	..	..	..	addr[2]
31	30	29	..	..	..	0

Fig. 2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2019/075725

A. CLASSIFICATION OF SUBJECT MATTER

G06F 13/42(2006.01)i; H04L 12/40(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F; H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS; CNTXT; CNKI; VEN; WOTXT; EPTXT; USTXT: slave, master, internal, external, address, SPI, mode, interface

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	CN 105468563 A (HANGZHOU SHILAN HOLDINGS CO., LTD.) 06 April 2016 (2016-04-06) description, paragraphs 28-191 and figure 1	1-10
Y	CN 1744068 A (BEIJING VIMICRO CO., LTD.) 08 March 2006 (2006-03-08) description, pages 3-4 and figure 4	1-10
A	US 7076584 B2 (FREESCALE SEMICONDUCTOR INC.) 11 July 2006 (2006-07-11) the whole document	1-10

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
09 August 2019	**16 August 2019**
Name and mailing address of the ISA/CN **National Intellectual Property Administration, PRC** **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing** **100088** **China** Facsimile No. **(86-10)62019451**	Authorized officer **LI,Qian** Telephone No. **86-(010)-62089374**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
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Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
CN 105468563 A	06 April 2016	CN 105468563 B	01 June 2018
CN 1744068 A	08 March 2006	CN 1744068 B	21 April 2010
US 7076584 B2	11 July 2006	US 2004225862 A1	11 November 2004