

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
11 June 2009 (11.06.2009)

PCT

(10) International Publication Number
WO 2009/073403 A1

(51) International Patent Classification:
G02B 6/132 (2006.01)

(21) International Application Number:
PCT/US2008/084308

(22) International Filing Date:
21 November 2008 (21.11.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/991,292 30 November 2007 (30.11.2007) US

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

Published:

- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

(54) Title: METHOD FOR MAKING OPTICAL WAVEGUIDES

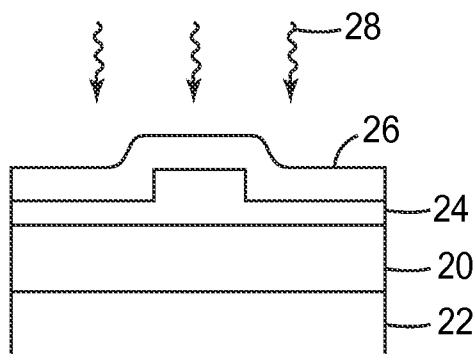


FIG. 2e

(57) Abstract: A method for making a waveguide comprises (a) providing a waveguide structure comprising a substrate (22), a lower cladding (20) layer on the substrate, and a core layer (24) comprising silicon nitride, amorphous silicon, or amorphous silicon-germanium alloy on the lower cladding layer; (b) patterning the core layer; and (c) annealing (28) the waveguide structure.

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METHOD FOR MAKING OPTICAL WAVEGUIDES

FIELD

5 This invention relates to a method for making optical waveguides. In another aspect, this invention relates to silicon nitride-based and amorphous silicon-based optical waveguides.

BACKGROUND

10 Optical waveguides are commonly utilized in optical communication applications. Optical waveguides usually include a core layer sandwiched between a lower cladding layer and an upper cladding layer. Typically, the core layer has a higher refractive index than the lower and upper cladding layers.

 Traditionally, silica was used to form the core and the cladding layers, but the
15 core layer was doped (for example, with germanium, phosphorous, or titanium) in order to increase its refractive index relative to the cladding layers. In recent years, there has been increasing focus on fabricating optical waveguides having greater index contrast between the core layer and the cladding layers by using plasma enhanced chemical vapor deposition (PECVD)-grown silicon nitride or silicon oxynitride core
20 layers.

 However, high optical losses (for example, 5 – 10 dB/cm) are often observed in PECVD-grown silicon nitride and silicon oxynitride core layers at infrared (IR) wavelengths used in optical communication applications. It is believed that the losses originate from Si-H, N-H and –OH bonds that are incorporated into the core layer
25 during PECVD from silane, nitrous oxide, and/or ammonia gaseous precursors. It is therefore necessary to anneal the core layer at high temperatures in order to remove the Si-H, N-H and –OH bonds in the core layer.

 Silicon nitride-based and silicon oxynitride-based ridge waveguides are thus typically fabricated using the sequence illustrated in **Figs. 1(a) – 1(e)**. First, as shown
30 in **Fig. 1(a)**, a lower cladding layer **10** (for example, a silicon dioxide lower cladding layer) is deposited on a silicon wafer substrate **12**. Then, as shown in **Fig. 1(b)**, the silicon nitride or silicon oxynitride core layer **14** is deposited on the lower cladding layer **10** using PECVD. Next, as depicted in **Fig. 1(c)**, the structure is annealed **18** and

then, as shown in **Fig. 1 (d)**, the core layer **14** is patterned. Finally, as shown in **Fig. 1(e)**, an upper cladding layer **16** (for example, a silicon dioxide upper cladding layer) is deposited on the annealed patterned core layer **14**.

Silicon oxynitride core layers having a refractive index above about 1.6, however, can develop cracks as a result of high temperature annealing (for example, annealing at about 1000 °C or above). The cracking is due to the differing thermal expansion coefficients of the silicon oxynitride core layer, the cladding layers, and the silicon wafer. The differing thermal expansion coefficients lead to unacceptably high values of induced tensile stress within the layers. The cracking problem can be even worse with silicon nitride because silicon nitride films have higher tensile stress than silicon oxynitride films.

SUMMARY

In view of the foregoing, we recognize that there is a need for a method for making low optical loss ridge waveguides with core layers having a refractive index above about 1.6.

Briefly, in one aspect, the present invention provides a method for making a waveguide. The method comprises (a) providing a waveguide structure comprising a substrate, a lower cladding layer on the substrate, and a core layer comprising silicon nitride, amorphous silicon, or amorphous silicon-germanium alloy on the lower cladding layer, (b) patterning the core layer, and (c) annealing the waveguide structure. Preferably, the method further comprises depositing an upper cladding layer over the core layer after patterning the core layer, but before annealing the waveguide structure.

Surprisingly, the method of the present inventions allows for effective and crack-free annealing of the silicon nitride, amorphous silicon, or amorphous silicon-germanium alloy core layer at reduced temperatures and in less time relative to conventional ridge waveguide fabrication methods in which annealing is carried out prior to patterning of the core layer. The reduced annealing temperatures of the method of the invention can reduce stress compared to high temperature annealing and thereby improve device quality.

In another aspect, the present invention provides a method for making a ring resonator. The method comprises (a) providing a waveguide structure comprising a substrate, a lower cladding layer on the substrate, and a core layer comprising silicon nitride, amorphous silicon, or amorphous silicon-germanium alloy on the lower
5 cladding layer, (b) patterning the core layer, (c) depositing an upper cladding layer on the core layer to provide a sandwich waveguide structure, (d) annealing the sandwich waveguide structure, (e) depositing a ring resonator layer comprising silicon nitride, amorphous silicon, or amorphous silicon-germanium alloy on the annealed sandwich waveguide structure, and (f) patterning a ring into the ring resonator layer.

10 In yet another aspect, the present invention provides a ridge or channel waveguide comprising a patterned core layer on a silicon dioxide lower cladding layer; wherein the core layer comprises silicon nitride, amorphous silicon, or amorphous silicon-germanium alloy, has a refractive index between about 1.6 and about 4.6, and is essentially crack-free.

15 As used herein:

“silicon dioxide” means SiO_2 , optionally doped with elements such as boron, phosphorous, fluorine, titanium, aluminum, zirconium, and the like, and combinations thereof;

20 “silicon nitride” includes Si_3N_4 and silicon oxynitride compounds represented by the formula SiO_xN_y , wherein $0 < y < \frac{4}{3}$ and $0 < x < 2$; and

“essentially crack-free” means that the core layer has no cracks within a 4 inch (10 cm) diameter wafer as observed using optical microscopy.

DESCRIPTION OF DRAWINGS

25 **Figs. 1 (a), (b), (c), (d), and (e)** illustrate a conventional method for making a ridge waveguide using schematic side views.

Figs. 2 (a), (b), (c), (d), and (e) illustrate a method for making a ridge waveguide of the invention using schematic side views.

30 **Figs. 3 (a), (b), (c), (d), and (e)** illustrate a method for making a channel waveguide of the invention using schematic side views.

Fig. 4 is a plot of Received Power versus Wavelength for the ring resonator of Example 1.

Fig. 5 is a plot of Received Power versus Wavelength for the ring resonator of Comparative Example 1.

DETAILED DESCRIPTION

5 Waveguides of the invention can be fabricated using the methods illustrated in **Figs. 2(a) – 2(e)** and **Figs. 3(a) – 3(e)**. The method illustrated in **Figs. 2(a) – 2(e)** illustrates making a ridge waveguide. First, as shown in **Fig. 2(a)**, a lower cladding layer **20** (for example, a silicon dioxide lower cladding layer) is deposited on a substrate **22** (for example, a silicon wafer substrate). Then, as shown in **Fig. 2(b)**, a silicon nitride or amorphous silicon core layer **24** is deposited on the lower cladding layer **20**. Next, as shown in **Fig. 2(c)**, the core layer **24** is patterned with a ridge pattern. Then, as shown in **Fig. 2(d)**, an upper cladding layer **26** (for example, a silicon dioxide upper cladding layer) is deposited on the patterned core layer **24**. Finally, as depicted in **Fig. 2(e)**, the waveguide is annealed **28**. **Figs. 3(a) – 3(e)** illustrate making a channel waveguide. The method for making a channel waveguide is essentially the same as the method for making a ridge waveguide except the core layer is etched completely through around the channel **34** (as shown in **Fig. 3(c)**).

Waveguides of the invention include a waveguide structure supported on a substrate. The substrate usually consists of a commercially available material such as silicon, sapphire or fused quartz. Preferably, the substrate is a silicon wafer.

The waveguide structure comprises a high index silicon nitride, amorphous silicon, or amorphous silicon-germanium alloy core layer on a low refractive index lower cladding layer (that is, a cladding layer comprising a material having a refractive index lower than the refractive index of the core layer). Preferably, the waveguide structure is a sandwich waveguide structure in which the core layer is sandwiched between a low refractive index lower cladding layer and a low refractive index upper cladding.

The lower cladding layer comprises a relatively low refractive index amorphous material such as, for example, silicon dioxide, zirconium oxide, aluminum oxide, magnesium fluoride, low index doped silica (for example, silica doped with boron, phosphorous, or fluorine), or the like. Preferably, the lower cladding layer comprises silicon dioxide. Preferably, the lower cladding layer has a refractive index

between about 1.3 and about 1.5. The lower cladding layer can be deposited on the substrate by methods known in the art. For example, the lower cladding layer can be deposited using a chemical vapor deposition (CVD) process such as PECVD, atmospheric pressure chemical vapor deposition (APCVD), or low pressure chemical vapor deposition (LPCVD); physical vapor deposition (PVD) processes such as sputtering, evaporation, electron beam evaporation, molecular beam epitaxy and pulsed laser deposition; flame hydrolysis deposition (FHD); and sol-gel processes. Preferably, the lower cladding layer is deposited using PECVD.

Typically, the lower cladding layer has a thickness between about 0.5 μm and about 50 μm (preferably, between about 0.5 and about 3 μm).

The core layer comprises silicon nitride, amorphous silicon, or amorphous silicon-germanium alloy (preferably, silicon nitride or amorphous silicon; more preferably, silicon nitride). When the core layer comprises silicon nitride, the nitrogen content of the core layer is typically greater than about 20 mol %. Preferably, the core layer has a refractive index between about 1.6 and 4.6; more preferably, between about 1.6 and about 3.8; most preferably, between about 1.6 and about 2.0. The core layer can be deposited on the lower cladding layer using any of the deposition techniques mentioned above. Preferably, the core layer is deposited using PECVD.

Typically, the core layer has a thickness between about 0.1 μm and about 2 μm (preferably, between about 0.1 μm and about 1 μm).

The core layer can be patterned using patterning techniques known in the art such as, for example by photolithography and reactive ion etching (RIE) or by ion beam etching (preferably, by photolithography and RIE). Typically, a ridge or channel will have a width between about 0.5 μm and about 7 μm .

After the core layer has been patterned, an optional upper cladding layer can be deposited on it. The upper cladding layer comprises a relatively low refractive index amorphous material such as, for example, silicon dioxide, zirconium oxide, aluminum oxide, magnesium fluoride, low index doped silica (for example, silica doped with boron, phosphorous, or fluorine), or the like. Preferably, the upper cladding layer comprises silicon dioxide. Preferably, the lower cladding layer has a refractive index between about 1.3 and about 1.5. The lower cladding layer can be deposited on the substrate by methods known in the art such as those mentioned above. Typically, the

upper cladding layer has a thickness between about 0.05 μm and about 50 μm
(preferably, between about 0.05 μm and about 3 μm

The waveguide structure can be annealed after the core layer has been
patterned (or after the upper cladding layer has been deposited if the waveguide
structure has a sandwich structure). The method of the invention allows for annealing
at lower temperatures than conventional processes and therefore provides waveguides
with less stress-induced birefringence. For example, the sandwich waveguide can be
effectively annealed at a temperature between about 600°C and about 1000°C
(preferably, between about 700 °C and about 900 °C). The method of invention also
allows for reduced annealing times and thus reduced production cost. Preferably, the
waveguide is annealed for at least about 1 hour (preferably, for about 2 hours to about
4 hours). The resulting waveguide is essentially crack-free and exhibits low optical
loss at wavelengths used in optical communication applications. Preferably, the
waveguides exhibit an optical loss of less than about 0.15 dB/cm at wavelengths
between about 1310 nm and about 1565 nm (more preferably, less than about 0.1
dB/cm).

Waveguides of the invention can be used to fabricate a variety of devices for
optical communications applications such as, for example, splitters, switches, optical
filters, directional couplers, and the like, or for optical biosensors.

EXAMPLES

Objects and advantages of this invention are further illustrated by the following
examples, but the particular materials and amounts thereof recited in these examples, as
well as other conditions and details, should not be construed to unduly limit this
invention.

Example 1: Ring Resonator with SiO₂/SiN ridge/SiO₂ sandwich (with annealing)

The invention is demonstrated by fabrication of a vertically coupled ring
resonator with a 100 μm diameter. The ring resonator was fabricated as follows.

A 3 μm thick borophosphosilicate glass (BPSG) lower cladding layer with a
refractive index of 1.46 was deposited on a 0.5 mm Si wafer (100) (Si wafer was
obtained from Montco Silicon Technologies, Inc., Spring City, PA) by plasma

enhanced chemical vapor deposition (PECVD, Model PlasmaLabTM System100 available from Oxford Instruments, Yatton, UK) using the following parameters listed in Table 1.

5 Table1. Conditions used for depositing BPSG low cladding layer

Reactant/Condition:	Value:
SiH ₄	17 sccm
B ₂ H ₆	3.5 sccm
PH ₃	1.8 sccm
N ₂ O	1500 sccm
N ₂	600 sccm
RF power	130 W
Pressure	2000 mTorr
Temperature	350°C

After the BPSG layer was formed on the Si wafer, the sample was heated to 1080°C in a furnace with a ramp rate of 5 °C/min and held at that temperature for approximately 4 hours to allow the BPSG to reflow. After the heat treatment, a 250
 10 nm thick SiN core layer was deposited on the BPSG lower cladding layer by PECVD using the following parameters described in Table 2.

Table 2. Conditions used for depositing SiN core layer

Reactant/Condition:	Value:
SiH ₄	400 sccm
NH ₃	20 sccm
N ₂	600 sccm
Pressure	650 mTorr
Temperature	350°C
High frequency (HF) power	20W
Low frequency (LF) power	20W

The refractive index of the SiN core layer was measured using a Metricon Model 2010 Prism Coupler (Metricon Corporation, Pennington, NJ) and was found to be 2.

After deposition of the SiN core layer was completed, a positive photoresist, referred to hereinafter as "PR" (Shipley PR1813 available from Electronic Materials Inc., Spartanburg, SC) was coated on the SiN core layer by spin coating. The PR layer was patterned using a waveguide pattern mask and standard photolithography techniques. An etch process was then performed to etch the waveguide core layer and form ridge waveguide cores. A reactive ion etch (RIE, Model PlasmaLabTM System100 available from Oxford Instruments, Yatton, UK) was conducted according to the following conditions described in Table 3. The waveguide was nominally 2.5 μm in width and the etch depth was 50 to 200 nm.

Table 3. Materials/Conditions used for Reactive Ion Etching

Reactant/Condition:	Value:
C ₄ F ₈	10-50 sccm
O ₂	0.5-5 sccm
RF power	50-100W
Inductive Coupling Plasma (ICP) power	1000-2000 W
Pressure	3-10 mTorr

Following the ion etching, a 100 nm thick SiO₂ upper cladding layer was deposited on the patterned waveguides, forming the SiO₂/SiN ridge/SiO₂ sandwich waveguide structure. The SiO₂ upper cladding layer was deposited using PECVD according to the following conditions described in Table 4.

Table 4. Conditions used for depositing 100nm SiO₂ layer

Reactant/Condition:	Value:
SiH ₄	15 sccm
N ₂ O	1500 sccm
N ₂	600 sccm
HF power	104 W

LF power	30W
Pressure	400 mTorr
Temperature	Temperature: 350°C

The resulting sample was placed in a furnace and annealed in air at 800°C for 5h using a heating and cooling rate of 2°C/min. The wave guide was crack-free as observed by optical microscopy.

After annealing the sandwich waveguide, a ring resonator was fabricated on the upper cladding layer. This was done by depositing a 250 nm thick SiN layer on the SiO₂/SiN ridge/SiO₂ sandwich waveguide, using identical deposition parameters as described in Table 2. A 100 µm diameter ring was defined by standard photolithography process using a ring mask followed by reactive ion etching (RIE), using identical etching parameters as described in Table 3. After etching of the PR, the individual chip was cut and polished for optical measurements. Optical measurements were obtained using a Nuphoton NP2500-ASE (Nuphoton Technologies, Inc., Murrieta, CA) as the optical source and a JDS Uniphase PS3 PDL Multimeter (JDS Uniphase Corporation, Milpitas, CA) as the detector. A plot of Received Power versus Wavelength for the ring resonator of the 100 µm ring is shown in **Fig. 4**. A relatively flat curve was observed. There was minimal absorption at wavelengths between 1495 nm and 1555 nm.

Comparative Example 1: Ring resonator of SiO₂/SiN ridge/SiO₂ sandwich (no annealing)

Another sample was fabricated using the process described in Example 1 except that the waveguide was not annealed. A plot of Received Power versus Wavelength for the ring resonator of the 100 µm ring is shown in **Fig. 5**. Strong waveguide absorption at wavelengths between 1495 nm and 1555 nm was observed for this sample due to absorption of N-H and Si-H vibrational overtones.

Comparative Example 2: Fabrication of planar SiON core layer (no pattern; annealed)

700 nm thick SiON core layers were deposited on several Si wafers by PECVD using the following parameters described in Table 5.

Table 5. Conditions used for depositing SiON layer

Reactant/Condition:	Value:
SiH ₄	400 sccm
NH ₃	20 sccm
N ₂ O	80 sccm
N ₂	600 sccm
Pressure	1000 mTorr
HF power	60 W
Temperature	350°C

5

The refractive index of the SiN core layer was measured using a Metricon Model 2010 Prism Coupler and was found to be 1.78.

SiON core layers of Comparative Example 2 were annealed in a furnace at a ramp rate of 2 °C/min at 600°C, 700°C, 800°C, 900°C and 1000°C for 30 minutes.

10

Examples 2 and 3: Fabrication of ridge SiON core layers (patterned; annealed)

Several of the Si wafers coated with 700 nm thick layer of SiON coatings prepared as described in Comparative Example 2 were coated with a PR, and the PR layer was patterned using a waveguide pattern mask and standard photolithography techniques. A reactive ion etch was conducted according to the conditions described in Table 3 to form ridge waveguide cores (100 µm ridge in Example 2; 50 µm ridge in Example 3).

15

SiON core layers of Examples 2 and 3 were annealed in a furnace at a ramp rate of 2 °C/min at 600°C, 700°C, 800°C, 900°C and 1000°C for 30 minutes. The SiON core layers were crack-free when observed using optical microscopy.

20

Comparative Examples 3: Fabrication of planar SiON core layer (no pattern; no annealing)

Comparative Example 3 samples were prepared in the same manner as Comparative Example 2, except that they were not annealed.

Comparative Examples 4 and 5: Fabrication of planar and ridge SiON core layers (patterned; no annealing)

Comparative Example 4 and 5 samples were prepared in the same manner as Example 2 materials, except that they were not annealed. A reactive ion etch was conducted according to the conditions described in Table 3 to form ridge waveguide cores (100 μm ridge in Comparative Example 4; 50 μm ridge in Comparative Example 5).

Fourier Transform InfraRed (FTIR) Analysis

Comparative Examples 2, 3, 4, and 5 and Examples 2 and 3 were analyzed using FTIR spectroscopy using a Nicolet Magna-IR 750 Spectrometer Series II (Nicolet Analytical Instruments, Madison, WI). A small peak around 3357 cm^{-1} is assigned to N-H vibrational mode. Table 6 shows the area underneath the N-H peak (3357 cm^{-1}) of SiON layers for the samples.

Table 6. Area Underneath N-H Peak

Example No:	Area under N-H peak:					
	Annealing Temperature ($^{\circ}\text{C}$)					
	No anneal	600	700	800	900	1000
Comp. Ex. 2		815	820	790	737	423
Comp. Ex. 3	780					
Comp. Ex. 4 (100Micron Ridge)	810					
Comp. Ex. 5 (50 micron Ridge)	810					
Example 2 (100 micron Ridge)		647	497	466	420	370
Example 3 (50 micron Ridge)		371	244	205	158	134

Example 4: Ring Resonator with SiO_2 /a-Si ridge/ SiO_2 sandwich (with annealing)

A 3 μ m thick borophosphosilicate glass (BPSG) lower cladding layer with a refractive index of 1.46 was deposited on a 0.5mm Si wafer (100) (Si wafer was obtained from Montco Silicon Technologies, Inc., Spring City, PA) by plasma enhanced chemical vapor deposition (PECVD, Model PlasmaLabTM System100 available from Oxford Instruments, Yatton, UK) using the parameters listed in Table 1.

After the BPSG layer was formed on the Si wafer, the sample was heated to 1080°C in a furnace with a ramp rate of 5 °C/min and held at that temperature for approximately 4 hours to allow the BPSG to reflow. After the heat treatment, a 250 nm thick amorphous silicon (a-Si) core layer was deposited on the BPSG lower cladding layer by PECVD using the following parameters described in Table 7.

Table 7. Conditions used for depositing a-Si layer

Reactant/Condition:	Value:
SiH ₄	100-400 sccm
Pressure	1000-2000 mTorr
HF power	30-150 W
Temperature	250-350°C

After deposition of the a-Si core layer was completed, a positive photoresist, referred to hereinafter as “PR” (Shipley PR1813 available from Electronic Materials Inc., Spartanburg, SC) was coated on the a-Si core layer by spin coating. The PR layer was patterned using a waveguide pattern mask and standard photolithography techniques. An etch process was then performed to etch the waveguide core layer and form ridge waveguide cores. A reactive ion etch (RIE, Model PlasmaLabTM System100 available from Oxford Instruments, Yatton, UK) was conducted according to the conditions described in Table 3. The waveguide was nominally 2.5 μ m in width and the etch depth was 50 to 200 nm.

Following the ion etching, a 100 nm thick SiO₂ upper cladding layer was deposited on the patterned waveguides, forming the SiO₂/a-Si ridge/SiO₂ sandwich waveguide structure. The SiO₂ upper cladding layer was deposited using PECVD according to the conditions described in Table 4.

The resulting waveguide sample was placed in a furnace and annealed in air at 800 °C for 5 hours using a heating and cooling rate of 2 °C/min. After annealing, the waveguide was crack-free when observed with optical microscopy.

5 Various modifications and alterations to this invention will become apparent to those skilled in the art without departing from the scope and spirit of this invention. It should be understood that this invention is not intended to be unduly limited by the illustrative embodiments and examples set forth herein and that such examples and
10 embodiments are presented by way of example only with the scope of the invention intended to be limited only by the claims set forth herein as follows.

We claim:

1. A method for making a waveguide comprising:

(a) providing a waveguide structure comprising a substrate, a lower cladding layer on the substrate, and a core layer comprising silicon nitride, amorphous silicon, or amorphous silicon-germanium alloy on the lower cladding layer;

(b) patterning the core layer; and

(c) annealing the waveguide structure.

2. The method of claim 1 further comprising depositing an upper cladding layer over the core layer after patterning the core layer and before annealing the waveguide structure.

3. The method of claim 1 or 2 wherein the substrate is a silicon wafer.

4. The method according to any one of claims 1 to 3 wherein the lower cladding layer comprises silicon dioxide.

5. The method according to any one of claims 1 to 4 wherein the lower cladding layer has a thickness between about 0.5 μm and about 50 μm .

6. The method of claim 5 wherein the lower cladding layer has a thickness between about 0.5 μm and about 3 μm .

7. The method according to any one of claims 1 to 6 wherein the core layer has a thickness between 0.1 μm and about 1 μm .

8. The method of claim 2 wherein the upper cladding layer has a thickness between about 0.05 μm and about 50 μm .

9. The method of claim 8 wherein the upper cladding layer has a thickness between about 0.05 μm and about 3 μm .

10. The method according to any one of claims 1 to 9 wherein the core layer
5 has a refractive index between about 1.6 and about 4.6.

11. The method of claim 10 wherein the core layer has a refractive index between about 1.6 and about 3.8.

10 12. The method according to any one of claims 1 to 11 wherein the core layer comprises silicon nitride or amorphous silicon, and the nitrogen content of the core layer is greater than about 20 mol %.

15 13. The method according to any one of claims 1 to 12 wherein patterning the core layer comprises photolithography and reactive ion etching.

14. The method according to any one of claims 1 to 12 wherein patterning the core layer comprises patterning a ridge in the core layer.

20 15. The method according to any one of claims 1 to 14 wherein annealing is at a temperature between about 600 $^{\circ}\text{C}$ and about 1000 $^{\circ}\text{C}$.

25 16. The method of claim 15 wherein annealing is at a temperature between about 700 $^{\circ}\text{C}$ and about 900 $^{\circ}\text{C}$.

30 17. A waveguide comprising a patterned core layer on a silicon dioxide lower cladding layer; wherein the core layer comprises silicon nitride, amorphous silicon, or amorphous silicon-germanium alloy, has a refractive index between about 1.6 and about 4.6, and is essentially crack-free; and wherein the waveguide is a ridge waveguide or a channel waveguide.

18. The waveguide of claim 17 further comprising a silicon dioxide upper cladding layer on the patterned core layer.

19. The waveguide of claim 17 or 18 wherein the waveguide exhibits an optical loss of less than about 0.15 dB/cm at wavelengths between about 1310 nm and about 1565 nm.

20. The waveguide according to any one of claims 17 to 19 wherein the waveguide is a ridge waveguide.

21. The waveguide according to any one of claims 17 to 19 wherein the waveguide is a channel waveguide.

22. A method for making a ring resonator comprising:

(a) providing a waveguide structure comprising a substrate, a lower cladding layer on the substrate, and a core layer comprising silicon nitride, amorphous silicon, or amorphous silicon-germanium alloy on the lower cladding layer;

(b) patterning the core layer;

(c) depositing an upper cladding layer on the core layer to provide a sandwich waveguide structure:

(d) annealing the sandwich waveguide structure;

(e) depositing a ring resonator layer comprising silicon nitride, amorphous silicon, or amorphous silicon-germanium alloy on the annealed sandwich waveguide structure; and

(f) patterning a ring into the ring resonator layer.



FIG. 1a



FIG. 1b

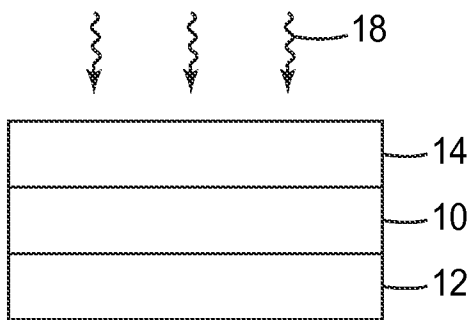


FIG. 1c

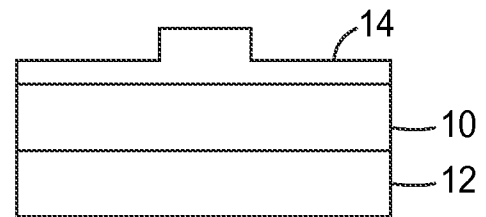


FIG. 1d

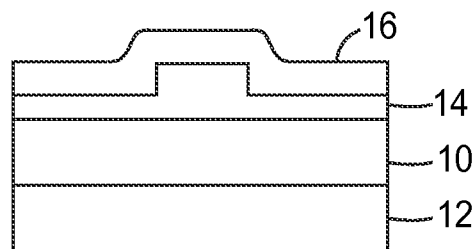


FIG. 1e



FIG. 2a



FIG. 2b

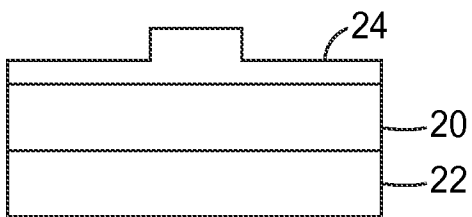


FIG. 2c

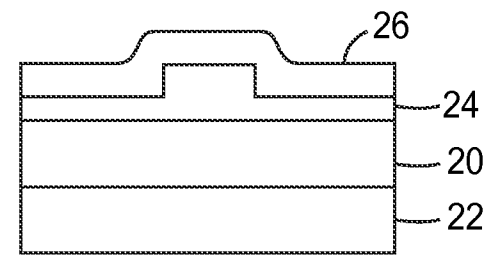


FIG. 2d

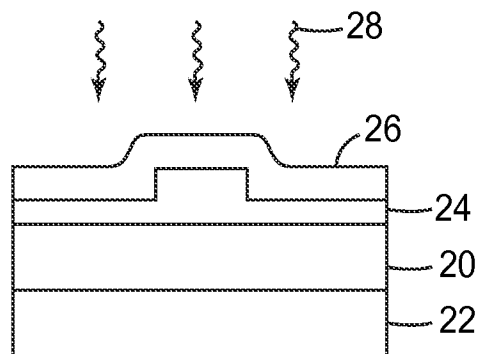
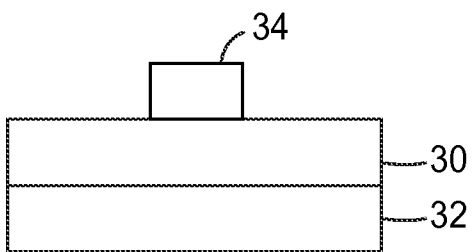
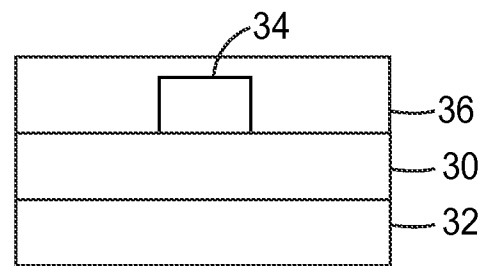
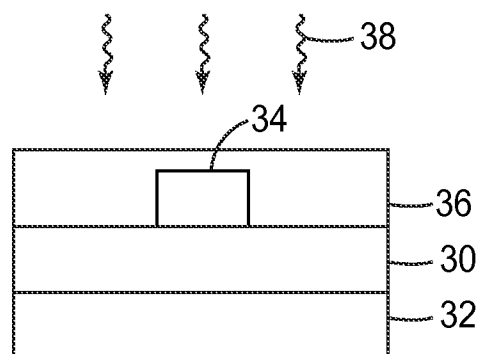
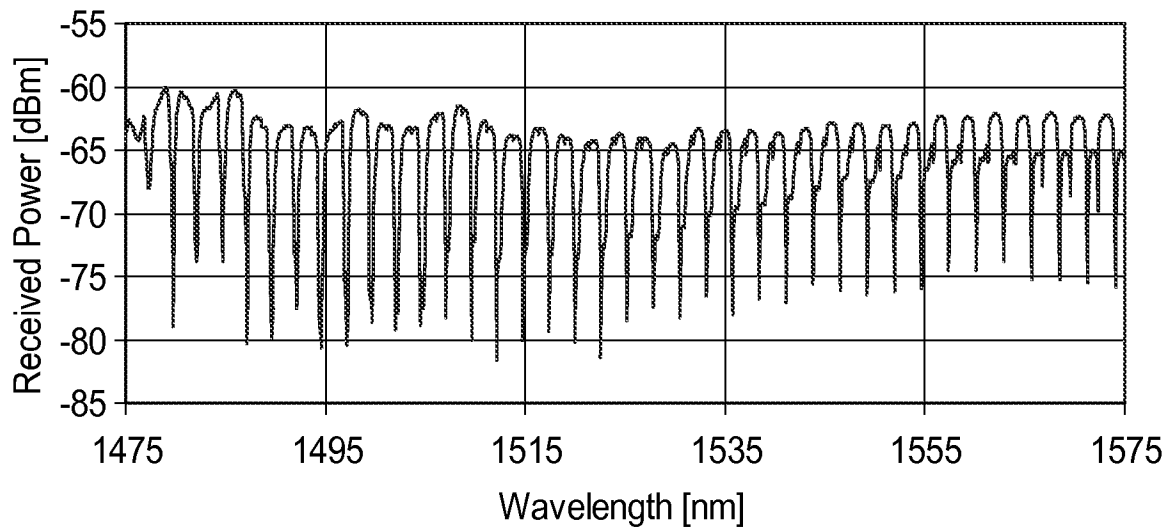
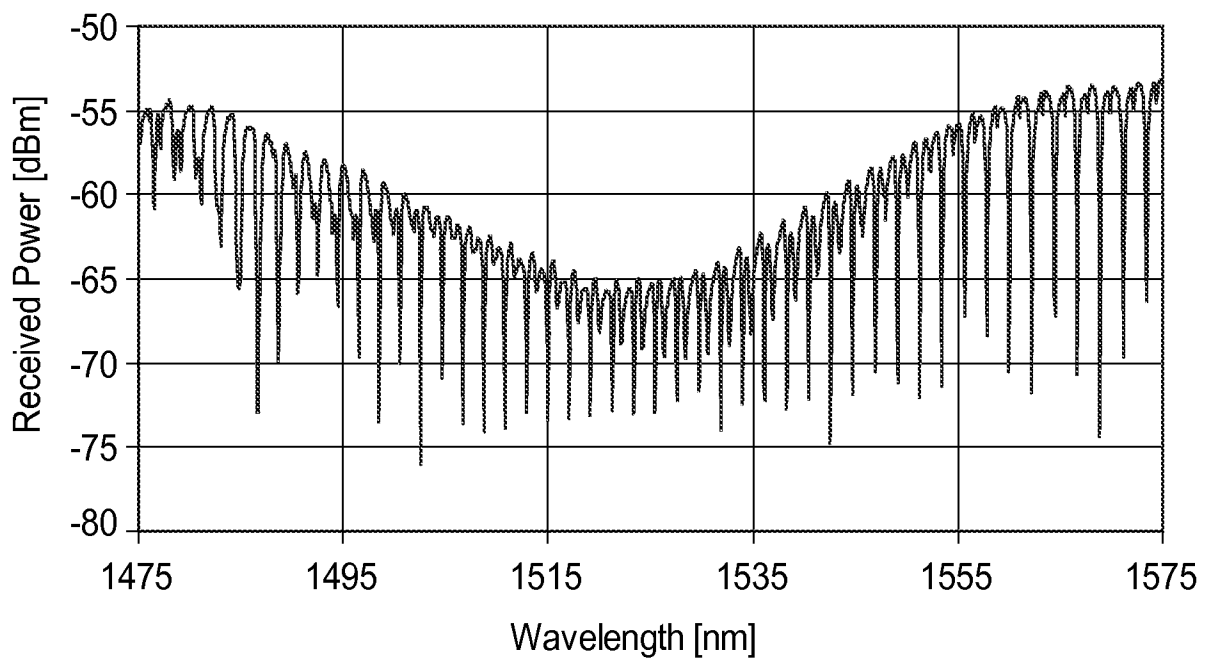


FIG. 2e

*FIG. 3a**FIG. 3b**FIG. 3c**FIG. 3d**FIG. 3e*

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*FIG. 4**FIG. 5*

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2008/084308

A. CLASSIFICATION OF SUBJECT MATTER
INV. G02B6/132

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G02B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	C.H. HENRY ET AL.: "Low loss Si3N4-SiO2 optical waveguides on Si" APPLIED OPTICA, vol. 26, no. 13, 1 July 1987 (1987-07-01), pages 2621-2624, XP002511553 the whole document	1-5, 7-12, 14, 17-21
Y		6, 13, 15, 16
	----- -/--	

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

A document defining the general state of the art which is not considered to be of particular relevance

E earlier document but published on or after the international filing date

L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

O document referring to an oral disclosure, use, exhibition or other means

P document published prior to the international filing date but later than the priority date claimed

T later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

* & * document member of the same patent family

Date of the actual completion of the international search

22 January 2009

Date of mailing of the international search report

27/04/2009

Name and mailing address of the ISA/

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Frisch, Anna Maria

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2008/084308

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	BULLA D AP ET AL: "Design and fabrication of SiO ₂ /Si ₃ N ₄ optical waveguides" MICROWAVE AND OPTOELECTRONICS CONFERENCE, 1999. SBMO/IEEE MTT-S, APS A ND LEOS - IMOC '99. INTERNATIONAL AUGUST 09-12, 1999, PISCATAWAY, NJ, USA, IEEE, vol. 2, 9 August 1999 (1999-08-09), pages 454-457, XP010509821 ISBN: 978-0-7803-5807-2 the whole document	6,13
Y	----- GONZALVEZ J M ET AL: "PLASMA-ENHANCED CHEMICALLY VAPOUR DEPOSITED Si ₃ N ₄ THIN FILMS FOR OPTICAL WAVEGUIDES" THIN SOLID FILMS, ELSEVIER-SEQUOIA S.A. LAUSANNE, CH, vol. 220, no. 1 / 02, 20 November 1992 (1992-11-20), pages 311-314, XP000354505 ISSN: 0040-6090 the whole document	15,16
Y	----- US 2002/178760 A1 (BONA GIAN-LUCA [CH] ET AL) 5 December 2002 (2002-12-05) paragraph [0044] -----	15,16

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2008/084308

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers allsearchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search reportcovers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-21

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-21

Subject 1 relates to a method for making a waveguide device with a core of a high-index material and lower clad on a substrate, to the patterning of a core in the high-index material, to an annealing step, and to further details of the waveguide structure like thicknesses of the layers, refractive index of the core, annealing temperatures, and material of the cladding layers, and to a corresponding waveguide device.

2. claim: 22

Subject 2 also relates to a method for making a waveguide device with a core of a high-index material and lower clad on a substrate, to the patterning of a core in the high-index material, to an annealing step, and to further steps needed for fabricating a resonator on top of the waveguide like planarisation with an upper clad.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2008/084308

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2002178760 A1	05-12-2002	NONE	