(12) UK Patent (19) GB (11) 2 083 283 B

(54) Title of invention

Resin molded type semiconductor device

(51) INT CL³; H01L 29/60

(21) Application No
8125494

(22) Date of filing
20 Aug 1981

(30) Priority data

(31) 55/119817

(32) 1 Sep 1980

(33) Japan (JP)

(43) Application published
17 Mar 1982

(45) Patent published
20 Jun 1984

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(52) Domestic classification
H1K 11A3 11D1 11D 1CA 3T1C 3U6A 4C11 4C14 4C1U 4C3U 4F1C HAX

(56) Documents cited
None

(58) Field of search
H1K

GB 2 083 283 B

2083283

FIG. 1

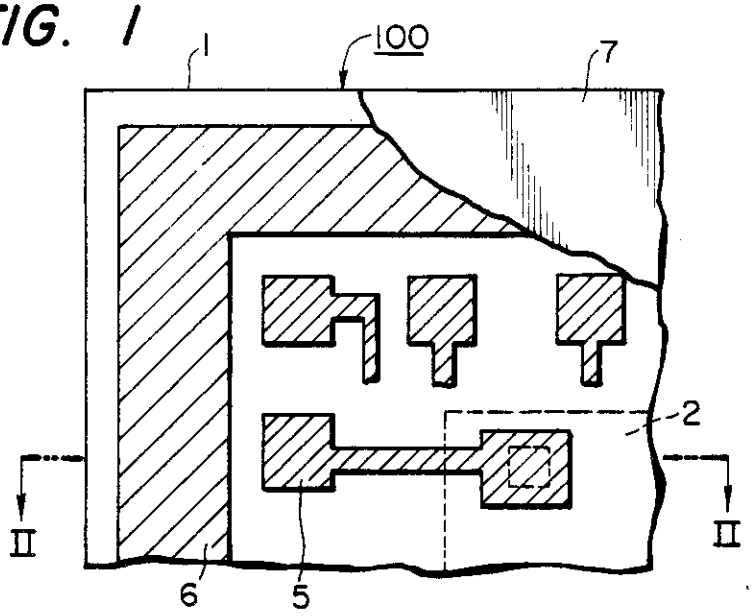

FIG. 2

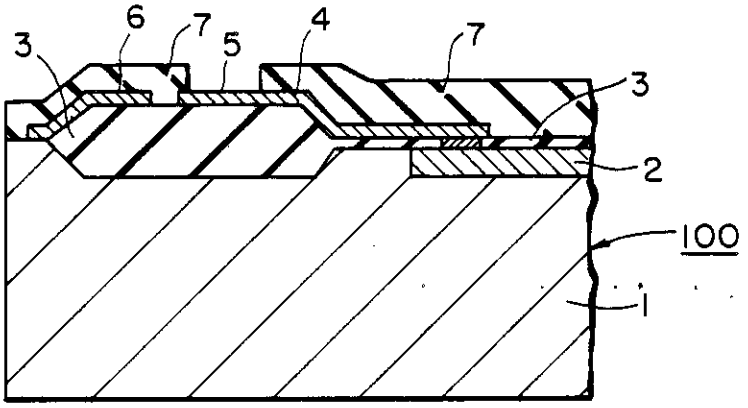

FIG. 3

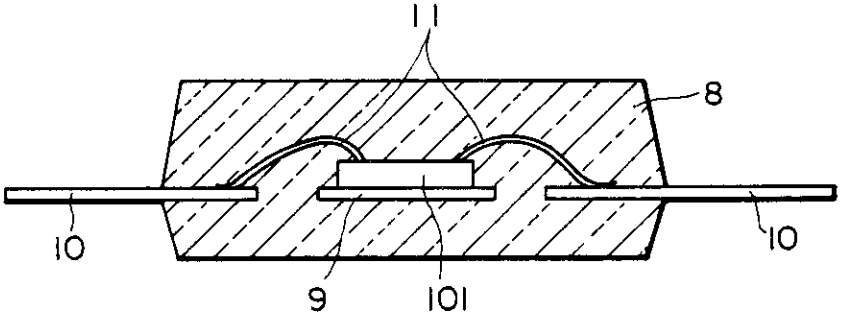

FIG. 4

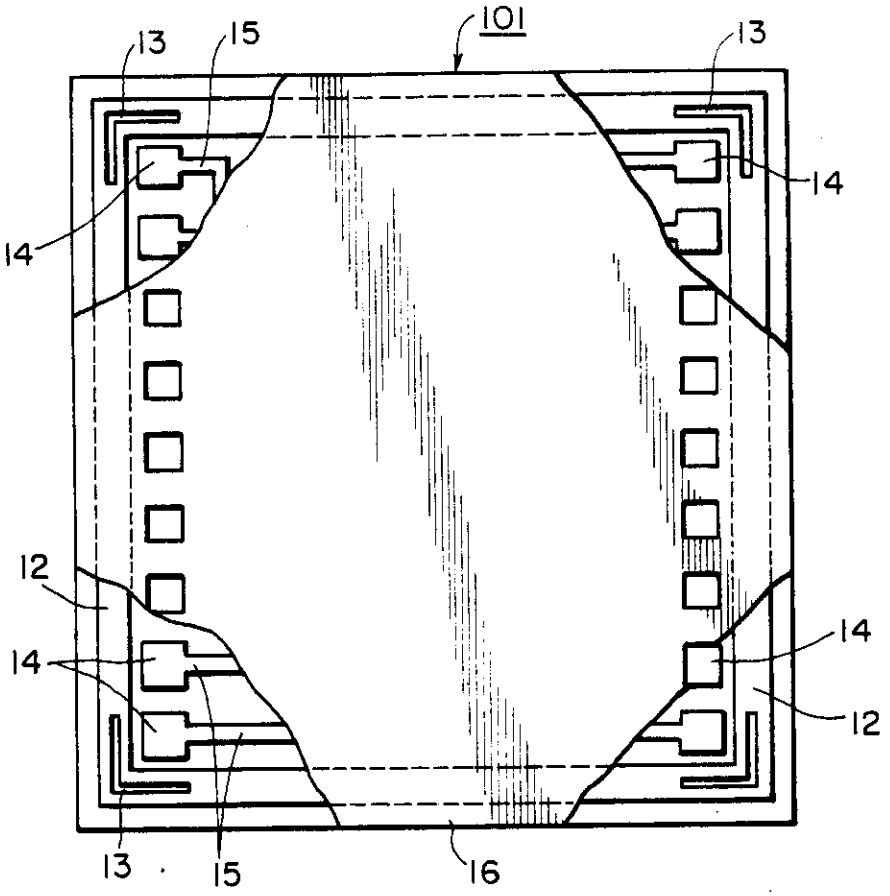

FIG. 5

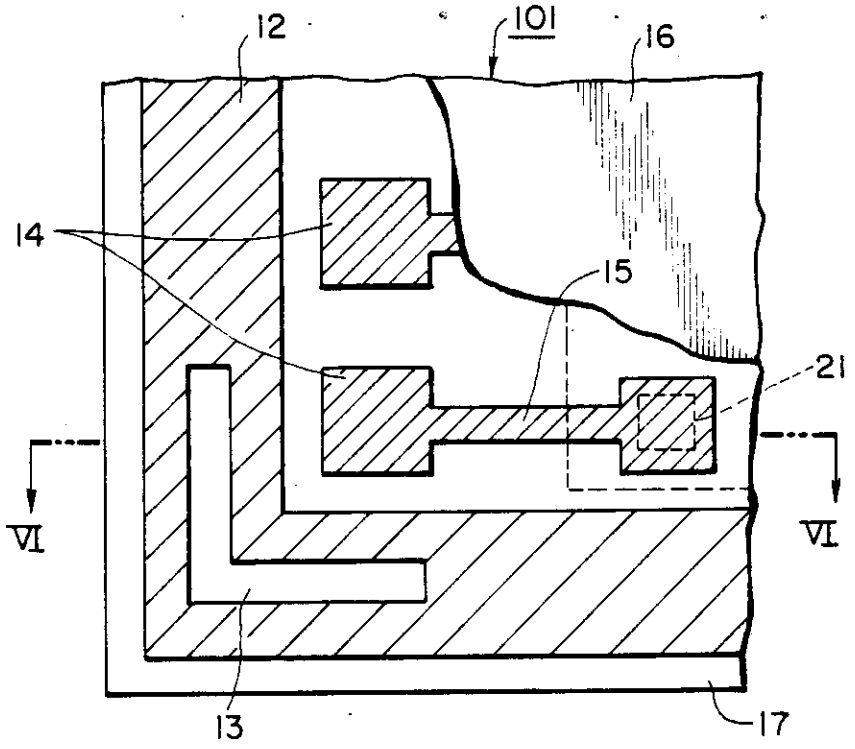

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FIG. 6

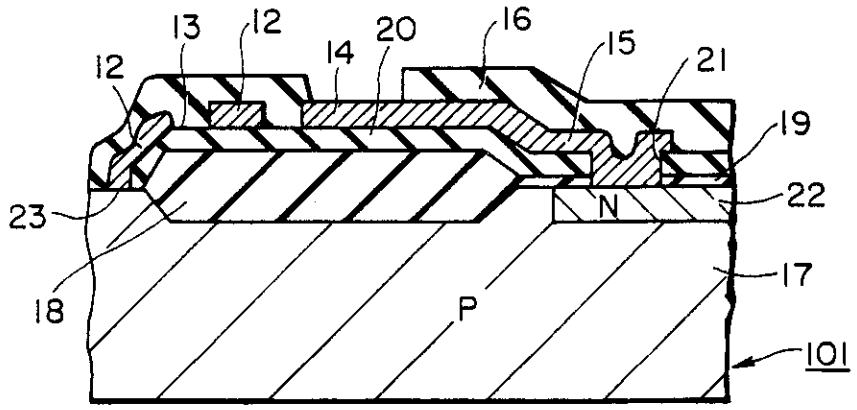

FIG. 7

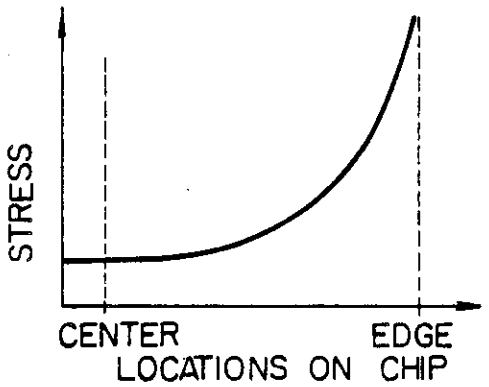

FIG. 8

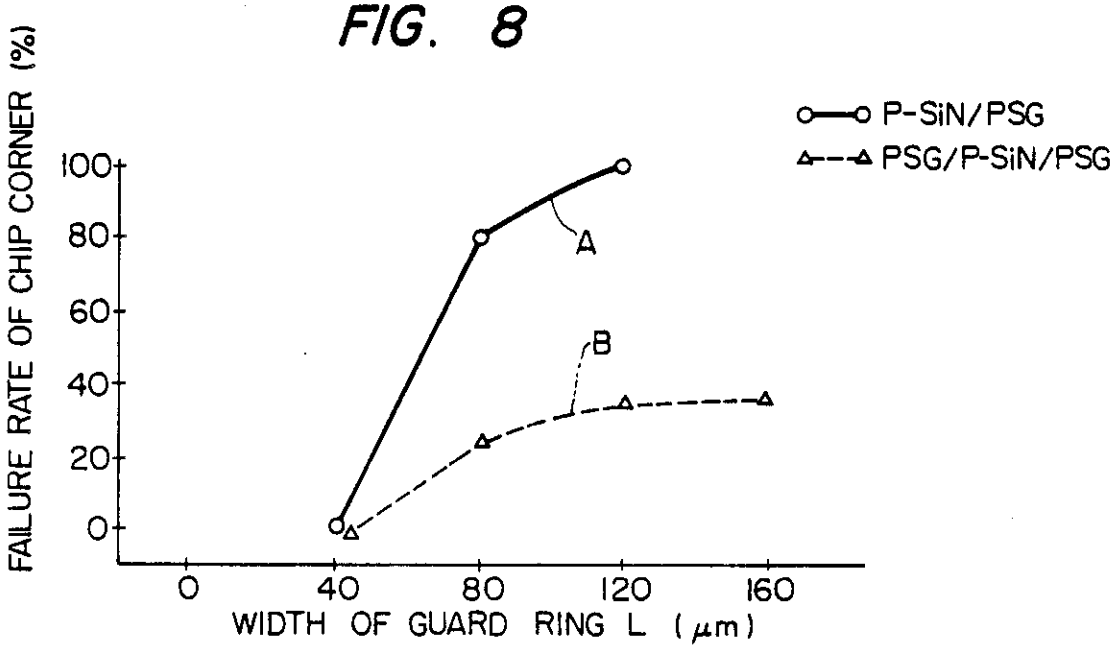

FIG. 9

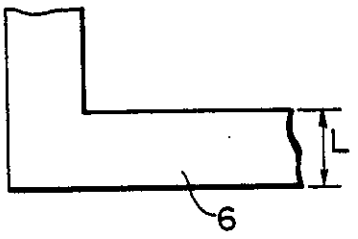

FIG. 11

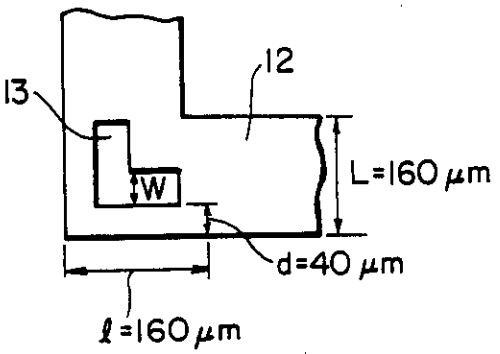

FIG. 10

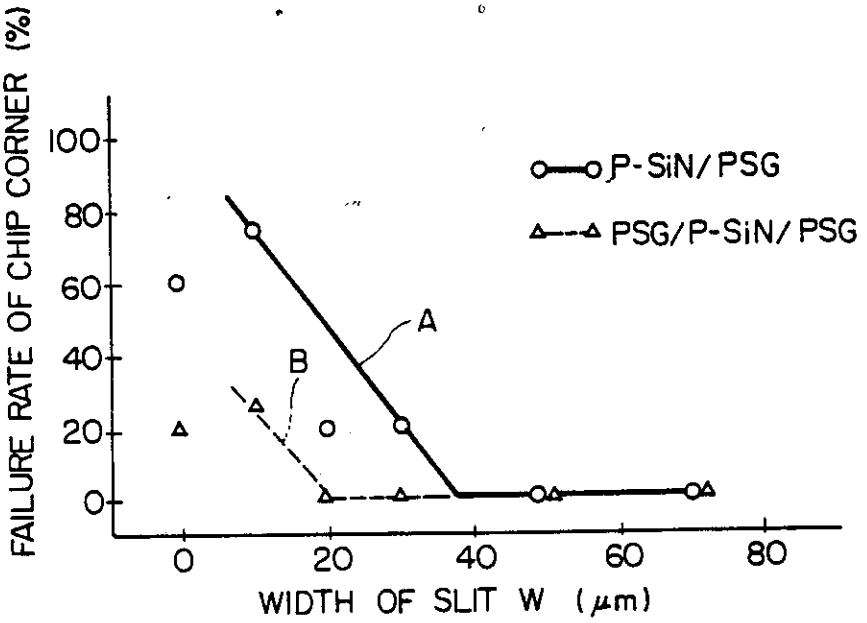

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FIG. 12

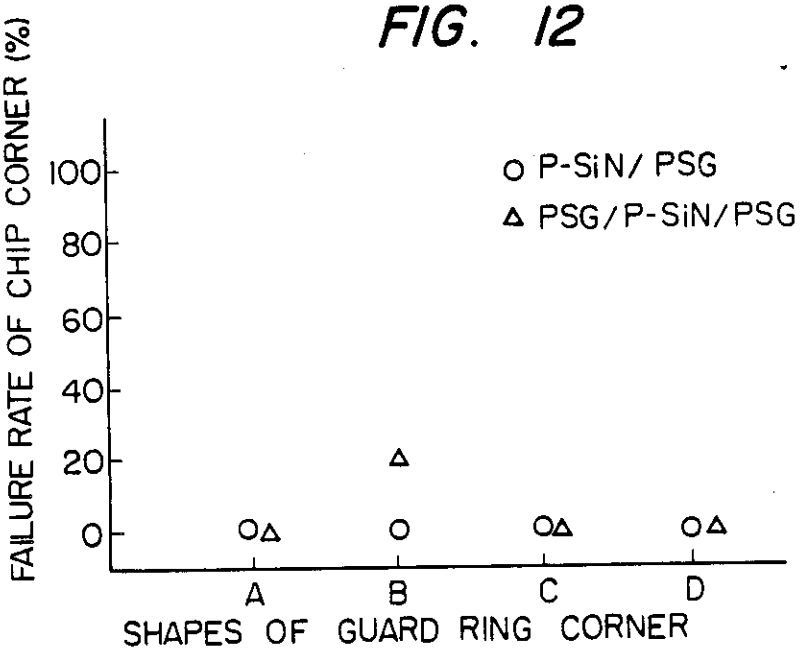


FIG. 13A

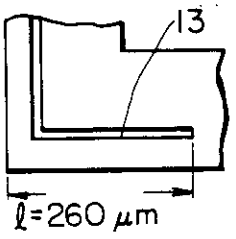


FIG. 13B

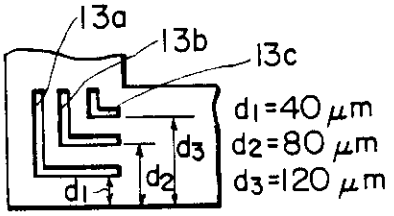


FIG. 13C

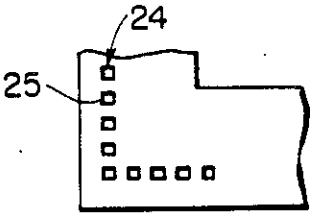
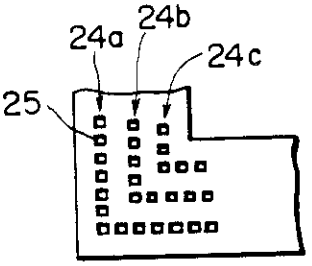


FIG. 13D



RESIN MOLDED TYPE SEMICONDUCTOR DEVICE

This invention relates to a resin molded type semiconductor device, and more particularly to a guard ring structure which is formed on a semiconductor substrate.

It has been well known for an insulating film to be formed on the surface of the peripheral edge of a silicon semiconductor substrate (chip) formed with one or more circuit elements, and for a conductive guard ring to be disposed on the insulating film in a manner to extend along the peripheral edge of the semiconductor substrate. Such structure is disclosed in, for example, West German Patent Laid Open Print (Offenlegungsschrift) 30 02 740. The guard ring is used for preventing an inversion layer in the semiconductor substrate surface on which the insulating film is formed. It can also be used as wiring for applying the ground potential (reference potential) or power source potential of a circuit.

In order to reduce the manufacturing cost of a discrete semiconductor device or a semiconductor integrated circuit device, it is requested to use a resin mold package instead of a ceramic package or glass package as a sealing structure for the device.

To reduce the manufacturing cost, accordingly, semiconductor substrates having the aforecited guard ring structure are also requested to be sealed in the resin mold package.

The inventors' experiments and researches, however, have revealed that where a semiconductor substrate having the guard ring structure is molded with a resin by the well-known transfer mold technique, high stresses ascribable to the molding resin act especially on the four corners of a rectangular semiconductor substrate (chip), resulting in cracks in a passivation film which overlies the guard ring at the corners of the chip and the semiconductor substrate near the corners. The cracks give rise to non-conforming samples of the semiconductor device, or form a cause for degradation in the characteristics of the semiconductor device. By way of example, the inventors studied the problem on a large-scale integrated circuit device (LSI) shown in Figures 1 and 2. In a chip 100 in Figures 1 and 2, semiconductor element regions 2 constructing active regions are formed in one major surface of a silicon semiconductor substrate 1. On an insulating film 3 overlying the surface of the peripheral edge of the substrate, wiring 4 and bonding pads 5 which are made of an aluminum film are formed and are surrounded

with a guard ring 6 for preventing an inversion layer. The guard ring 6 is connected to the substrate 1 (ground line). A passivation film (final passivation film) 7 of phosphosilicate glass (PSG) or silicon nitride is formed on the surface of the chip in a manner to expose the pad portions 5. It has been revealed that, where the chip 100 is molded with a resin, high stresses attributed to the molding resin act especially on the four corners of the peripheral edge of the chip, so the passivation film 7 cracks on and around the guard ring 6.

The semiconductor device of such structure was subjected to a moisture-resistance test in a high-temperature and high-humidity atmosphere. As a result, the following has been revealed. When using a PSG (phosphorus oxide-containing silicate glass) film as the inter-layer insulating film which underlies the aluminum wiring, moisture invades the device through the cracks which have appeared in the final passivation film. Thus, phosphorus in the PSG film liquates out and corrodes the aluminum wiring overlying this PSG film. The corrosion of the aluminum wiring reaches the active region of the chip, resulting in the occurrence of a defective unit of the chip or degradation of the characteristics thereof.

As the result of experiments and researches, the inventors have found out that such defects as cracks in the passivation film existent on and around the guard ring at the corner parts of the chip as described before relate to the width of the guard ring. The reason therefor is considered as follows. When the chip is molded with the resin by the transfer mold technique, the temperature of the molding resin material lowers from a high temperature to the normal temperature, or when the finished semiconductor product in the resin mold package is operated, the chip generates heat, so that the corner parts of the chip undergo high stresses on account of the expansion and shrinkage of the molding resin. The stresses displace or expand and shrink the guard ring of aluminum. Due to the displacements of the aluminum guard ring, the cracks appear in the final passivation film or the passivation film underlying the guard ring which is difficult to displace. It is accordingly considered that, in order to reduce the stresses which the aluminum

guard ring at the corner parts exerts on the passivation films nearby, the width of the guard ring at the chip corner parts may be made small.

The present invention has been made with note taken of this idea, and provides a semiconductor device having a ring-shaped conductor film which is formed on an insulating film on a major surface of a semiconductor substrate in a manner to extend along a peripheral part of the major surface, and a sealing member of a resin molded around the semiconductor substrate; wherein said conductor film includes means in at least one corner portion which reduces the effective width of the film at that corner portion.

Hereunder, this invention will be described with reference to the drawings, wherein:-

Figure 1 is a plan view of a semiconductor device having a prior-art guard ring configuration as was used in the experimental researches of this invention;

Figure 2 is a sectional view of the semiconductor device of Figure 1 taken along line II - II indicated in Figure 1;

Figure 3 is a sectional view showing the finished body of a semiconductor device according to this invention;

Figure 4 is a fragmentary plan view showing the chip of the semiconductor device of Figure 3;

Figure 5 is an enlarged partial plan view of the chip shown in Figure 4;

Figure 6 is a sectional view of the semiconductor device of Figure 5 taken along line VI - VI indicated in Figure 5;

Figure 7 is a graph showing the distribution of stresses which arise in the chip plane due to the molding resin;

Figure 8 is a graph showing the relationships between the width of an aluminum guard ring and cracks which appear at the corner parts of a passivation film;

Figure 9 is a schematic plan view showing the shape of a guard ring at a corner part in order to explain the graph of Figure 8;

Figure 10 is a graph showing the relationships between the width of a slit in a guard ring and the failure rate of chip corners, in semiconductor devices embodying this invention;

Figure 11 is a schematic plan view showing the shape of a guard ring at a corner part in order to explain the graph of Figure 10;

Figure 12 is a graph showing the relationships between the shape of a guard ring and the failure rate of chip corners, in semiconductor devices according to other embodiments of this invention; and

Figures 13A - 13D are schematic plan views showing various shapes of guard rings at corner parts in order

to explain the graph of Figure 12.

Figures 3 - 6 are views for explaining a preferred embodiment of this invention. Figure 3 shows a semiconductor device including a resin mold package as is fabricated in accordance with this invention. In the figure, numeral 8 designates a sealing member of a resin formed by the well-known transfer mold technique. The resinous sealing member 8 seals a **rectangular** silicon chip 101, a metallic lead 9 having a holding portion to which the chip 101 is fastened, parts of a plurality of metallic external leads 10, and connector wires 11 electrically connected between the chip 101 and the respective external leads 10.

Figure 4 shows a plan view of the chip 101. The chip 101 is made of a semiconductor substrate of single-crystal silicon, in which active regions of circuit elements such as source regions and drain regions are formed by the well-known impurity diffusion technique. This embodiment illustrates the case of a MOS IC (Metal-Oxide-Semiconductor Integrated Circuit) where logic circuits constructed of MOS FETs are formed in the shape of an integrated circuit. In Figure 4, numeral 12 designates a guard ring of aluminum which is formed on an insulating film on the silicon semiconductor substrate. The guard

ring 12 is used as an inversion preventive guard ring for checking the formation of an inversion layer in the surface of the silicon semiconductor substrate, and is also used as ground wiring for the logic circuits. The outside terminating part of the guard ring 12 is electrically connected with the silicon semiconductor substrate. The four corner parts of the guard ring 12 are respectively formed with L-shaped slits 13 in accordance with this invention. The slits 13 will be discussed in detail later. Bonding pads 14 for bonding the wire connectors 11 (Figure 3) are formed along the inner sides of the guard ring 12. Wirings 15 extend from the respective bonding pads 14 to the active regions. The wirings 15 are covered with a final passivation film 16. The final passivation film 16 has openings for exposing the bonding areas of the bonding pads 14. The connector wires 11 are connected to the bonding areas.

Figures 5 and 6 are an enlarged partial plan view of the chip 101 shown in Figure 4 and a corresponding sectional view, respectively. As apparent from the sectional view of Figure 6, the chip 101 includes a thick silicon-oxide (SiO_2) film (field insulating film) 18 which is formed in one major surface of the silicon semiconductor substrate 17, and a thin silicon-oxide

(SiO_2) film 19 which covers the regions forming the circuit elements. The technique of forming a thick oxide film on selected parts of a single silicon semiconductor substrate except regions to form elements is well known from, for example, "Philips Research Reports, Vol. 26, No. 3, pp. 157-165, June 1971". The embodiment is the MOS IC of the so-called LOCOS (Local Oxidation of Silicon) type described in this literature. The thin oxide film 19 formed on the element regions is used as the gate oxide films of the MOS FETs constituting the MOS IC. Although not shown in the drawings, gate electrodes of polycrystalline silicon are formed directly on parts of the thin oxide film 19, thereby to form the MOS FETs. A phosphosilicate glass (PSG) (phosphorus oxide-containing silicate glass) film 20 is formed in a manner to cover the silicon gate electrodes and those parts of the field oxide film 18 and the thin oxide film 19 on which the silicon gate electrodes are not formed. The PSG film 20 serves as a getter for impurities such as sodium ions entering from the exterior, and is necessary for stabilizing the electrical characteristics of the surface of the silicon semiconductor substrate of the semiconductor device. On the PSG film 20, there are formed the foregoing guard ring 12, bonding pads 14 and wirings 15 all of which are

made of aluminum. These can be simultaneously formed in such a way that a film of aluminum is formed on the entire surface of the chip by the well-known evaporation technique and that the film is patterned by the etching technique. The aluminum wirings 15 lie in ohmic contact with semiconductor regions 22 being some of the element regions, via through-holes 21 formed in the PSG film 20 and the SiO_2 film 19. The aluminum guard ring 12 lies in ohmic contact with the silicon semiconductor substrate 17 at its outer terminating part 23. Thus, the potential of the guard ring 12 is made identical to that of the substrate 17. Since, in the embodiment, the guard ring is especially used as the ground line of the circuitry, the ohmic contact part 23 forms a current path for supplying current to the lead 9 (Figure 3) which is connected to the rear major surface of the semiconductor substrate 17. In the corner parts of the guard ring corresponding to the corners of the chip, the L-shaped slits 13 are formed along the corners and centrally of the guard ring. The final passivation film 16 is made up of one layer either of PSG film, a silicon oxide (SiO_2) film formed by the well-known CVD (Chemical Vapor Deposition) process or a silicon nitride film formed by the well-known plasma process (hereinbelow, simply termed the "P-SiN film"),

or a multilayer structure consisting of at least two of the films. Examples of the present embodiment adopted for the final passivation the two sorts of a two-layer structure which consisted of a PSG film as a first layer (lower layer) and a P-SiN layer formed thereon, and a three-layer structure which consisted of a PSG film as a first layer, a P-SiN film as an intermediate layer and a PSG film as a third layer.

In the examples, the size of the chip was 4.7 mm x 4.7 mm. The width of the guard ring was set at 100 μm or greater in order to prevent the increase of the resistance of the aluminum film as the wiring, while the width of the slit was set at approximately 10 μm in order to prevent the increase of the resistance of the guard ring at the corner part.

According to such structure, the guard ring is provided with the slits, and hence, the occurrence of the cracks in the passivation film can be prevented for the following reason.

Regarding the fact that the guard ring on the peripheral part of the resin-molded semiconductor chip causes the cracks etc. of the passivation film, stresses tend to concentrate in the edge of the chip more than the center thereof as shown in Figure 7, especially in the corners of the rectangular chip. On

the other hand, it has been experimentally confirmed that the tendency is more remarkable as the width of the aluminum film of the guard ring is greater. It has also been confirmed by various experiments that when the slits are formed at the corner parts of the guard ring, the effective width of the guard ring decreases by the width of the slits, whereby the stresses at the corner parts are reduced, with the result that the cause for the occurrence of the cracks is eliminated.

With the structure described above, accordingly, the displacements of the aluminum guard ring at the corner parts to be induced by the molding resin are reduced owing to the slits, and the reduced displacements do not exert high stresses on the passivation films lying in contact with the aluminum film and being less displaced than the metal. Therefore, the passivation films are not cracked.

In order to facilitate understanding of the effect of this invention, the relationship between the rate of occurrence of the cracks of the passivation film and the width L of the guard ring was experimentally found by employing the shape of the prior-art guard ring of aluminum as shown in Figure 9. Figure 8 illustrates this relationship, in which the percentage of samples having undergone the cracks is taken on the axis of

ordinates as the failure rate of chip corners and the width L (Figure 9) of the guard ring is taken on the axis of abscissas. In this case, the chip size was 4.7 x 4.7 mm^2. As the final passivation films, the two sorts of the three-layer structure of PSG/P-SiN/PSG and the two-layer structure of P-SiN/PSG were used. The thicknesses of the passivation films were PSG/P-SiN/PSG = 0.85 μm/1.1 μm/0.2 μm and P-SiN/PSG = 1.1 μm/0.2 μm. As temperature cycles, a temperature change of from −55 °C to +150 °C was repeated 20 times. Thus, the stresses which occur on expansion and shrinkage of the resin package owing to temperature changes were acceleratedly applied to the chip corners. In Figure 8, a curve A corresponds to the passivation film of P-SiN/PSG, while a curve B the passivation film of PSG/P-SiN/PSG.

As understood from Figure 8, the failure rate is smaller as the width L of the guard ring is smaller. That is, the stresses to be exerted from the resinous sealing member on the chip are higher as the width of the guard ring is greater.

Figure 10 is a graph illustrating the fact that the percentage of occurrence of the cracks of the passivation film corresponding to the guard ring portion in the case of forming the L-shaped slits according to

this invention in the corner parts of the guard ring as shown in Figure 11 depends upon the width W of the slits. As the passivation films in this case, a curve A corresponds to the two-layer film of P-SiN/PSG = 1.1 μm/0.2 μm, and a curve B the three-layer film of PSG/P-SiN/PSG = 0.85 μm/1.1 μm/0.2 μm. As understood from Figure 10, the failure rate of chip corners lowers remarkably at slit widths of 20 μm - 40 μm. The conditions of the chip size and the temperature cycles in this case were the same as in the case illustrated in Figure 8.

Figures 13A - 13D show further embodiments of this invention. While the figures schematically illustrate various shapes of the corner part of the aluminum guard ring 160 μm wide in a semiconductor device, the remaining construction of the semiconductor device is the same as explained with reference to Figures 3 - 6.

The embodiment shown in Figure 13A corresponds to a case where one elongate slit is formed so that its length ℓ from the corner of the guard ring may be 260 μm.

Figure 13B illustrates a case where three short slits 13a, 13b and 13c are juxtaposed to one another.

Figure 13c illustrates a case where small square holes 25 are arrayed in the L-letter shape 24. This embodiment is more advantageous than the case of forming

the L-shaped slit in that the increase of the resistance at the corner part of the guard ring can be prevented.

Figure 13D illustrates a case where small holes 25 are arrayed into three L-shaped rows 24a, 24b and 24c. The size of the hole 25 in this case is made, for example, 10 μm square.

As to the embodiments of Figures 13A - 13D, the rates of occurrence of the cracks of the final passivation films at the corner parts were studied. The results are shown in Figure 12. The semiconductor pellets in this case were 4.7 x 4.7 mm square, and the temperature cycles were temperature changes of from −55 °C to +150 °C repeated 20 times. Likewise to the case of Figure 10, the passivation films were of the two-layer structure of P-SiN/PSG and the three-layer structure of PSG/P-SiN/PSG. In Figure 12, marks O correspond to the cases of employing the passivation films of P-SiN/PSG, and marks Δ the case of employing the passivation films of PSG/P-SiN/PSG.

As understood from Figure 12, the failure rates of the chip corners can be lowered by forming the slits or the rows of the holes.

As apparent from the foregoing embodiments, means for reducing the effective width of the guard ring at the corner part, such as the slit

or the row of the holes, is added to the corner part of the guard ring. Thus, the stress which the molding resin exerts on the passivation films adjoining the guard ring at the corner part can be reduced, so that the passivation films can be prevented from cracking.

This invention is not restricted to only the foregoing embodiments. By way of example, the construction and shape of the passivation film to be formed on the guard ring of aluminum can be properly modified. The shape of the guard ring itself is sometimes modified depending upon the arrangement of the internal circuits or the bonding pads. The resinous sealing member may well include an undercoating resin which is directly applied on the surface of the guard ring portion. While aluminum has been referred to as the material of the guard ring, a different metal film may well be used.

Further, this invention is effective for enhancing the moisture resistance when applied to semiconductor devices which have a guard ring and which employ a passivation film lying in contact with wirings and containing a high concentration of phosphorus, especially semiconductor devices such as plastics molded type LSIs.

CLAIMS:

1. A semiconductor device having a ring-shaped conductor film which is formed on an insulating film on a major surface of a semiconductor substrate in a manner to extend along a peripheral part of the major surface, and a sealing member of a resin molded around the semiconductor substrate; wherein said conductor film includes means in at least one corner portion which reduces the effective width of the film at that corner portion.

2. A semiconductor device according to claim 1 wherein said width reducing means comprises at least one slit or an array of holes arranged to substantially limit the effective width thereof, in at least one corner of said semiconductor substrate.

3. A semiconductor device according to claim 2, wherein said conductor film is covered with a film of phosphosilicate glass.

4. A semiconductor device according to claim 2 or claim 3, wherein said slit is L-shaped.

5. A semiconductor device according to claim 2 or claim 3, wherein said holes are arrayed into the shape of a letter L.

6. A semiconductor device according to any one of the preceding claims wherein said conductor film is electrically connected with said semiconductor substrate

at an outer edge of the ring.

7. A semiconductor device according to any one of the preceding claims, wherein said conductor film is made of aluminum.

8. A semiconductor device substantially as any described herein with reference to Figs 3 to 6 or Figs. 13A to 13D of the accompanying drawings.

2083283

Dated:	Application No.:	Published:
20 August 1981	8125494	17 March 1982

Priority: 1 September 1980 Japan 119817

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Request for examination: 20 AUG 1982	
Application refused or withdrawn:	
Patent granted: WITH EFFECT FROM SECTION 25(1) — 20 JUN 84	
Renewal Fee paid in respect of	
5th Year	
6th Year	
7th Year	
8th Year	
9th Year	
10th Year	
11th Year	
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18th Year	
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Patent ceased or expired:	