

[54] **MEANS AND METHOD FOR TIME-SHARING MULTICHANNEL WELL LOGGING**

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340/15.5 PP, 340/15.5 BH,
179/15.55, 235/92 CM

[51] Int. Cl. **G01v 1/22**

[58] Field of Search **340/18 CM,**
340/15.5 PP; 179/15.55;
235/155, 92 CM

[56] **References Cited**

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Primary Examiner—Benjamin A. Borchelt

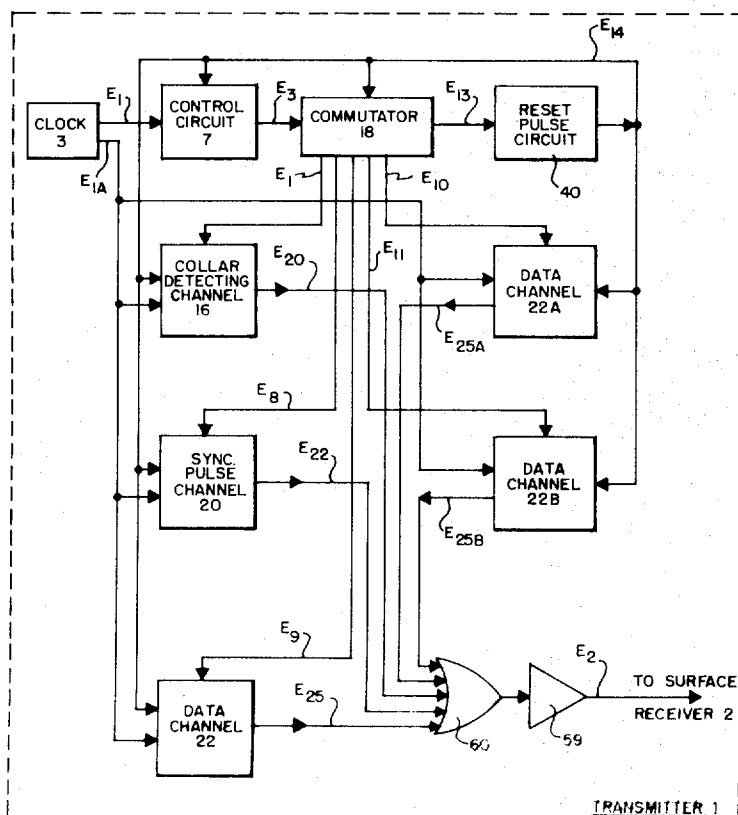
Assistant Examiner—N. Moskowitz

Attorney—Thomas H. Whaley

[57] **ABSTRACT**

A transmitter in a borehole provides a pulse train to a surface receiver. Each cycle of the pulse train is divided into a plurality of time intervals, and the pulses in each time interval correspond to a different sensed condition of the borehole or the nature of the earth formation traversed by the borehole. The receiver separates the pulses of the pulse train according to time interval and provides an output for each time interval. Each output provided by the receiver corresponds to a different sensed condition of the borehole or nature of the earth formation.

33 Claims, 16 Drawing Figures



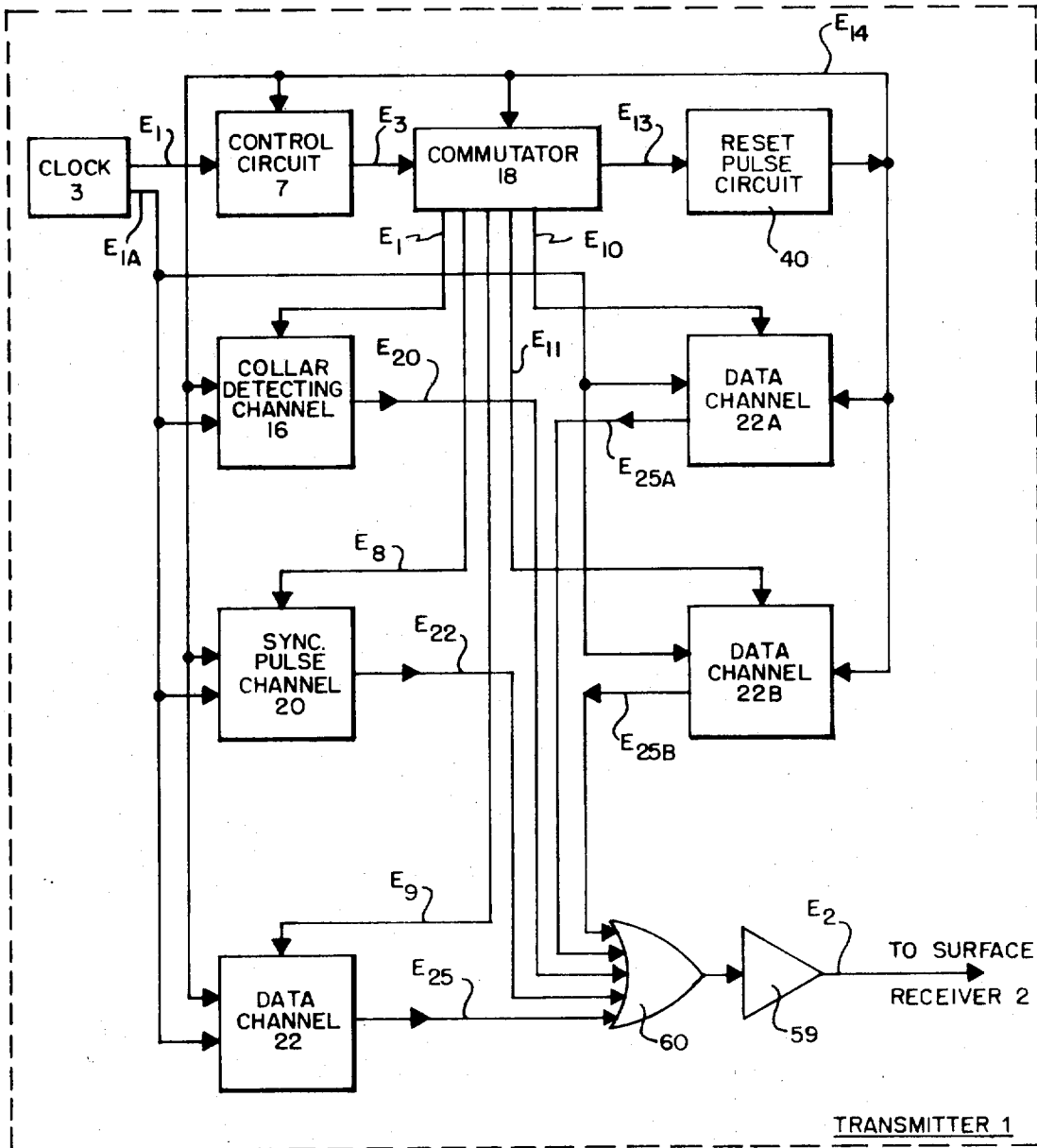


FIG 1

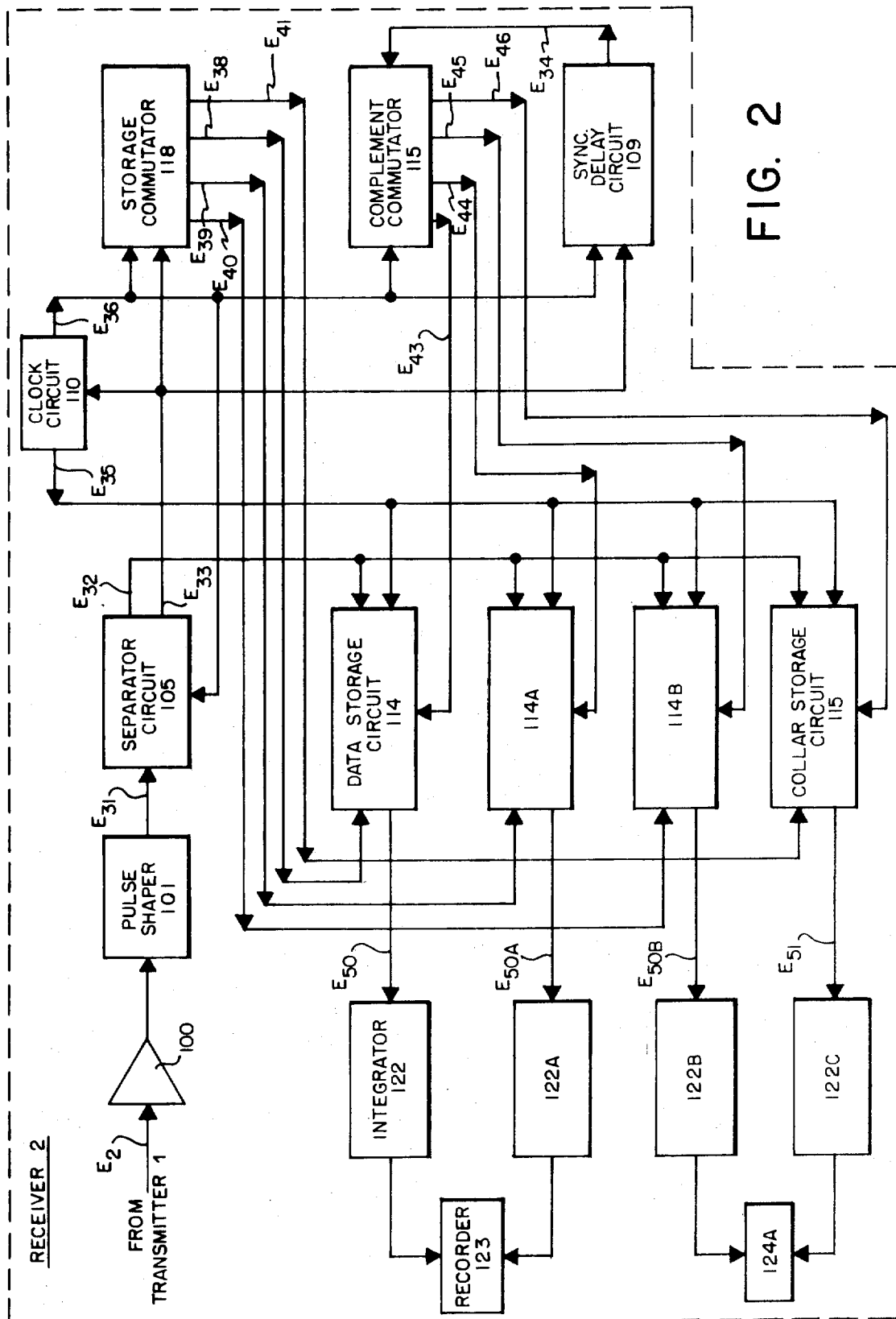


FIG. 2

FIG. 3

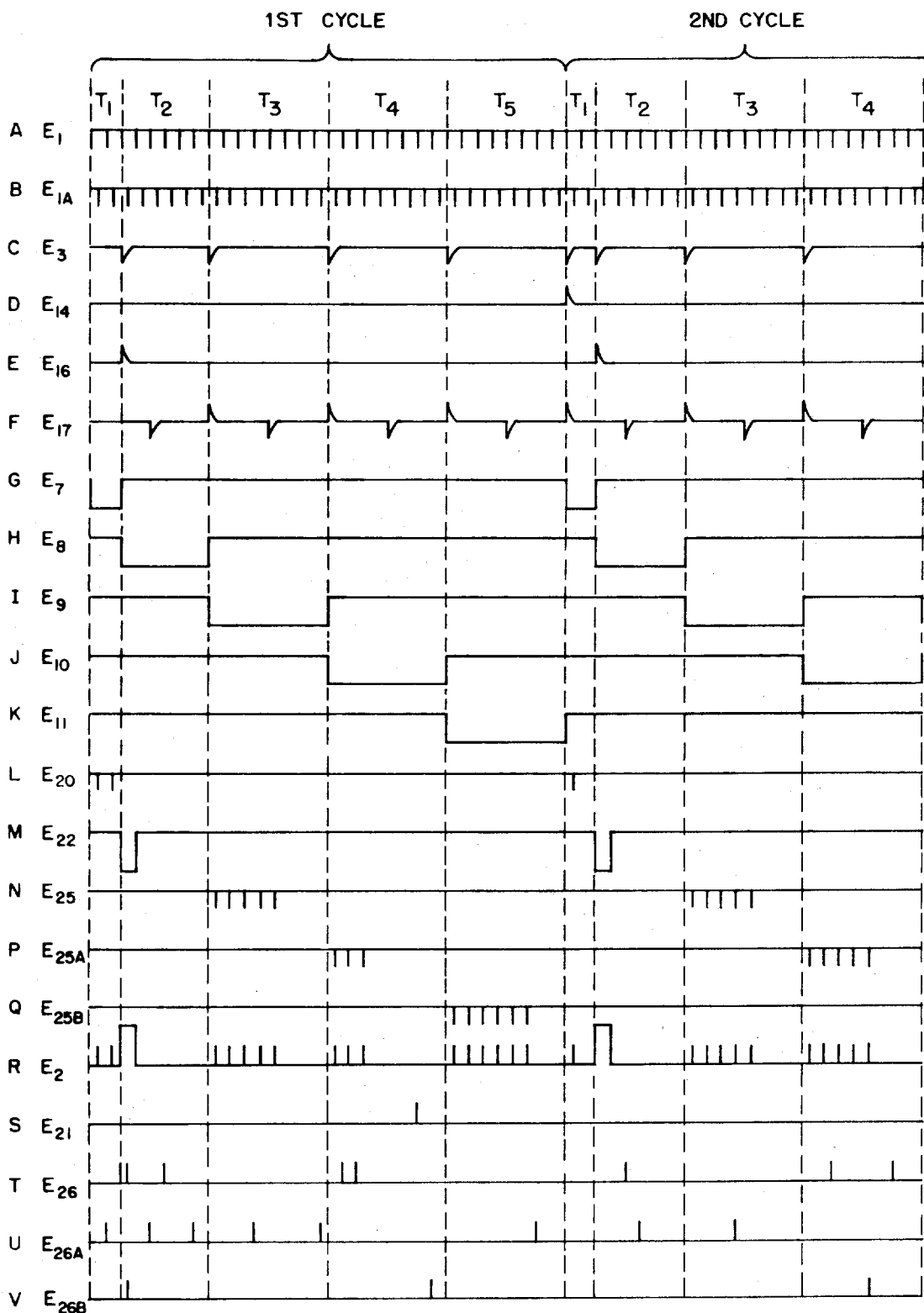


FIG. 4

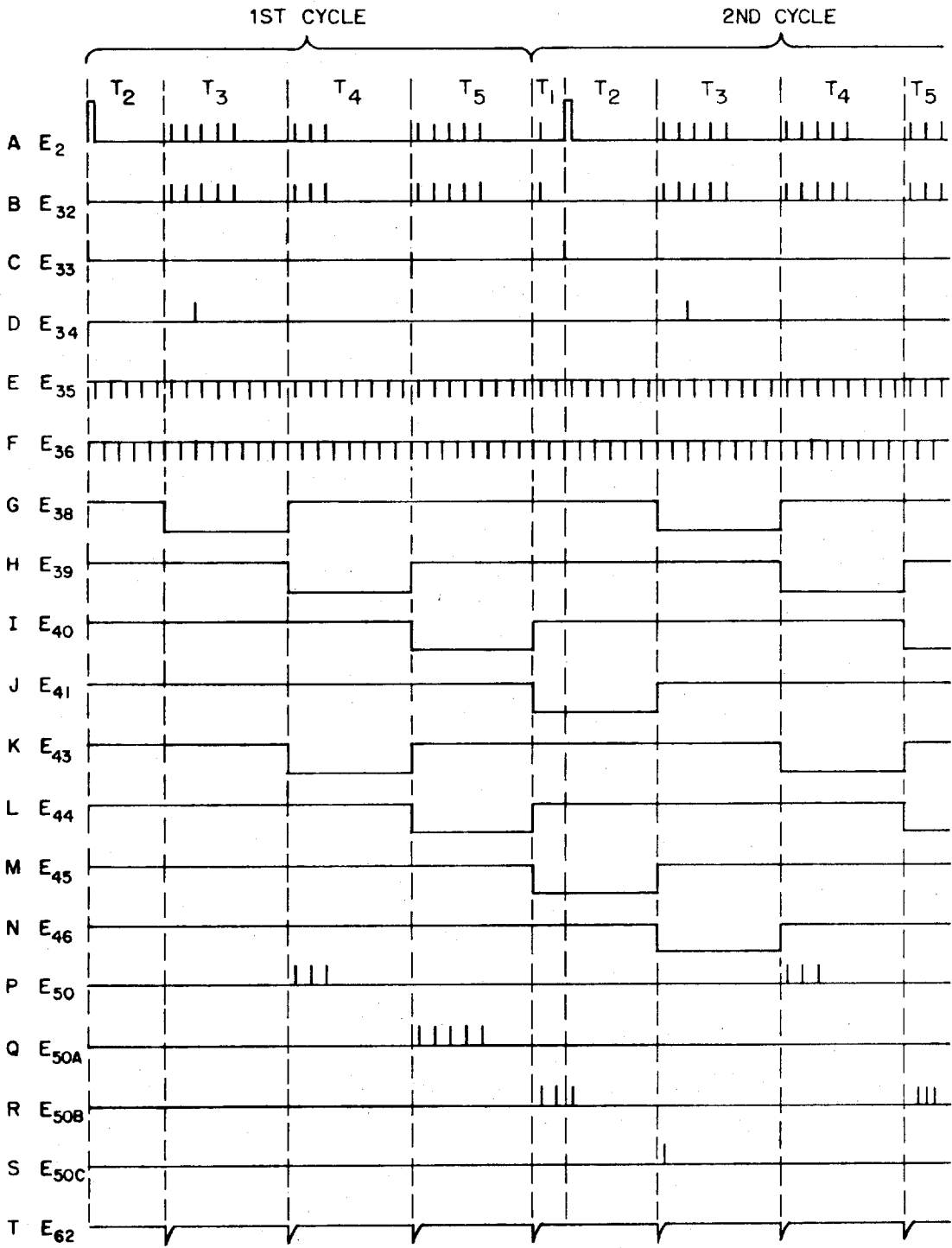


FIG. 5

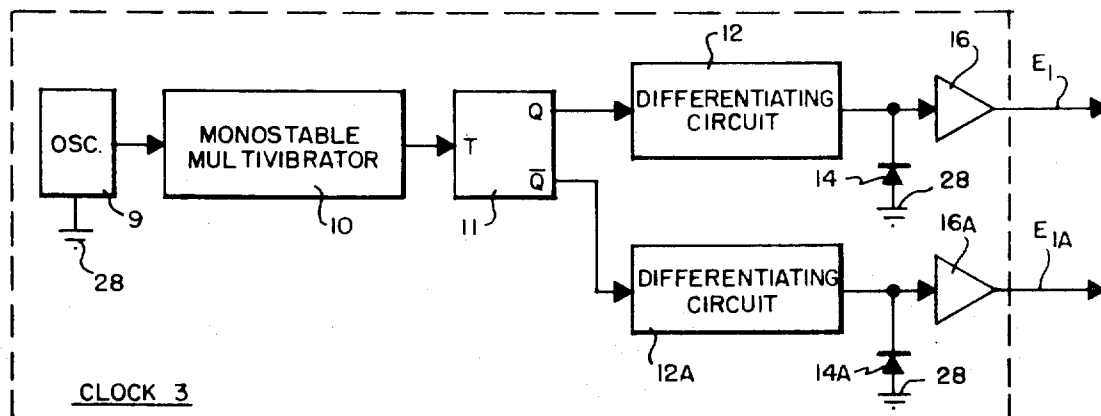


FIG. 6

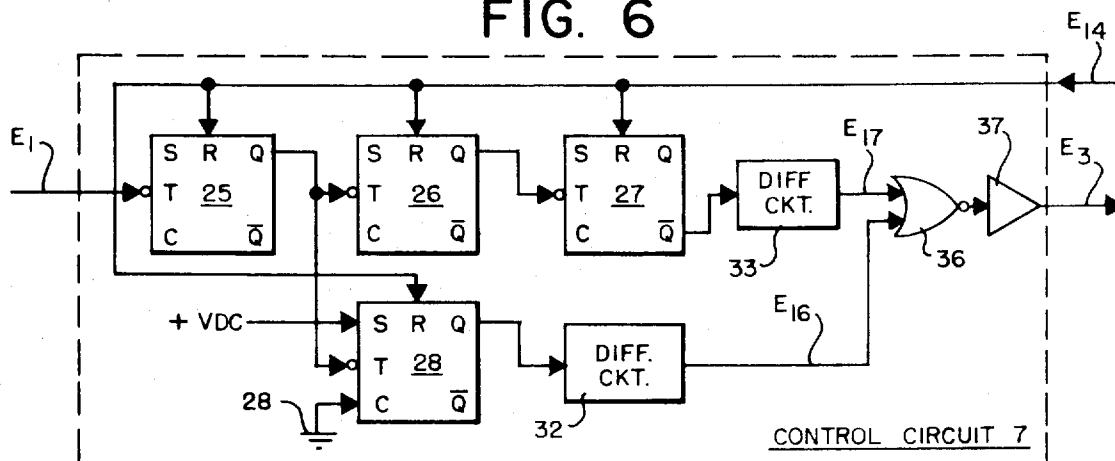


FIG. 7

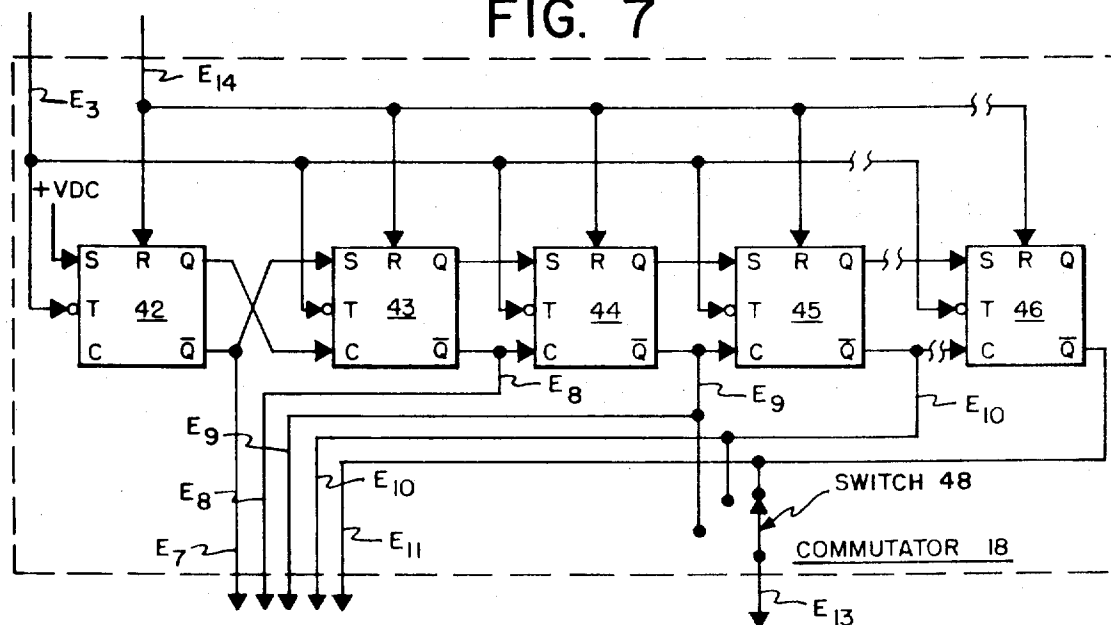


FIG. 8

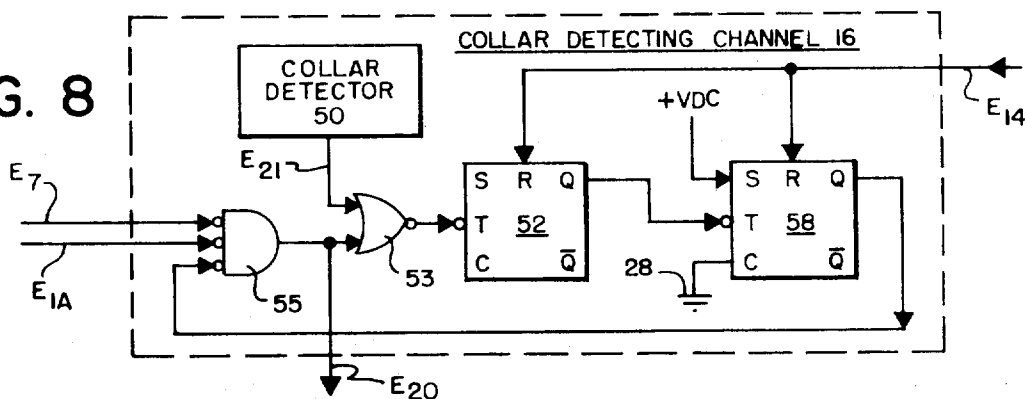


FIG. 9

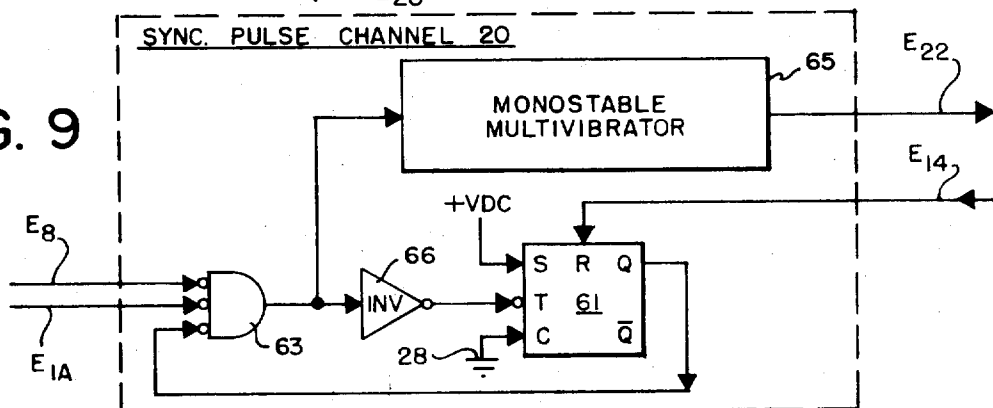


FIG. 10

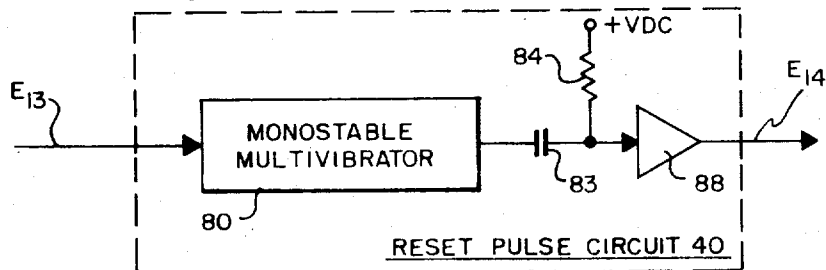
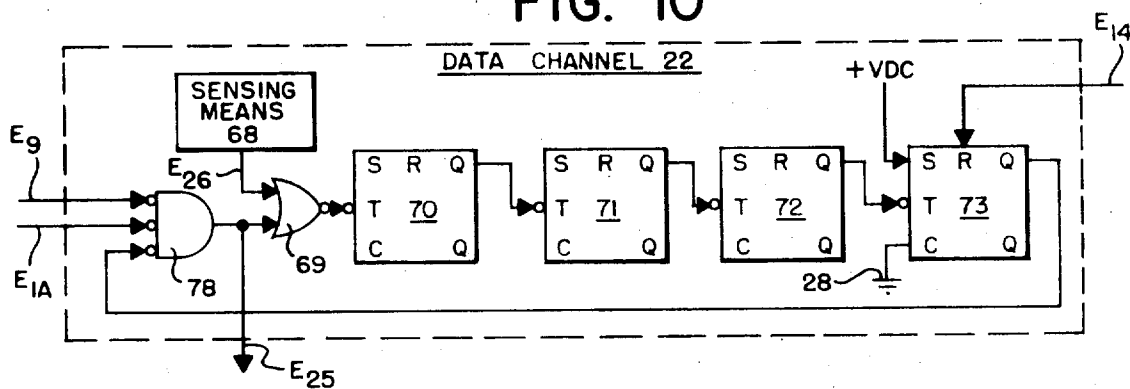


FIG. 11

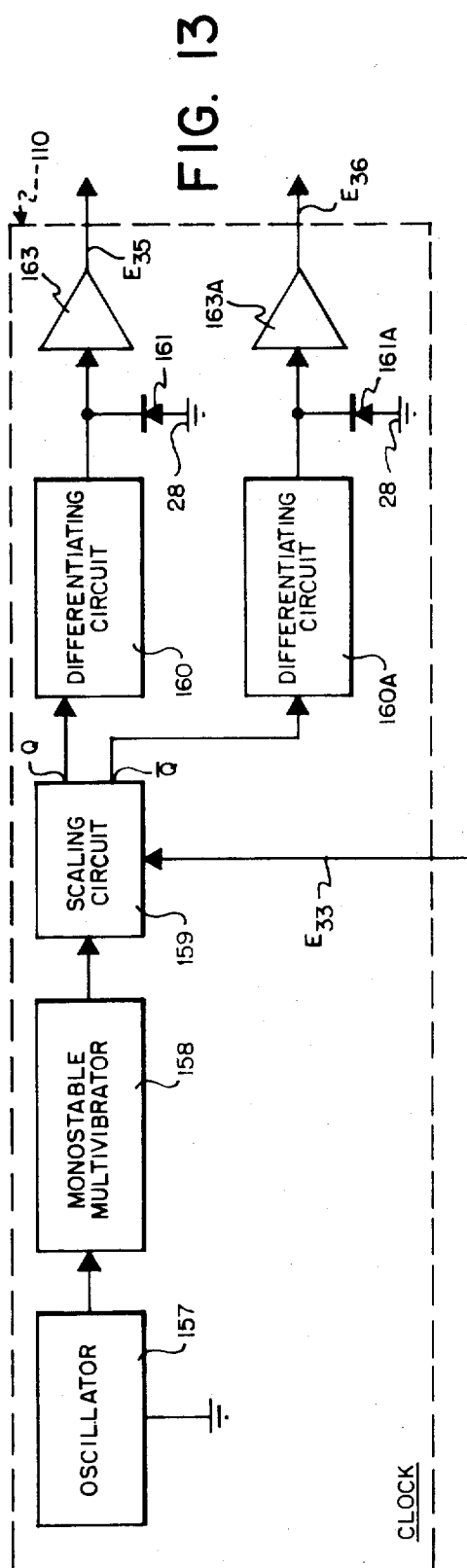
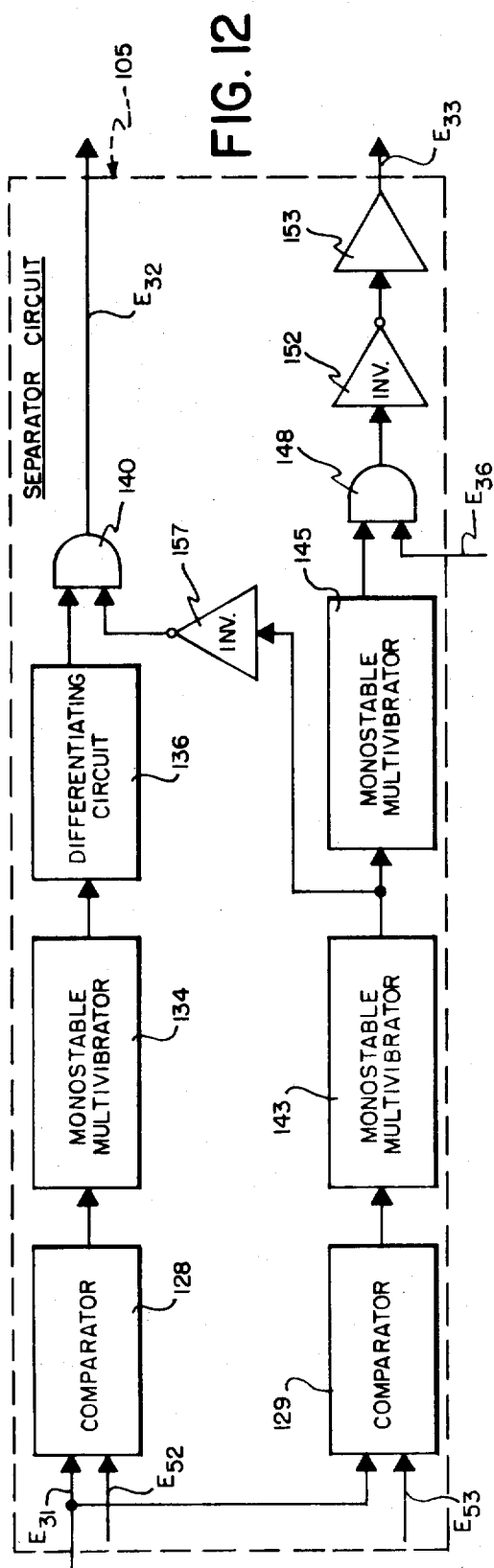
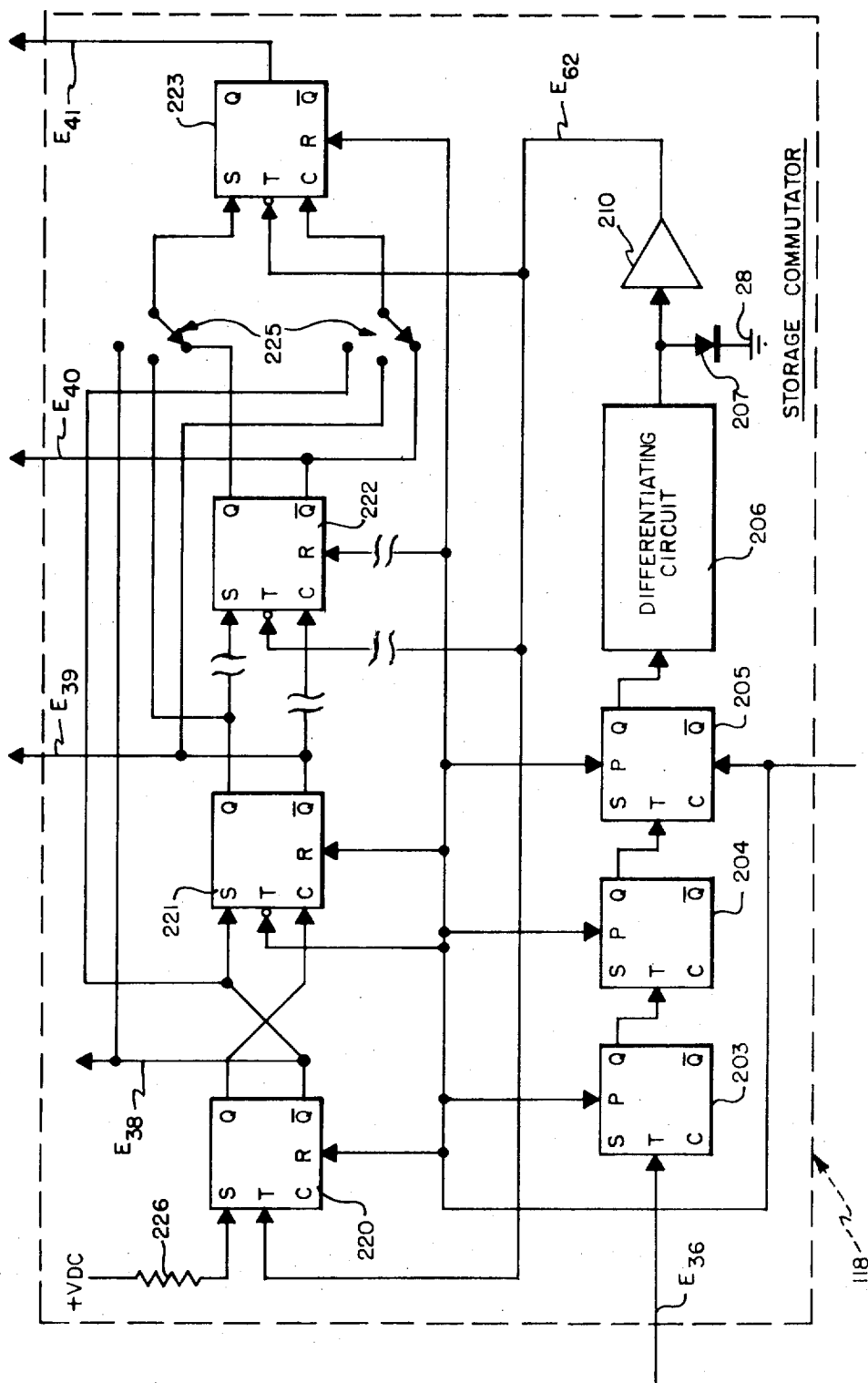


FIG. 15



MEANS AND METHOD FOR TIME-SHARING MULTICHANNEL WELL LOGGING

BACKGROUND OF INVENTION

1. Field of the Invention

The present invention relates to well logging systems and, more particularly, to a multichannel well logging system.

2. Description of the Prior Art

Heretofore, multichannel well logging systems use a conductor in a cable for each channel in transmitting information from the downhole sensors to the surface logging equipment. This type of logging equipment requires multiconductor cables which present several problems. The number of conductors in a cable limits the number of channels that can be used. If enough conductors are used, the cable may become unwieldy. Another problem with a multiconductor cable is that substantial cross talk may exist between conductors which would affect the well logging. A third problem is economics; a multiconductor cable is usually more expensive than a single conductor cable.

The present invention offers an almost unlimited number of channels for the logging of conditions of a borehole. It presents a unique arrangement for time sharing by which a single conductor can handle many channels and thereby eliminate cross talk and reduce cost while using a cable having less bulk for transmitting data from the borehole to the surface.

SUMMARY OF THE INVENTION

A system for providing a plurality of outputs, each output corresponding to a different condition. The system includes a plurality of sensors, each sensor sensing a different condition and providing pulses corresponding in number to the condition. A circuit connected to the sensors is responsive to the pulses from the sensors to provide a pulse train. Each cycle of the pulse train may be divided into time intervals, with the number of pulses in each time interval corresponding to a different sensed condition. A network separates the pulses in the pulse train according to the time intervals and applies the separated pulses to different output circuits. Each output circuit provides the output corresponding to a condition in accordance with the separated pulses for a particular time interval.

One object of the present invention is to use a plurality of sensors to sense different conditions and to transmit the outputs of the sensors to a receiver by a single conductor.

Another object of the present invention is to use sensors in a borehole to provide pulses which correspond in numbers to the sensed conditions, and to transmit the complements of the numbers corresponding to the conditions to a receiver.

Another object of the present invention is to synchronize operation of the well logging electronics in a borehole with the surface well logging electronics so that pulses in a pulse train from the borehole electronics may be separated by the surface electronics according to time interval.

Another object of the present invention is to transmit digital signals corresponding to different information at different time intervals so that the digital signals may be separated according to time interval and thereby require only one signal path for the transmission of the digital signals.

Another object of the present invention is to provide a multichannel well logging system having the capability of increasing or decreasing the number of operative channels by merely setting switches.

The foregoing and other objects and advantages of the invention will appear more fully hereinafter from a consideration of the detailed description which follows, taken together with the accompanying drawings wherein one embodiment of the invention is illustrated by way of example. It is to be expressly understood, however, that the drawings are for illustration purposes only and are not to be construed as defining the limits of the invention.

DESCRIPTION OF THE DRAWINGS

FIGS. 1 and 2 are simplified block diagrams of a well logging system constructed in accordance with the present invention, for providing readouts of a plurality of sensed conditions of a borehole.

FIGS. 3 and 4 are diagrammatic representations of wave forms occurring during operation of the well logging system shown in FIGS. 1 and 2, respectively.

FIGS. 5 through 11 are detailed block diagrams of the clock, the control circuit, the commutator, the collar detecting channel, the sync pulse channel, a data channel, and the reset pulse circuit, respectively, shown in FIG. 1.

FIGS. 12 through 16 are detailed block diagrams of the separator circuits, the clock circuit, the delay sync circuit, the storage commutator, and a data storage circuit, respectively, shown in FIG. 2.

DESCRIPTION OF THE INVENTION

In a preferred embodiment of the invention, a transmitter 1, shown in FIG. 1, in a borehole provides a pulse train E_2 to a receiver 2 outside of the borehole, by way of a single conductor. Each cycle of pulse train E_2 is divisible into several time intervals. The number of pulses in some of the time intervals correspond to different conditions of the borehole or of the earth's formation traversed by the borehole.

Referring now to FIG. 1, a clock 3 provides timing pulses E_1 and E_{1A} , as shown in FIGS. 3A and 3B, respectively. Timing pulses E_1 are used in the generation of control signals, as hereinafter explained, while timing pulses E_{1A} are used with the various channels, as hereinafter explained. Timing pulses E_{1A} are delayed from timing pulses E_1 so that a control signal will not start simultaneously with a timing pulse E_{1A} so as to avoid an ambiguous situation. Clock 3, shown in detail in FIG. 5, includes a conventional type oscillator 9 connected to ground 28 and providing a signal to a monostable multivibrator 10 which, in turn, provides a pulse train to a flip-flop 11. Flip-flop 11 changes state in response to each pulse from multivibrator 10. Differentiating circuits 12, 12A differentiate the Q, $\bar{Q}$ outputs from flip-flop 11 to provide positive and negative spike pulses. Diodes 14, 14A connected to differentiating circuits 12 and 12A, respectively, shunt the negative spike pulses to ground 28 so that only positive spike pulses are applied to inverting amplifiers 16, 16A by differentiating circuits 12 and 12A, respectively. Amplifiers 16, 16A provide timing pulses E_1 and E_{1A} , respectively. It should be noted that since the $\bar{Q}$ output is 180° out of phase from the Q output from flip-flop 11, timing pulses E_{1A} are delayed in time from timing pulses E_1 .

Timing pulses E_1 are applied to a control circuit 7, which provides a pulse train E_3 , shown in FIG. 3C, to a commutator 18 whose pulses initiate the time intervals previously mentioned. Control circuit 7, shown in detail in FIG. 6, includes conventional type flip-flops 25, 26, and 27 connected as a three-stage counter. Control circuit 7 also includes another flip-flop 28 having its toggle input connected to the Q output of flip-flop 25, its set input receiving a positive direct current voltage, and its clear input connected to ground 28. After the flip-flops are reset by a reset pulse E_{14} , shown in FIG. 3D, the first two timing pulses E_1 cause the Q output of flip-flop 28 to change from a low level direct current voltage to a high level direct current voltage. A differentiating circuit 32, which may be of a conventional type, differentiates the change in level of flip-flop 28 Q output to provide a positive spike pulse E_{16} , as shown in FIG. 3E. Flip-flop 28 will not change state again until reset by pulse E_{14} so that differentiating circuit 32 provides pulse E_{16} in response to every second timing pulse E_1 after reset pulse E_{14} .

A conventional type differentiating circuit 33 differentiates the Q output flip-flop 27 to alternately provide negative and positive spike pulses E_{17} , as shown in FIG. 3F, as flip-flop 27 changes state in response to every fourth timing pulse E_1 . The positive pulses E_{16} , E_{17} are inverted and passed by an OR gate 36 to a non-inverting amplifier 37 which provides pulse train E_3 to commutator 18, while the negative pulses E_{17} are blocked by OR gate 36.

Referring to FIG. 1 again, commutator 18 provides control signals E_7 through E_{11} , shown in FIGS. 3G through 3K, respectively, to a collar detecting channel 16, a sync pulse channel 20, and to data channels 22, 22A and 22B, respectively. Each control signal controls a different channel so that timing pulses E_{14} from clock 3 may enter the channel in a particular time interval of each cycle of pulse train E_2 provided to the receiver and so that the channel may provide a pulse output which will become part of pulse train E_2 during the particular time interval. The number of control signals provided by the commutator 18 may be added to or subtracted from as hereinafter explained. Commutator 18 also provides the last control signal in time as signal E_{13} to a reset pulse circuit 40 which provides reset pulse E_{14} .

As shown in FIG. 7, commutator 18 includes flip-flops 42 through 46 connected in a manner so that only one flip-flop is in a set state at any one time and that flip-flops 42 through 46 change states in sequence in response to the pulses in pulse train E_3 from control circuit 7. When a flip-flop is in a set state, its $\bar{Q}$ output is a low level direct current voltage. Control signals E_7 through E_{11} are the $\bar{Q}$ outputs from flip-flops 42 through 46, respectively.

Commutator 18 also includes a rotary switch 48 which may be set to control the number of operative data channels. When switch 48 is set at a position shown in FIG. 7, switch 48 passes control signal E_{11} as signal E_{13} . Switch 48 may be set so that as few as two control signals are used.

The breaks shown with flip-flop 46 indicate that additional flip-flops may be added between the breaks to provide more control signals, if desired.

When reset pulse E_{14} is applied to flip-flop 42, flip-flop 42 will change to a set state since its set input is

receiving a positive direct current voltage. However, since the Q of flip-flop 42 is now a high level direct current voltage, the $\bar{Q}$ output must be applied to the clear input to flip-flop 43 otherwise flip-flop 43 would also be set by the reset pulse. The $\bar{Q}$ output of flip-flop 42, which is now a low level direct current voltage, is applied to the set input of flip-flop 43 so that on next pulse in pulse train E_3 flip-flop 43 is set. The Q and $\bar{Q}$ outputs of flip-flops 43 through 45 are applied to the set inputs and the clear inputs, respectively, of flip-flops 44 through 46, respectively, since none of those flip-flops are set by reset pulse E_{14} .

Collar detecting channel 16, shown in detail in FIG. 8, is rendered operative during a first time interval T_1 of each cycle of pulse train E_2 by the low level of control signal E_7 from flip-flop 42 to provide a pulse signal E_{20} . Pulse signal E_{20} , shown in FIG. 3L, has one pulse when a collar has been detected and two pulses when a collar has not been detected. Collar detecting channel 16 includes a collar detector 50, which may be of the type that uses a changing flux field when a collar is passed to provide a pulse. Detector 50 provides a pulse when a collar is detected to a flip-flop 52 through an OR gate 53 toggling flip-flop 52 to a set state. Control signal E_7 from commutator 18 is applied to a NAND gate 55, which is already partially enabled by a low level direct current voltage from the Q output of a flip-flop 58, causing NAND gate 55 to pass and invert timing pulses E_{14} to flip-flop 52 and to an amplifier 59 in transmitter 1 through an OR gate 60 as pulse signal E_{20} . When detector 50 has detected a collar, flip-flop 52 is in a set state and the first timing pulse E_{14} passed by NAND gate 55 toggles flip-flop 52 to a clear state. The changing level of the Q output from flip-flop 52 toggles flip-flop 58 to a set state causing the Q output from flip-flop 58 to change to a high level thereby disabling NAND gate 55. The disabled NAND gate 55 blocks timing pulses E_{14} so that only one pulse is passed to amplifier 59 during time interval T_1 . Since the set and clear inputs to flip-flop 58 are receiving a positive direct current voltage and being connected to ground 28, respectively, flip-flop 58 will not change state until reset by reset pulse E_{14} . When detector 50 has not detected a collar, flip-flop 52 is not in a set state when control signal E_7 enables NAND gate 55. The first passed pulse E_{14} sets flip-flop 52 while the second passed pulse E_{14} clears flip-flop 52 causing it to set flip-flop 58 so that NAND gate 55 is disabled after passing two pulses to the receiver as pulse signal E_{20} . Pulse signal E_{20} from NAND gate 55 is applied to an amplifier 59 through an OR gate 60 which in turn provides pulse train E_2 in accordance with signal E_{20} and other signals from other channels.

During time interval T_2 of each cycle of pulse train E_2 , control signal E_8 activates sync pulse channel 20, shown in detail in FIG. 9, to provide a sync pulse E_{22} through OR gate 60 to amplifier 59. Sync pulse E_{22} , shown in FIG. 3M, is used to synchronize the operation of receiver 2 with transmitter 1 every cycle, as hereinafter explained. Sync pulse channel 20 includes a flip-flop 61 which provides a low level direct current voltage to a NAND gate 63, when flip-flop 61 is in a clear state, to partially enable NAND gate 63. Control signal E_8 also partially enables NAND gate 63 during time interval T_2 so that a timing pulse E_{14} is inverted

and passes by NAND gate 63. A conventional type monostable multivibrator 65 is triggered by the pulse from NAND gate 63 and provides sync pulse E_{22} whose amplitude is substantially greater than the amplitudes of the pulses from the other channels. Inverter 66 inverts the pulse from NAND gate 63 to trigger flip-flop 61 to a set state thereby disabling NAND gate 63 so that during time interval T_2 , NAND gate 63 inverts and passes only one pulse. Since the set input of flip-flop 61 receives a positive direct current voltage and the clear input is connected to ground 28, flip-flop 61 remains in the set state until reset by reset pulse E_{14} .

During each time interval T_3 , data channel 22 is controlled by control signal E_9 to provide a pulse signal E_{25} to amplifier 59. Pulse signal E_{25} , shown in FIG. 3N, corresponds to a sensed condition of the borehole, as hereinafter explained. Referring to FIG. 10, data channel 22 includes sensing means 68 continually sensing a condition of the borehole such as the surrounding earth formation and providing pulses E_{26} , as shown in FIG. 3T, corresponding in number to the amount of chlorine in the earth formation, through an OR gate 69 to a counter including flip-flops 70 through 73. The details of sensing means 68 are not necessary to one skilled in the art in understanding the present invention and are therefore not shown. However, sensing means 68 may include a sodium iodide (thallium activated), a photomultiplier tube and a discriminator. The discriminator being adjusted to provide pulses E_{26} on a one-to-one basis for those pulses from the photomultiplier tube whose amplitudes correspond to the presence of chlorine in the earth formation. The number of pulses E_{26} in a given time period corresponds to the amount of chlorine in the earth formation. By way of example, there are three pulse signals E_{26} entered in the counter prior to time interval T_3 of the first cycle of pulse train E_2 . A flip-flop 73 is initially in a clear state until a count of eight is reached at which time the Q output of flip-flop 72 triggers flip-flop 73 to a set state. Since its set input is receiving a positive direct current voltage and its clear input is connected to ground 28, flip-flop 73 remains in the set state until reset by pulse E_{14} . The Q output of flip-flop 73 is a low level direct current voltage when flip-flop 73 is in its clear state which partially enables a NAND gate 78 receiving timing pulses E_3 and control signal E_9 . The set input of flip-flop 73 receives a positive direct current voltage while the clear input is connected to ground 28 so that flip-flop 73, when triggered by the Q output of flip-flop 72, remains in a set state until reset by pulse E_{14} . During time interval T_3 , control signal E_9 changes to a low level fully enabling NAND gate 78 along with the Q output from flip-flop 73, so that NAND gate 78 inverts and passes timing pulses E_{14} . The pulses from NAND gate 78 are applied to flip-flop 70 and to amplifier 59, through OR gate 60, as pulse signal E_{25} . The counter counts the pulses from NAND gate 78 until a count of eight is reached. At a count of eight, flip-flop 73 is triggered to its set state thereby disabling NAND gate 78 thus blocking timing pulses E_{14} . The number of pulses in pulse signal E_{25} is equal to eight minus the number of pulses from sensing means 68, or number of E_{25} pulses = 8 - the condition count 1. Thus the number of E_{25} pulses in the first cycle of pulse train E_2 is five.

Data channels 22A and 22B operate during time intervals T_4 and T_5 , respectively, in the same manner as data channel 22 to provide signals E_{25A} and E_{25B} , shown in FIGS. 3P and 3Q, respectively, except that the sensed conditions are temperature and sonic velocity, respectively. The sensing means in data channel 22A may be a conventional type temperature to frequency converter providing signal E_{26A} , as shown in FIG. 3U. The sensing means in channel 22B may be a conventional type time-to-frequency converter and providing signal E_{26B} , shown in FIG. 3V.

Referring to FIG. 11, reset pulse circuit 40 is shown in detail. During the operation of transmitter 1 as heretofore described, commutator 18 applies control signal E_{11} as signal E_{13} to reset pulse circuit 40. When control signal E_{13} changes to a high level at the end of time interval T_5 , a conventional type monostable multivibrator 80 in reset pulse circuit 40 is triggered by the change. The pulse from multivibrator 80 is differentiated by a capacitor 83 and a resistor 84 to provide a positive and a negative spike pulse to an amplifier 88. Amplifier 88 is saturated by a positive direct current voltage applied through resistor 84 so that it effectively passes the negative spike pulse as reset pulse E_{14} and blocks the positive spike pulse. Reset pulse E_{14} resets control circuit 7, commutator 18, and channels 16, 20, 22, 22A and 22B to recycle the operation of the transmitter.

Amplifier 59 amplifies pulse signals E_{20} , E_{22} , E_{25} , E_{25A} and E_{25B} to provide pulse train E_2 .

Referring to FIG. 2, pulse train E_2 , shown in FIG. 4A, is applied by way of a single conductor to an amplifier 100 and a pulse shaping circuit 105 where the pulses in pulse train E_2 are amplified and shaped to provide a pulse train E_{31} . A separator circuit 105 provides data pulses E_{32} , shown in FIG. 4B, on a one-for-one basis with E_{20} , E_{25} , E_{25A} and E_{25B} pulses from collar detecting channel 16 and data channels 22, 22A and 22B in accordance with pulse train E_{31} . Separator circuit 105 also provides sync pulses E_{33} , shown in FIG. 4C, on a one-for-one basis with sync pulses E_{22} from sync pulse channel 20. Sync pulses E_{33} are applied to a sync delay circuit 109 which provides delayed sync pulses E_{34} , shown in FIG. 4D.

A clock circuit 110 provides negative timing pulses E_{35} and E_{36} , shown in FIGS. 4E and 4F, respectively, which are synchronized with timing pulses E_{14} and E_{11} , respectively, from clock 3 by synchronizing pulses E_{32} .

Timing pulses E_{35} and data pulses E_{32} are applied to data storage circuits 114, 114A and 114B and to collar storage circuit 115. Storage circuits 114, 114A, 114B and 115 are controlled by control signals E_{38} , E_{39} , E_{40} and E_{41} , respectively, from a storage commutator 118, to enter data pulses E_{32} during time intervals T_3 , T_4 , T_5 and T_1 , respectively. Each circuit 114, 114A, 114B or 115 is controlled by a control signal E_{43} , E_{44} , E_{45} or E_{46} , respectively, from a complement commutator 120 to enter timing pulses E_{35} during a time interval, other than the time interval that data pulses E_{32} are being entered, until a count of eight is reached, as hereinafter explained, and then not to enter timing pulses E_{35} until the next control signal from complement commutator 120. Storage commutator 118 develops control signals E_{38} , E_{39} , E_{40} and E_{41} , shown in FIGS. 4G through 4J, respectively, in accordance with timing pulses E_{36} and

sync pulse E_{33} . Complement commutator 120 develops control signal E_{43} through E_{46} , shown in FIGS. 4K through 4N, respectively, in accordance with positive timing pulses E_{36} and delayed sync pulses E_{34} .

Timing pulses E_{35} entered by a storage circuit are applied by the storage circuit to a corresponding integrator 122, 122A, 122B or 122C, which may be of a conventional type, as a pulse signal E_{50} , E_{50A} or E_{50B} , respectively. The integrated outputs from integrators 122 and 122A are applied to a recorder 123, which may be of the type manufactured by the Leeds & Northrup Company as a Speedomax G recorder. Recorder 123 provides a log of the conditions sensed in the borehole in accordance with the integrated outputs from integrators 122 and 122A. Integrators 122B and 122C and recorder 124A are connected and operate in a similar manner as integrators 122, 122A, and recorder 124.

Separator circuit 105, shown in detail in FIG. 12, includes conventional type comparators 128, 129 receiving pulse train E_{31} from pulse shaper 101 and direct current reference voltages E_{52} and E_{53} , respectively. The amplitude of reference voltage E_{53} is such that all pulses in pulse train E_{31} cause comparator 128 to provide an output to trigger a monostable multivibrator 134. When triggered, multivibrator 134 provides a pulse output which is differentiated by differentiating circuit 136 to provide a positive and negative spike pulse to an AND gate 140.

The amplitude of reference voltage E_{53} is such that only the sync pulses in pulse train E_{31} cause comparator 129 to trigger another monostable multivibrator 143. Multivibrator 143 when triggered provides a positive pulse which triggers yet another monostable multivibrator 145 to provide an enabling pulse to an AND gate 148. AND gate 148 also receives timing pulses E_{36} from clock circuit 110. AND gate 148 passes a timing pulse E_{36} when multivibrator 145 provides an enabling pulse which is subsequently inverted by an inverter 152 and amplified by amplifier 153 to become sync pulse E_{33} .

When multivibrator 143 provides a positive pulse, the positive pulse is inverted by an inverter 157 and applied to AND gate 140 to disable AND gate 140. When disabled, AND gate 140 blocks the positive and negative spike pulses resulting from the triggering of multivibrator 134 caused by the same pulse in pulse train E_{31} that caused multivibrator 143 to be triggered. The net effect is that there is an absence of a data pulse E_{32} when sync pulse E_{33} occurs to provide for the condition that a data pulse can occur simultaneously with a sync pulse in pulse train E_2 .

Clock 110 is similar to clock 3, except that clock 110 includes an oscillator 157 having a frequency 100 times greater than the frequency of oscillator 9. Oscillator 157 triggers a monostable multivibrator 158 which in turn triggers a series of flip-flops, connected in a conventional manner, to comprise a scaling circuit 159. Scaling circuit 159 provides one pulse for every one hundred pulses from multivibrator 158 and is periodically reset by sync pulse E_{33} to minimize any frequency error between clock 3 and clock 110. The Q, $\bar{Q}$ outputs of the output flip-flop in scaling circuit 159 are applied to differentiating circuits 160 and 160A, respectively. Differentiating circuit 160, a diode 161, and an amplifier

er 163 are connected and operate in the same manner as differentiating circuit 11, diode 14 and amplifier 16, to provide timing pulses E_{35} . Differentiating circuit 160A, a diode 161A, and an inverting amplifier 164 are connected and operate in a similar manner as differentiating circuit 11, diode 14, and amplifier 16, to provide timing pulses E_{36} . Timing pulses E_{35} are delayed in time from timing pulse E_{36} for the same reason that timing pulses E_{14} are delayed in time from timing pulses E_1 .

Referring to FIGS. 2 and 14, sync pulses E_{33} are applied to sync delay circuit 109 which provides a delayed sync pulse E_{34} , shown in FIG. 4D, for every sync pulse E_{33} . Each sync pulse E_{33} resets a flip-flop 166 and a three stage counter including flip-flops 167, 168, and 169. When flip-flop 166 is reset to a clear state, its Q output is a low level direct current voltage which enables a NAND gate 175. NAND gate 175 inverts and passes timing pulses E_{35} from clock circuit 110 when enabled and blocks timing pulses E_{35} when disabled by a high level direct current voltage from flip-flop 166 Q output. The pulses from NAND gate 175 are inverted by an inverter 178 and counted by flip-flops 167, 168 and 169. The Q output of flip-flop 169 changes from a low level to a high level direct current voltage while the Q output changes in an opposite sense in response to the fourth inverted pulse from inverter 178. The change in the $\bar{Q}$ output from flip-flop 169 is differentiated by a differentiating circuit 180 to provide a negative spike pulse to a diode 181 which shunts the negative spike pulse to ground 28. Flip-flop 166 is not affected by the change in the Q output from flip-flop 169 from a low level to a high level direct current voltage.

Flip-flop 169 again changes state in response to the eighth inverted pulse so that its $\bar{Q}$ output changes to a high level direct current voltage. The $\bar{Q}$ output is differentiated by a differentiating circuit 180 to provide a positive spike pulse, which is not shunted to ground 28 by diode 181, to a noninverting amplifier 185 which amplifies the positive spike pulse to provide delayed sync pulse E_{34} . The change in the $\bar{Q}$ output from flip-flop 169 toggles flip-flop 166 to a set state causing the Q output of flip-flop 166 to change to a high level direct current voltage, thereby disabling NAND gate 175. Flip-flop 166 remains in the set state until reset by sync pulse E_{33} since its set input is receiving a positive direct current voltage and its clear input is connected to ground 28.

Storage commutator 118, shown in detail in FIG. 15, includes a counter comprising flip-flops 203 through 206, which may be of the type manufactured by Texas Instruments as circuit type SN 5470, and an amplifier 210 for providing a pulse train E_{63} , as shown in FIG. 4T. The counter is preset to a count of three by sync pulse E_{33} . There are 32 E_{36} pulses for every sync pulse E_{33} . Pulse train E_{63} has negative pulses coinciding with the 5th, 13th, and 29th E_{36} pulses after each sync pulse E_{33} . Flip-flops 203, 204, and 205 count timing pulses E_{36} and the Q output of flip-flop 205 is differentiated by a differentiating circuit 206 to provide positive spike pulses and negative spike pulses. The positive spike pulses are shunted to ground 28 by a diode 207, while the negative spike pulses are amplified by amplifier 210 to provide pulse train E_{63} .

Storage commutator 118 also includes flip-flops 220 through 223, each flip-flop being reset by sync pulse E_{33} and having pulse train E_{42} from amplifier 210 applied to its toggle input. Flip-flops 220, 221 and 222 are connected and operate in a manner similar to flip-flops 42, 43 and 44 of commutator 18, shown in FIG. 7. After being reset to a clear state, flip-flops 220, 221 and 222 change to a set state and then back to the clear state in sequence in response to pulse train E_{42} to provide control signals E_{38} , E_{39} and E_{40} .

The breaks shown with flip-flop 222 indicate that additional flip-flops may be added between the breaks to provide more control signals, if desired.

In the generation of pulse train E_2 in the borehole, the collar detecting time interval T_1 precedes the sync pulse time interval T_2 and each cycle of pulse train E_2 is initiated by reset pulse E_{14} . However, the cycle of operation in the surface electronics is initiated by the sync pulse E_{22} in pulse train E_2 so that time interval T_1 must follow the last time interval assigned to a data channel. In this instance the time interval may be changed by operation of switch 48 in commutator 18. A double check manually operative rotary switch 225 permits time interval T_1 to follow the last time interval assigned to a data channel, as hereinafter explained.

The $\bar{Q}$ output of flip-flop 220 and the Q outputs from flip-flops 221, 222 are connected to different terminals of one deck of rotary switch 225. The Q output of flip-flop 220 and the $\bar{Q}$ outputs of flip-flops 221, 222 are connected to corresponding terminals of a second deck of switch 225. The poles for the first and second decks of switch 48 are connected to the set and the clear inputs, respectively, of flip-flop 223. Switch 225 may be changed to a position corresponding to the number of operative channels. Flip-flop 223 follows in sequence the flip-flop to whose outputs flip-flop 223 is connected to through switch 225.

Complement commutator 120 is identical in construction and operation to storage commutator 118, except that commutator 120 is reset by delay sync pulse E_{34} from sync delay circuit 104 instead of sync pulse E_{33} . This results in complement commutator 120 providing control signals E_{43} through E_{46} which are delayed in time from control signals E_{40} through E_{41} , respectively, from storage commutator 118.

Data storage circuit 114, shown in detail in FIG. 16, includes NAND gates 253 and 254, OR gate 257, flip-flops 260 through 263, and noninverting amplifier 266. NAND gate 253 is controlled by control signal E_{38} from storage commutator 118 so that data pulses E_{32} from separator circuit 105 are inverted and passed during time interval T_3 and blocked during the other time intervals. The passed pulses from NAND gate 253 are applied through OR gate 257 to a three-stage counter comprising flip-flops 260, 261 and 262. Upon termination of time interval T_3 , the count in flip-flops 260, 261 and 262 is the complement of the condition count that was in flip-flops 70, 21 and 72 in data channel 22.

NAND gate 254 is partially enabled by the Q output from flip-flop 263 so that when control signal E_{43} changes to a low level direct current voltage, NAND gate 254 is fully enabled and inverts and passes timing pulses E_{38} to OR gate 257. OR gate 257 inverts and passes the pulses to the counter comprising flip-flops 260, 261 and 262.

When the flip-flops 260, 261 and 262 reach a count of eight, the Q output from flip-flop 262 changes from a high level to a low level direct current voltage which toggles flip-flop 263 to a clear state. While in the clear state, the Q output from flip-flop 263 is a high level direct current voltage which disables NAND gate 254 causing NAND gate 254 to block timing pulses E_{38} . The set input of flip-flop 263 receives a positive direct current voltage while the clear input is connected to ground 28 so that flip-flop 263 when toggled to the clear state remains in the clear state until reset. Control signal E_{35} is amplified by amplifier 266 and applied to flip-flop 263. The trailing edge of control signal E_{35} resets flip-flop 263.

The pulses inverted and passed by NAND gate 254 are also applied to integrator 122 as signal E_{50} . The number of pulses E_{50} equals the count of eight less the complement count in flip-flops 260, 261 and 262, or number of pulses $E_{50} = 8 - \text{complement count}$ 2. However, the complement count is equal to the number of pulses E_{38} occurring during time interval T_3 , so that equation 2 may be rewritten as number of E_{50} pulses = $8 - \text{number of } E_{38} \text{ pulses}$ 3. Substituting for the number of E_{38} pulses from equation 1, equation 3 may be rewritten as number of E_{50} pulses = $8 - (8 - \text{the condition count})$ 4, which reduces to number of E_{50} pulses = the condition count 5.

Data storage circuits 114A and 114B are constructed and operated in a manner identical to data storage circuit 114. Collar storage circuit 115 is similar to data storage circuit 114, except that collar storage circuit 115 has two flip-flops corresponding to flip-flops 260, 263 in data storage circuit 114. The Q output of the flip-flop corresponding to flip-flop 260 is applied to the toggle input of the flip-flop corresponding to flip-flop 263. The maximum number of pulses E_{51} provided by collar storage circuit 115 in a cycle is two.

Although the present invention is shown as providing outputs corresponding to different conditions, it may also be used with radioactive sensing means well known in the art, such as a detector and photo-multiplier tube. The pulses from the photo-multiplier tube are applied to a conventional type pulse height analyzer. The pulse outputs from the analyzer are applied to different data channels as signals E_{38} through E_{46} where they are processed as heretofore described.

The device of the present invention, as heretofore described, uses a plurality of sensors to sense different conditions and to transmit the output of the sensors to a receiver by a single conductor. The sensors are in a borehole and provide pulses which correspond in number to the sensed conditions and the complement of those numbers are transmitted to a receiver. The device of the present invention, as heretofore described, synchronizes the operation of the electronics in a borehole with the operation of electronics on the surface so that the pulse train from the borehole electronics may be separated by the surface electronics according to time intervals. Digital signals corresponding to different information at different time intervals are transmitted by the device of the present invention so that the digital signals may be separated according to time interval by the device of the present invention and thereby require only one signal path for transmitting the digital signals. The device of the present invention,

as heretofore described, is a multichannel well logging system having one signal path between a transmitter in a borehole and a receiver at the surface and has the capability of increasing or decreasing the number of operative channels by merely setting switches.

What is claimed is:

1. A well logging system for providing a plurality of outputs corresponding to different conditions sensed in a borehole, comprising a logging instrument including means for providing pulse signals, each pulse signal being representative of a different condition sensed in the borehole, a plurality of counters connected to the pulse signal means, each counter counting the pulses in a different pulse signal, and means connected to the counters for providing a pulse train, each cycle of the pulse train being divided into predetermined time intervals and the number of pulses occurring in a predetermined time interval is the complement of a count in a corresponding counter; means connected to pulse train means in the logging instrument for transmitting the pulse train; and surface electronics adjacent to the borehole including means connected to the transmitting means for separating the pulses in the pulse train according to the predetermined time intervals, and output means connected to the separating means, each output means receiving the pulses in the pulse train for a different time interval for providing an output corresponding to a sensed condition in accordance with the pulses from the separating means.

2. A system as described in claim 1 in which the pulse train means include a source of timing pulses, means for providing control pulses, each control pulse occurs during a different predetermined time interval, and switching means, each switching means being connected to the source of timing pulses, to a corresponding counter, to the control pulse means and to the transmission system and controlled by the output from the counter and a control pulse from the control pulse means to pass timing pulses to the transmission system and to the counter during a predetermined time interval until the counter reaches a predetermined count so that the number of timing pulses passed by the switching means corresponds to the complement of the count in the counter and to block the timing pulses during the absence of a control pulse or during the presence of the predetermined count in the counter.

3. A system as described in claim 2 in which the pulse train means includes reset means periodically providing a reset pulse.

4. A system as described in claim 3 in which each cycle of the pulse train includes one more time interval, and the pulse train means includes means for providing a synchronizing pulse during the last mentioned time interval.

5. A system as described in claim 4 in which the pulse train means also includes counting means connected to the reset means and being periodically reset by the reset pulse, each counting means being connected to corresponding sensing means and counting the condition pulses therefrom, a source of timing pulses, means for providing a plurality of control signals, and first switching means connected to the separating means, to the counting means and to the control signal means, and responsive to the control signals from the control signal means to pass the timing pulses to different

counting means and to the separating means during each time interval until the counting means controls the first switching means to block the timing pulses when a predetermined count is reached so that the timing pulses provided to the separating means in any time interval correspond to the predetermined count less the count of the pulses from the corresponding sensing means.

6. A system as described in claim 5 in which the synchronizing pulse means includes a flip-flop connected to the reset means and being changed to one state by a reset pulse from the reset means and providing an output, while the flip-flop is in the one state, and providing no output while the flip-flop is in another state, a NAND gate connected to the flip-flop, to the control signal means and to the timing pulse source and controlled by the presence of a control signal from the control signal means and the absence of an output from the flip-flop to pass a timing pulse from the timing pulse source to the flip-flop causing the flip-flop to change from the one state to the other state, and controlled by the absence of a control signal from the control signal means or the presence of an output from the flip-flop to block the timing pulses from the timing pulse source, and a monostable multivibrator connected to the last mentioned NAND gate and to the conductor and responsive to the passed timing pulse from the last mentioned NAND gate for providing a synchronizing pulse having a substantially larger amplitude than the timing pulses from the timing pulse source.

7. A system as described in claim 5 in which the separating means includes a separator network for separating synchronizing pulses from the other pulses in the pulse train, second means for providing a plurality of control signals, each control signal occurring during a different time interval, third means for providing a plurality of control signals, each control signal from the third control signal means being delayed in time by a predetermined amount from a corresponding control signal from the second control signal means, and second switching connected to the first switching means to the control signal means and to the output means and being controlled by the control signals from the second control signal means to pass the pulse train from the first switching means to different output means during each time interval so as to separate the pulses in the pulse train according to time interval.

8. A system as described in claim 9 further comprising a second source of timing pulses, and in which each output means includes counting means connected to the third control signal means, to the second switching means and to the second timing pulse source and counting the pulses passed by the second switching means during a particular time interval of each cycle of the pulse train from the first switching means and controlled by a control signal from the third control signal means to simultaneously count and pass timing pulses from the second timing pulse source as an output corresponding to a condition until a predetermined count of the pulses from the second switching means and the second timing pulse source is reached.

9. A system as described in claim 5 in which the switching means includes a plurality of NAND gates, each NAND gate being connected to the timing pulse source, to the control signal means, to the separating

means and to corresponding counting means and controlled by the control signal means and the counting means to pass the timing pulses during a particular time interval to the separating means and to the counting means until the predetermined count is reached by the counting means, and to block the timing pulses during the remainder of the time interval and during any other time interval.

10. A system as described in claim 9 in which each counting means includes an OR gate connected to corresponding sensing means and to a corresponding NAND gate for passing the condition pulses from the sensing means and the passed timing pulses from the NAND gate, and a counter connected to the OR gate, to the NAND gate and to the reset means for providing a direct current output of one level to the NAND gate while counting the pulses passed by the OR gate until the predetermined count is reached at which time the counter provides a direct current output of another level to the NAND gate so as to disable the NAND gate until the counter is reset by a reset pulse from the reset means.

11. A system as described in claim 5 in which the timing pulse source provides control pulses at the same rate but differing in time from the other pulses; and control signal means includes means connected to the timing pulse source and to the reset means and providing a pulse train whose pulses coincide with the start of each time interval, except for the time interval, in accordance with the control pulses from the timing source and the reset pulse from the reset means, and a plurality of flip-flops connected to the reset means and connected in series to the last mentioned pulse train so that the flip-flop connected to the last mentioned pulse train means is reset to one state while the other flip-flops are reset to another state by the reset pulse from the reset means, the flip-flop connected to the last mentioned pulse train means changes from the one state to the other state in response to a first pulse in the pulse train from the last mentioned pulse train means, each flip-flop of the other flip-flops changes from the other state to the one state in response to a pulse in the pulse train from the last mentioned pulse train means occurring while the preceding flip-flop is in the one state and changing back to the other state in response to the next pulse in the pulse train from the last mentioned pulse train means, and each flip-flop of the plurality of flip-flops remaining in the other state after changing from the one state until reset by a reset pulse from the reset means and providing a control signal while in the one state and providing no control signal while in the other state.

12. A system as described in claim 11 in which the reset pulse means includes a monostable multivibrator connected to the last flip-flop of the series connected flip-flops in the control means and responsive to its control signal to provide a pulse output, a differentiating circuit for providing positive and negative spike pulses in response to the pulse from the monostable multivibrator, and amplifying means connected to the differentiating circuit and biased by a direct current voltage so as to amplify only the positive spike pulse to provide the reset pulse.

13. A system as described in claim 11 in which the last mentioned pulse train means includes a counter

connected to the timing pulse source and to the reset means and being reset by the reset pulse from the reset means, and providing a direct current output which alternately changes from one level to another level in response to every fourth control pulse after being reset, a flip-flop receiving a positive direct current voltage and being connected to ground, to the reset means, and to a first stage of the counter and providing a direct current output which changes from a low level to a higher level in response to a change in the direct current output from a first stage of the counter resulting from the counting of the second control pulse from the timing pulse source after being reset by a reset pulse from the reset means, a pair of differentiating circuits, one differentiating circuit being connected to the third stage of the counter and differentiating the output from the third stage of the counter to provide a positive spike pulse when the output from the third stage of the counter changes from a low level to a higher level and a negative spike pulse when the output from the third stage of the counter changes from the higher level to the low level; the other differentiating circuit being connected to the last mentioned flip-flop and differentiating the output from the last mentioned flip-flop to provide a positive spike pulse when the last mentioned flip-flop changes state, and an OR gate connected to the differentiating circuits for inverting and passing the positive spike pulses from the differentiating circuits and blocking the negative spike pulses.

14. A system as described in claim 13 in which the sensing means and the first mentioned pulse train means are inserted in a borehole having a casing, and one of the sensing means and one of the counting means are used to detect collars in the casing of the borehole.

15. A system as described in claim 14 in which the reset pulse means further includes a manually operable rotary switch connected to some of the series connected flip-flops and which may be set to a predetermined position to select one of the control signals as the control signal that triggers the monostable multivibrator so as to control the number of time intervals in a cycle and the number of conditions to be sensed.

16. A system as described in claim 4 in which the separating means includes a separator network for separating the synchronizing pulses from the other pulses in the pulse train from the pulse train means to provide data pulses and synchronization pulses, first means for providing a plurality of control signals, each control signal occurring during a different time interval, second means for providing a plurality of control signals, each control signal from the second control signal means being delayed in time by a predetermined amount from a corresponding control signal from the first control signal means, and switching means connected to the pulse train means and to the control signal means and having a plurality of output terminals and controlled by the control signals to pass the pulse train to a different output terminal during each time interval so as to separate the pulses in the pulse train according to time interval.

17. A system as described in claim 16 in which the separating means includes means connected to the separator network for providing a delayed synchronization pulse which is delayed in time from the synchronization pulse from the separator network.

18. A system as described in claim 17 in which the separating means further includes a NAND gate connected to the timing pulse source for passing the timing pulses in the other train from the timing pulse source during the absence of a control voltage and blocking the timing pulses during the presence of a control voltage, a counter connected to the amplifier in the separating means and to the NAND gate which is reset by the synchronization pulse from the amplifier and counting the passed timing pulses from the NAND gate to provide an output when a predetermined count is reached, a differentiating circuit connected to the counter and differentiating the output from the counter to provide a positive and a negative spike pulse, switching means connected to the differentiating circuit for passing one of the spike pulses from the differentiating circuit as a delayed synchronization pulse and blocking the other spike pulse, a flip-flop connected to the counter, to the NAND gate and to the amplifier of the separating means and being reset to one state by the synchronization pulse from the amplifier to provide no control voltage and changing to another state in response to an output from the counter to provide a control voltage to the NAND gate until reset by the next synchronization pulse so as to prevent the counter from counting after the predetermined count has been reached until the next synchronization pulse.

19. A system as described in claim 17 in which each control signal means includes counting means connected to the timing pulse source for counting the timing pulses in the one train from the timing pulse source to provide a pulse train whose pulses coincide with the start of each time interval, except the synchronizing pulse time interval, a plurality of flip-flops connected in series to the counting means, and the flip-flop connected to the counting means is reset to one state, while the other flip-flops are reset to another state, the flip-flop connected to the counting means changes from the one state to the other state in response to a first pulse in the pulse train from the counting means, each flip-flop of the other flip-flops changes from the other state to the one state in response to a pulse in the pulse train from the counting means occurring when a preceding flip-flop is in the one state and changing back to the other state in response to the next pulse in the pulse train from the counting means, each flip-flop remaining in the other state after changing from the one state until reset and providing a control signal while in the one state and providing no control signal while in the other state; and the counting means of the first control signal means is periodically preset to another predetermined count by the synchronization pulse and the flip-flops of the first control signal means are periodically reset by the synchronization pulses from the separator network, while the counting means of the second control signal means is periodically preset to the last mentioned predetermined count by the delayed synchronization pulses and the flip-flops of the second control signal means are periodically reset by the delayed synchronization pulses.

20. A system as described in claim 19 in which the first control signal means includes switching means connecting some of the flip-flops to the reset means for controlling the reset means so as to control the number of time intervals in each cycle of the pulse train from the pulse train means.

21. A system as described in claim 20 in which the second and third control signal means each include switching means connecting a last flip-flop of the plurality of flip-flops to some of the other flip-flops for controlling the number of control signals.

22. A system as described in claim 16 in which the synchronizing pulses have substantially larger amplitudes than the other pulses in the pulse train from the pulse train means, and the separator network uses the difference in amplitude to separate the synchronizing pulses from the other pulses in the pulse train.

23. A system as described in claim 22 in which the separator network includes first and second comparators connected to the pulse train means, the first comparator receiving a direct current reference voltage whose amplitude is less than the amplitudes of the pulses in the pulse train and providing an output when a pulse occurs in the pulse train and providing no output when there is no pulse in the pulse train from the pulse train means, and the second comparator receiving a direct current reference voltage whose amplitude is less than the amplitude of the synchronizing pulses but greater than the amplitudes of the other pulses in the pulse train and providing an output when a synchronizing pulse occurs in the pulse train and providing no output when a synchronizing pulse does not occur in the pulse train, first and second monostable multivibrators connected to the first and second comparators, respectively, each multivibrator being responsive to an output from its corresponding comparator to provide a pulse, a differentiating circuit connected to the first multivibrator for differentiating the pulses from the first multivibrator to provide positive and negative spike pulses, an inverter connected to the second multivibrator for inverting the pulses from the other multivibrator, and an AND gate connected to the differentiating circuit and to the inverter for passing the positive spike pulses during the absence of an inverted pulse from the inverter and blocking the spike pulses during the presence of an inverted pulse from the inverter so as to provide a data pulse whenever a pulse, other than a synchronizing pulse, occurs in the pulse train from the pulse train means.

24. A system as described in claim 23 in which a separator network further includes a third monostable multivibrator connected to the second multivibrator and responsive to a pulse from the second multivibrator to provide a pulse, a source providing two trains of timing pulses having the same repetition rate, the timing pulses of one train differing in time from the timing pulses of the other train, a second AND gate connected to the third multivibrator and to the timing pulse source for passing a timing pulse when the third multivibrator provides a pulse and for blocking the timing pulses when the third multivibrator provides no pulse, a second inverter connected to the second AND gate for inverting the passed pulses from the second AND gate, and an amplifier connected to the inverter for amplifying the inverted pulses to provide synchronization pulses coinciding with the synchronizing pulses in the pulse train from the pulse train means.

25. A system as described in claim 24 in which each output means includes counting means connected to the second control signal means, to the switching means and to the timing pulse source for counting pulses passed by the switching means of the separator cir-

cuit during a particular time interval of each cycle of the pulse train from the pulse train means, and controlled by a control signal from the second control signal means to simultaneously count and pass timing pulses in the other train from the timing pulse source as an output corresponding to a condition, until a predetermined number of pulses from the switching means of the separator network and the timing pulse source has been counted.

26. A system as described in claim 25 in which the counting means in each output means resets itself after the termination of the control signal applied to the counting means from the second control signal means.

27. A system as described in claim 26 in which the counting means in each output means includes a flip-flop initially in one state and providing a low level direct current voltage while in that state, and high level direct current voltage while in another state, a NAND gate connected to the timing pulse source, to the second control signal means, and to the flip-flop for passing the timing pulses in the other train from the timing pulse source as an output corresponding to a condition in response to a control signal from the second control signal means and a low level direct current voltage from the flip-flop and blocking the timing pulses in response to high level direct current voltage from the flip-flop or during the absence of a control signal from the second control signal means, an OR gate connected to the switching means of the separator circuit and to the NAND gate for passing the pulses passed by the switching means during a particular time interval of each cycle of the pulse train from the pulse train means and the pulses passed by the NAND gate, a counter connected to the flip-flop and to the OR gate for counting the pulses passed by the OR gate and providing an output to the flip-flop when a predetermined count is reached triggering the flip-flop to another state thereby causing the NAND gate to block the timing pulses in the other train from the timing pulse source, and an amplifier connected between the second control signal means and the flip-flop for amplifying the control signal from the second control signal means so that the trailing edge of the control signal resets the flip-flop to the one state.

28. A well logging method for providing a plurality of outputs corresponding to different conditions sensed in a borehole, which comprises the steps of providing a plurality of pulse signals in the borehole, each pulse

signal being representative of a different condition sensed in the borehole; counting the pulses in each pulse signal in the borehole to provide different counts; providing a pulse train being divided into predetermined time intervals and the number of pulses in a predetermined time interval is the complement of a corresponding count; separating the pulses in the pulse train at the surface according to the predetermined time intervals, and providing the plurality of outputs, each output corresponding to a sensed condition in accordance with the separated pulses for a particular predetermined time interval.

27. A method as described in claim 28 in which the pulse train providing step includes providing timing pulses, adding the timing pulses to one of the counts during one of the predetermined time intervals until the count reaches a predetermined value, passing the timing pulses being added to the count to surface as the pulse train so that the number of passed timing pulses is the complement of the count, and repeating the next previous two steps for each of the remaining counts.

30. A method as described in claim 29 in which the step of providing a pulse train includes a plurality of steps, each step comprises providing timing pulses during a different time interval, counting the condition pulses, counting the timing pulses until a predetermined count of the condition pulses and the timing pulses is reached, and providing the counted timing pulses as part of the pulse train during the time interval.

31. A method as described in claim 29 in which the step of separating the pulses includes separating the synchronizing pulses from the other pulses in the pulse train.

32. A method as described in claim 31 in which the separating step further includes controlling switching means to pass the pulses in the pulse train in a different time interval, other than the synchronizing pulse time interval, as a pulse signal.

33. A method as described in claim 32 in which the providing of each output step includes counting the pulses in a different pulse signal, providing timing pulses, counting the last mentioned timing pulses until a predetermined count of the pulses in the pulse signal and of the last mentioned timing pulses is reached, and providing an output in accordance with the counted last mentioned timing pulses so that the output corresponds to a sensed condition.

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