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[Continued on next page]

(54) Title: RF LOGIC DIVIDER

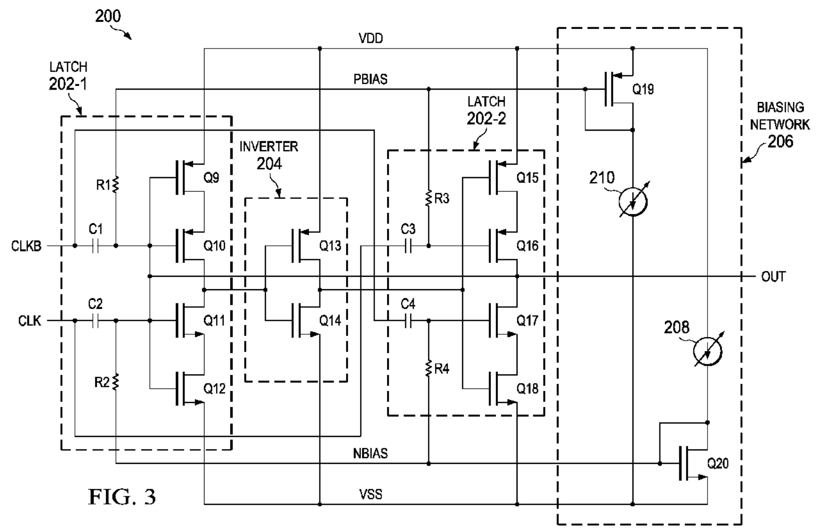

FIG. 3

(57) **Abstract**: A divider (200) apparatus includes latches (202-1,202-2) that are coupled in series with one another in a ring configuration. Each latch includes a tri- state inverter (Q9-1Q12), a first resistor-capacitor network (R1, C1), and a second RC network (R2, C2). The tri-state inverter has a first clock terminal (CLKB) and a second clock terminal (CLK). The first RC network is coupled to the first clock terminal. The second RC network is coupled to the second clock terminal. A biasing network (206) is also provided. The biasing network has a first bias voltage generator (Q19, 210) that is coupled to the first RC network for each latch and a second bias voltage generator (Q20, 208) that is coupled to the second RC network for each latch.

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RF LOGIC DIVIDER

[0001] This relates generally to a divider and, more particularly, to a radio frequency (RF) logic divider.

BACKGROUND

[0002] FIG. 1 shows an example of a conventional phase lock loop (PLL) 100. In operation, a phase/frequency detector (PFD) 102 is able to generate an up signal UP and a down signal DN for the charge pump 104 based on a comparison between a reference signal REF and a feedback signal FB. The charge pump 104 is then able to vary the charge held on low pass filter (LPF) 106 based on the signals UP and DN. The charge held on the LPF 106 can then be used by the voltage controlled oscillator (VCO) 108 to generate an output signal FOUT, and the output signal FOUT can be divided by the divider 110 to generate the feedback signal FB. As a result, the frequency of the output signal FOUT can be chosen from the reference signal REF.

[0003] PLLs (like PLL 110) can be used in RF synthesizers, which can, for example, produce local oscillator signals for RF modulators, and the dividers (like divider 110) can be dynamic-logic based dividers or current mode logic dividers. As an example of a digital dynamic-logic divider that is comprised of two tri-state inverters (e.g., transistors Q1 to Q8) that are coupled in series with one another to form a ring can be seen in FIG. 2. These tri-state inverters (e.g., transistors Q1 to Q8) are coupled between voltage rails VDD and VSS and are coupled to the VCO terminals of VCO 108 so as to receive signals CLK and CLKB. These dividers, however, can have very high current consumption, which makes them impractical for low current (e.g., sub-mA) radios. Therefore, there is a need for an improved divider with lower current consumption.

[0004] An example of a conventional circuit is described in U.S. Patent No. 4,119,867.

SUMMARY

[0005] An apparatus is provided that comprises a plurality of latches coupled in series with one another in a ring configuration, wherein each latch includes: a tri-state inverter with a first clock terminal and a second clock terminal; a first resistor-capacitor (RC) network that is coupled to the first clock terminal; and a second RC network that is coupled to the second clock terminal; and a biasing network having: a first bias voltage generator that is coupled to the first RC network for each latch; and a second bias voltage generator that is coupled to the second RC network for each latch.

[0006] In example implementations, the first RC network may further comprise a capacitor that is coupled to the first clock terminal and that is configured to receive a clock signal; and a resistor that is coupled to the first clock terminal and the first bias voltage generator.

[0007] The capacitor, resistor, and clock signal may further comprise a first capacitor, a first resistor, and a first clock signal, and wherein the second RC network further comprises: a capacitor that is coupled to the first clock terminal and that is configured to receive a clock signal; and a resistor that is coupled to the first clock terminal and the first bias voltage generator.

[0008] The tri-state inverter may further comprise an input terminal; an output terminal; a first PMOS transistor that is coupled to the input terminal at its gate; a second PMOS transistor that is coupled to the drain of the first PMOS transistor at its source, the first clock terminal at its gate, and the output terminal at its drain; a first NMOS transistor that is coupled to the second clock terminal at its gate and the output terminal at its drain; and a second NMOS transistor that is coupled to the source of the first NMOS transistor at its drain and the input terminal at its gate.

[0009] The first bias voltage generator may further comprise a third PMOS transistor that is coupled to the first resistor of each latch at its gate and drain; and an adjustable current source that is coupled to the gate and drain of the third PMOS transistor.

[0010] The adjustable current source may further comprise a first adjustable current source, and wherein the second bias voltage generator further comprises: a third NMOS transistor that is coupled to the second resistor of each latch at its gate and drain; and an adjustable current source that is coupled to the gate and drain of the third NMOS transistor.

[0011] An apparatus is also provided that comprises a first latch having: a first tri-state inverter with a first input terminal, a first output terminal, a first clock terminal, and a second clock terminal; a first resistor-capacitor (RC) network that is coupled to the first clock terminal, wherein the first RC network is configured to receive a first clock signal; and a second RC network that is coupled to the second clock terminal, wherein the second RC network is configured to receive a second clock signal; a second latch having: a second tri-state inverter with a second input terminal, a second output terminal, a third clock terminal, and a fourth clock terminal, wherein the second output terminal is coupled to the first input terminal; a third resistor-capacitor (RC) network that is coupled to the third clock terminal, wherein the third RC network is configured to receive the second clock signal; and a fourth RC network that is coupled to the fourth clock terminal, wherein the fourth RC network is configured to receive the first clock signal; a biasing network having: a first bias voltage generator that is coupled to the first and third RC networks; and a second bias voltage generator that is coupled to the second and fourth RC networks; and an inverter that is coupled to the first output terminal and the second input terminal.

[0012] In example implementations, each of the first, second, third, and fourth RC networks may further comprise a capacitor that is coupled to its clock terminal; and a resistor that is coupled to its clock terminal and its bias voltage generator.

[0013] Each of the first and second tri-state inverters may further comprise a first PMOS transistor; a second PMOS transistor that is coupled to the drain of the first PMOS transistor at its source; a first NMOS transistor that is coupled to the drain of the second PMOS transistor at its drain; and a second NMOS transistor that is coupled to the source of the first NMOS transistor at its drain and the gate of the first PMOS transistor at its gate.

[0014] The provided apparatus may also comprise a phase/frequency detector (PFD) that is configured to receive a reference signal; a charge pump that is coupled to the PFD; a low pass filter (LPF) that is coupled to the charge pump; a voltage controller oscillator (VCO) that is coupled to the LPF, wherein the VCO has a first VCO terminal and a second VCO terminal; and a divider having: a first latch having: a first tri-state inverter with a first input terminal, a first output terminal, a first clock terminal, and a second clock terminal; a first resistor-capacitor (RC) network that is coupled to the first clock terminal, wherein the first RC network is coupled to the first VCO terminal; and a second RC network that is coupled to the second clock terminal, wherein the second RC network is coupled to the second VCO terminal; a second latch having: a second tri-state inverter with a second input terminal, a second output terminal, a third clock terminal, and a fourth clock terminal, wherein the second output terminal is coupled to the first input terminal and to the PFD; a third resistor-capacitor (RC) network that is coupled to the third clock terminal, wherein the third RC network coupled to the second VCO terminal; and a fourth RC network that is coupled to the fourth clock terminal, wherein the fourth RC network is coupled to the first VCO terminal; a biasing network having: a first bias voltage generator that is coupled to the first and third RC networks; and a second bias voltage generator that is coupled to the second and fourth RC networks; and an inverter that is coupled to the first output terminal and the second input terminal.

[0015] The VCO may be configured to output first and second clock signals through the first and second VCO terminals, and wherein the second clock signal is an inverse of the first clock signal. The divider may be configured to divide the first and second clock signals by 2.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] FIG. 1 is a diagram of an example of a conventional PLL;

[0017] FIG. 2 is a diagram of an example of a conventional divider within the PLL of FIG. 1; and

[0018] FIG. 3 is a diagram of an example of a divider in accordance with the present invention that can be used in the PLL of FIG. 1.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0019] FIG. 3 illustrates an example of a divider 200. As shown in this example, divider 200 is a divide-by-2 divider, and this divider 200 can replace divider 110 in PLL 100. Divider 200 is generally comprised of cascaded latches 202-1 and 202-2 coupled together to form a ring with an inverter 204 (which is generally comprised of PMOS transistor Q13 and NMOS transistor Q14) interposed therebetween. Additional stages (e.g., latches and inverters) may be added to increase the division ratio. These latches 202-1 and 202-2 can receive clock signals CLK and CLKB (which are, for example and as shown, inverses of one another) and generate output signal OUT. Bias network 206 is also included to provide bias voltages PBIAS and NBIAS to the latches 202-1 and 202-2.

[0020] In operation, the divider 200 is able to receive, for example, a clock signals CLK and CLKB (which, in this example, form a differential clock signal that can be supplied from VCO terminals of VCO 108) and to produce, for example, a single-ended output signal OUT having a frequency that is one-half of the differential clock signal CLK/CLKB. These latches 202-1 and 202-2 generally comprise tri-state inverters (e.g., MOS transistors Q9 to Q12 and Q15 to Q18) that have input terminals, output terminals, and clock terminals and resistor-capacitor

(RC) networks (e.g., R1/C1 to R4/C4). In this example, the signal CLKB is applied to the clock terminals of the tri-state inverters (e.g., gates of PMOS transistor Q10 and NMOS transistor Q16) through RC networks (e.g., R1/C1 and R4/C4), and, in this example, signal CLK is applied to the clock terminals of the tri-state inverters (e.g., gates of NMOS transistor Q11 and PMOS transistor Q17) through RC networks (e.g., R2/C2 and R3/C3). Capacitors C1 to C4, in this example, should have capacitances that are larger than the capacitance of transistors Q10, Q11, Q16, and Q17. This can allow the latches 202-1 and 202-2 to toggle on the appropriate edges of the differential clock signal CLK/CLKB.

[0021] To allow the latches 202-1 and 202-2 to operate with lower dynamic currents, the gates of transistors Q10, Q11, Q16, and Q17 can be biased. In particular, the bias voltage PBIAS applied through resistors R1 and R3 and the bias voltage NBIAS applied through resistors R2 and R4 cause the gate voltages of transistors Q10, Q11, Q16, and Q17 to be near or above their respective threshold voltages during operation. This means that smaller voltages applied to the gates of transistors Q10, Q11, Q16, and Q17 can cause the latches 202-1 and 202-2 to toggle. Typically, bias voltages PBIAS and NBIAS can be generated with the use of adjustable current sources 208 and 210 (e.g., current digital-to-analog converter or DAC) and diode-connected transistors Q19 and Q20. As shown in this example, PMOS transistor Q19 can be a scaled version of PMOS transistors Q10 and Q16, and NMOS transistor Q20 can be a scaled version of NMOS transistors Q11 and Q17. Alternatively, each latch 202-1 and 202-2 can include a biasing network 206 instead of sharing bias network 206 as shown. Also, as another alternative, the current sources 208 and 210 can be fixed or generally constant current sources. Bias voltages PBIAS and NBIAS could alternatively be generated from a programmable/fixed resistor divider between supply rails.

[0022] As a result of employing this configuration, several advantages can be realized. First, the divider 200 can have lower current consumption than traditional dividers (e.g., divider 110). Second, the biasing network 206 can be configured to provide a self-adaptive bias to circumvent mismatches related to process and temperature variation. Third, the dynamic range can be improved through a direct current (DC) bias setting.

[0023] Those skilled in the art will appreciate that modifications may be made to the example embodiments, and also that many other embodiments are possible, within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. An apparatus comprising:

a plurality of latches coupled in series with one another in a ring configuration, wherein each latch includes:

a tri-state inverter with a first clock terminal and a second clock terminal, a first resistor-capacitor (RC) network that is coupled to the first clock terminal, and a second RC network that is coupled to the second clock terminal; and

a biasing network having a first bias voltage generator that is coupled to the first RC network for each latch, and a second bias voltage generator that is coupled to the second RC network for each latch.

2. The apparatus of Claim 1, wherein the first RC network further comprises a capacitor that is coupled to the first clock terminal and that is configured to receive a clock signal, and a resistor that is coupled to the first clock terminal and the first bias voltage generator.

3. The apparatus of Claim 2, wherein the capacitor, resistor, and clock signal further comprise a first capacitor, a first resistor, and a first clock signal, and wherein the second RC network further comprises:

a capacitor that is coupled to the first clock terminal and that is configured to receive a clock signal; and

a resistor that is coupled to the first clock terminal and the first bias voltage generator.

4. The apparatus of Claim 3, wherein the tri-state inverter further comprises:

an input terminal;

an output terminal;

a first PMOS transistor that is coupled to the input terminal at its gate;

a second PMOS transistor that is coupled to the drain of the first PMOS transistor at its source, the first clock terminal at its gate, and the output terminal at its drain;

a first NMOS transistor that is coupled to the second clock terminal at its gate and the output terminal at its drain; and

a second NMOS transistor that is coupled to the source of the first NMOS transistor at its drain and the input terminal at its gate.

5. The apparatus of Claim 4, wherein the first bias voltage generator further comprises:

a third PMOS transistor that is coupled to the first resistor of each latch at its gate and drain; and

an adjustable current source that is coupled to the gate and drain of the third PMOS transistor.

6. The apparatus of Claim 5, wherein the adjustable current source further comprises a first adjustable current source, and wherein the second bias voltage generator further comprises:

a third NMOS transistor that is coupled to the second resistor of each latch at its gate and drain; and

an adjustable current source that is coupled to the gate and drain of the third NMOS transistor.

7. An apparatus comprising:

a first latch having:

a first tri-state inverter with a first input terminal, a first output terminal, a first clock terminal, and a second clock terminal;

a first resistor-capacitor (RC) network that is coupled to the first clock terminal, wherein the first RC network is configured to receive a first clock signal; and

a second RC network that is coupled to the second clock terminal, wherein the second RC network is configured to receive a second clock signal;

a second latch having:

a second tri-state inverter with a second input terminal, a second output terminal, a third clock terminal, and a fourth clock terminal, wherein the second output terminal is coupled to the first input terminal;

a third resistor-capacitor (RC) network that is coupled to the third clock terminal, wherein the third RC network is configured to receive the second clock signal; and

a fourth RC network that is coupled to the fourth clock terminal, wherein the fourth RC network is configured to receive the first clock signal;

a biasing network having:

a first bias voltage generator that is coupled to the first and third RC networks; and

a second bias voltage generator that is coupled to the second and fourth RC networks; and

an inverter that is coupled to the first output terminal and the second input terminal.

8. The apparatus of Claim 7, wherein each of the first, second, third, and fourth RC networks further comprises a capacitor that is coupled to its clock terminal, and a resistor that is coupled to its clock terminal and its bias voltage generator.

9. The apparatus of Claim 8, wherein each of the first and second tri-state inverters further comprises:

a first PMOS transistor;

a second PMOS transistor that is coupled to the drain of the first PMOS transistor at its source;

a first NMOS transistor that is coupled to the drain of the second PMOS transistor at its drain; and

a second NMOS transistor that is coupled to the source of the first NMOS transistor at its drain and the gate of the first PMOS transistor at its gate.

10. The apparatus of Claim 9, wherein the first bias voltage generator further comprises:

a third PMOS transistor that is coupled to the resistor of each of the first and third RC networks at its gate and drain; and

an adjustable current source that is coupled to the gate and drain of the third PMOS transistor.

11. The apparatus of Claim 10, wherein the adjustable current source further comprises a first adjustable current source, and wherein the second bias voltage generator further comprises:

a third NMOS transistor that is coupled to the resistor of each of the second and fourth RC networks at its gate and drain; and

an adjustable current source that is coupled to the gate and drain of the third NMOS transistor.

12. An apparatus comprising:

a phase/frequency detector (PFD) that is configured to receive a reference signal;

a charge pump that is coupled to the PFD;

a low pass filter (LPF) that is coupled to the charge pump;

a voltage controller oscillator (VCO) that is coupled to the LPF, wherein the VCO has a first VCO terminal and a second VCO terminal; and

a divider having:

a first latch having:

a first tri-state inverter with a first input terminal, a first output terminal, a first clock terminal, and a second clock terminal;

a first resistor-capacitor (RC) network that is coupled to the first clock terminal, wherein the first RC network is coupled to the first VCO terminal; and

a second RC network that is coupled to the second clock terminal, wherein the second RC network is coupled to the second VCO terminal;

a second latch having:

a second tri-state inverter with a second input terminal, a second output terminal, a third clock terminal, and a fourth clock terminal, wherein the second output terminal is coupled to the first input terminal and to the PFD;

a third resistor-capacitor (RC) network that is coupled to the third clock terminal, wherein the third RC network coupled to the second VCO terminal; and

a fourth RC network that is coupled to the fourth clock terminal, wherein the fourth RC network is coupled to the first VCO terminal;

a biasing network having:

a first bias voltage generator that is coupled to the first and third RC networks; and

a second bias voltage generator that is coupled to the second and fourth RC networks; and

an inverter that is coupled to the first output terminal and the second input terminal.

13. The apparatus of Claim 12, wherein each of the first, second, third, and fourth RC networks further comprises:

a capacitor that is coupled to its clock terminal; and

a resistor that is coupled to its clock terminal and its bias voltage generator.

14. The apparatus of Claim 13, wherein each of the first and second tri-state inverters further comprises:

a first PMOS transistor;

a second PMOS transistor that is coupled to the drain of the first PMOS transistor at its source;

a first NMOS transistor that is coupled to the drain of the second PMOS transistor at its drain; and

a second NMOS transistor that is coupled to the source of the first NMOS transistor at its drain and the gate of the first PMOS transistor at its gate.

15. The apparatus of Claim 14, wherein the first bias voltage generator further comprises:

a third PMOS transistor that is coupled to the resistor of each of the first and third RC networks at its gate and drain; and an adjustable current source that is coupled to the gate and drain of the third PMOS transistor.

16. The apparatus of Claim 15, wherein the adjustable current source further comprises a first adjustable current source, and wherein the second bias voltage generator further comprises:

a third NMOS transistor that is coupled to the resistor of each of the second and fourth RC networks at its gate and drain; and

an adjustable current source that is coupled to the gate and drain of the third NMOS transistor.

17. The apparatus of Claim 16, wherein the VCO is configured to output first and second clock signals through the first and second VCO terminals, and wherein the second clock signal is an inverse of the first clock signal.

18. The apparatus of Claim 17, wherein the divider is configured to divide the first and second clock signals by 2.

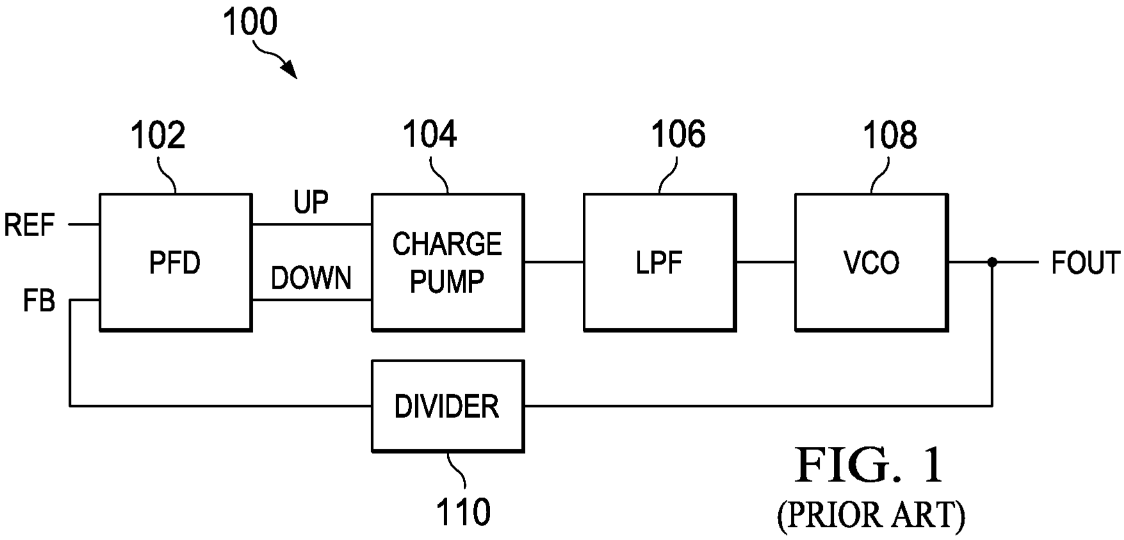

FIG. 1
(PRIOR ART)

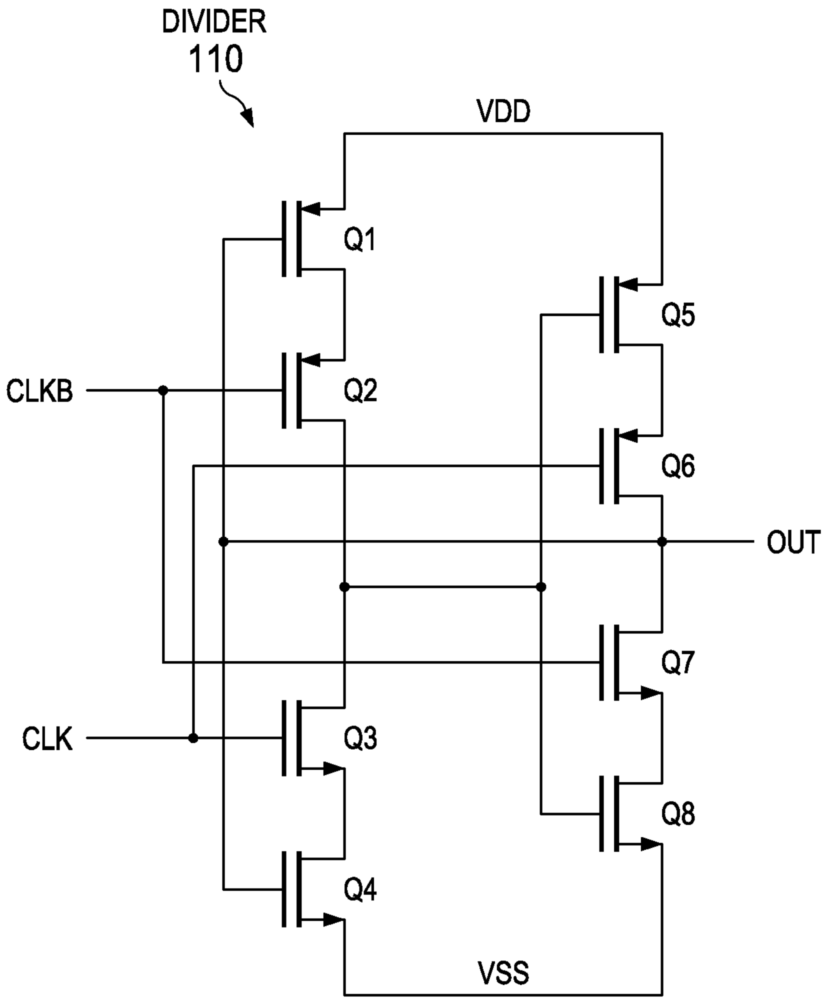

FIG. 2
(PRIOR ART)

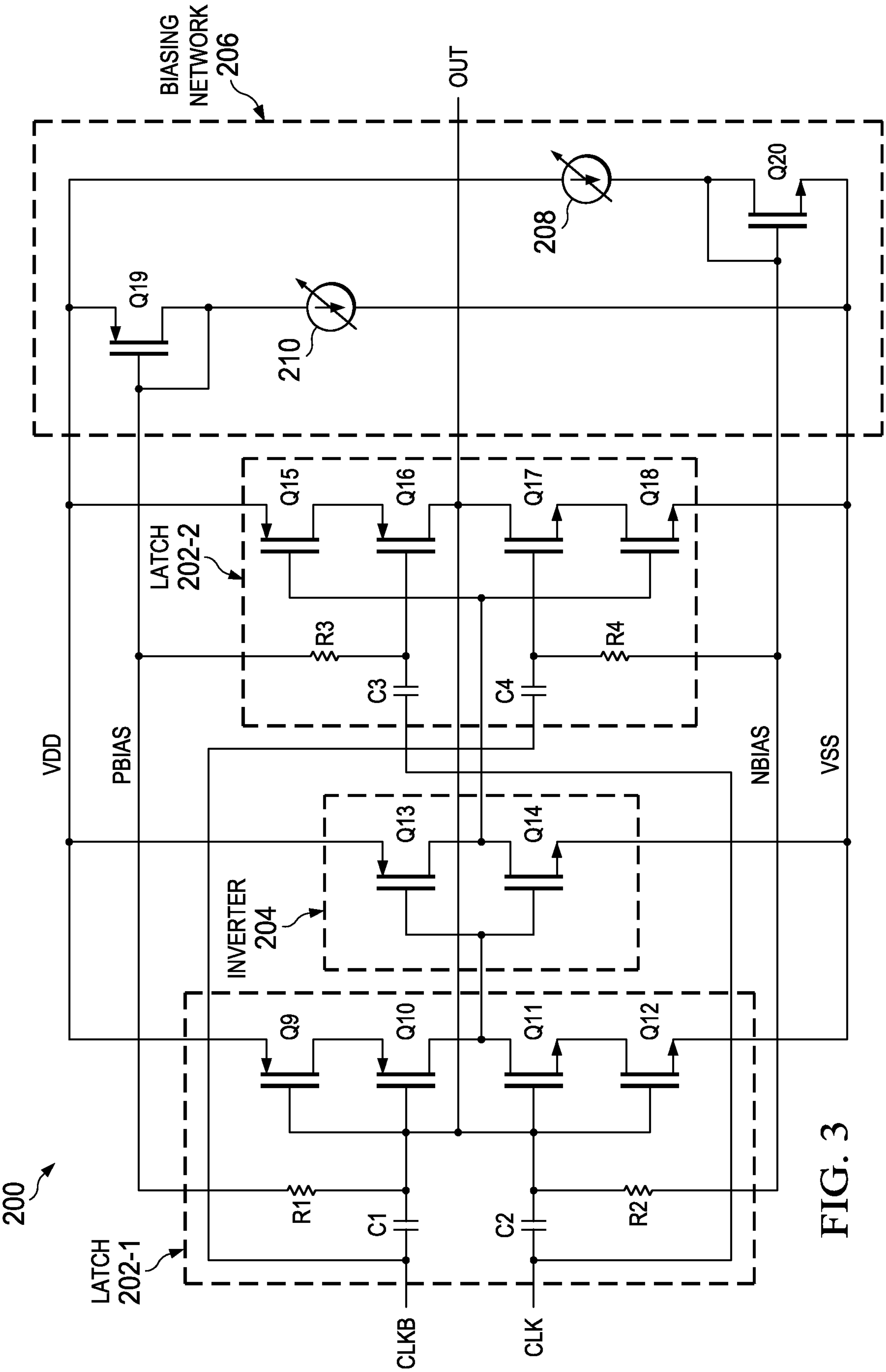
BIASING NETWORK 206
OUT
Q19
210
208
Q20
LATCH 202-2
Q15
Q16
Q17
Q18
R3
R4
C3
C4
VDD
PBIAS
NBIAS
VSS
INVERTER 204
Q13
Q14
200
Q9
Q10
Q11
Q12
R1
R2
C1
C2
LATCH 202-1
CLKB
CLK

FIG. 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/059451

A. CLASSIFICATION OF SUBJECT MATTER

H03K 21/00(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K 21/00; H03B 19/00; H03K 19/094; G06F 1/04; H03L 5/00; G06F 7/44; H03K 3/354

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: divider, charge pump, inverter, transistor, latch, biasing network, voltage generator, current

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2009-0256596 A1 (OH) 15 October 2009 See paragraphs [0066]-[0075], and figures 7-9.	1-18
A	US 2010-0073027 A1 (ZHANG et al.) 25 March 2010 See paragraphs [0020]-[0030], and figures 1-3.	1-18
A	US 2008-0042699 A1 (NARATHONG et al.) 21 February 2008 See abstract, paragraphs [0033]-[0050], and figures 3-10.	1-18
A	JP 2001-257567 A (HITACHI LTD) 21 September 2001 See abstract, paragraphs [0031]-[0050], and figures 1-8.	1-18
A	US 2010-0219873 A1 (CHANG et al.) 02 September 2010 See abstract, paragraphs [0021]-[0029], and figures 1-6.	1-18

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 December 2013 (23.12.2013)	**24 December 2013 (24.12.2013)**

Name and mailing address of the ISA/KR	Authorized officer
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