



- (51) International Patent Classification:
H01L 21/302 (2006.01) *H01L 21/764* (2006.01)
- (21) International Application Number:
PCT/CN2011/079859
- (22) International Filing Date:
20 September 2011 (20.09.2011)
- (25) Filing Language: English
- (26) Publication Language: English
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- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: METHOD FOR FORMING AIR GAP INTERCONNECT STRUCTURE

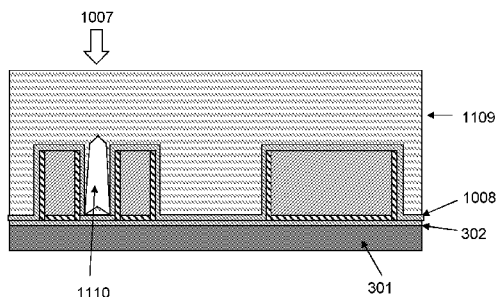


FIG 10

(57) Abstract: Embodiments of the present invention provide a method for forming air gap interconnect structure. A first step of the method is to form conductive structures on a substrate, the conductive structures are separated by sacrificial material. A scale of the conductive structures is lower than 65nm and the conductive structures are polished by both Chemical Mechanical Polishing (CMP) and Stress-Free ElectroPolishing (SFP). A second step of this method is to remove the sacrificial material to form recesses between the conductive structures. And a third step of this method is to non-conformally deposit dielectric material over the conductive structure and in the recesses, so as to form air gaps within the dielectric material in the recesses. No hard mask is deposited during the formation of the conductive structures.



METHOD FOR FORMING AIR GAP INTERCONNECT STRUCTURE

FIELD OF THE INVENTION

[0001] The present invention relates to semiconductor manufacture. More specifically, the present invention relates to improvements to an air gap interconnect structure for applications in 65nm or smaller technology.

BACKGROUND

[0002] With the recent semiconductor development, very large scale integrated circuits (VLSI) and ultra large scale integration (ULSI) are widely required in the semiconductor industry. VLSI and ULSI typically have complex multilevel structures, tiny line width and line space which contain patterns of metal wiring layer and dielectric material to insulate the metal wire. The performance of VLSI and ULSI are limited by the interconnect capacitance, especially in ultra tiny feature size integrated circuit. In a RC circuit, the value of time constant is equal to the product of the circuit resistance and the circuit capacitance (RC), and the power consumption is equal to the product of the capacitance, square of the voltage and the frequency (CV^2f). Therefore the resistance and capacitance determine the performance of the semiconductor devices. In order to reduce the resistance, copper (Cu) is used as an effectively conductive line to replace aluminum (Al) in VLSI and ULSI, and a low-k dielectric material, such as aromatics hydrocarbon thermosetting polymer (SiLK) is considered to replace the traditional dielectric material, such as silicon dioxide (SiO_2), which can effectively reduce the capacitance of VLSI and ULSI.

[0003] The mechanical property of low-k dielectric material restricts the developments of VLSI and ULSI, due to the low Young's modulus of low-k dielectric, as shown in TABLE 1. The mechanical strength of copper will weaken square with the copper line width decrement, as shown in FIG.1. With the purpose of removing the excess copper line, a planarizing polish process, such as a chemical mechanical planarization (CMP) is applied. Because of the mechanical weakness of low-k material and the huge young's modulus difference between the low-k dielectric material and copper, the conductive line will appear deformed during the

CMP process and result in a short circuit or an open circuit of VLSI and ULSI. It would be very possible that the copper line may be destroyed by the CMP during the process. Therefore, low-k dielectric material can not become a main current dielectric material and replace the traditional dielectric material.

[0004] Table 1 Mechanical and electrical property of dielectric material

Dielectric Material	Young's Modulus (GPa)	Permittivity
SiO ₂	70	3.9
SiLK	2.5	2.2

[0005] In order to overcome this issue, air gap interconnection structure is developed. The permittivity of air is equal to 1, which is much lower than traditional dielectric material (SiO₂) at approximately 3.9, if air is formed between copper lines, the dielectric constant of the dielectric layer will be decreased significantly. The air gap process can provide a relative low-k dielectric constant, the air gap combined with dielectric material can be consider as a porous material with permittivity depending on the volume of the air gap. US 7,501,347, US 7,629,268 and US 7,361,991 have provided some methods to form air-gap structures larger than 90-nm scale, however, when the feature size is decreased, the traditional damascene processes, especially the processes using CMP to planarize the copper line surfaces, are facing serious bottleneck. It would be a big problem on how to eliminate the stress on the copper lines.

[0006] Hence, the stress-free-polishing (SFP) is invented to overcome this bottleneck. SFP bases on the electrochemical mechanism to polish the excess copper line without erosion and mechanical stress. By using SFP, the copper line will not be damaged. The damascene technique integrated with SFP process can form an air-gap structure with a scale smaller than 65 nm.

SUMMARY

[0007] According to the present invention, an improved damascene technique integrated with SFP technique is provided. The technique uses copper as a main conductor layer and solves the following problems:

[0008] 1) No hard mask is used. In prior art, in order to protect the sacrificial polymer layer, commonly a hard mask is formed above the sacrificial polymer layer, the hard mask has a higher mechanical strength to resist the stress during the CMP process. The method according to the present invention utilizes SFP instead of CMP to 错误！超链接引用无效。 the excess copper, as a result the processes of depositing and removing the hard mark may be removed because the SFP process will not bring any stress to the copper lines. The method of the present invention simplifies the whole process and reduces the cost by removing the processes of the hard mask.

[0009] 2) In prior art, a part of the dielectric materials will be reserved to protect the flanks of copper lines so as to avoid potential damages to the copper lines caused by the polishing process. Therefore, the air gaps can not be formed in narrow line space areas or only smaller air gaps can be formed in these areas. That is the reason why air gap interconnect structure is not applied to narrow interconnect structures, such as first metal layer (M1 layer) structures, even the permittivity has the most significant impact in this layer. The method of the present invention may also remove the reserved dielectric materials since no stress will be applied by the SFP process. Therefore, the air gaps can be formed in narrow line spaces, such as the spaces having a scale less than 65nm. And a relatively larger air gap may be formed in the spaces between copper lines and the shape of the air gap is optimized. The permittivity of dielectric will be significantly reduced, and the RC delay and the power consumption will be further reduced. The tiny node VLSI and ULSI dissipation problem will be solved.

[0010] According to an embodiment of the present invention, a method for forming air gap interconnect structure is provided. Trench and via are selectively etched in an insulating structure composed by sacrificial material. Conductive structures are formed in the trench and via, the conductive structures are separated by sacrificial material. A scale of the conductive structures is lower than 65nm. Then deposit a barrier and remove the barrier by XeF_2 selective thermal flow etching. The conductive structures are plated by copper and the copper is polished by both Chemical Mechanical Polishing (CMP) and Stress-Free ElectroPolishing (SFP) in sequence. The sacrificial material are removed by plasma etch to form recesses between the conductive structures. Then deposit a insulating film serving as a sealing dielectric on entire surface. Dielectric material is non-conformally deposited over the

conductive structure and in the recesses by Chemical vapor deposition (CVD) so as to form air gaps within the dielectric material in the recesses. No hard mask is deposited during the formation of the conductive structures.

[0011] According to an embodiment of the present invention, a copper sealing layer is non-conformally deposited on the conductive structure after removing the sacrificial material and prior to non-conformally depositing dielectric material.

[0012] According to an embodiment of the present invention, a sacrificial removal stop layer is formed on the substrate prior to forming conductive structure on the substrate.

BRIFE DESCRIPTION OF THE DRAWING

[0013] FIG. 1 is a diagram illustrating the relation between copper line width and its mechanical strength.

[0014] FIG. 2 is a cross-sectional view of the initial structure of the substrate according to the method for forming an air gap interconnect structure of the present invention.

[0015] FIG. 3 is a cross-sectional view of the structure of the substrate after a pattern process according to the method for forming air gap interconnect structure of the present invention.

[0016] FIG. 4 is a cross-sectional view of the structure of the substrate after recesses are formed according to the method for forming air gap interconnect structure of the present invention.

[0017] FIG. 5 is a cross-sectional view of the structure of the substrate after a barrier layer and a main conductive copper layer is deposited according to the method for forming air gap interconnect structure of the present invention.

[0018] FIG. 6 is a cross-sectional view of the structure of the substrate after the main conductive copper layer is smoothed by CMP according to the method for forming air gap interconnect structure of the present invention.

[0019] FIG. 7 is a cross-sectional view of the structure of the substrate after the main conductive copper layer is polished by SFP according to the method for forming air gap interconnect structure of the present invention.

[0020] FIG. 8 is a cross-sectional view of the structure of the substrate after etching the barrier layer according to the method for forming air gap interconnect structure of the present invention.

[0021] FIG. 9 is a cross-sectional view of the structure of the substrate after removing the insulating film according to the method for forming air gap interconnect structure of the present invention.

[0022] FIG. 10 is a cross-sectional view of the structure of the air gap interconnect structure formed according to the method for forming air gap interconnect structure of the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS

[0023] As shown in FIG. 2, a first dielectric layer 302 is deposited on substrate 301. The first dielectric layer 302 may be one of SiCN, SiC, SiN and SiOC or their combination. A second dielectric layer (sacrificial layer) 303 is deposited on the first dielectric layer 302. The second dielectric layer 303 may be a low-k material or insulating film like an organic film such as a SiLK film. A reflection preventive film 304 and a photo-resist film 305 is sequentially deposited on the second dielectric layer 303.

[0024] The photo-resist film 305 is patterned by exposure to form a photo-resist pattern 405 as shown in FIG. 3. The reflection preventive film 304 is selectively removed by dry etching using the photo-resist pattern 405 as an etching mask and forms a patterned reflection preventive film 404.

[0025] As shown in FIG. 4, the second dielectric layer 503 is selectively removed to form trenches by dry etching using the photo-resist pattern 405 as an etching mask. Thereafter, the photo-resist pattern 405 and the patterned reflection preventive film 404 are removed. Refer to FIG. 4, trenches 506 are formed within the second dielectric layer 503.

[0026] A barrier layer of TaN/Ta 606a is deposited on entire main surface of substrate 301 by using sputtering. Then, the metal layer of copper 606b is deposited on the barrier layer of TaN/Ta 606a by using sputtering and plating in sequence. FIG. 5 shows the structure after the depositions of the barrier layer of TaN/Ta 606a and the metal layer of copper 606b.

[0027] The metal layer of copper 606b is polished to 100nm~200nm of remaining copper film thickness by CMP for smoothing the surface topography, as shown in FIG 6. The remaining copper film is numbered as 706b.

[0028] A stress-free electropolishing (SFP) is performed on the remaining copper film 706b. FIG.7 illustrates the structure after a stress-free electropolishing (SFP) process. After the SFP process, the copper film 806b is polished back to the surface of non-recessed areas, such that metal layer within the recessed regions, i.e., the trenches and/or vias, is isolated from adjacent recessed regions. SFP is a chemical-electrical process: the copper on the wafer substrate works as an anode and an electrolyte nozzle works as a cathode. The copper is dissolved and polished by contacted electrolyte when positive voltage is applied between the anode and the cathode. SFP is a stress free and selective copper removal process. WO2010/020092 discloses a detailed process of SFP.

[0029] The barrier layer of Ta/TaN 906a on the top surface of wafer is removed by XeF_2 gas phase etching. The XeF_2 reacts spontaneously with Ta/TaN at a certain temperature and pressure. XeF_2 is an isotropic selective etching method of Ta/TaN (the barrier layer of Ta/TaN 606a). The XeF_2 gas has good selectivity to both copper 806b and the second dielectric layer 503, which is formed by dielectric materials such as SiO_2 , SiLK, or low k Si-C-O-H based materials. The value k of the low k Si-C-O-H based materials varies from 1.2 to 4.2 and 1.3~2.4 is preferred. During the whole process there is no mechanical stress applied to the barrier layer of Ta/TaN 906a or the second dielectric layer 503 directly, so there is no damage to copper 806b or the second dielectric layer 503 (the dielectric materials). According to an embodiment, the temperature of the substrate varies from 0°C to 300°C and 25°C~200°C is preferred. The pressure of XeF_2 gas during the process is between 0.1Torr and 100 Torr and 0.5 Torr~20 Torr is preferred. FIG. 8 shows the above process.

[0030] The chemical reaction products of XeF_2 and Ta/TaN are in gas phase, such as Xe or volatiles with the processing pressure. An example of the volatiles is tantalum fluoride. Thus, there is no residual on the surface of the wafer.

[0031] As shown in Fig. 8, when the barrier layer 906a exposed on the top surface is removed completely by XeF_2 gas phase etching, the trenches 906 in the semiconductor device is electrically separated completely. The copper layer or copper film 806b and the remaining barrier layer (of Ta/TaN) 906a are completely separated by the low k dielectric layer 503 (formed from the second dielectric layer 303).

[0032] The low k dielectric layer 503 (formed from the second dielectric layer 303) is removed by using reducing gas NH_3 , or H_2/N_2 to form trench 1007, and first dielectric layer 302 serves as an etching stopper. The depth for removal becomes uniform. At the same time, the copper layer or copper film 806b and remaining barrier layer of TaN/Ta 906a does not get any damage. The FIG. 9 shows the above process.

[0033] A third dielectric layer 1008 is deposited on entire surface of substrate, and serves as a sealing dielectric in FIG. 9. The third dielectric layer 1008 maybe one of SiCN, SiC, SiN and SiOC or their combination.

[0034] As shown in FIG. 10, a fourth dielectric layer 1109 is deposited on the third dielectric layer of SiCN 1008 by using non-conformally plasma enhance chemical vapor deposition (PECVD) or thermal chemical vapor deposition (TCVD). Tetraethyl Orthosilicate (TEOS) and Ozone (O_3) are applied in TCVD. Air gap structure are formed by TCVD with temperature from 300°C and 450°C , with best temperature 400°C . Air gaps 1110 are formed in trenches 1007. The trenches 1007 shall have a space between 10nm to 250nm. The fourth dielectric layer 1109 may be one of SiOF, SiOC, Black Diamond (BD) and Black Diamond II (BDII) or their combination.

What is claimed is:

1. A method for forming air gap interconnect structure comprising,
depositing a first dielectric layer;
depositing a second dielectric layer (sacrificial layer);
putting photo mask, then selectively etching the second dielectric layer to form trenches and vias in the second dielectric layer;
depositing barrier layer and seed layer on the second dielectric layer with trench and via;
depositing a metal layer on the seed layer;
partially polishing the metal layer by using Chemical Mechanical Polishing (CMP);
polishing the metal layer to barrier layer by using Stress-Free ElectroPolishing (SFP);
etching the barrier layer;
removing the second dielectric layer by plasma etch to form recesses between the metal structures;
depositing a third dielectric layer serving as a sealing dielectric on entire surface;
non-conformally depositing a fourth dielectric layer over the metal structure and in the recesses by Chemical vapor deposition (CVD) , so as to form air gap structure between the metal lines;
planarizing the top surface of the fourth dielectric layer CMP for smoothing the surface topography.
2. The method of claim 1, wherein the first dielectric layer is on of one of SiCN, SiC, SiN and SiOC or their combination.
3. The method of claim 1, wherein the second dielectric layer is organic material.
4. The method of claim 3, wherein the organic material is SiLK.
5. The method of claim 1, wherein the second dielectric layer is SiOF, SiOC.
6. The method of claim 1, wherein the barrier layer is Ta/TaN, Ti/TiN, or Ru.

7. The method of claim 6, wherein the barrier layer of TaN/Ta or TiN/Ti is deposited by sputtering.

8. The method of claim 1, wherein the seed layer is copper.

9. The method of claim 1, wherein the metal layer is copper.

10. The method of claim 9, wherein the metal layer is deposited by sputtering or Electrochemical plating (ECP).

11. The method of claim 1, wherein partially polishing the copper layer to 100nm~200nm of remaining thickness by Chemical Mechanical Polishing (CMP) for smoothing the surface topography.

12. The method of claim 1, wherein the rest of the metal layer in non-recessed areas is polished by Stress-Free ElectroPolishing (SFP) to isolate the barrier layer of within the recessed regions.

13. The method of claim 1, wherein the barrier layer comprising Ta/TaN or Ti/TiN is removed by XeF₂ gas phase etching.

14. The method of claim 1, wherein the barrier layer comprising Ta/TaN or Ti/TiN is removed by plasma etching.

15. The method of claim 1, wherein the second dielectric layer comprising SiLK comprises is plasma etched by using NH₃, or H₂/N₂ as a reducing gas, and using the first dielectric layer as an etching stopper.

16. The method of claim 1, wherein one of SiCN, SiC, SiN and SiOC or their combination is deposited as the third dielectric layer.

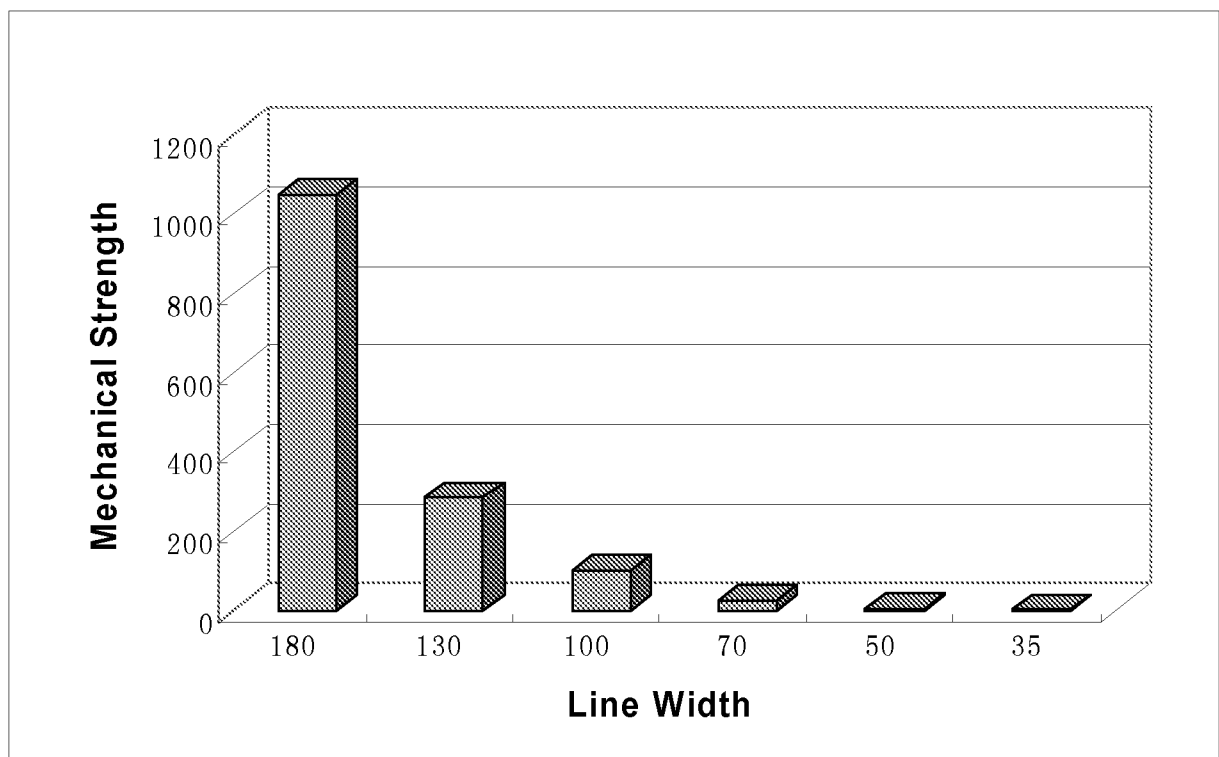
17. The method of claim 1, wherein SiOF, SiOC, Black Diamond (BD), or Black Diamond II (BDII) is non-conformally deposited as the fourth dielectric layer by using Chemical Vapor Deposition (CVD).

18. The method of claim 17, wherein CVD is Plasma Enhance Chemical Vapor Deposition (PECVD) or Thermal Chemical Vapor Deposition (TCVD).

19. The method of claim 18, wherein Tetraethyl Orthosilicate (TEOS) and Ozone (O₃) are applied in the TCVD.

20. The method of claim 18, wherein air gap structure formed by TCVD with temperature from 300°C and 450°C, with best temperature 400°C.

21. The method of claim 1, wherein air gaps are only formed on recesses with a space between 10nm to 250nm.

**FIG 1**

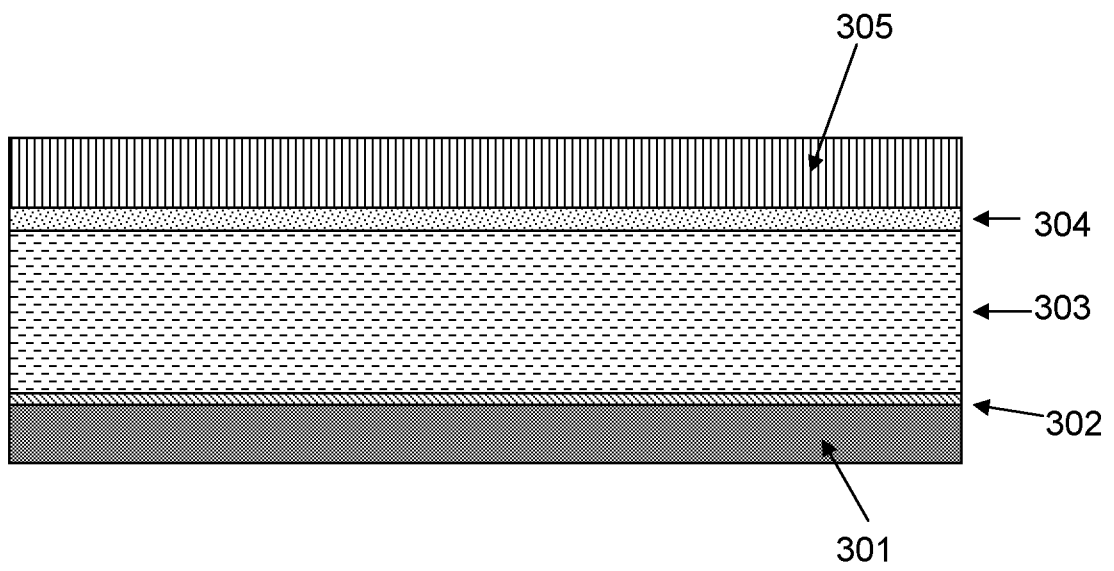


FIG 2

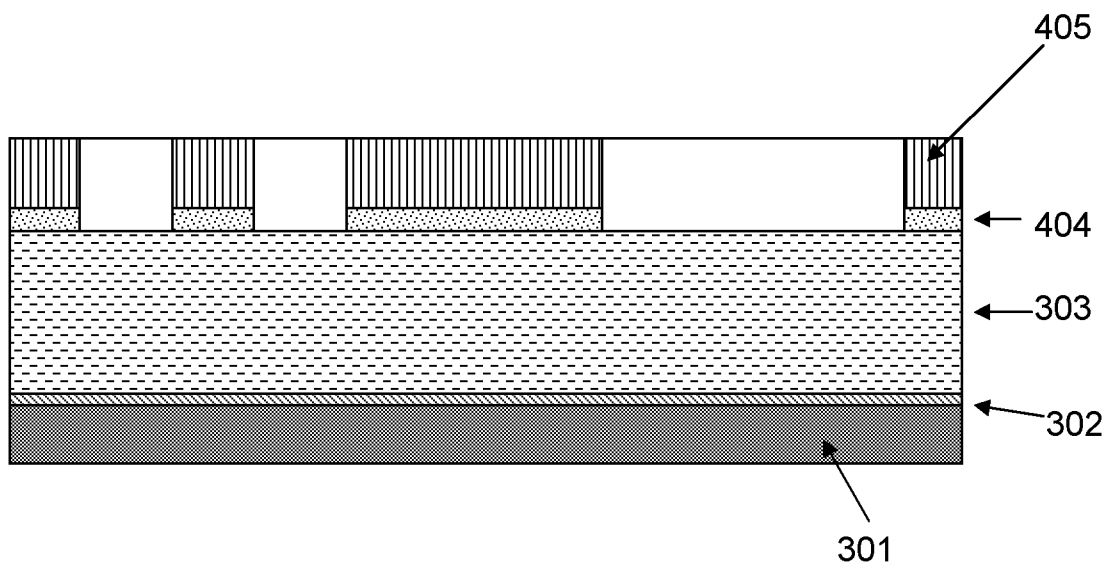


FIG 3

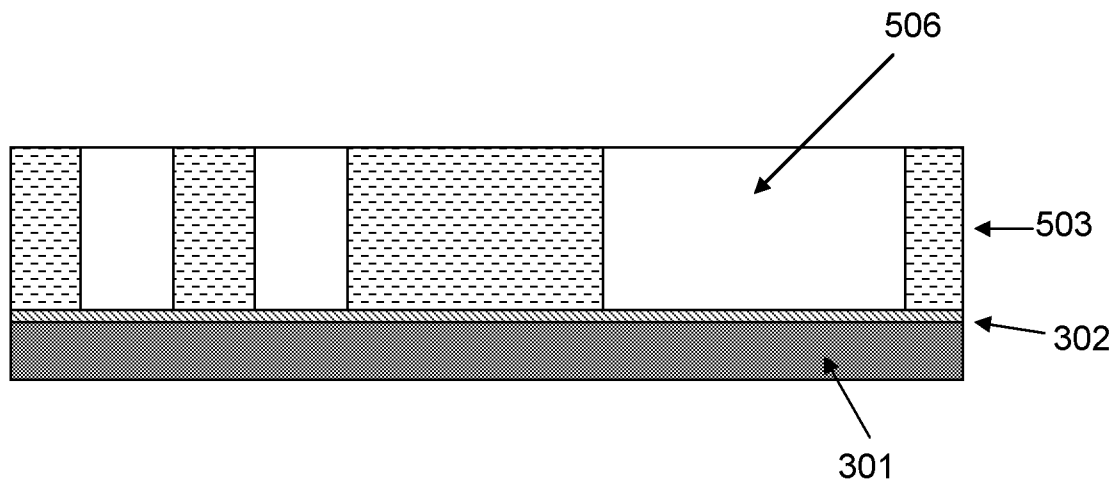


FIG 4

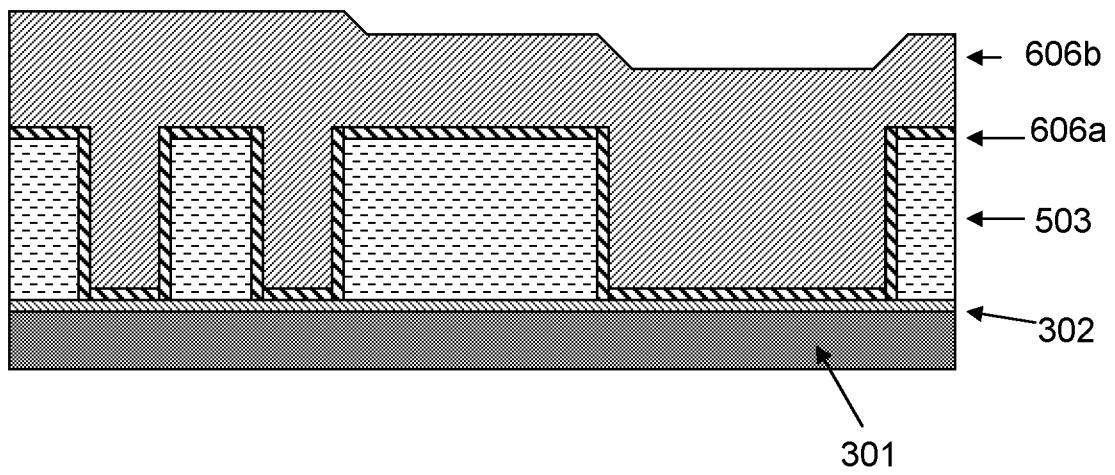


FIG 5

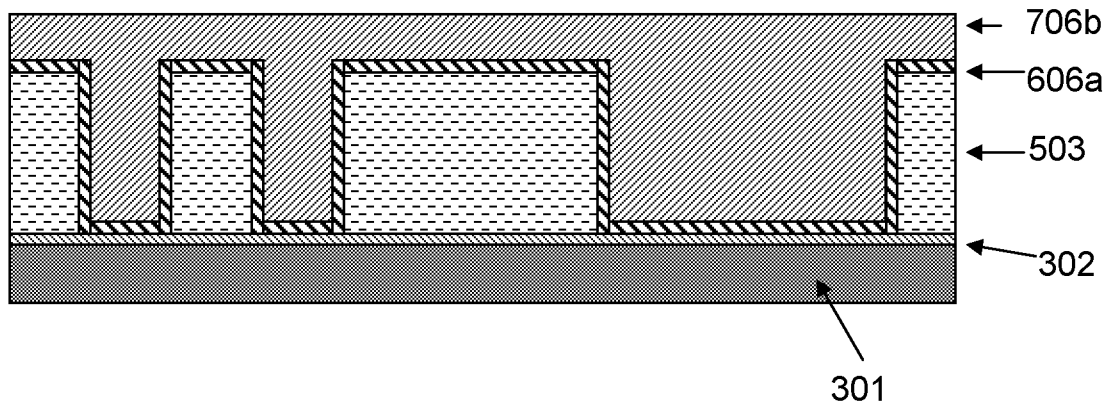


FIG 6

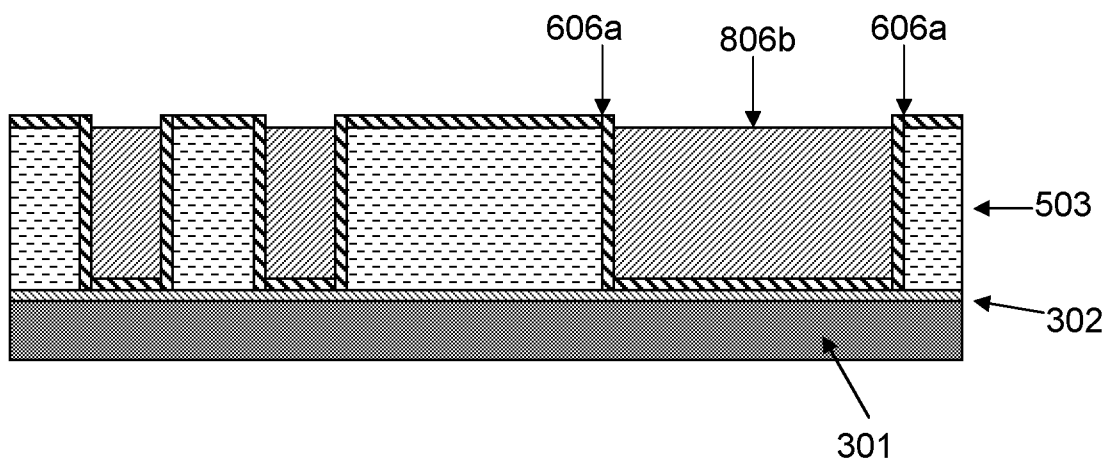


FIG 7

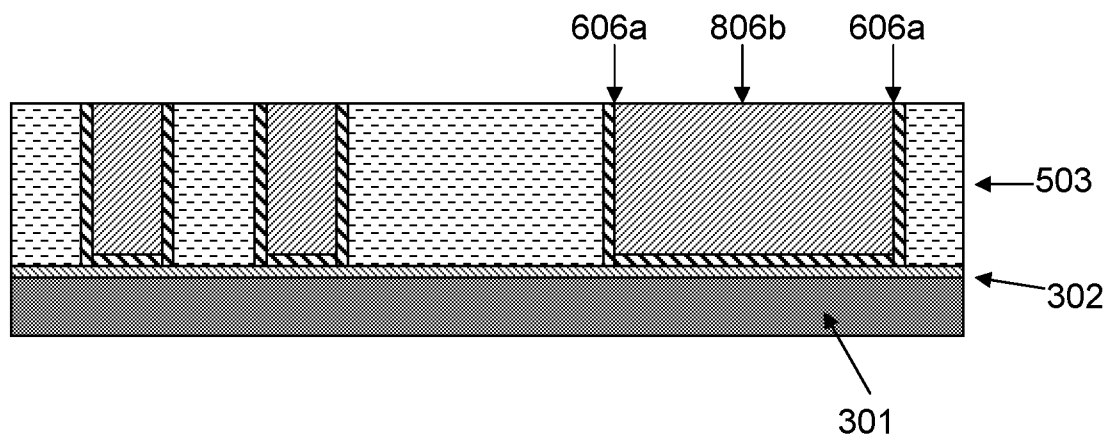


FIG 8

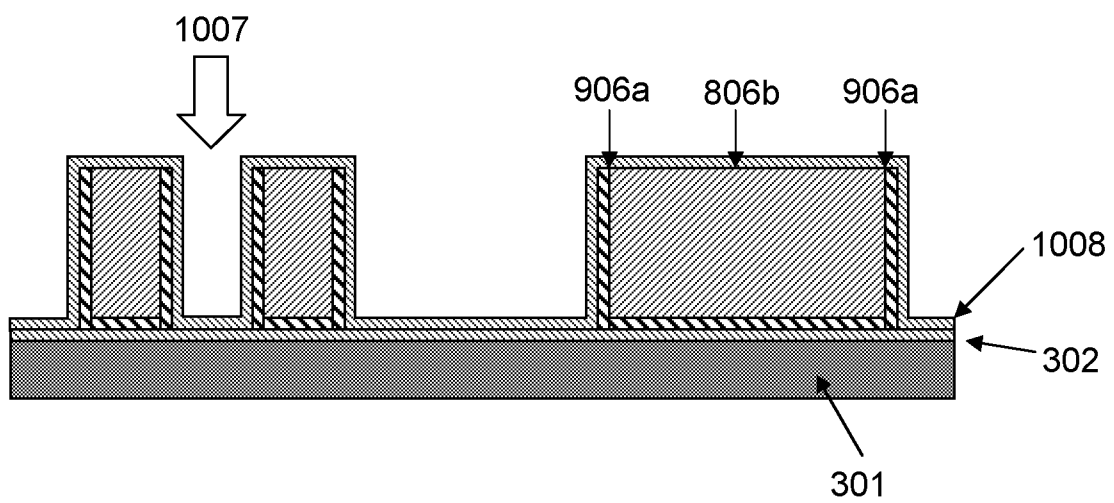


FIG 9

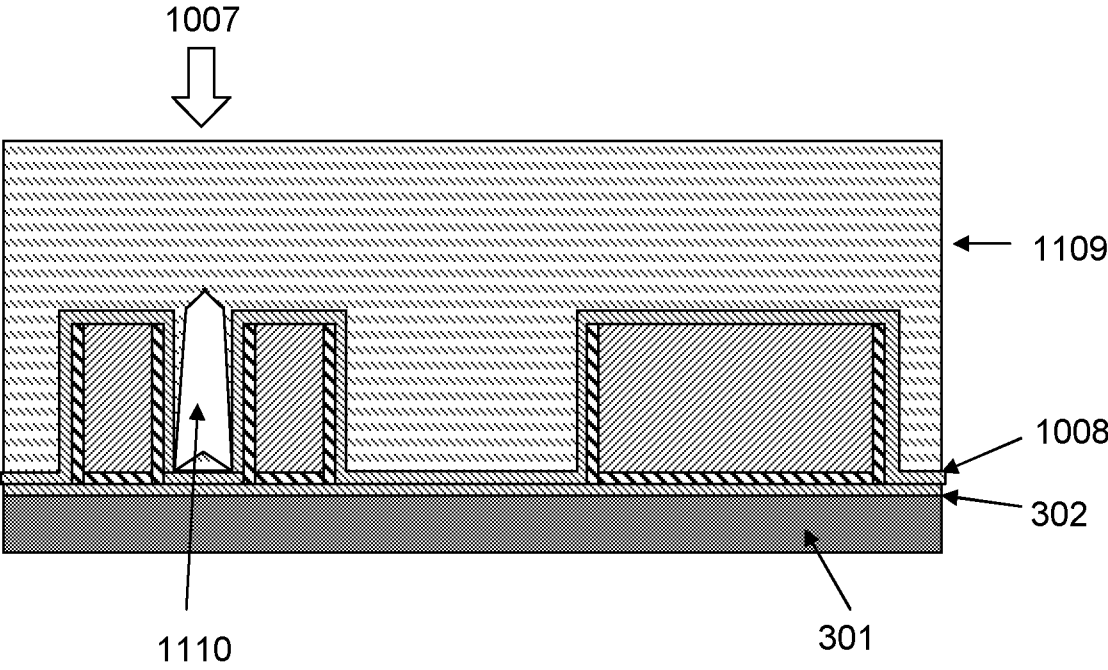


FIG 10

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2011/079859

A. CLASSIFICATION OF SUBJECT MATTER

See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC:H01L21/-;H01L23/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT;CNKI;WPI;EPODOC:INTERCONNECT+, CMP, CHEMICAL+, MECHANICAL+, PLANAR+, POLISH+, LOW K, DIELECT+, CU, COPPER, SFP, STRESS+, FREE+, AIR+, GAP?, CAPACIT+

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US2009068840A1 (MINAMIHABA, Gaku et al.) 12 Mar.2009(12.03.2009) description paragraphs 32-90, figs. 2-11	1-21
Y	WO2010/020092A1 (ACM RESEARCH (SHANGHAI) INC.) 25 Feb.2010(25.02.2010) description paragraphs 25-44, figs. 1-6	1-21
A	US2008102631A1 (ANDRYUSHCHENKO, Tatyana N. et al.) 01 May2008(01.05.2008) the whole document	1-21
A	US2006088975A1 (MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.) 27 Apr. 2006 (27.04.2006) the whole document	1-21
A	US2006276030A1 (WANG, Jean et al.) 07 Dec.2006(07.12.2006) the whole document	1-21

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier application or patent but published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 08 Jun. 2012(08.06.2012)	Date of mailing of the international search report 28 Jun. 2012 (28.06.2012)
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Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer FANG Yan Telephone No. (86-10)62413948
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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2011/079859

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
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INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2011/079859

CLASSIFICATION OF SUBJECT MATTER

H01L21/302 (2006.01) i

H01L21/764 (2006.01) i