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— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

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[Continued on next page]

(54) Title: BANDGAP VOLTAGE GENERATION

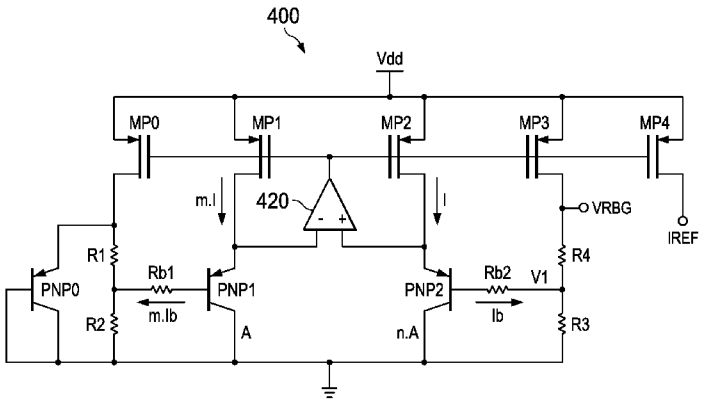

FIG. 4

(57) Abstract: In described examples, a bandgap reference voltage generator includes first and second bipolar junction transistors (PNPl, PNP2). The second transistor (PNP2) is biased at a lower current per unit emitter area than that of the first transistor (PNPl). Accordingly, the base to emitter voltage of the first transistor (PNPl) is higher than that of the second transistor (PNP2), and a delta VBE is generated at the base of the first transistor (PNPl) with respect to the base of the second transistor (PNP2). A first voltage divider (R1/R2) generates a divided voltage of a VBE (fractional VBE) at a first center node. The fractional VBE is added to the VBE of the first transistor (PNPl) and subtracted from the VBE of the second transistor (PNP2) by closed loop feedback action (via 420) to generate a temperature compensated reference voltage at the base of second transistor (PNP2). The reference voltage can be amplified to higher voltage levels (VRGB) by using a resistor divider (R4/R3) at the base of second transistor (PNP2).

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BANDGAP VOLTAGE GENERATION

BACKGROUND

[0001] Many applications of integrated circuits are embodied within a highly integrated system, such as a system-on-chip (SoC). In some of these applications, the SoCs are required to work from low supply voltages and to consume relatively low amounts of power. In such applications, the SoCs incorporate functions (such as a wakeup detect function) that are enabled during a sleep mode of the SoC. In such sleep modes, various battery or system monitoring applications are "on," and accordingly are designed to work from low voltages to save power. Almost all of these SoCs have a bandgap reference circuit to provide a constant voltage reference. Such bandgap reference circuits are typically required to have capability to generate accurate reference voltages, even at low supply voltages.

SUMMARY

[0002] In described examples, a bandgap reference voltage generator includes first and second bipolar junction transistors. The second transistor is biased at a lower current per unit emitter area than that of the first transistor. Accordingly, the base to emitter voltage of the first transistor is higher than that of the second transistor, and a delta VBE is generated at the base of the first transistor with respect to the base of the second transistor. A first voltage divider generates a divided voltage of a VBE (fractional VBE) at a first center node. The fractional VBE is added to the VBE of the first transistor and subtracted from the VBE of the second transistor by closed loop feedback action to generate a temperature compensated reference voltage at the base of second transistor. The reference voltage can be amplified to higher voltage levels by using a resistor divider at the base of second transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] FIG. 1 shows an illustrative electronic device in accordance with example embodiments.

[0004] FIG. 2 is a schematic of a bandgap circuit.

[0005] FIG. 3 is a schematic of a bandgap circuit.

[0006] FIG. 4 is a schematic diagram of low supply voltage bandgap generator in accordance

with example embodiments.

[0007] FIG. 5 is a waveform diagram illustrating equalization of the emitter voltages of two bipolar junction transistors by controlling bias currents sourced by PMOS current mirrors in accordance with example embodiments.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0008] If a first device couples to a second device, that connection can be made through a direct electrical connection, or through an indirect electrical connection via other devices and connections. The term "input" can mean either a source or a drain (or even a control input, such as a gate, where context indicates) of a PMOS (positive-type metal oxide semiconductor) or NMOS (negative-type metal oxide semiconductor) transistor.

[0009] FIG. 1 shows an illustrative computing device 100 in accordance with example embodiments. For example, the computing device 100 is, or is incorporated into, or is coupled (e.g., connected) to an electronic system 129, such as a computer, electronics control "box" or display, communications equipment (including transmitters or receivers), or any type of electronic system operable to process information.

[0010] In some embodiments, the computing device 100 includes a megacell or a system-on-chip (SoC) that includes control logic, such as a CPU 112 (central processing unit), a storage 114 (e.g., random access memory (RAM)) and a power supply 110. For example, the CPU 112 can be a CISC-type (complex instruction set computer) CPU, RISC-type CPU (reduced instruction set computer), MCU-type (microcontroller unit), or a digital signal processor (DSP). The storage 114 (which can be memory, such as on-processor cache, off-processor cache, RAM, flash memory or disk storage) stores one or more software applications 130 (e.g., embedded applications) that, when executed by the CPU 112, perform any suitable function associated with the computing device 100.

[0011] The CPU 112 includes memory and logic that store information frequently accessed from the storage 114. The computing device 100 is often controlled by a user using a UI (user interface) 116, which provides output to and receives input from the user during the execution the software application 130. The output is provided using the display 118, indicator lights, a speaker and vibrations. The input is received using audio and/or video inputs (e.g., using voice or image recognition), and electrical and/or mechanical devices, such as keypads, switches, proximity detectors, gyros and accelerometers.

[0012] The CPU 112 and power supply 110 are coupled to I/O (input-output) port 128, which provides an interface that is configured to receive input from (and/or provide output to) networked devices 131. The networked devices 131 can include any device (such as test equipment) capable of point-to-point and/or networked communications with the computing device 100. The computing device 100 is often coupled to peripherals and/or computing devices, including tangible, non-transitory media (such as flash memory) and/or cabled or wireless media. These and other input and output devices are selectively coupled to the computing device 100 by external devices using wireless or cabled connections. For example, the storage 114 is accessible by the networked devices 131. The CPU 112, storage 114 and power supply 110 are also optionally coupled to an external power supply (not shown), which is configured to receive power from a power source (such as a battery, solar cell, "live" power cord, inductive field, fuel cell, and capacitor).

[0013] The power supply 110 includes power generating and control components for generating power to enable the computing device 100 to execute the software application 130. For example, the power supply 110 provides one or more power switches, each of which can be independently controlled, that supply power at various voltages to various components of the computing device 100. The power supply 110 is optionally in the same physical assembly as computing device 100, or is coupled to computing device 100. The computing device 100 optionally operates in various power-saving modes (such as a sleep mode), in which individual voltages are supplied (and/or turned off) in accordance with a selected power-saving mode, and the various components are arranged within a specific power domain.

[0014] The computing device 100 includes an LSV (low supply voltage) bandgap voltage reference generator 138. This bandgap reference architecture is operable over a wide range of supply voltages as low as approximately 1.1V. This architecture can be manufactured using ultra-deep sub-micron processes without deep n-well support.

[0015] FIG. 2 is a schematic of a bandgap circuit 200. The bandgap circuit 200 includes PMOS transistor 210, resistors 212, 214, 216, 222 and 224, operational amplifier 220, and bipolar transistors 280 and 282. Circuit 200 generates a constant voltage by adding an amplified difference between the base-to-emitter voltage (VBE) of the bipolar transistor 280 and VBE of bipolar transistor 282 (e.g., "m*deltaVBE") to the VBE generated by bipolar transistor 280 to generate a temperature compensated reference voltage (VBG). The VBG signal is temperature

compensated because the temperature coefficients of m*deltaVBE are ideally exactly equal and opposite to the temperature coefficients associated with VBE of transistor 280.

[0016] Bandgap circuit 200 is a first example bandgap architecture. The minimum voltage supply (Vdd) required to operate circuit 200 is VBE+m*dVBE+Vdsat, where m*dVBE is an amplified difference between base-to-emitter voltage(VBE) of the bipolar transistor 280 and VBE of bipolar transistor 282, and where Vdsat is the minimum source to drain voltage needed to keep transistor 210 in current saturation region of operation. VBE+m*dVBE is the usual bandgap voltage for Si, which is approximately 1.23V. If a minimum Vdsat of 0.1V is required, the minimum operating Vdd is approximately 1.33V. Accordingly, circuit 200 is not well-suited for operation with digital logic voltage supplies or with circuitry operating from a low voltage supply. Also, during startup of circuit 200, all the current from the PMOS transistor 210 will be flowing through resistor 216 over a certain range of PMOS gate voltages. For at least this reason, circuit 200 has multiple operating points (e.g., more than two operating points) and might not reach a correct operating point without additional control circuitry. An operating point is a point (e.g., for a given set of selected values of components of a circuit) in which a stable operating voltage is achieved by the circuit. A valid (e.g., correct) operating point is a point at which the circuit operates in accordance with its intended function. Accordingly, an operating point can be valid or invalid depending on context.

[0017] A second example bandgap architecture is the Banba architecture (not shown), which operates in a current (e.g., flow) domain (as compared to the voltage domain in which bandgap circuit 200 operates). The Banba bandgap architecture generates a constant voltage by adding the delta VBE dependent current to a correct proportion of the VBE dependent current and passing it through a similar type resistor by which VBE and deltaVBE current has been generated. VBE+Vdsat is the minimum voltage supply (Vdd) required to operate the Banba bandgap architecture. For example, when the bipolar transistor has a VBE of 0.8V and the PMOS control transistor has a Vdsat of 0.1V, the minimum operating Vdd is approximately 0.9V.

[0018] However, the Banba bandgap architecture operates with higher inaccuracies that result from the current mirroring used to generate the reference voltage. Further, such inaccuracies progressively become even greater as the Vdsat is decreased, and as increasingly deeper sub-micron processes are used. The Banba bandgap architecture also has multiple operating

points and might not reach a correct operating point without additional control circuitry.

[0019] FIG. 3 is a schematic of a bandgap circuit 300. The bandgap circuit 300 is described by Patent No. US 7,411,443, which is hereby fully incorporated herein by reference for all purposes. The bandgap circuit 300 includes PMOS transistor 310, resistors 312, 314, 322, 324 and 326, operational amplifier 320, and bipolar transistors 380 and 382. In circuit 300, a VBE and a correct fraction of VBE (e.g., 1/m*VBE) are generated at the emitter of bipolar junction transistor 380. The VBE of transistor 382 is subtracted from this voltage to yield a deltaVBE+1/m*VBE value, such that the temperature coefficients of the delta VBE signal and the fractional VBE signal cancel. The minimum voltage supply (Vdd) required to operate the circuit 300 is VRBG+VBE+Vdsat. For example, if the VRGB is approximately 0.18V, the bipolar transistor has a VBE of 0.8V, and the PMOS control transistor has a Vdsat of 0.1V, then the minimum operating Vdd is approximately 1.08V.

[0020] However, the circuit 300 is normally limited to generating a bandgap reference voltage (e.g., VRBG) of approximately 0.18V. Further, the circuit 300 does not function using substrate PNP bipolar junction transistors where the collector terminals are by default coupled to the substrate. The circuit 300 also has multiple operating points and might not reach a correct operating point without additional control circuitry.

[0021] FIG. 4 is a schematic diagram of low supply voltage bandgap generator in accordance with example embodiments. The circuit 400 is an example embodiment of the LSV bandgap generator 138 of FIG. 1. Generally, the circuit 400 includes PMOS transistors MP0, MP1, MP2, MP3 and MP4, resistors R1, R2, R3, R4, Rb1 and Rb2, operational amplifier 420, and bipolar transistors PNP0, PNP1 and PNP2. The circuit 400 is optionally formed in a substrate that usually does not support deep N-well formation. For example, each of the bipolar transistors PNP0, PNP1 and PNP2 is a substrate PNP bipolar junction transistor that includes a collector coupled to a ground (e.g., voltage potential) structure formed in the substrate (e.g., in the same substrate). The substrate PNP bipolar junction transistors are usually the only bipolar transistors available in processes that do not support a deep N well formation.

[0022] In operation, circuit 400 generates a temperature-compensated bandgap reference voltage (VRBG) by adding a fractional VBE signal (e.g., divided from the emitter of transistor PNP0) to a delta VBE signal (e.g. generated from transistors PNP1 and PNP2, each of which is biased to have a different current density), such that the temperature coefficients of the delta

VBE signal and the fractional VBE signal cancel. Such a reference voltage is generated at the base of PNP2 (e.g. V1, if drop across Rb2 is neglected). The minimum voltage supply (Vdd) required to operate the circuit 400 is V1+VBE+Vdsat. For example, if the voltage of node V1 is approximately 0.18V, the bipolar transistor has a maximum VBE of 0.8V and the PMOS control transistor has a Vdsat of 0.1V, then the minimum operating Vdd is approximately 1.08V.

[0023] Transistors MP0, MP1, MP2, MP3 and MP4 are each operable to provide an operating current in response to an output of an operational amplifier 420. Transistor PNP1 has an emitter area of A. Transistor PNP2 has an emitter area that is larger (e.g., an integer multiple N larger) than A. Transistor MP1 generates a current (m*I) that is a multiple (m) of the current generated by the transistor MP2, such that transistor PNP1 is biased using an overall higher current per unit emitter area than the current per unit emitter area that is used for biasing transistor PNP2. The operational amplifier 420 is operable to force the emitter voltage of transistor PNP1 to be equal to the emitter voltage of PNP2. Accordingly, the reference voltage V1, which is developed at the base of transistor PNP2 (neglecting the drop across Rb2), is temperature compensated.

[0024] The transistor PNP0 has a collector coupled (e.g., connected) to its base. The transistor PNP0 has a base-to-emitter voltage (VBE0) as described below. Resistors R1 and R2 (where R1 is "high-side" resistor, and R2 is the "low-side" resistor) are arranged in series (e.g., where a first terminal of R1 is coupled to the emitter of PNP0) to form a voltage divider operable to generate the fractional VBE voltage. The resistor Rb1 is coupled to the middle of the voltage divider (e.g., to the node between R1 and R2). The current through resistor Rb1 is operable to offset any error resulting from the finite base current of the bipolar transistor PNP1.

[0025] As discussed above, the transistor PNP1 is biased using a higher current per unit emitter area than the current per unit emitter area of transistor PNP2. Accordingly, the base-to-emitter voltage of PNP1 (VBE1) is higher than the VBE of transistor PNP2 (VBE2). The operational amplifier 420 forces the emitter voltage of transistor PNP2 to be equal to the emitter voltage of transistor PNP1. Accordingly, the voltage at the base of transistor PNP1 is higher than the base voltage of transistor PNP2 by VBE1-VBE2 ("delta VBE"). The delta VBE quantity is added to the fractional VBE generated by R1 and R2 voltage divider.

[0026] The operational amplifier 420 forces the emitter voltage of PNP1 and PNP2 to be equal by injecting current through transistor MP3 and into resistor R3 until the reverse bandgap voltage V1 is developed across the resistor R3 (which is the low-side resistor). The resistor Rb2 is

coupled to the non-ground terminal of resistor R3 to cancel the error caused by finite base current of bipolar transistor PNP2.

[0027] Selecting the resistance value of R4 (which is the high side resistor) allows the output voltage developed across R3 (e.g., in an embodiment) to be amplified to higher voltages (e.g., the output voltage can be higher than the reverse bandgap voltage generated by the circuit as described in FIG. 3). In various embodiments, the amplified bandgap reference voltage can be nearly as high as the minimum supply voltage minus the source to drain voltage (Vdsat) required by transistor MP3 to be in current saturation. Accordingly, adjusting the ratio of the voltage divider formed by R4 and R3 causes the possible amplified voltage range of VRBG to vary from V1 to the operating voltage minus the Vdsat of transistor MP3. Resistor R4 can optionally be zero ohms (e.g., not included per se in the circuit).

[0028] Transistors MP0, MP1, MP2, MP3 and MP4 are matched current mirror transistors. For example, the amount of current flowing through the current mirror transistors is determined approximately by voltage V1 divided by resistor R3 flowing thru transistor MP3 (in this example, the base current is considered to be negligible). The transistor MP0 is operable to provide an operating current to the emitter of a transistor PNP0 and to a voltage divider formed by resistors R1 and R2. The transistor MP1 is operable to provide an operating current to the emitter of the transistor PNP1. The transistor MP2 is operable to provide an operating current to the emitter of a transistor PNP2. The transistor MP4 is operable to provide a reference current, IREF to be used by other circuits in the system (e.g., a processor that is arranged to select an operating mode in response to a comparison of an operating parameter signal with a voltage produced by the reference current or to be used as biasing current for various other types of circuits).

[0029] In accordance with Kirchhoff's circuit laws, the voltage at the negative input terminal of operational amplifier 420 is:

$$VBE0\frac{R2}{R1+R2}+m*Ib*(R1\,||\,R2)+m*Ib*Rb1+VBE1+Voff \qquad (1)$$

where Voff is the input referred offset voltage of operational amplifier 420. Further, the voltage at positive input terminal of amplifier 420 is:

$$VBE2+Ib*Rb2+V1 \qquad (2)$$

where V1 is the voltage generated across resistor R3, and where V1 is stabilized by the feedback

loop-arrangement of the operational amplifier 420.

[0030] Equations (1) and (2) are equal due to the error correction signal generated by the operational amplifier 420. Combining equations (1) and (2) yields:

$$\begin{cases} VBE\,0\dfrac{R2}{R1+R2}+m*Ib*(R1\,||\,R2)+m*Ib*Rb1+VBE\,1+Voff\;= \\ VBE\,2+Ib*Rb\,2+V1 \end{cases} \tag{3}$$

[0031] Expressed in terms of Vrbg (and substituting in terms of R4/R3 for V1):

$$Vrbg=\begin{cases} \left(VBE0\dfrac{R2}{R1+R2}+dVBE\right)\left(1+\dfrac{R4}{R3}\right)+ \\ Voff\left(1+\dfrac{R4}{R3}\right)+ \\ Ib\left[m*(R1\,||\,R2+Rb1)*\left(1+\dfrac{R4}{R3}\right)-Rb2*\left(1+\dfrac{R4}{R3}\right)-R4\right] \end{cases} \tag{4}$$

[0032] In the above equation (4), the first part is the required bandgap voltage. The second part is the error due to input referred offset voltage of the amplifier 420, which can be removed by either using a one-time trimming of this error or by using dynamic offset cancellation methods. The third part of the equation (4) is the error due to the finite base current. The finite base current can be negated by choosing optimum values for resistors Rb1 and Rb2.

[0033] FIG. 5 is a waveform diagram illustrating equalization of the emitter voltages of two bipolar junction transistors by controlling bias currents sourced by PMOS current mirrors in accordance with example embodiments. Generally, waveform diagram 500 illustrates a waveform 510 of the non-inverting input of the operational amplifier 420 (amp_plus) and a waveform 520 of the inverting input of the operational amplifier 420 (amp-minus) of a low supply voltage bandgap generator operation. The axis 502 represents voltage, and the axis 504 represents bias current. The waveform 510 illustrates that the operational amplifier 420 can stabilize the circuit (when both the inputs of the amplifier are equal) at Bias Current = 0uA or at 2uA. Because only two operating points are possible, the complexity of making this circuit operational without the need of intricate startup circuits is substantially reduced.

[0034] In an embodiment, a controller (e.g., such as a microcontroller or a digital signal processor) is used to control one or more attributes of the LSV bandgap generator 138 and other system level controlled variables, such as power mode selection and power mode transitioning.

Some of the variables are software programmable, which allows more flexibility for implementing the disclosed control schemes and provides an enhanced ability to adaptively adjust to dynamically changing conditions for optimized system performance. Other variables can be programmed during the manufacturing process (e.g., to compensate for lot characteristics) by trimming trim-able resistors to increase operational stability and accuracy in measuring signals that provide indications of dynamically changing operating conditions.

[0035] Components of various embodiments can be implemented in hardware or software, internally or externally, and share functionality with other modules and components as illustrated herein. For example, the processing and memory portions of the LSV bandgap generator 138 can be implemented outside of a device and/or substrate upon which the power converter is formed.

[0036] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A circuit for generating a bandgap reference voltage, comprising:

a first voltage divider operable to generate a fractional VBE voltage at a first center node, wherein the first center node is coupled to the base of the first transistor;

first circuitry operable to generate a first VBE by biasing a current into a first circuitry bipolar transistor across the first voltage divider;

a first transistor and a second transistor operable for biasing at a lower current per unit emitter area than that of the first transistor, wherein a delta VBE (voltage base-to-emitter) is generated at the base of the first transistor with respect to the base of the second transistor; and

second circuitry operable to force emitter voltage of the first transistor to be equal to emitter voltage of the second transistor.

2. The circuit of claim 1, comprising a second voltage divider operable to amplify the reference voltage generated at a second center node, wherein the second center node is coupled to the base of the second transistor.

3. The circuit of claim 2, wherein the second circuitry is operable to control a first current mirror operable to supply a first mirror current to the first voltage divider and the first circuitry.

4. The circuit of claim 3, wherein the second circuitry is operable to control a second current mirror operable to supply a second mirror current to the first transistor.

5. The circuit of claim 4, wherein the second circuitry is operable to control a third current mirror operable to supply a third mirror current to the second transistor.

6. The circuit of claim 5, wherein the second circuitry is operable to control a fourth current mirror operable to supply a fourth mirror current to the second voltage divider.

7. The circuit of claim 5, wherein the second voltage divider is operable to generate a temperature-compensated voltage reference signal.

8. The circuit of claim 5, wherein the second circuitry is operable to drive a fifth current mirror operable to generate a current reference signal.

9. The circuit of claim 1, wherein an error due to the first base current and the second base current are corrected by a first base resistor and a second base resistor.

10. The circuit of claim 9, wherein the first base resistor and the second base resistor values are selected to compensate for the error due to the first base current flowing into first voltage

divider and error due to the second base current flowing into second voltage divider.

11. The circuit of claim 2, wherein the value of the high-side resistor of the second voltage divider is substantially zero ohms or greater.

12. The circuit of claim 1, wherein the first and second transistors are substrate PNP-type transistors, wherein each transistor includes a collector coupled to a ground structure formed in a substrate in which the first and second transistors and the first circuitry bipolar transistor are formed.

13. An electronic system, comprising

a first transistor and a second transistor operable for biasing at a lower current per unit emitter area than that of the first transistor, wherein a delta VBE (voltage base-to-emitter) is generated at the base of the first transistor with respect to the base of the second transistor;

a first voltage divider operable to generate a fractional VBE voltage at a first center node, wherein the first center node is coupled to the base of the first transistor;

first circuitry operable to force emitter voltage of the first transistor to be equal to emitter voltage of the second transistor;

second circuitry operable to generate a first VBE across the first voltage divider; and

a processor that is operable in response to a temperature-compensated voltage reference signal generated at the base of the second transistor.

14. The system of claim 13, wherein the first transistor, the second transistor, the first voltage divider, the first circuitry, the second circuity and the processor are formed in a common substrate.

15. The system of claim 13, wherein the minimum operating voltage of a circuit formed by the first transistor, the second transistor, the first voltage divider and the first circuitry is around a voltage determined in accordance with the equation V1+VBE+Vdsat, where V1 is a first reference voltage generated across a low-side resistor of a second voltage divider, VBE (voltage base-to-emitter) is a voltage generated at the emitter of the second transistor with respect to its base, and Vdsat is a minimum source to drain voltage at which a current mirror coupled to the emitter of the first transistor operates in a current saturation region.

16. The system of claim 15, wherein the temperature-compensated voltage reference signal is a voltage that is higher than the base voltage of the second transistor.

17. A method for generating a bandgap reference voltage, comprising:

biasing a first transistor at a higher current per unit emitter area than a bias current of a second transistor, wherein a delta VBE (voltage base-to-emitter) is generated at the base of the first transistor with respect to the base of the second transistor;

generating a fractional VBE voltage at a first center node of a first voltage divider, wherein the first center node is coupled the base of the first transistor;

forcing an emitter voltage of the first transistor to be equal to an emitter voltage of the second transistor; and

generating a first VBE across the first voltage divider.

18. The method of claim 17, comprising a second voltage divider operable to amplify the reference voltage generated at a second center node, wherein the second center node is coupled to the base of the second transistor.

19. The method of claim 17, comprising generating a temperature-compensated voltage reference signal, wherein circuitry used to practice the method does not include multiple invalid operating points.

20. The method of claim 19, comprising selecting an operating mode in response to a comparison of an operating parameter signal to the temperature-compensated voltage reference signal.

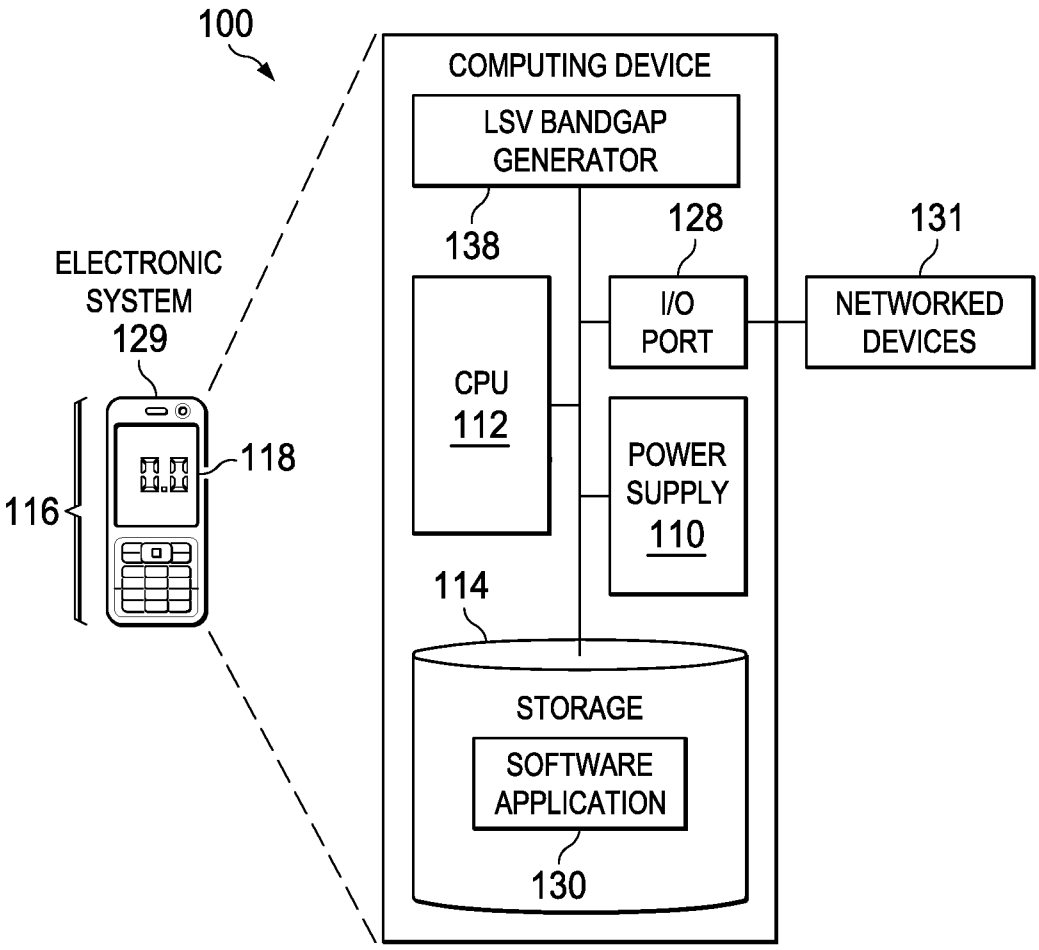

FIG. 1

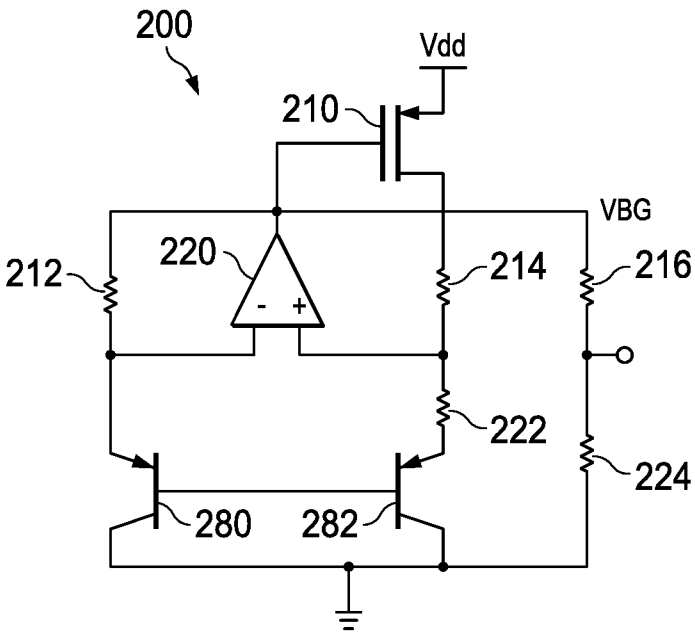

FIG. 2
(PRIOR ART)

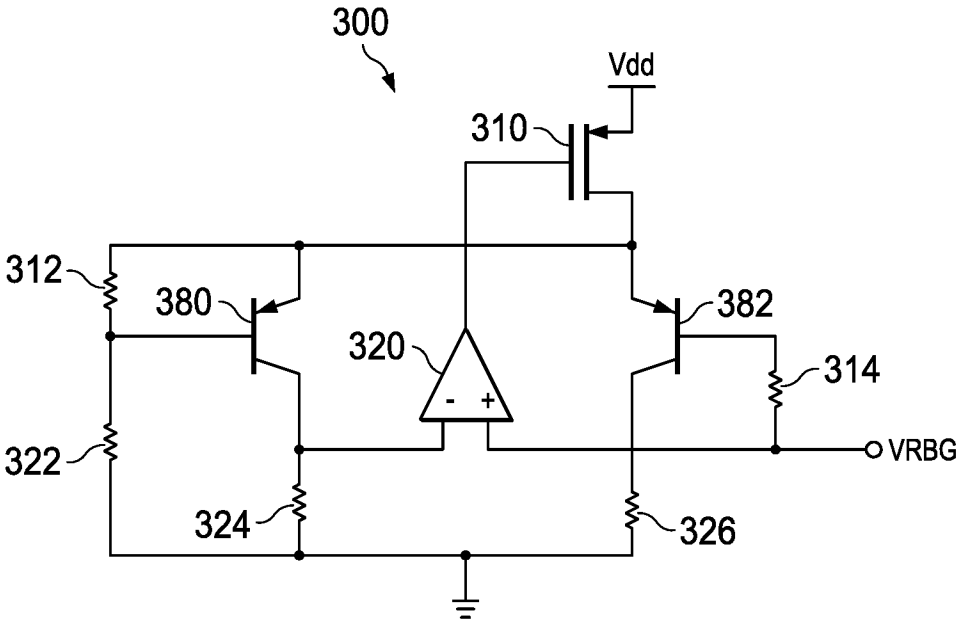

FIG. 3
(PRIOR ART)

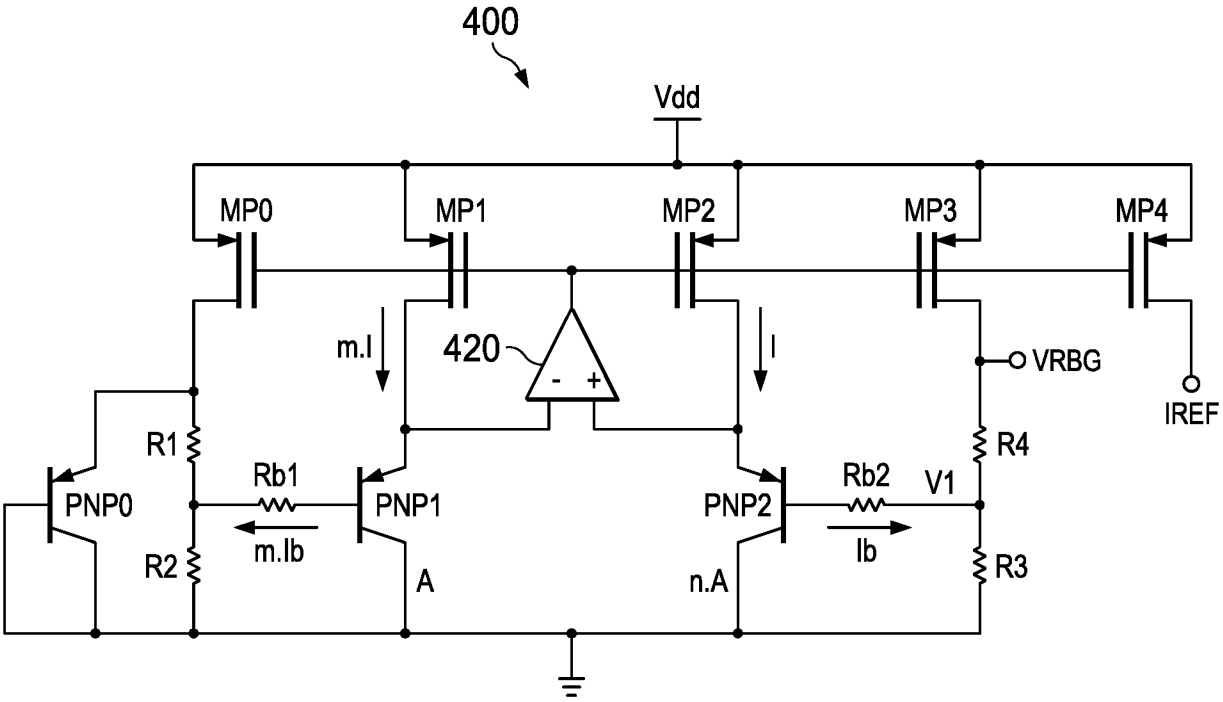

FIG. 4

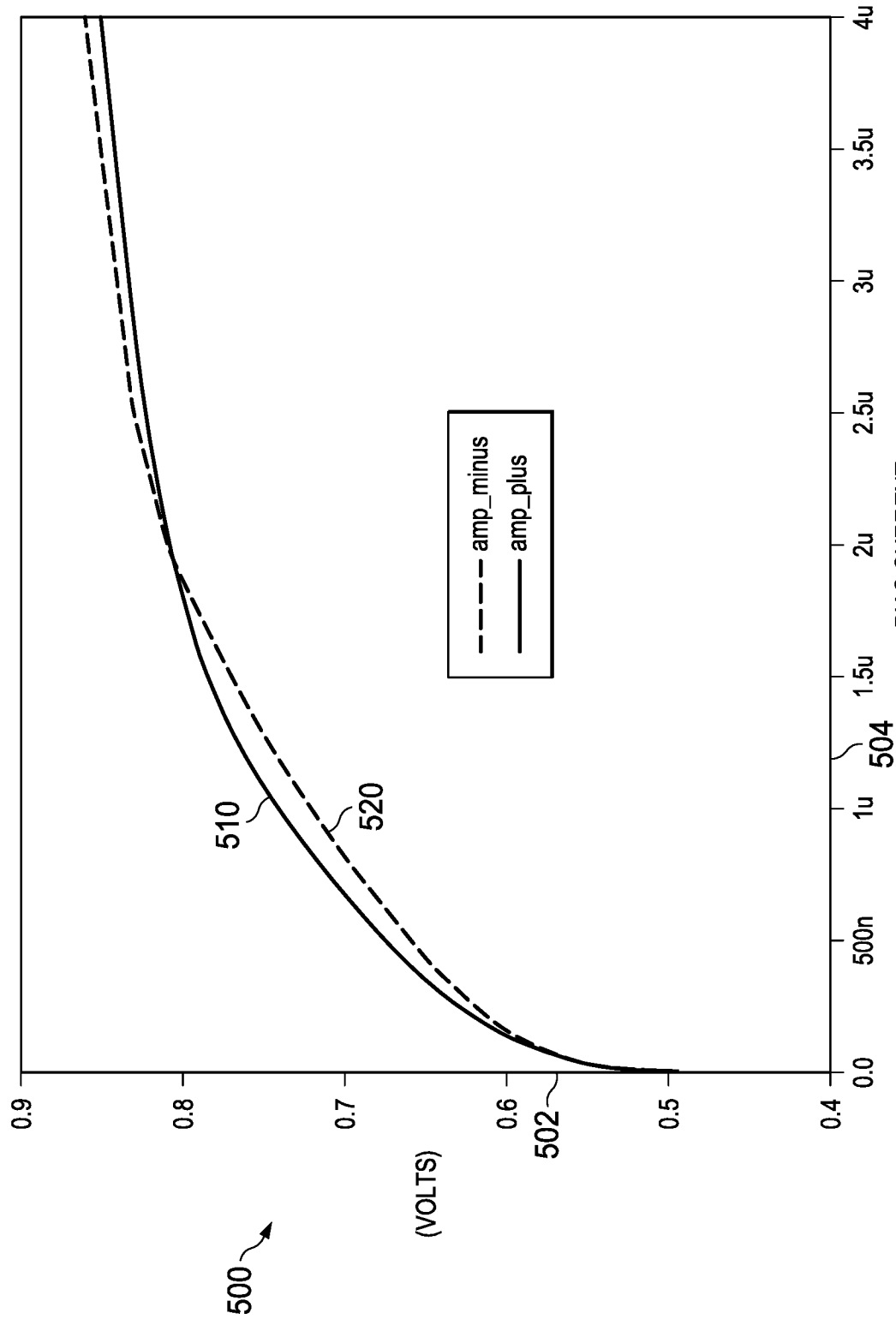
500
0.9
0.8
0.7
0.6
0.5
0.4
(VOLTS)
502
510
520
amp_minus
amp_plus
0.0
500n
1u
1.5u
2u
2.5u
3u
3.5u
4u
BIAS CURRENT
504

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2016/023451

A. CLASSIFICATION OF SUBJECT MATTER

G05F 3/16 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G05F 3/00, 3/02, 3/08, 3/10, 3/16, 3/20, 3/26, H03K 3/00, 3/01, 3/011, H02M 3/00, 3/02, 3/04, 3/06, A61N 1/00, 1/18, 1/32, 1/36, 1/362, 1/365, G11C 7/00, G01K 7/00, 13/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, K-PION, Esp@cenet, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5053640 A (SILICON GENERAL, INC.) 01.10.1991, abstract, col.1, line 9, col.3, lines 56-65, col.4, lines 43-64, col. 5, lines 6-39, col.6, lines 36-38, col.7, lines 1-13, fig. 4, 7	1, 2, 9-14, 17-20
A		3-8, 15, 16
Y	WO 2013/177425 A1 (NANOSTIM, INC.) 28.11.2013, paragraphs [0077], [0097], fig. 15, 20	1, 2, 9-12,
A		3-8
Y	US 2002/0041531 A1 (HITOSHI TANAKA et al.) 11.04.2002, paragraphs [0122], [0123], fig. 17	1, 2, 9-14, 17-20
A		3-8, 15, 16
Y	US 2011/0187445 A1 (FREESCALE SEMICONFUCTOR, INC.) 04.08.2011, paragraphs [0018], [0023], [0029], [0033], [0034], [0073], [0089], fig. 1, 6, 7	2, 9-12, 14, 18-20

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

* Special categories of cited documents:

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
08 June 2016 (08.06.2016)	30 June 2016 (30.06.2016)

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 2016/023451

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 7524107 B1 (NATIONAL SEMICONDUCTOR CORPORATION) 28.04.2009, claims 14, 16	20