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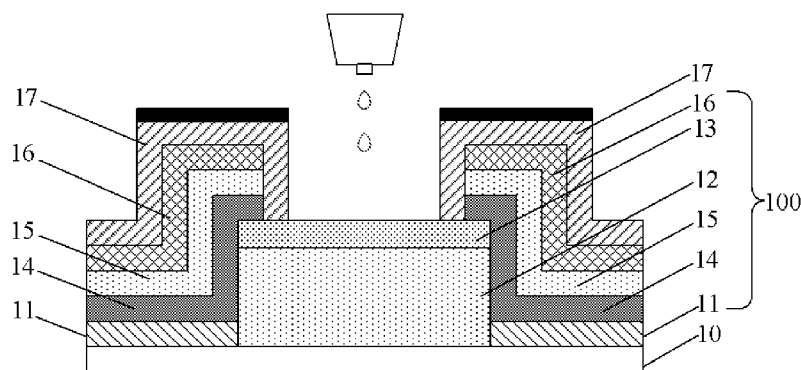


Fig. 1i

(57) Abstract: A pixel structure may include a base substrate (10); a first insulating island (12) on a side of the base substrate (10); a first electrode (13) on a side of the first insulating island (12) opposite from the base substrate (10); a second electrode (11) on the base substrate (10) and at a peripheral area of the first insulating island (12); an active layer (14) electrically connected to the first electrode (13) and the second electrode (11); a second insulating layer (15) on a side of the active layer (14) opposite from the base substrate (10); a gate electrode (16) on a side of the second insulating layer (15) opposite from the base substrate (10); and a third insulating layer (17) on a side of the gate electrode (16) opposite from the base substrate (10).



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1 area of the first insulating island; an active layer electrically connected to the first
2 electrode and the second electrode; a second insulating layer on a side of the active
3 layer opposite from the base substrate; a gate electrode on a side of the second
4 insulating layer opposite from the base substrate; and a third insulating layer on a
5 side of the gate electrode opposite from the base substrate. The third insulating layer
6 encloses a groove structure with the first electrode; the third insulating layer covers
7 at least a side surface of one of the active layer, the second insulating layer or the
8 gate electrode to form the groove structure with the first electrode; a height of the
9 first insulating island in a direction perpendicular to the base substrate is greater than
10 a height of the second electrode in the direction perpendicular to the base substrate;
11 and the first electrode and the second electrode are two different electrodes selected
12 from a source electrode and a drain electrode.

13 [0005] Optionally, a surface of the second electrode opposite from the base
14 substrate is not in a same level with a surface of the first insulating island opposite
15 from the base substrate.

16 [0006] Optionally, the third insulating layer serves as side walls of the groove
17 structure, and the first electrode serves as a bottom of the groove structure.

18 [0007] Optionally, the second electrode surrounds the first insulating island.

19 [0008] Optionally, the second electrode comprises a first sub-electrode and a
20 second sub-electrode spaced apart from each other, and the first sub-electrode and the
21 second sub-electrode are on opposite sides of the first insulating island.

22 [0009] Optionally, the second electrode is in contact with side surfaces of the
23 first insulating island.

24 [0010] Optionally, the first electrode is conformal with the first insulating
25 island.

26 [0011] Optionally, the active layer contacts with the first electrode, and side
27 surfaces of the first insulating island and the second electrode.

28 [0012] Optionally, the second insulating layer is conformal with the active
29 layer.

1 [0013] Optionally, the gate electrode is conformal with the second insulating
2 layer.

3 [0014] Optionally, a portion of the third insulating layer is conformal with the
4 gate electrode and another portion thereof covers side surfaces of the active layer, the
5 second insulating layer and the gate electrode to form the groove structure with the
6 first electrode.

7 [0015] Optionally, the active layer contacts with a side surface of the first
8 insulating island and a side surface of the first electrode.

9 [0016] Optionally, at least a surface of the third insulating layer opposite from
10 the base substrate is hydrophobic.

11 [0017] One embodiment of the present disclosure is a display apparatus,
12 comprising the pixel structure according to one embodiment of the present disclosure.

13 [0018] One embodiment of the present disclosure is a method of
14 manufacturing a pixel structure. The method may include forming a base substrate;
15 forming a first insulating island on a side of the substrate; forming a first electrode on
16 a side of the first insulating island opposite from the base substrate; forming a second
17 electrode on the base substrate and at a peripheral area of the first insulating island;
18 forming an active layer electrically connected to the first electrode and the second
19 electrode; forming a second insulating layer on a side of the active layer opposite
20 from the base substrate; forming a gate electrode on a side of the second insulating
21 layer opposite from the base substrate; and forming a third insulating layer on a side
22 of the gate electrode opposite from the base substrate. The third insulating layer
23 encloses a groove structure with the first electrode; the third insulating layer covers
24 at least a side surface of one of the active layer, the second insulating layer or the
25 gate electrode to form the groove structure with the first electrode; a height of the
26 first insulating island in a direction perpendicular to the base substrate is greater than
27 a height of the second electrode in the direction perpendicular to the base substrate;
28 and the first electrode and the second electrode are two different electrodes selected
29 from a source electrode and a drain electrode.

1 [0019] Optionally, a surface of the second electrode opposite from the base
2 substrate is not in a same level with a surface of the first insulating island opposite
3 from the base substrate.

4 [0020] Optionally, the second electrode surrounds the first insulating island.

5 [0021] Optionally, the third insulating layer serves as side walls of the groove
6 structure and the first electrode serves as a bottom of the groove structure.

7 [0022] Optionally, the second electrode comprises a first sub-electrode and a
8 second sub-electrode spaced apart from each other, and the first sub-electrode and the
9 second sub-electrode are on opposite sides of the first insulating island.

10 [0023] Optionally, The method of manufacturing a display substrate further
11 comprises exposing a portion of the third insulating layer outside the groove structure
12 to an ultraviolet ray, so that a surface of the portion of the insulating film layer outside
13 the groove structure opposite from the base substrate is hydrophobic.

14 **BRIEF DESCRIPTION OF THE DRAWINGS**

15 [0024] The subject matter which is regarded as the disclosure is particularly
16 pointed out and distinctly claimed in the claims at the conclusion of the specification.
17 The foregoing and other objects, features, and advantages of the present disclosure are
18 apparent from the following detailed description taken in conjunction with the
19 accompanying drawings in which:

20 [0025] Figs. 1a-1i are schematic diagrams showing a process of
21 manufacturing a display substrate according to one embodiment of the present
22 disclosure;

23 [0026] Fig. 2 is a first top plan view of a thin film transistor according to one
24 embodiment of the present disclosure;

25 [0027] Fig. 3 is a second top plan view of a thin film transistor according to
26 one embodiment of the present disclosure; and

27 [0028] Fig. 4 is a flow chart of a process of manufacturing a display substrate
28 according to one embodiment of the present disclosure.

29 **DETAILED DESCRIPTION**

1 [0029] The present disclosure will be described in further detail with reference
2 to the accompanying drawings and embodiments in order to provide a better
3 understanding by those skilled in the art of the technical solutions of the present
4 disclosure. Throughout the description of the disclosure, reference is made to Figs. 1 -
5 3. When referring to the figures, like structures and elements shown throughout are
6 indicated with like reference numerals.

7 [0030] Unless otherwise defined, technical terms or scientific terms used in
8 the present disclosure are intended to be in the ordinary meaning of those of ordinary
9 skill in the art. The words "first," "second" and similar words used in the present
10 disclosure do not denote any order, quantity or importance, but are merely used to
11 distinguish different components. The words "including" or "comprising" and the like
12 mean that the element or the item preceding the word includes the element or item
13 listed after the word and its equivalent and do not exclude other components or
14 objects. "Connected" and the like are not limited to physical or mechanical
15 connections, but may include electrical connections, whether direct or indirect.
16 "Upper," "lower," "left," "right," etc. are only used to indicate the relative positional
17 relationship. When the absolute position of the object being described is changed, the
18 relative positional relationship may also change accordingly.

19 [0031] It will be understood that when an element such as a layer, a film, a
20 region or a substrate is referred to as being "on" or "under" another element, the
21 element may be "directly" "on" or "under" another element, or an intermediate
22 element may be present.

23 [0032] In the description of the following embodiments, specific features,
24 structures, materials or characteristics may be combined in any suitable manner in any
25 one or more embodiments or examples.

26 [0033] The pixel defining layer used in the related art is usually subjected to
27 coating, exposing, developing and curing processes. Thus, the preparation process is
28 very complicate. Furthermore, organic material used for the pixel defining layer tends
29 to pollute the environment.

30 [0034] In order to further explain the display substrate and the manufacturing
31 method thereof and the display apparatus provided by the embodiments of the present

disclosure, detailed description will be made below with reference to the accompanying drawings. One example of the present disclosure provides a pixel structure. The pixel structure may include a base substrate; a first insulating island on a side of the base substrate; a first electrode on a side of the first insulating island opposite from the base substrate; a second electrode on the base substrate and at a peripheral area of the first insulating island; an active layer electrically connected to the first electrode and the second electrode; a second insulating layer on a side of the active layer opposite from the base substrate; a gate electrode on a side of the second insulating layer opposite from the base substrate; and a third insulating layer on a side of the gate electrode opposite from the base substrate. The third insulating layer encloses a groove structure with the first electrode. The third insulating layer covers at least a side surface of one of the active layer, the second insulating layer or the gate electrode to form the groove structure with the first electrode. A height of the first insulating island in a direction perpendicular to the base substrate is greater than a height of the second electrode in the direction perpendicular to the base substrate. The first electrode and the second electrode are two different electrodes selected from a source electrode and a drain electrode.

[0035] In one embodiment, a surface of the second electrode opposite from the base substrate is not in a same level with a surface of the first insulating island opposite from the base substrate. The third insulating layer may serve as side walls of the groove structure, and the first electrode may serve as a bottom of the groove structure. The second electrode may surround the first insulating island.

[0036] In one embodiment, the second electrode comprises a first sub-electrode and a second sub-electrode spaced apart from each other, the first sub-electrode and the second sub-electrode are on opposite sides of the first insulating island.

[0037] In one embodiment, the second electrode is in contact with side surfaces of the first insulating island.

[0038] In one embodiment, the first electrode is conformal with the first insulating island. "Conformal with" herein means that orthographic projection of the

1 first electrode on the base substrate is substantially the same or located within
2 orthographic projection of the first insulating island on the base substrate.

3 [0039] In one embodiment, the active layer contacts with the first electrode,
4 and side surfaces of the first insulating island and the second electrode. In one
5 embodiment, a portion of the active layer is in contact with the first electrode, a
6 portion thereof is in contact with the second electrode, and a portion thereof is in
7 contact with the side surface of the first insulating island and the first electrode.

8 [0040] In one embodiment, the second insulating layer is conformal with the
9 active layer. That is, orthographic projection of the second insulating layer on the base
10 substrate is substantially the same or located within orthographic projection of the
11 active layer on the base substrate.

12 [0041] In one embodiment, the gate electrode is conformal with the second
13 insulating layer. That is, orthographic projection of the gate electrode on the base
14 substrate is substantially the same or located within orthographic projection of the
15 second insulating island on the base substrate.

16 [0042] In one embodiment, wherein a portion of the third insulating layer is
17 conformal with the gate electrode and another portion thereof covers side surfaces of
18 the active layer, the second insulating layer and the gate electrode to form the groove
19 structure with the first electrode. That is, orthographic projection of a portion of the
20 third insulating layer on the base substrate is substantially the same or located within
21 orthographic projection of the gate electrode on the base substrate.

22 [0043] In one embodiment, the active layer contacts with a side surface of the
23 first insulating island and a side surface of the first electrode.

24 [0044] Figs. 1a-1i show a method of forming a display substrate according to
25 one embodiment of the present application. As shown in Figs. 1a-1i, the display
26 substrate includes a base substrate 10, a thin film transistor array layer 100, a third
27 insulating layer 17, and a plurality of light-emitting units. The thin film transistor
28 array layer 100 is disposed on the base substrate 10, and the thin film transistor array
29 layer 100 defines a plurality of groove structures 2 on a side of the thin film transistor
30 array layer opposite from the base substrate 10. The third insulating layer 17 is

disposed on a side of the thin film transistor array layer 100 opposite from the base substrate 10. The third insulating layer 17 defines a plurality of pixel regions 3 in the plurality of groove structures respectively. The pixel regions 3 and the groove structures 2 are in one to one correspondence. The plurality of light-emitting units is disposed in the plurality of pixel regions 3 in one-to-one correspondence.

[0045] In one embodiment, when the thin film transistor array layer 100 is formed on the base substrate 10, the position, shape and size of each film layer pattern included in the thin film transistor array layer 100 can be set such that the thin film transistor array layer 100 defines a plurality of groove structures 2 on a side opposite from the base substrate 10. Then, a third insulating layer 17 is formed on a side of the thin film transistor layer opposite from the base substrate 10, and the third insulating layer 17 can define a plurality of pixel regions 3 in the plurality of groove structures 2. Finally, light-emitting units can be formed correspondingly in the pixel regions 3.

[0046] It should be noted that the groove structure 2 defined by the thin film transistor array layer 100 has a depth which can at least accommodate the light-emitting layer in the light emitting unit. As such, when the third insulating layer 17 defines the pixel region 3 in the groove structure 2, the inner walls of the groove structure 2 corresponding to the pixel region 3 corresponds to a bank of a pixel defining layer in the prior art. The in-slot space of the groove structure corresponding to the pixel region is equivalent to the pixel opening area defined by the pixel defining layer in the prior art. When the light-emitting layer in the light-emitting unit is fabricated in the pixel region 3, an inkjet printing technology can be employed. The ink droplets for forming the light-emitting layer in the light-emitting unit can be stably and accurately dropped into the pixel region 3 to form a corresponding light-emitting layer.

[0047] It should be noted that the pixel region 3 is defined by the third insulating layer 17 so that it is also possible to prevent some of the film layers (for example, the gate electrode 16 and the like) having electrical conductivity in the thin film transistor array layer 100 from being short-circuited with the electrodes in the pixel unit.

1 [0048] According to specific structure and manufacturing process of the
2 display substrate, in the display substrate provided by the embodiments of the present
3 disclosure, a plurality of groove structures 2 are defined by the thin film transistor
4 array layer 100. Then, a corresponding plurality of pixel regions 3 are defined in the
5 plurality of groove structures 2 respectively through the insulating film layer 17. The
6 inner wall of the groove structure 2 corresponding to the pixel region 3 is equivalent
7 to the bank of the pixel defining layer in the prior art, and the in-slot space of the
8 groove structure 2 corresponding to the pixel region 3 is equivalent to the pixel
9 opening area defined by the pixel defining layer in the prior art. Therefore, when the
10 light-emitting layer in the light-emitting unit is fabricated, the light-emitting layer can
11 be directly formed in the pixel region 3 defined by the third insulating layer 17 by
12 using an inkjet printing technique, and there is no need to additionally create a pixel
13 defining layer to define the pixel region 3 for fabricating the light-emitting unit.
14 Therefore, the method of fabricating the display substrate provided by the
15 embodiment of the present disclosure avoids the processes of coating, exposing,
16 developing and curing to form the pixel defining layer, thereby simplifying the
17 manufacturing process of the display substrate. At the same time, potential problem of
18 environmental pollution caused by the use of organic materials for the pixel defining
19 layer is also avoided.

20 [0049] In some embodiments, as shown in Fig. 1f, the thin film transistor
21 array layer 100 may include a plurality of thin film transistors, and each of the groove
22 structures 2 corresponds to at least one thin film transistor. The at least one thin film
23 transistor defines a corresponding groove structure 2, and an output electrode 13 of
24 the at least one thin film transistor serves as a bottom of the groove structure 2. As
25 shown in Fig. 1g, the third insulating layer 17 includes a plurality of openings
26 corresponding to the plurality of groove structures 2 respectively. The opening
27 exposes the first electrode, that is, the output electrode, 13 of the corresponding at
28 least one thin film transistor. The output electrode 13 of the at least one thin film
29 transistor is in contact with the corresponding light emitting unit. The at least one thin
30 film transistor is configured to output a driving signal to the corresponding light-
31 emitting unit through the output electrode 13 to drive the light-emitting unit to emit
32 light.

[0050] In one embodiment, the thin film transistor array layer 100 may include a plurality of thin film transistors distributed in an array. Each of the groove structures 2 may be defined by a corresponding one or more thin film transistors, and each thin film transistor can only define one groove structure 2 correspondingly. The structure of the thin film transistor generally includes the gate electrode 16, the second electrode (that is, the input electrode) 11, the first electrode (that is, the output electrode) 13, the active layer 14, and the insulating layers, etc. The operational mode of the thin film transistor is that under the control of the gate electrode 16, the driving signal received by the input electrode 11 is output to the light-emitting unit through the output electrode 13 to drive the light-emitting unit to emit light. Therefore, in manufacturing the thin film transistor, the output electrode 13 in the thin film transistor can be disposed as the groove bottom of the groove structure 2 to be defined, and the output electrode 13 can be exposed by forming an opening in the third insulating layer 17. In this way, when the light-emitting unit is subsequently fabricated, the output electrode 13 can contact the light-emitting unit more conveniently, thereby better driving the light-emitting unit to emit light.

[0051] It should be noted that the size of the opening provided on the third insulating layer 17 can be set according to actual needs. In one embodiment, the opening exposes only the output electrode 13 at the groove bottom of the groove structure 2 without exposing other film layers included in the thin film transistor. Specifically, the third insulating layer 17 may be provided to completely cover the inner side walls of the groove structure 2, so that the light-emitting unit formed in the pixel region 3 can only be in contact with the output electrode 13 at the bottom of the groove structure without contacting other film layers in the thin film transistor. Short circuit between the light-emitting unit and other film layers in the thin film transistor can be avoided, thereby ensuring stable performance of the display substrate.

[0052] In one embodiment, the light-emitting unit provided by the above embodiment includes two electrodes disposed opposite to each other and a light-emitting layer disposed between the two electrodes. The output electrode 13 of the at least one thin film transistor is in contact with the light-emitting layer in the corresponding light-emitting unit, and the output electrode 13 of the at least one thin

1 film transistor is commonly used as one of the electrodes of the corresponding light-
2 emitting unit.

3 [0053] Specifically, the output electrode 13 of the at least one thin film
4 transistor corresponding to the light-emitting unit can be exposed through the opening
5 in the third insulating layer 17, and the output electrode 13 can be in contact with the
6 light-emitting unit and provide the driving signal for the light-emitting unit. Therefore,
7 the output electrode 13 can be directly multiplexed into one of the light-emitting units.
8 Thus, when the light-emitting unit is fabricated, the light-emitting layer can be
9 directly formed on the output electrode 13. Then, the other electrode of the light-
10 emitting unit can be fabricated on the side of the light-emitting layer opposite from
11 the output electrode 13. As such, the manufacturing process of the light-emitting unit
12 is simplified, and the manufacturing cost of the display substrate is reduced.

13 [0054] The manner in which the groove structure 2 is defined by the thin film
14 transistor described above is various, and two specific definitions are given below for
15 illustration purpose only.

16 [0055] In the first manner, as shown in FIG. 2, each of the groove structures 2
17 corresponds to one thin film transistor, that is, one corresponding thin film transistor
18 defines a corresponding groove structure 2. The thin film transistor specifically
19 includes the following: an input electrode 11 and a first insulating island 12 in the
20 same layer on the base substrate 10. In a direction perpendicular to the base substrate
21 10, a height of the first insulating island 12 is greater than a height of the input
22 electrode 11. Orthographic projection of the input electrode 11 on the base substrate
23 10 surrounds Orthographic projection of the first insulating island 12 on the base
24 substrate 10.

25 [0056] In one embodiment, the thin film transistor further includes an output
26 electrode 13 disposed on a surface of the first insulating island 12 opposite from the
27 base substrate 10 and an active layer 14 disposed on a side of the input electrode 11
28 opposite from the base substrate 10. The active layer 14 is in contact with the input
29 electrode 11 and a portion of the output electrode 13, respectively, and orthographic
30 projection of the active layer 14 on the base substrate 10 surrounds orthographic
31 projection of the output electrode 13 on the base substrate 10.

[0057] In one embodiment, the thin film transistor further includes a second insulating layer 15 and a gate electrode 16 disposed on one side of the active layer 14 opposite from the base substrate 10 and sequentially stacked in a direction away from the base substrate 10. Orthographic projection of the gate electrode 16 on the base substrate 10 is located inside orthographic projection of the second insulating layer 15 on the base substrate 10. The orthographic projection of the gate electrode 16 on the base substrate 10 and orthographic projection of the output electrode 13 on the base substrate 10 at least partially overlap. The orthographic projection of the gate electrode 16 on the base substrate 10 and the orthographic projection of the second insulating layer 15 on the base substrate 10 both surround the orthographic projection of the output electrode 13 on the base substrate 10.

[0058] Specifically, in the thin film transistor of the above structure, the input electrode 11 and the first insulating island 12 are formed on the base substrate 10, and the output electrode 13 is formed on the first insulating island 12 such that a height difference is formed between the input electrode 11 and the output electrode 13. Then, the active layer 14, the second insulating layer 15, and the gate electrode 16 are sequentially formed in stacks on the input electrode 11 and the output electrode 13, so that a height difference is formed between the gate electrode 16 and the output electrode 13. Since the active layer 14, the second insulating layer 15, and the gate electrode 16 are all formed around the output electrode 13 and expose a part of the output electrode 13, a groove structure 2 is formed on the output electrode 13. That is, the output electrode 13 serves as the groove bottom of the groove structure 2, and side walls of the active layer 14, the second insulating layer 15, and the gate electrode 16 serve as the inner walls of the groove structure 2. When the third insulating layer 17 is subsequently formed, the third insulating layer 17 can expose the output electrode 13 at the bottom of the groove structure while covering the inner walls of the groove structure 2 and the gate electrode 16 at the topmost layer of the thin film transistor.

[0059] The thin film transistor of the above structure can define a closed groove structure 2 such that the third insulating layer 17 can define a pixel region 3 in the groove structure 2 as a closed region. Thus, when the ink droplets for forming the light-emitting layer in the light-emitting unit are dropped into the pixel region 3 by the ink-jet printing technique, the ink droplets can be defined in the pixel region 3 without

1 flowing into other non-pixel regions. As such, the ink droplets can be prevented from
2 spreading into other areas to contaminate adjacent pixels, thereby causing cross-color
3 phenomenon.

4 [0060] In the second manner, as shown in FIG. 3, each groove structure 2
5 corresponds to two thin film transistors. That is, the corresponding groove structure 2
6 is defined by two thin film transistors. In this manner, two thin film transistors are
7 disposed on opposite sides of the groove structure 2, and the thin film transistor
8 specifically includes an input electrode 11 and a first insulating island 12 disposed in
9 the same layer on the base substrate 10. The height of the first insulating island 12 is
10 greater than the height of the input electrode 11 in a direction perpendicular to the
11 base substrate 10.

12 [0061] In one embodiment, the thin film transistor further includes an output
13 electrode 13 disposed on a surface of the first insulating island 12 opposite from the
14 base substrate 10 and an active layer 14 disposed on a side of the input electrode 11
15 opposite from the base substrate 10. The active layer 14 is in contact with the input
16 electrode 11 and a portion of the output electrode 13, respectively.

17 [0062] In one embodiment, the thin film transistor further includes a second
18 insulating layer 15 and a gate electrode 16 disposed on one side of the active layer 14
19 opposite from the base substrate 10 and sequentially stacked in a direction away from
20 the base substrate 10. The orthographic projection of the gate electrode 16 on the base
21 substrate 10 is located inside the orthographic projection of the second insulating
22 layer 15 on the base substrate 10. The orthographic projection of the gate electrode 16
23 on the base substrate 10 at least partially overlaps the orthographic projection of the
24 output electrode 13 on the base substrate 10.

25 [0063] In one embodiment, the gate electrodes 16 of the two thin film
26 transistors are connected, the input electrodes 11 of the two thin film transistors are
27 connected, and the two thin film transistors share the same output electrode 13 and the
28 same first insulating island 12.

29 [0064] Specifically, in the thin film transistor of the above structure, the input
30 electrode 11 and the first insulating island 12 are formed on the base substrate 10, and
31 the output electrode 13 is formed on the first insulating island 12 such that a height

1 difference is formed between the input electrode 11 and the output electrode 13. Then,
2 the active layer 14, the second insulating layer 15 and the gate electrode 16 are
3 sequentially formed in stacks on the input electrode 11 and the output electrode 13,
4 thereby forming a height difference between the gate electrode 16 and the output
5 electrode 13. Since the active layer 14, the second insulating layer 15, and the gate
6 electrode 16 are stacked, and respectively expose a part of the output electrodes 13,
7 the output electrode 13 serves as the groove bottom of the groove structure 2, and the
8 sidewalls of the active layer 14, the second insulating layer 15, and the gate electrode
9 16 serve as the inner walls of the groove structure 2.

10 [0065] Therefore, two thin film transistors are disposed on opposite sides of
11 the corresponding groove structure 2. The two thin film transistors can form the
12 groove bottom of the groove structure 2 and the opposite side walls of the groove
13 structure 2, so that the two thin film transistors define a non-closed groove structure 2.
14 When the third insulating layer 17 is subsequently formed, the third insulating layer
15 17 can expose the output electrode 13 at the bottom of the groove structure while
16 covering the inner sidewalls of the groove structure 2 and the gate electrode 16 at the
17 topmost layer of the thin film transistor. When an inkjet printing technique is used to
18 drop ink droplets for forming a light-emitting layer in a light-emitting unit into a pixel
19 region, the ink droplets can also be confined in the pixel region without flowing into
20 other non-pixel regions.

21 [0066] In one embodiment, in the above two manners, the input electrode 11
22 may be a drain electrode, and the output electrode 13 may be a source electrode; or
23 the input electrode 11 may be a source electrode, and the output electrode 13 may be a
24 drain electrode.

25 [0067] In some embodiments, a surface of a portion of the third insulating
26 layer 17 that is disposed outside the groove structure 2 opposite from the base
27 substrate 10 may be hydrophobic. In one embodiment, the third insulating layer in the
28 groove structure may also be hydrophobic.

29 Specifically, after the third insulating layer 17 is formed, a portion of the third
30 insulating layer 17 outside the groove structure 2 may be exposed to an ultraviolet ray
31 so that the surface of the portion of the third insulating layer 17 outside the groove

1 structure 2 opposite from the base substrate 10 is hydrophobic. That is, a static water
2 contact angle θ on the surface of the portion of the third insulating layer 17 outside
3 the groove structure 2 opposite from the base substrate 10 is $>90^\circ$.

4 [0068] Since the light-emitting layer in the light-emitting unit is generally
5 fabricated by inkjet printing technology, the portion of the third insulating layer 17
6 disposed outside the groove structure 2 is hydrophobic on its surface opposite from
7 the base substrate 10, thereby enabling droplets for forming the light-emitting layer to
8 be printed into the pixel region more stably and accurately when the light-emitting
9 layer is formed by inkjet printing technology.

10 [0069] One example of the present disclosure further provides a display
11 apparatus, which comprises the display substrate provided by any of the above
12 embodiments. One example of the present disclosure provides a method of
13 manufacturing a pixel structure. The method may include forming a base substrate;
14 forming a first insulating island on a side of the substrate; forming a first electrode on
15 a side of the first insulating island opposite from the base substrate; forming a second
16 electrode on the base substrate and at a peripheral area of the first insulating island;
17 forming an active layer electrically connected to the first electrode and the second
18 electrode; forming a second insulating layer on a side of the active layer opposite
19 from the base substrate; forming a gate electrode on a side of the second insulating
20 layer opposite from the base substrate; and forming a third insulating layer on a side
21 of the gate electrode opposite from the base substrate. The third insulating layer
22 encloses a groove structure with the first electrode. The third insulating layer covers at
23 least a side surface of one of the active layer, the second insulating layer or the gate
24 electrode to form the groove structure with the first electrode. A height of the first
25 insulating island in a direction perpendicular to the base substrate is greater than a
26 height of the second electrode in the direction perpendicular to the base substrate. The
27 first electrode and the second electrode are two different electrodes selected from a
28 source electrode and a drain electrode.

29 [0070] In one embodiment, a surface of the second electrode opposite from
30 the base substrate is not in a same level with a surface of the first insulating island
31 opposite from the base substrate. The second electrode surrounds the first insulating

1 island. The second insulating layer serves as inner walls of the groove structure and
2 the first electrode serves as a bottom of the groove structure. In one embodiment, the
3 second electrode comprises a first sub-electrode and a second sub-electrode spaced
4 apart from each other, and the first sub-electrode and the second sub-electrode are on
5 opposite sides of the first insulating island.

6
7 [0071] In the method of manufacturing the display substrate according to one
8 embodiment of the present disclosure, the processes of coating, exposing, developing
9 and curing used to fabricate the pixel defining layer are avoided. Thus, the preparation
10 process of the display substrate is simplified. Moreover, the problem of environmental
11 pollution caused by the use of organic material to form the pixel defining layer is also
12 avoided. Therefore, when the display apparatus provided by the embodiments of the
13 present disclosure includes the display substrate provided by the above embodiments,
14 the display apparatus has the advantages of simple manufacturing process, low
15 manufacturing cost, and no pollution to the environment.

16 [0072] One example of the present disclosure further provides a method for
17 fabricating a display substrate, which is used for manufacturing the display substrate
18 provided by the above embodiments. As shown in FIG. 1a - FIG. 1i and Fig. 4, the
19 manufacturing method includes the following:

20 [0073] In step 101, a thin film transistor array layer 100 is formed on the base
21 substrate 10, and the thin film transistor array layer 100 defines a plurality of groove
22 structures 2 on a side opposite from the base substrate 10.

23 [0074] In step 102, a third insulating layer 17 is formed on a side of the thin
24 film transistor array layer 100 opposite from the base substrate 10. The third
25 insulating layer 17 defines a plurality of pixel regions 3 in the plurality of groove
26 structures 2, and the pixel regions 3 and the groove structures 2 are in one to one
27 correspondence.

28 [0075] In step 103, a plurality of light-emitting units is formed in the plurality
29 of pixel regions 3 respectively, and the light-emitting units are in one-to-one
30 correspondence with the pixel regions 3.

[0076] In one embodiment, a base substrate 10 is provided first, and the base substrate 10 can be a glass substrate. Then, a thin film transistor array layer 100 is formed on the base substrate 10. The thin film transistor array layer 100 includes a plurality of film layer patterns, and by arranging the positions, shapes and sizes of the film layer patterns, the thin film transistor array layer 100 can define a plurality of groove structures 2 on a side opposite from the base substrate 10. Then, an third insulating layer 17 is formed on a side of the thin film transistor layer opposite from the base substrate 10, and the third insulating layer 17 can define a plurality of pixel regions 3 in the plurality of groove structures 2. The material of the third insulating layer 17 may be selected from silicon oxide, silicon nitride or aluminum oxide, etc., and the third insulating layer 17 may serve as a passivation layer. Finally, corresponding light-emitting units are formed in the pixel regions 3 respectively.

[0077] In the method for fabricating the display substrate provided by the embodiment of the present disclosure, the thin film transistor array layer 100 can be configured to define a plurality of groove structures 2. Then, a corresponding plurality of pixel regions 3 are defined in the plurality of groove structures 2 through the insulating film layer 17. The groove inner walls of the groove structure 2 corresponding to the pixel region 3 is equivalent to the bank of the pixel defining layer in the prior art, and the in-slot space of the groove structure 2 corresponding to the pixel region 3 is equivalent to the pixel opening area defined by the pixel defining layer in the prior art. Therefore, when the light-emitting layer in the light-emitting unit is fabricated, the light-emitting layer can be directly formed in the pixel region 3 defined by the third insulating layer 17 by using an inkjet printing technique. Thus, there is no need to additionally create a pixel defining layer to define the pixel region 3 for fabricating the light-emitting units. In the method of preparing the display substrate according to one embodiment of the present disclosure, the processes of coating, exposing, developing and curing used to fabricate the pixel defining layer are avoided, thereby simplifying the preparation process of the display substrate. Moreover, the problem of environmental pollution caused by the use of organic material to form the pixel defining layer is also avoided.

[0078] In some embodiments, the step of fabricating the thin film transistor array layer 100 on the base substrate 10 specifically includes forming a plurality of

1 thin film transistors on the base substrate 10. Each groove structure 2 corresponds to
2 at least one thin film transistor, at least one thin film transistor defines a
3 corresponding groove structure 2, and the output electrode 13 of the at least one thin
4 film transistor serves as groove bottom of the groove structure 2.

5 [0079] In some embodiments, the step of fabricating the third insulating layer
6 17 covering the thin film transistor array layer 100 specifically includes the following:

7 [0080] A plurality of openings corresponding to the groove structure 2 is
8 formed in the third insulating layer 17. The opening exposes the output electrode 13
9 of the corresponding at least one thin film transistor, and the output electrode 13 of
10 the at least one thin film transistor is in contact with the corresponding light-emitting
11 unit. At least one thin film transistor is configured to output a driving signal to the
12 corresponding light-emitting unit through the output electrode 13 to drive the light-
13 emitting unit to emit light.

14 [0081] In one embodiment, a plurality of thin film transistors can be fabricated
15 on the base substrate 10 by using a fabrication process of the thin film transistor in the
16 prior art, and a plurality of groove structures 2 are defined by the plurality of thin film
17 transistors. The groove bottom of each groove structure 2 is the output electrode 13 of
18 the corresponding thin film transistor. After the thin film transistor array layer 100 is
19 fabricated, a third insulating layer 17 may be deposited on a side of the thin film
20 transistor array layer 100 opposite from the base substrate 10. Furthermore, by the
21 patterning process, a plurality of openings corresponding to the groove structures 2 in
22 one-to-one correspondence is formed in the insulating film layer 17. Each opening
23 exposes the output electrode 13 of the corresponding at least one thin film transistor.
24 In this way, when the light-emitting unit is subsequently fabricated, the output
25 electrode 13 can be more conveniently contacted with the light-emitting unit, thereby
26 better driving the light-emitting unit to emit light.

27 [0082] It should be noted that the size of the opening provided in the third
28 insulating layer 17 can be set according to actual needs. Illustratively, the opening
29 exposes only the output electrode 13 at the bottom of the groove structure 2 without
30 exposing other layers included in the thin film transistor. In one embodiment, the third
31 insulating layer 17 may be provided to completely cover the inner side walls of the

1 groove structure 2. In this way, the light-emitting unit formed in the pixel region 3 can
2 only be in contact with the output electrode 13 at the bottom of the groove structure
3 without contacting other film layers in the thin film transistor. As such, the short
4 circuit between the light-emitting unit and other film layers in the thin film transistor
5 is avoided, thereby ensuring stable performance of the display substrate.

6 [0083] In some embodiments, the above-mentioned light emitting unit may
7 include two electrodes disposed opposite to each other and a light emitting layer
8 disposed between the two electrodes. In one embodiment, the step of fabricating the
9 light emitting unit in the pixel region 3 specifically includes forming a light-emitting
10 layer in the pixel region. The light-emitting layer is in contact with the output
11 electrode 13 of the corresponding at least one thin film transistor, and the output
12 electrode 13 of the at least one thin film transistor is commonly used or shared as one
13 electrode of the corresponding light-emitting unit. The other electrode of the light-
14 emitting unit is fabricated on the side of the light-emitting layer opposite from the
15 base substrate 10.

16 [0084] In one embodiment, the output electrode 13 of the at least one thin film
17 transistor corresponding to the light emitting unit can be exposed through the opening
18 in the insulating film layer 17, and the output electrode 13 can be in contact with the
19 light-emitting unit to provide the driving signal to the light-emitting unit. Thus, the
20 output electrode 13 can be directly used as one electrode of the light emitting unit. As
21 such, when the light-emitting unit is fabricated, ink droplets for forming the light-
22 emitting layer in the light-emitting unit are dropped onto the exposed output electrode
23 13 in the pixel region 3, and a light-emitting layer is formed on the output electrode
24 13. Then, another electrode of the light-emitting unit is fabricated on the side of the
25 light-emitting layer opposite from the output electrode 13, thereby completing the
26 fabrication of the light-emitting unit.

27 [0085] In the embodiments, using the output electrode 13 as one electrode of
28 the light-emitting unit simplifies the manufacturing process of the light-emitting unit
29 and reduces the manufacturing cost of the display substrate.

1 [0086] The manner in which the groove structure 2 is defined by the thin film
2 transistor is various. The fabrication of the thin film transistor in two specific manners
3 is described in detail below for illustration purpose only.

4 [0087] In the first manner, when each of the groove structures 2 corresponds
5 to one thin film transistor, as shown in Figs. 1a-1i, the step of fabricating the thin film
6 transistor specifically include the following:

7 [0088] First, the input electrode 11 and the first insulating island 12 are
8 formed on the base substrate 10. The input electrode 11 and the first insulating island
9 12 are disposed in the same layer. In the direction perpendicular to the substrate 10,
10 the height of the first insulating island 12 is greater than the height of the input
11 electrode 11. The orthographic projection of the input electrode 11 on the base
12 substrate 10 surrounds the orthographic projection of the first insulating island 12 on
13 the base substrate 10.

14 [0089] Then, the output electrode 13 is formed on the surface of the first
15 insulating island 12 opposite from the base substrate 10.

16 [0090] Then, an active layer 14 is formed on a side of the input electrode 11
17 opposite from the base substrate 10. The active layer 14 is in contact with the input
18 electrode 11 and a portion of the output electrode 13, respectively. The orthographic
19 projection of the active layer 14 on the base substrate 10 surrounds the orthographic
20 projection of the output electrode 13 on the base substrate 10.

21 [0091] Then, a second insulating layer 15 is formed on a side of the active
22 layer 14 opposite from the base substrate 10. Orthographic projection of the second
23 insulating layer 15 on the base substrate 10 surrounds the orthographic projection of
24 the output electrode 13 on the base substrate 10.

25 [0092] Then, a gate electrode 16 is formed on a side of the second insulating
26 layer 15 opposite from the base substrate 10, and orthographic projection of the gate
27 electrode 16 on the base substrate 10 is located inside the orthographic projection of
28 the second insulating layer 15 on the base substrate 10. The orthographic projection of
29 the gate electrode 16 on the base substrate 10 surrounds the orthographic projection of
30 the output electrode 13 on the base substrate 10. The orthographic projection of the

gate electrode 16 on the base substrate 10 at least partially overlaps the orthographic projection of the output electrode 13 on the base substrate 10.

[0093] In one embodiment, a conductive film is deposited on the base substrate 10 by using a magnetron sputtering device, and the conductive film is patterned to form the input electrode 11. The material of the conductive film may be Cu, Al or indium tin oxide (ITO), etc. Then, a first insulating film is formed by plasma enhanced chemical vapor deposition, and the first insulating film is patterned to form the first insulating island 12. The material of the first insulating film may be selected from silicon oxide, silicon nitride, or the like, or the first insulating island 12 may be made of an organic material. The input electrode 11 and the first insulating island 12 are formed in the same layer. In a direction perpendicular to the base substrate 10, the height of the first insulating island 12 is greater than the height of the input electrode 11, and the orthographic projection of the input electrode 11 on the base substrate 10 surrounds the orthographic projection of the first insulating island 12 on the base substrate 10.

[0094] Then, a conductive film is deposited on the side of the first insulating island 12 opposite from the base substrate 10 by using a magnetron sputtering device, and the conductive film is patterned to form an output electrode 13. The output electrode 13 is located on the surface of the first insulating island 12 opposite from the base substrate 10. The material of the conductive film may be Cu, Al or indium tin oxide (ITO) or the like.

[0095] Then, the active layer 14 is formed on the side of the input electrode 11 opposite from the base substrate 10 by using a magnetron sputtering apparatus or a solution method in combination with a patterning process. The active layer 14 is in contact with the input electrode 11 and a portion of the output electrode 13, respectively, and the orthographic projection of the active layer 14 on the base substrate 10 surrounds the orthographic projection of the output electrode 13 on the base substrate 10.

[0096] Then, a second insulating film is formed on the side of the active layer 14 opposite from the base substrate 10 by using plasma enhanced chemical vapor deposition, and the second insulating film is patterned to form a second insulating

1 layer 15. The material of the second insulating film may be selected from silicon
2 oxide, silicon nitride or the like, and the second insulating layer 15 serves as a gate
3 insulating layer in the thin film transistor. The orthographic projection of the second
4 insulating layer 15 on the base substrate 10 surrounds the orthographic projection of
5 the output electrode 13 on the base substrate 10.

6 [0097] Finally, a conductive film is deposited on the side of the second
7 insulating layer 15 opposite from the base substrate 10 by using a magnetron
8 sputtering device, and the conductive film is patterned to form the gate electrode 16.
9 The orthographic projection of the gate electrode 16 on the base substrate 10 is
10 located inside the orthographic projection of the second insulating layer 15 on the
11 base substrate 10. The orthographic projection of the gate electrode 16 on the base
12 substrate 10 surrounds the orthographic projection of the output electrode 13 on the
13 base substrate 10. The orthographic projection of the gate electrode 16 on the base
14 substrate 10 and the orthographic projection of the output electrode 13 on the base
15 substrate 10 at least partially overlap. The material of the conductive film may be
16 selected from Cu, Al or indium tin oxide (ITO).

17 [0098] In the thin film transistor fabricated by the above fabrication method,
18 the input electrode 11 and the first insulating island 12 are formed on the base
19 substrate 10, and the output electrode 13 is formed on the first insulating island 12
20 such that a height difference between the input electrode 11 and the output electrode
21 13 is formed. Then, the active layer 14, the second insulating layer 15 and the gate
22 electrode 16 are sequentially formed on the input electrode 11 and the output
23 electrode 13, thereby forming a height difference between the gate electrode 16 and
24 the output electrode 13. Since the active layer 14, the second insulating layer 15, and
25 the gate electrode 16 are all formed around the output electrode 13, and expose the
26 output electrodes 13, a groove structure 2 is formed on the output electrode 13. That is,
27 the output electrode 13 serves as the groove bottom of the groove structure 2, and the
28 side walls of the active layer 14, the second insulating layer 15, and the gate electrode
29 16 serve as the groove inner side walls of the groove structure 2. When the third
30 insulating layer 17 is subsequently formed, the third insulating layer 17 can expose the
31 output electrode 13 at the bottom of the groove structure while covering the inner

walls of the groove structure 2 and the gate electrode 16 at the topmost layer of the thin film transistor.

[0099] The thin film transistor fabricated by the above fabrication method can define an enclosed groove structure 2 such that third insulating layer 17 can define the pixel region 3 in the groove structure 2 as an enclosed region. Thus, when the ink droplets for forming the light-emitting layer in the light-emitting unit are dropped into the pixel region 3 by the ink-jet printing technique, the ink droplets can be defined in the pixel region 3 without flowing into other non-pixel regions. Therefore, the ink droplets are prevented from spreading into other areas to contaminate adjacent pixels, thereby avoiding cross-color phenomenon.

[00100] In the second manner, when each of the groove structures corresponds to two thin film transistors, two thin film transistors are disposed on opposite sides of the groove structure 2, as shown in FIGS. 1a to 1i, and the steps of fabricating the thin film transistor specifically include the following:

[00101] First, an input electrode 11 and a first insulating island 12 are formed on the base substrate 10. The input electrode 11 and the first insulating island 12 are disposed in the same layer. In a direction perpendicular to the base substrate 10, a height of the first insulating island 12 is greater than a height of the input electrode 11.

[00102] Then, the output electrode 13 is formed on the surface of the first insulating island 12 opposite from the base substrate 10.

[00103] Then, an active layer 14 is formed on a side of the input electrode 11 opposite from the base substrate 10, and the active layer 14 is in contact with the input electrode 11 and a portion of the output electrode 13, respectively.

[00104] Then, a second insulating layer 15 is formed on a side of the active layer 14 opposite from the base substrate 10.

[00105] Finally, a gate electrode 16 is formed on a side of the second insulating layer 15 opposite from the base substrate 10. Orthographic projection of the gate electrode 16 on the base substrate 10 is located inside orthographic projection of the second insulating layer 15 on the base substrate 10. The orthographic projection of the

gate electrode 16 on the base substrate 10 at least partially overlaps the orthographic projection of the output electrode 13 on the base substrate 10.

[00106] In one embodiment, the gate electrodes 16 of the two thin film transistors are connected, the input electrodes 11 of the two thin film transistors are connected, and the two thin film transistors share the same output electrode 13 and the same first insulating island 12.

[00107] In one embodiment, a conductive film is deposited on the base substrate 10 by using a magnetron sputtering device, and the conductive film is patterned to form an input electrode 11. The material of the conductive film may be selected from Cu, Al or indium tin oxide (ITO). Then, a first insulating film is formed by plasma enhanced chemical vapor deposition, and the first insulating film is patterned to form a first insulating island 12. The material of the first insulating film may be selected from silicon oxide, silicon nitride, or the like, or the first insulating island 12 may be made of an organic material. The input electrode 11 and the first insulating island 12 are disposed in the same layer, and the height of the first insulating island 12 is greater than the height of the input electrode 11 in a direction perpendicular to the base substrate 10.

[00108] In one embodiment, a conductive film is deposited on the side of the first insulating island 12 opposite from the base substrate 10 by using a magnetron sputtering device, and the conductive film is patterned to form an output electrode 13. The output electrode 13 is located on the surface of the first insulating island 12 opposite from the base substrate 10. The material of the conductive film may be Cu, Al or indium tin oxide (ITO).

[00109] In one embodiment, the active layer 14 is formed on the side of the input electrode 11 opposite from the base substrate 10 by using a magnetron sputtering device or a solution method in combination with a patterning process. The active layer 14 is in contact with the input electrode 11 and a portion of the output electrode 13 respectively.

[00110] In one embodiment, a second insulating film is formed on the side of the active layer 14 opposite from the base substrate 10 by using plasma enhanced chemical vapor deposition, and the second insulating film is patterned to form a

second insulating layer 15. The material of the second insulating film may be selected from silicon oxide, silicon nitride, or the like, and the second insulating layer 15 serves as a gate insulating layer in the thin film transistor.

[00111] Finally, a conductive film is deposited on the side of the second insulating layer 15 opposite from the base substrate 10 by using a magnetron sputtering device, and the conductive film is patterned to form the gate electrode 16. The orthographic projection of the gate electrode 16 on the base substrate 10 is located inside the orthographic projection of the second insulating layer 15 on the base substrate 10. The orthographic projection of the gate electrode 16 on the base substrate 10 at least partially overlaps the orthographic projection of the output electrode 13 on the base substrate 10. The material of the above conductive film may be selected from Cu, Al or indium tin oxide (ITO).

[00112] In fabricating the thin film transistor according to some embodiments of the present disclosure, the input electrode 11 and the first insulating island 12 are formed on the base substrate 10, and the output electrode 13 is formed on the first insulating island 12 such that a height difference is formed between the input electrode 11 and the output electrode 13. Then, the active layer 14, the second insulating layer 15 and the gate electrode 16 are sequentially formed on the input electrode 11 and the output electrode 13, thereby forming a height difference between the gate electrode 16 and the output electrode 13. The active layer 14, the second insulating layer 15, and the gate electrode 16 are stacked on the output electrode 13, and all the layers can expose at least a part of the output electrode 13. Therefore, the output electrode 13 can serve as the groove bottom of the groove structure 2, and the sidewalls of the active layer 14, the second insulating layer 15, and the gate 16 serve as the groove inner sidewalls of the groove structure 2. Therefore, the two thin film transistors are disposed on opposite sides of the corresponding groove structure by using the above manufacturing method, so that the two thin film transistors form opposite side walls of the groove structure 2. As such, the two thin film transistors define an unenclosed groove structure 2. When the third insulating layer 17 is subsequently formed, the third insulating layer 17 can expose the output electrode 13 at the bottom of the groove structure while covering the sidewalls of the groove structure 2 and the gate electrode 16 at the topmost layer of the thin film transistor.

When an inkjet printing technique is used to drop ink droplets for forming a light-emitting layer in a light-emitting unit into a pixel region, the ink droplets can also be confined in the pixel region without flowing into other non-pixel regions.

[00113] In some embodiments, the manufacturing method provided by the above embodiments further includes the following:

[00114] The portion of the third insulating layer 17 outside the groove structure 2 is exposed to an ultraviolet ray, so that a surface of the portion of the third insulating layer 17 outside the groove structure 2 opposite from the base substrate 10 is hydrophobic.

[00115] In one embodiment, after the third insulating layer 17 is formed, the portion of the third insulating layer 17 outside the groove structure 2 may be exposed to an ultraviolet ray, and a surface of the portion of the third insulating layer 17 outside the groove structure 2 opposite from the base substrate 10 is hydrophobic. More specifically, the mask plate including a light-shielding region and a light-transmitting region may be aligned with the third insulating layer 17 such that the light-transmitting region of the mask plate corresponds to the portion of the third insulating layer 17 outside the groove structure 2, and the light-shielding region of the mask corresponds to the portion other than the portion of the third insulating layer 17 outside the groove structure 2. Then, the third insulating layer 17 is exposed to the ultraviolet ray through the mask, so that the portion of the third insulating layer 17 located outside the groove structure 2 under irradiation of the ultraviolet ray changes the surface property. As such, the surface of the portion of the third insulating layer 17 located outside the groove structure 2 is made hydrophobic.

[00116] In the embodiment, the light-emitting layer in the light-emitting unit is generally fabricated by inkjet printing technology, and the portion where the third insulating layer 17 is disposed outside the groove structure 2 is hydrophobic on its surface opposite from the base substrate 10. As such, it is possible to enable droplets for forming the light-emitting layer to be printed into the pixel region 3 more stably and accurately when the light-emitting layer is formed by inkjet printing technology.

[00117] The principles and the embodiments of the present disclosure are set forth in the specification. The description of the embodiments of the present

1 disclosure is only used to help understand the apparatus and method of the present
2 disclosure and the core idea thereof. Meanwhile, for a person of ordinary skill in the
3 art, the disclosure relates to the scope of the disclosure, and the technical scheme is
4 not limited to the specific combination of the technical features, but also covers other
5 technical schemes which are formed by combining the technical features or the
6 equivalent features of the technical features without departing from the inventive
7 concept. For example, a technical scheme may be obtained by replacing the features
8 described above as disclosed in this disclosure (but not limited to) with similar
9 features.

CLAIMS

What is claimed is:

1. A pixel structure, comprising:

a base substrate;

a first insulating island on a side of the base substrate;

a first electrode on a side of the first insulating island opposite from the base substrate;

a second electrode on the base substrate and at a peripheral area of the first insulating island;

an active layer electrically connected to the first electrode and the second electrode;

a second insulating layer on a side of the active layer opposite from the base substrate;

a gate electrode on a side of the second insulating layer opposite from the base substrate; and

a third insulating layer on a side of the gate electrode opposite from the base substrate; wherein,

the third insulating layer encloses a groove structure with the first electrode;

the third insulating layer covers at least a side surface of one of the active layer, the second insulating layer or the gate electrode to form the groove structure with the first electrode;

a height of the first insulating island in a direction perpendicular to the base substrate is greater than a height of the second electrode in the direction perpendicular to the base substrate; and

the first electrode and the second electrode are two different electrodes selected from a source electrode and a drain electrode.

2. The pixel structure of claim 1, wherein a surface of the second electrode opposite from the base substrate is not in a same level with a surface of the first insulating island opposite from the base substrate.

3. The pixel structure of claim 1, wherein the third insulating layer serves as side walls of the groove structure, and the first electrode serves as a bottom

1 of the groove structure.

2 4. The pixel structure of any one of claims 1-3, wherein the second electrode
3 surrounds the first insulating island.

4 5. The pixel structure of any one of claims 1-3, wherein the second electrode
5 comprises a first sub-electrode and a second sub-electrode spaced apart from
6 each other, the first sub-electrode and the second sub-electrode are on
7 opposite sides of the first insulating island.

8 6. The pixel structure of claim 3 or 4, wherein the second electrode is in
9 contact with side surfaces of the first insulating island.

10 7. The pixel structure of any one of claims 1-6, wherein the first electrode is
11 conformal with the first insulating island.

12 8. The pixel structure of any one of claims 1-7, wherein the active layer
13 contacts with the first electrode, and side surfaces of the first insulating
14 island and the second electrode.

15 9. The pixel structure of any one of claims 1-8, wherein the second insulating
16 layer is conformal with the active layer.

17 10. The pixel structure of any one of claims 1-9, wherein the gate electrode is
18 conformal with the second insulating layer.

19 11. The pixel structure of any one of claims 1-10, wherein a portion of the third
20 insulating layer is conformal with the gate electrode and another portion
21 thereof covers side surfaces of the active layer, the second insulating layer
22 and the gate electrode to form the groove structure with the first electrode.

23 12. The pixel structure of any one of claims 1-11, wherein the active layer
24 contacts with a side surface of the first insulating island and a side surface of
25 the first electrode.

26 13. The display substrate of any one of claims 1-12, wherein at least a surface of
27 the third insulating layer opposite from the base substrate is hydrophobic.

28 14. A display apparatus, comprising the pixel structure of any one of claims 1-
29 13.

30 15. A method of manufacturing a pixel structure, comprising:

31 forming a base substrate;

32 forming a first insulating island on a side of the substrate;

forming a first electrode on a side of the first insulating island opposite from the base substrate;

forming a second electrode on the base substrate and at a peripheral area of the first insulating island;

forming an active layer electrically connected to the first electrode and the second electrode;

forming a second insulating layer on a side of the active layer opposite from the base substrate;

forming a gate electrode on a side of the second insulating layer opposite from the base substrate; and

forming a third insulating layer on a side of the gate electrode opposite from the base substrate; wherein,

the third insulating layer encloses a groove structure with the first electrode;

the third insulating layer covers at least a side surface of one of the active layer, the second insulating layer or the gate electrode to form the groove structure with the first electrode;

a height of the first insulating island in a direction perpendicular to the base substrate is greater than a height of the second electrode in the direction perpendicular to the base substrate; and

the first electrode and the second electrode are two different electrodes selected from a source electrode and a drain electrode.

16. The method of claim 15, wherein a surface of the second electrode opposite from the base substrate is not in a same level with a surface of the first insulating island opposite from the base substrate.

17. The method of claim 15, wherein the second electrode surrounds the first insulating island.

18. The method of claim 15, wherein the third insulating layer serves as side walls of the groove structure and the first electrode serves as a bottom of the groove structure.

19. The method of claim 15, wherein the second electrode comprises a first sub-electrode and a second sub-electrode spaced apart from each other, and the

- 1 first sub-electrode and the second sub-electrode are on opposite sides of the
2 first insulating island.
- 3 20. The method of manufacturing a display substrate of any one of claims 15-19,
4 further comprising:
5 exposing a portion of the third insulating layer outside the groove structure
6 to an ultraviolet ray, so that a surface of the portion of the insulating film
7 layer outside the groove structure opposite from the base substrate is
8 hydrophobic.

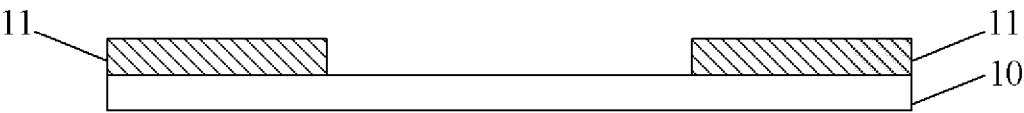


Fig. 1a

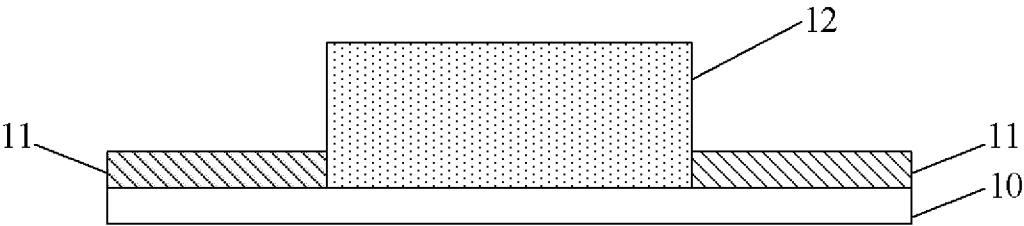


Fig. 1b

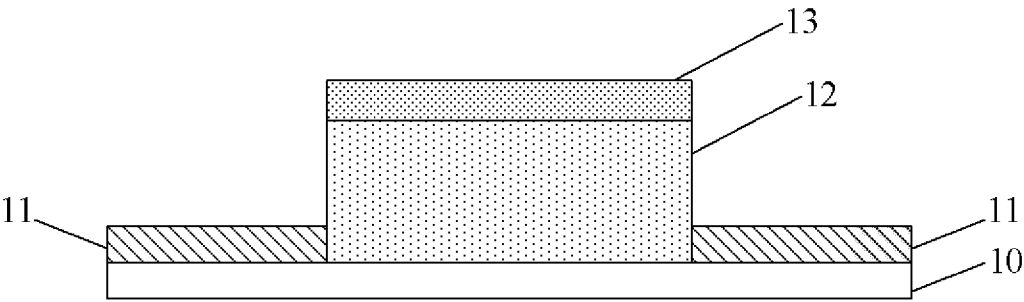


Fig. 1c

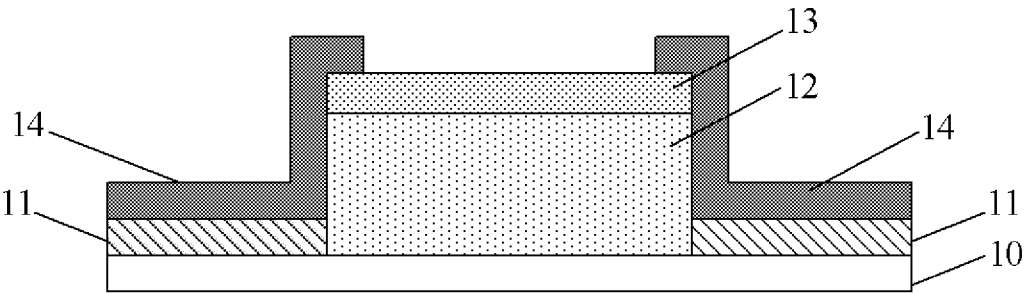


Fig. 1d

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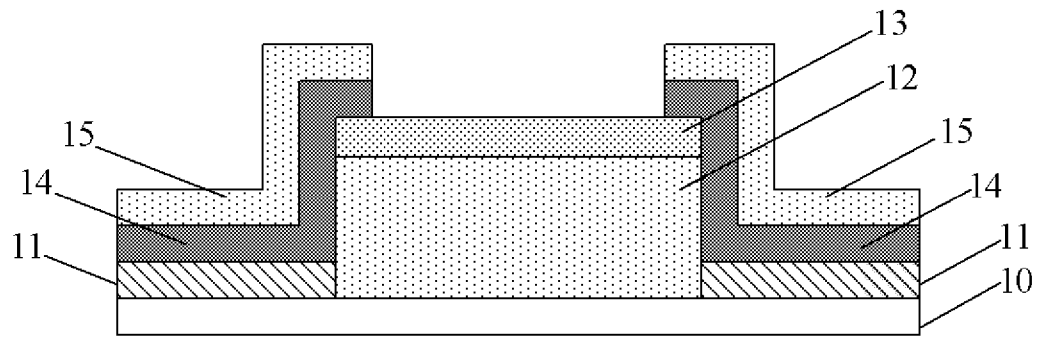


Fig. 1e

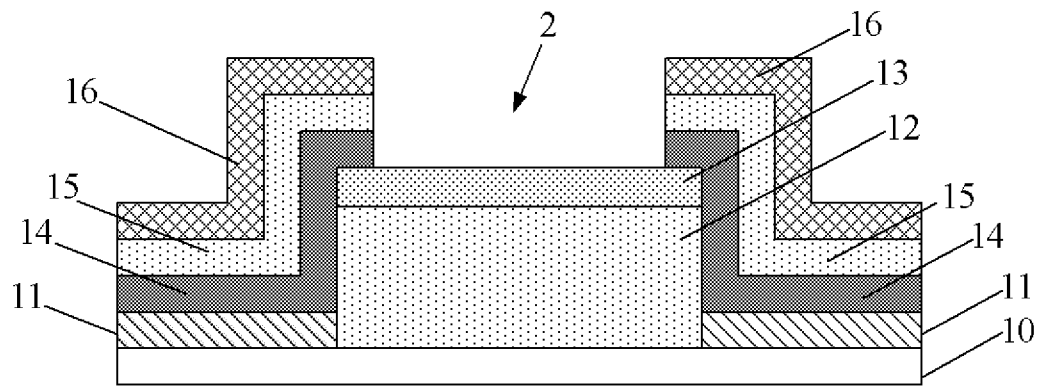


Fig. 1f

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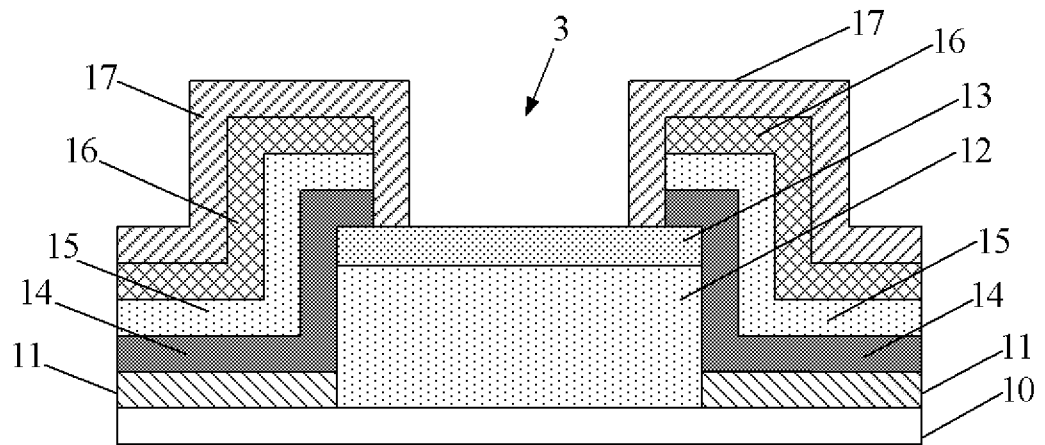


Fig. 1g

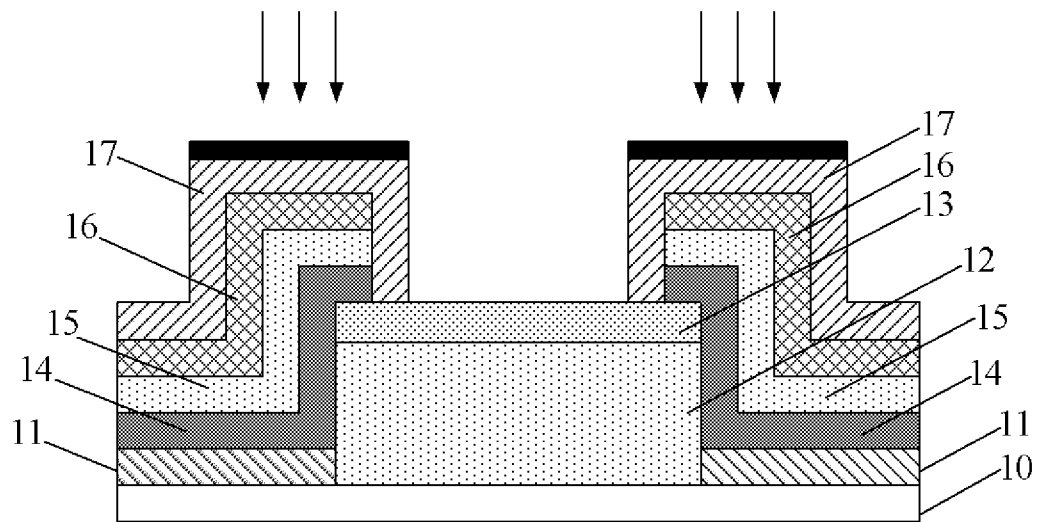


Fig. 1h

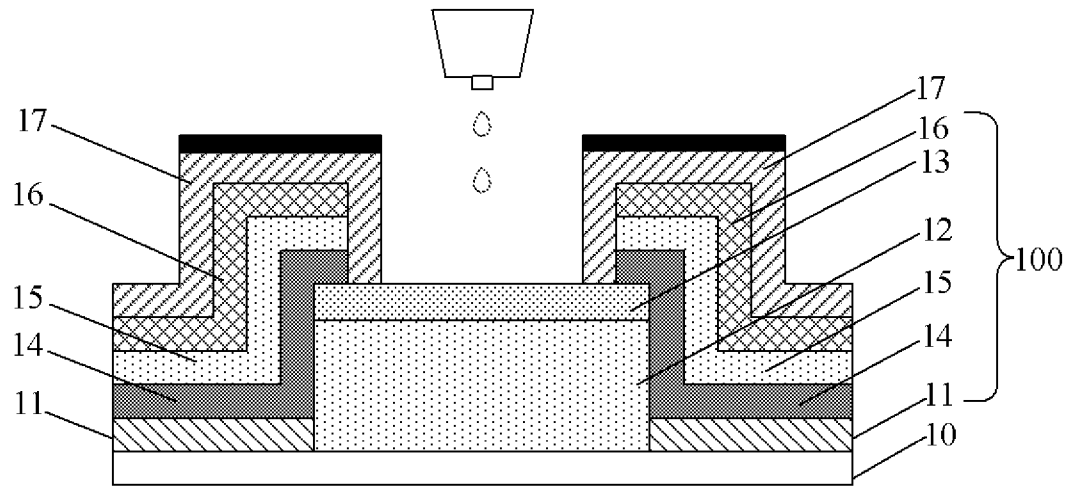


Fig. 1i

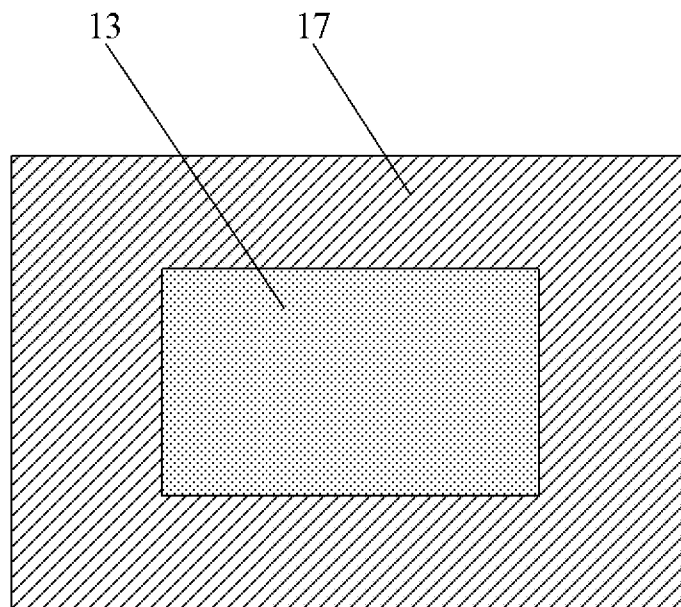


Fig. 2

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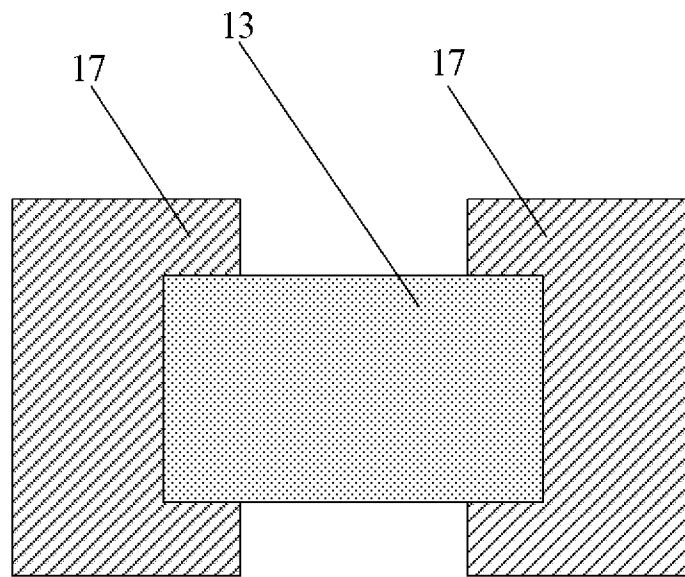


Fig. 3

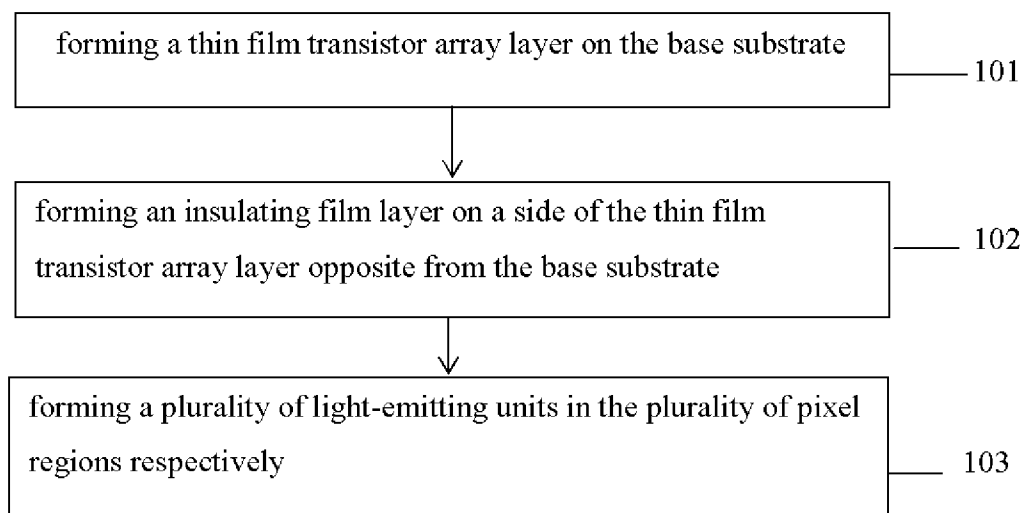


Fig. 4

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2019/079284

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/32(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT,WPI,EPODOC,IEEE,CNKI,GOOGLE: pixel, array, trench, groove, concave, dam, limit, define, ink, print, vertical, thin film transistor, tft, channel, active area

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN 107369691 A (SAMSUNG DISPLAY CO., LTD.) 21 November 2017 (2017-11-21) description, paragraphs [0047]-[0055], [0119-0121], figures 1 and 9	1-20
A	CN 207517701 U (EMMO TECHNOLOGIES LTD.) 19 June 2018 (2018-06-19) the whole document	1-20
A	CN 107665905 A (LG DISPLAY CO., LTD.) 06 February 2018 (2018-02-06) the whole document	1-20
A	US 2007102731 A1 (SAKAGAMI, EIJI) 10 May 2007 (2007-05-10) the whole document	1-20
A	US 2011049611 A1 (KABUSHIKI KAISHA TOSHIBA) 03 March 2011 (2011-03-03) the whole document	1-20

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

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“E” earlier application or patent but published on or after the international filing date

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“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

23 August 2019

Date of mailing of the international search report

04 September 2019

Name and mailing address of the ISA/CN

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Telephone No. 86-(10)-53961226

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2019/079284

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	107369691	A	21 November 2017	KR	20170128665	A	23 November 2017
				US	2017330924	A1	16 November 2017
CN	207517701	U	19 June 2018	None			
CN	107665905	A	06 February 2018	US	2018033842	A1	01 February 2018
				KR	20180013377	A	07 February 2018
				EP	3276666	A1	31 January 2018
US	2007102731	A1	10 May 2007	JP	2007129136	A	24 May 2007
				US	8043930	B2	25 October 2011
				US	2012025295	A1	02 February 2012
				JP	4791799	B2	12 October 2011
				US	2009130809	A1	21 May 2009
US	2011049611	A1	03 March 2011	JP	2011049395	A	10 March 2011
				JP	4987918	B2	01 August 2012