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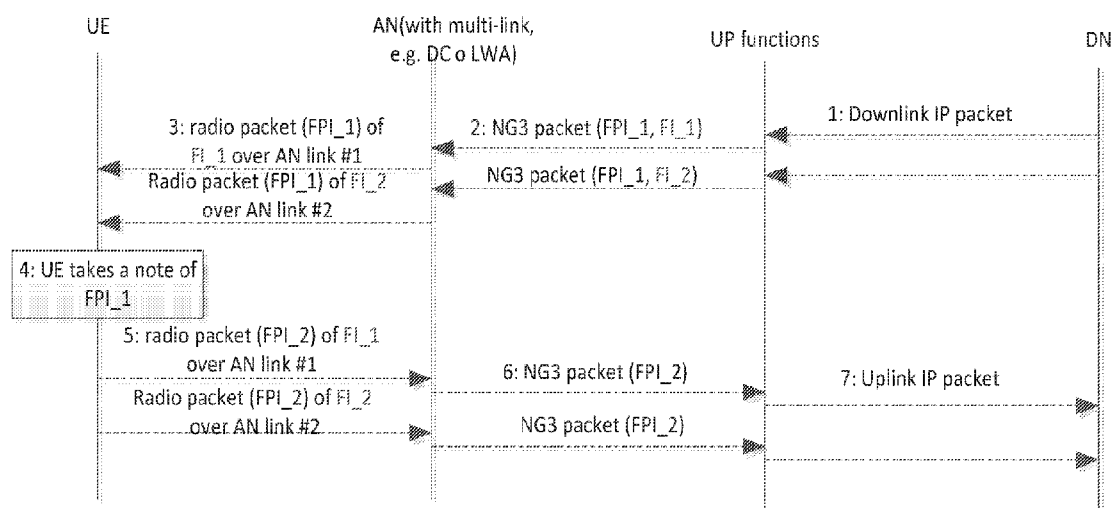
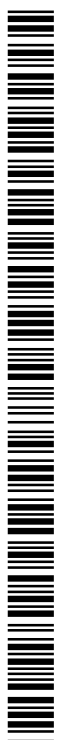


FIG. 9

(57) Abstract: In the 5G core network (CN), aggregates of data packets are mapped to different quality of service (QoS) flows as indicated by a QoS marking in the header of a protocol used to transport the packets through the CN. Different service data flows (SDF) through the CN may belong the same QoS flow. Described herein are methods and apparatus by which the 5G CN and RAN may more flexibly handle individual SDFs belonging to the same QoS flow in order to obtain greater throughput and/or lower latency.



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CORE NETWORK-ASSISTED FLOW-BASED BEARER SPLITTING

Priority Claim

- 5 [0001] This application claims priority to United States Provisional Patent Application Serial No. 62/406,240, filed October 10, 2016, which is incorporated herein by reference in its entirety.

Technical Field

- [0002] Embodiments described herein relate generally to wireless
10 networks and communications systems. Some embodiments relate to cellular communication networks including 3GPP (Third Generation Partnership Project) networks, 3GPP LTE (Long Term Evolution) networks, 3GPP LTE-A (LTE Advanced), and 3GPP fifth generation networks, although the scope of the embodiments is not limited in this respect.

15

Background

- [0003] Mobile wireless communications systems have evolved from early voice-only systems to today's highly sophisticated integrated communication platforms in which fourth generation (4G) LTE networks provide data for
20 massive mobile services. Next generation (a.k.a, fifth generation or 5G) technology is being developed to meet the increased future demands brought about by use cases such as enhanced mobile broadband, ultra-reliable and low-latency communications, and machine-to-machine communications for enabling the Internet of Things (IoT). 5G technology builds on a combination of existing
25 4G and new technologies to meet these demands. In order to meet the quality of service (QoS) requirements of future applications, a new QoS framework has been developed for 5G networks. A concern of the present disclosure is enabling flexible routing of individual application data flows within the context of the 5G QoS framework.

30

Brief Description of the Drawings

- [0004] FIG. 1 is a block diagram of a radio architecture in accordance with
5 some embodiments.
- [0005] FIG. 2 illustrates a front-end module circuitry for use in the radio
architecture of FIG. 1 in accordance with some embodiments.
- [0006] FIG. 3 illustrates a radio IC circuitry for use in the radio architecture
of FIG. 1 in accordance with some embodiments.
- 10 [0007] FIG. 4 illustrates a baseband processing circuitry for use in the radio
architecture of FIG. 1 in accordance with some embodiments.
- [0008] FIG. 5 illustrates an example of a computing machine such as an
evolved Node B (eNB) or next generation evolved node B (gNB) according to
some embodiments.
- 15 [0009] FIG. 6 illustrates an example of a user equipment (UE) device
according to some embodiments.
- [0010] FIG. 7 illustrates the architecture of a 5G network in accordance with
some embodiments.
- [0011] FIG. 8 illustrates the user plane protocol stacks of a user equipment,
20 and access network, and a user plane function in accordance with some
embodiments.
- [0012] FIG. 9 illustrates an example of a core network-assisted flow-
based bearer splitting call-flow procedure in accordance with some
embodiments.

25

Detailed Description

- [0013] The QoS provided by a network to users relates to the network's
performance in handling data packets. The quality of service afforded to a
30 particular class of data packets may include a guaranteed or non-guaranteed bit
rate (GBR or non-GBR) as well as other parameters relating to latency, packet

loss, and bandwidth. In the 4G evolved packet system (EPS), the QoS is managed based on the EPS bearer in both the evolved packet core (EPC) and the radio access network (RAN). That is, all types of traffic mapped to the same EPS bearer receive the same level packet forwarding treatment, where a bearer represents a transmission pathway through the network. In contrast, the bearer concept is not considered in the 5G core network (CN) but may be used in 5G RAN. In the 5G CN, aggregates of data packets are mapped to different QoS flows as indicated by a QoS marking in the header of a protocol used to transport the packets through the CN.

[0014] A user equipment (UE) receives services from the 5G by establishing a protocol data unit (PDU) session that represents a logical connection between the UE and a data network (DN) to which the 5G CN is connected. Applications in the UE and the DN are then able to exchange PDUs according to various protocols such as internet protocol (IP) and Ethernet. From the perspective of the 5G CN, these PDUs are service data units (SDUs) and may be referred to as service data flows (SDFs). For example, a particular SDF may be an IP flow as specified by an IP-tuple that includes a source address, a destination address, source port value, destination port value, and transport protocol type (e.g., transport control protocol (TCP) or user datagram protocol (UDP)). A particular SDF may also represent an aggregate of IP or other protocol flows such as an SDF specified by an IP-tuple that includes a range of source and destination addresses. Described herein are methods and apparatus by which the 5G CN and RAN may more flexibly handle individual SDFs belonging to the same QoS flow in order to obtain greater throughput and/or lower latency.

Example Radio Architecture

[0015] FIG. 1 is a block diagram of a radio architecture 100 in accordance with some embodiments. Radio architecture 100 may include radio front-end module (FEM) circuitry 104, radio IC circuitry 106 and baseband processing circuitry 108. Radio architecture 100 as shown includes both Wireless Local Area Network (WLAN) functionality and Bluetooth (BT) functionality although embodiments are not so limited. In this disclosure, “WLAN” and “Wi-Fi” are used interchangeably.

[0016] FEM circuitry 104 may include a WLAN or Wi-Fi FEM circuitry 104A and a Bluetooth (BT) FEM circuitry 104B. The WLAN FEM circuitry 104B may include a receive signal path comprising circuitry configured to operate on WLAN RF signals received from one or more antennas 101, to
5 amplify the received signals and to provide the amplified versions of the received signals to the WLAN radio IC circuitry 106A for further processing. The BT FEM circuitry 104B may include a receive signal path which may include circuitry configured to operate on BT RF signals received from one or more antennas 102, to amplify the received signals and to provide the amplified
10 versions of the received signals to the BT radio IC circuitry 106B for further processing. FEM circuitry 104A may also include a transmit signal path which may include circuitry configured to amplify WLAN signals provided by the radio IC circuitry 106A for wireless transmission by one or more of the antennas 101. In addition, FEM circuitry 104B may also include a transmit signal path
15 which may include circuitry configured to amplify BT signals provided by the radio IC circuitry 106B for wireless transmission by the one or more antennas. In the embodiment of FIG. 1, although FEM 104A and FEM 104B are shown as being distinct from one another, embodiments are not so limited, and include within their scope the use of an FEM (not shown) that includes a transmit path
20 and/or a receive path for both WLAN and BT signals, or the use of one or more FEM circuitries where at least some of the FEM circuitries share transmit and/or receive signal paths for both WLAN and BT signals.

[0017] Radio IC circuitry 106 as shown may include WLAN radio IC circuitry 106A and BT radio IC circuitry 106B. The WLAN radio IC circuitry
25 106a may include a receive signal path which may include circuitry to down-convert WLAN RF signals received from the FEM circuitry 104A and provide baseband signals to WLAN baseband processing circuitry 108A. BT radio IC circuitry 106B may in turn include a receive signal path which may include circuitry to down-convert BT RF signals received from the FEM circuitry 104B
30 and provide baseband signals to BT baseband processing circuitry 108B. WLAN radio IC circuitry 106A may also include a transmit signal path which may include circuitry to up-convert WLAN baseband signals provided by the WLAN baseband processing circuitry 108A and provide WLAN RF output

signals to the FEM circuitry 104A for subsequent wireless transmission by the one or more antennas 101. BT radio IC circuitry 106B may also include a transmit signal path which may include circuitry to up-convert BT baseband signals provided by the BT baseband processing circuitry 108B and provide BT RF output signals to the FEM circuitry 104B for subsequent wireless transmission by the one or more antennas 101. In the embodiment of FIG. 1, although radio IC circuitries 106A and 106B are shown as being distinct from one another, embodiments are not so limited, and include within their scope the use of a radio IC circuitry (not shown) that includes a transmit signal path and/or a receive signal path for both WLAN and BT signals, or the use of one or more radio IC circuitries where at least some of the radio IC circuitries share transmit and/or receive signal paths for both WLAN and BT signals.

[0018] Baseband processing circuitry 108 may include a WLAN baseband processing circuitry 108A and a BT baseband processing circuitry 108B. The WLAN baseband processing circuitry 108A may include a memory, such as, for example, a set of RAM arrays in a Fast Fourier Transform or Inverse Fast Fourier Transform block (not shown) of the WLAN baseband processing circuitry 108A. Each of the WLAN baseband circuitry 108A and the BT baseband circuitry 108B may further include one or more processors and control logic to process the signals received from the corresponding WLAN or BT receive signal path of the radio IC circuitry 106, and to also generate corresponding WLAN or BT baseband signals for the transmit signal path of the radio IC circuitry 106. Each of the baseband processing circuitries 108A and 108B may further include physical layer (PHY) and medium access control layer (MAC) circuitry, and may further interface with application processor 110 for generation and processing of the baseband signals and for controlling operations of the radio IC circuitry 106.

[0019] Referring still to FIG. 1, according to the shown embodiment, WLAN-BT coexistence circuitry 113 may include logic providing an interface between the WLAN baseband circuitry 108A and the BT baseband circuitry 108B to enable use cases requiring WLAN and BT coexistence. In addition, a switch 103 may be provided between the WLAN FEM circuitry 104A and the BT FEM circuitry 104B to allow switching between the WLAN and BT radios

according to application needs. In addition, although the antennas 101 are depicted as being respectively connected to the WLAN FEM circuitry 104A and the BT FEM circuitry 104B, embodiments include within their scope the sharing of one or more antennas as between the WLAN and BT FEMs, or the provision
5 of more than one antenna connected to each of FEM 104A or 104B.

[0020] In some embodiments, the front-end module circuitry 104, the radio IC circuitry 106, and baseband processing circuitry 108 may be provided on a single radio card, such as wireless radio card 102. In some other embodiments, the one or more antennas 101, the FEM circuitry 104 and the radio IC circuitry
10 106 may be provided on a single radio card. In some other embodiments, the radio IC circuitry 106 and the baseband processing circuitry 108 may be provided on a single chip or integrated circuit (IC), such as IC 112.

[0021] In some embodiments, the wireless radio card 102 may include a WLAN radio card and may be configured for Wi-Fi communications, although
15 the scope of the embodiments is not limited in this respect. In some of these embodiments, the radio architecture 100 may be configured to receive and transmit orthogonal frequency division multiplexed (OFDM) or orthogonal frequency division multiple access (OFDMA) communication signals over a multicarrier communication channel. The OFDM or OFDMA signals may
20 comprise a plurality of orthogonal subcarriers.

[0022] In some of these multicarrier embodiments, radio architecture 100 may be part of a Wi-Fi communication station (STA) such as a wireless access point (AP), a base station or a mobile device including a Wi-Fi device. In some of these embodiments, radio architecture 100 may be configured to transmit and
25 receive signals in accordance with specific communication standards and/or protocols, such as any of the Institute of Electrical and Electronics Engineers (IEEE) standards including, 802.11n-2009, IEEE 802.11-2012, 802.11n-2009, 802.11ac, and/or 802.11ax standards and/or proposed specifications for WLANs, although the scope of embodiments is not limited in this respect. Radio
30 architecture 100 may also be suitable to transmit and/or receive communications in accordance with other techniques and standards.

[0023] In some embodiments, the radio architecture 100 may be configured for high-efficiency (HE) Wi-Fi (HEW) communications in accordance with the

IEEE 802.11ax standard. In these embodiments, the radio architecture 100 may be configured to communicate in accordance with an OFDMA technique, although the scope of the embodiments is not limited in this respect.

[0024] In some other embodiments, the radio architecture 100 may be
5 configured to transmit and receive signals transmitted using one or more other modulation techniques such as spread spectrum modulation (e.g., direct sequence code division multiple access (DS-CDMA) and/or frequency hopping code division multiple access (FH-CDMA)), time-division multiplexing (TDM) modulation, and/or frequency-division multiplexing (FDM) modulation,
10 although the scope of the embodiments is not limited in this respect.

[0025] In some embodiments, as further shown in FIG. 1, the BT baseband circuitry 108B may be compliant with a Bluetooth (BT) connectivity standard such as Bluetooth, Bluetooth 4.0 or Bluetooth 5.0, or any other iteration of the Bluetooth Standard. In embodiments that include BT functionality as shown for
15 example in Fig. 1, the radio architecture 100 may be configured to establish a BT synchronous connection oriented (SCO) link and or a BT low energy (BT LE) link. In some of the embodiments that include functionality, the radio architecture 100 may be configured to establish an extended SCO (eSCO) link for BT communications, although the scope of the embodiments is not limited in
20 this respect. In some of these embodiments that include a BT functionality, the radio architecture may be configured to engage in a BT Asynchronous Connection-Less (ACL) communications, although the scope of the embodiments is not limited in this respect. In some embodiments, as shown in FIG. 1, the functions of a BT radio card and WLAN radio card may be combined
25 on a single wireless radio card, such as single wireless radio card 102, although embodiments are not so limited, and include within their scope discrete WLAN and BT radio cards

[0026] In some embodiments, the radio-architecture 100 may include other radio cards, such as a cellular radio card configured for cellular (e.g., 3GPP such
30 as LTE, LTE-Advanced or 5G communications).

[0027] In some IEEE 802.11 embodiments, the radio architecture 100 may be configured for communication over various channel bandwidths including bandwidths having center frequencies of about 900 MHz, 2.4 GHz, 5 GHz, and

bandwidths of about 1 MHz, 2 MHz, 2.5 MHz, 4 MHz, 5MHz, 8 MHz, 10 MHz, 16 MHz, 20 MHz, 40MHz, 80MHz (with contiguous bandwidths) or 80+80MHz (160MHz) (with non-contiguous bandwidths). In some embodiments, a 320 MHz channel bandwidth may be used. The scope of the embodiments is not limited with respect to the above center frequencies however.

[0028] FIG. 2 illustrates FEM circuitry 200 in accordance with some embodiments. The FEM circuitry 200 is one example of circuitry that may be suitable for use as the WLAN and/or BT FEM circuitry 104A/104B (FIG. 1), although other circuitry configurations may also be suitable.

[0029] In some embodiments, the FEM circuitry 200 may include a TX/RX switch 202 to switch between transmit mode and receive mode operation. The FEM circuitry 200 may include a receive signal path and a transmit signal path. The receive signal path of the FEM circuitry 200 may include a low-noise amplifier (LNA) 206 to amplify received RF signals 203 and provide the amplified received RF signals 207 as an output (e.g., to the radio IC circuitry 106 (FIG. 1)). The transmit signal path of the circuitry 200 may include a power amplifier (PA) to amplify input RF signals 209 (e.g., provided by the radio IC circuitry 106), and one or more filters 212, such as band-pass filters (BPFs), low-pass filters (LPFs) or other types of filters, to generate RF signals 215 for subsequent transmission (e.g., by one or more of the antennas 101 (FIG. 1)).

[0030] In some dual-mode embodiments for Wi-Fi communication, the FEM circuitry 200 may be configured to operate in either the 2.4 GHz frequency spectrum or the 5 GHz frequency spectrum. In these embodiments, the receive signal path of the FEM circuitry 200 may include a receive signal path duplexer 204 to separate the signals from each spectrum as well as provide a separate LNA 206 for each spectrum as shown. In these embodiments, the transmit signal path of the FEM circuitry 200 may also include a power amplifier 210 and a filter 212, such as a BPF, a LPF or another type of filter for each frequency spectrum and a transmit signal path duplexer 214 to provide the signals of one of the different spectrums onto a single transmit path for subsequent transmission by the one or more of the antennas 101 (FIG. 1). In some embodiments, BT communications may utilize the 2.4 GHZ signal paths and may utilize the same FEM circuitry 200 as the one used for WLAN communications.

[0031] FIG. 3 illustrates radio IC circuitry 300 in accordance with some embodiments. The radio IC circuitry 300 is one example of circuitry that may be suitable for use as the WLAN or BT radio IC circuitry 106A/106B (FIG. 1), although other circuitry configurations may also be suitable.

5 [0032] In some embodiments, the radio IC circuitry 300 may include a receive signal path and a transmit signal path. The receive signal path of the radio IC circuitry 300 may include at least mixer circuitry 302, such as, for example, down-conversion mixer circuitry, amplifier circuitry 306 and filter circuitry 308. The transmit signal path of the radio IC circuitry 300 may include
10 at least filter circuitry 312 and mixer circuitry 314, such as, for example, up-conversion mixer circuitry. Radio IC circuitry 300 may also include synthesizer circuitry 304 for synthesizing a frequency 305 for use by the mixer circuitry 302 and the mixer circuitry 314. The mixer circuitry 302 and/or 314 may each, according to some embodiments, be configured to provide direct conversion
15 functionality. The latter type of circuitry presents a much simpler architecture as compared with standard super-heterodyne mixer circuitries, and any flicker noise brought about by the same may be alleviated for example through the use of OFDM modulation. FIG. 3 illustrates only a simplified version of a radio IC circuitry, and may include, although not shown, embodiments where each of the
20 depicted circuitries may include more than one component. For instance, mixer circuitry 320 and/or 314 may each include one or more mixers, and filter circuitries 308 and/or 312 may each include one or more filters, such as one or more BPFs and/or LPFs according to application needs. For example, when mixer circuitries are of the direct-conversion type, they may each include two or
25 more mixers.

[0033] In some embodiments, mixer circuitry 302 may be configured to down-convert RF signals 207 received from the FEM circuitry 104 (FIG. 1) based on the synthesized frequency 305 provided by synthesizer circuitry 304. The amplifier circuitry 306 may be configured to amplify the down-converted
30 signals and the filter circuitry 308 may include a LPF configured to remove unwanted signals from the down-converted signals to generate output baseband signals 307. Output baseband signals 307 may be provided to the baseband processing circuitry 108 (FIG. 1) for further processing. In some embodiments,

the output baseband signals 307 may be zero-frequency baseband signals, although this is not a requirement. In some embodiments, mixer circuitry 302 may comprise passive mixers, although the scope of the embodiments is not limited in this respect.

- 5 **[0034]** In some embodiments, the mixer circuitry 314 may be configured to up-convert input baseband signals 311 based on the synthesized frequency 305 provided by the synthesizer circuitry 304 to generate RF output signals 209 for the FEM circuitry 104. The baseband signals 311 may be provided by the baseband processing circuitry 108 and may be filtered by filter circuitry 312.
- 10 The filter circuitry 312 may include a LPF or a BPF, although the scope of the embodiments is not limited in this respect.

- [0035]** In some embodiments, the mixer circuitry 302 and the mixer circuitry 314 may each include two or more mixers and may be arranged for quadrature down-conversion and/or up-conversion respectively with the help of synthesizer
- 15 304. In some embodiments, the mixer circuitry 302 and the mixer circuitry 314 may each include two or more mixers each configured for image rejection (e.g., Hartley image rejection). In some embodiments, the mixer circuitry 302 and the mixer circuitry 314 may be arranged for direct down-conversion and/or direct up-conversion, respectively. In some embodiments, the mixer circuitry 302 and
- 20 the mixer circuitry 314 may be configured for super-heterodyne operation, although this is not a requirement.

- [0036]** Mixer circuitry 302 may comprise, according to one embodiment: quadrature passive mixers (e.g., for the in-phase (I) and quadrature phase (Q) paths). In such an embodiment, RF input signal 207 from Fig. 3 may be down-
- 25 converted to provide I and Q baseband output signals to be sent to the baseband processor

- [0037]** Quadrature passive mixers may be driven by zero and ninety degree time-varying LO switching signals provided by a quadrature circuitry which may be configured to receive a LO frequency (f_{LO}) from a local oscillator or a
- 30 synthesizer, such as LO frequency 305 of synthesizer 304 (FIG. 3). In some embodiments, the LO frequency may be the carrier frequency, while in other embodiments, the LO frequency may be a fraction of the carrier frequency (e.g., one-half the carrier frequency, one-third the carrier frequency). In some

embodiments, the zero and ninety degree time-varying switching signals may be generated by the synthesizer, although the scope of the embodiments is not limited in this respect.

5 [0038] In some embodiments, the LO signals may differ in duty cycle (the percentage of one period in which the LO signal is high) and/or offset (the difference between start points of the period). In some embodiments, the LO signals may have a 25% duty cycle and a 50% offset. In some embodiments, each branch of the mixer circuitry (e.g., the in-phase (I) and quadrature phase (Q) path) may operate at a 25% duty cycle, which may result in a significant
10 reduction in power consumption.

[0039] The RF input signal 207 (FIG. 2) may comprise a balanced signal, although the scope of the embodiments is not limited in this respect. The I and Q baseband output signals may be provided to low-noise amplifier, such as amplifier circuitry 306 (FIG. 3) or to filter circuitry 308 (FIG. 3).

15 [0040] In some embodiments, the output baseband signals 307 and the input baseband signals 311 may be analog baseband signals, although the scope of the embodiments is not limited in this respect. In some alternate embodiments, the output baseband signals 307 and the input baseband signals 311 may be digital baseband signals. In these alternate embodiments, the radio IC circuitry may
20 include analog-to-digital converter (ADC) and digital-to-analog converter (DAC) circuitry.

[0041] In some dual-mode embodiments, a separate radio IC circuitry may be provided for processing signals for each spectrum, or for other spectrums not mentioned here, although the scope of the embodiments is not limited in this
25 respect.

[0042] In some embodiments, the synthesizer circuitry 304 may be a fractional-N synthesizer or a fractional N/N+1 synthesizer, although the scope of the embodiments is not limited in this respect as other types of frequency synthesizers may be suitable. For example, synthesizer circuitry 304 may be a
30 delta-sigma synthesizer, a frequency multiplier, or a synthesizer comprising a phase-locked loop with a frequency divider. According to some embodiments, the synthesizer circuitry 304 may include digital synthesizer circuitry. An advantage of using a digital synthesizer circuitry is that, although it may still

include some analog components, its footprint may be scaled down much more than the footprint of an analog synthesizer circuitry. In some embodiments, frequency input into synthesizer circuitry 304 may be provided by a voltage controlled oscillator (VCO), although that is not a requirement. A divider
5 control input may further be provided by either the baseband processing circuitry 108 (FIG. 1) or the application processor 110 (FIG. 1) depending on the desired output frequency 305. In some embodiments, a divider control input (e.g., N) may be determined from a look-up table (e.g., within a Wi-Fi card) based on a channel number and a channel center frequency as determined or indicated by
10 the application processor 110.

[0043] In some embodiments, synthesizer circuitry 304 may be configured to generate a carrier frequency as the output frequency 305, while in other embodiments, the output frequency 305 may be a fraction of the carrier frequency (e.g., one-half the carrier frequency, one-third the carrier frequency).
15 In some embodiments, the output frequency 305 may be a LO frequency (f_{LO}).

[0044] FIG. 4 illustrates a functional block diagram of baseband processing circuitry 400 in accordance with some embodiments. The baseband processing circuitry 400 is one example of circuitry that may be suitable for use as the baseband processing circuitry 108 (FIG. 1), although other circuitry
20 configurations may also be suitable. The baseband processing circuitry 400 may include a receive baseband processor (RX BBP) 402 for processing receive baseband signals 309 provided by the radio IC circuitry 106 (FIG. 1) and a transmit baseband processor (TX BBP) 404 for generating transmit baseband signals 311 for the radio IC circuitry 106. The baseband processing circuitry 400
25 may also include control logic 406 for coordinating the operations of the baseband processing circuitry 400.

[0045] In some embodiments (e.g., when analog baseband signals are exchanged between the baseband processing circuitry 400 and the radio IC circuitry 106), the baseband processing circuitry 400 may include ADC 410 to
30 convert analog baseband signals received from the radio IC circuitry 106 to digital baseband signals for processing by the RX BBP 402. In these embodiments, the baseband processing circuitry 400 may also include DAC 412

to convert digital baseband signals from the TX BBP 404 to analog baseband signals.

[0046] In some embodiments that communicate OFDM signals or OFDMA signals, such as through baseband processor 108a, the transmit baseband processor 404 may be configured to generate OFDM or OFDMA signals as appropriate for transmission by performing an inverse fast Fourier transform (IFFT). The receive baseband processor 402 may be configured to process received OFDM signals or OFDMA signals by performing an FFT. In some embodiments, the receive baseband processor 402 may be configured to detect the presence of an OFDM signal or OFDMA signal by performing an autocorrelation, to detect a preamble, such as a short preamble, and by performing a cross-correlation, to detect a long preamble. The preambles may be part of a predetermined frame structure for Wi-Fi communication.

[0047] Referring back to FIG. 1, in some embodiments, the antennas 101 (FIG. 1) may each comprise one or more directional or omnidirectional antennas, including, for example, dipole antennas, monopole antennas, patch antennas, loop antennas, microstrip antennas or other types of antennas suitable for transmission of RF signals. In some multiple-input multiple-output (MIMO) embodiments, the antennas may be effectively separated to take advantage of spatial diversity and the different channel characteristics that may result. Antennas 101 may each include a set of phased-array antennas, although embodiments are not so limited.

[0048] Although the radio-architecture 100 is illustrated as having several separate functional elements, one or more of the functional elements may be combined and may be implemented by combinations of software-configured elements, such as processing elements including digital signal processors (DSPs), and/or other hardware elements. For example, some elements may comprise one or more microprocessors, DSPs, field-programmable gate arrays (FPGAs), application specific integrated circuits (ASICs), radio-frequency integrated circuits (RFICs) and combinations of various hardware and logic circuitry for performing at least the functions described herein. In some embodiments, the functional elements may refer to one or more processes operating on one or more processing elements.

Example Machine Description

[0049] FIG. 5 illustrates a block diagram of an example machine 500 upon which any one or more of the techniques (e.g., methodologies) discussed herein may performed. In alternative embodiments, the machine 500 may operate as a standalone device or may be connected (e.g., networked) to other machines. In a networked deployment, the machine 500 may operate in the capacity of a server machine, a client machine, or both in server-client network environments. In an example, the machine 500 may act as a peer machine in peer-to-peer (P2P) (or other distributed) network environment. The machine 500 may be a user equipment (UE), evolved Node B (eNB), next generation evolved Node B (gNB), next generation access network (AN), next generation user plane function (UPF), Wi-Fi access point (AP), Wi-Fi station (STA), personal computer (PC), a tablet PC, a set-top box (STB), a personal digital assistant (PDA), a mobile telephone, a smart phone, a web appliance, a network router, switch or bridge, or any machine capable of executing instructions (sequential or otherwise) that specify actions to be taken by that machine. Further, while only a single machine is illustrated, the term “machine” shall also be taken to include any collection of machines that individually or jointly execute a set (or multiple sets) of instructions to perform any one or more of the methodologies discussed herein, such as cloud computing, software as a service (SaaS), other computer cluster configurations.

[0050] Examples, as described herein, may include, or may operate on, logic or a number of components, modules, or mechanisms. Modules are tangible entities (e.g., hardware) capable of performing specified operations and may be configured or arranged in a certain manner. In an example, circuits may be arranged (e.g., internally or with respect to external entities such as other circuits) in a specified manner as a module. In an example, the whole or part of one or more computer systems (e.g., a standalone, client or server computer system) or one or more hardware processors may be configured by firmware or software (e.g., instructions, an application portion, or an application) as a module that operates to perform specified operations. In an example, the software may reside on a machine readable medium. In an example, the software, when

executed by the underlying hardware of the module, causes the hardware to perform the specified operations.

[0051] Accordingly, the term “module” is understood to encompass a tangible entity, be that an entity that is physically constructed, specifically
5 configured (e.g., hardwired), or temporarily (e.g., transitorily) configured (e.g., programmed) to operate in a specified manner or to perform part or all of any operation described herein. Considering examples in which modules are temporarily configured, each of the modules need not be instantiated at any one moment in time. For example, where the modules comprise a general-purpose
10 hardware processor configured using software, the general-purpose hardware processor may be configured as respective different modules at different times. Software may accordingly configure a hardware processor, for example, to constitute a particular module at one instance of time and to constitute a different module at a different instance of time.

[0052] Machine (e.g., computer system) 500 may include a hardware
processor 502 (e.g., a central processing unit (CPU), a graphics processing unit (GPU), a hardware processor core, or any combination thereof), a main memory
504 and a static memory 506, some or all of which may communicate with each other via an interlink (e.g., bus) 508. The machine 500 may further include a
20 display unit 510, an alphanumeric input device 512 (e.g., a keyboard), and a user interface (UI) navigation device 514 (e.g., a mouse). In an example, the display unit 510, input device 512 and UI navigation device 514 may be a touch screen display. The machine 500 may additionally include a storage device (e.g., drive unit) 516, a signal generation device 518 (e.g., a speaker), a network interface
25 device 520, and one or more sensors 521, such as a global positioning system (GPS) sensor, compass, accelerometer, or other sensor. The machine 500 may include an output controller 528, such as a serial (e.g., universal serial bus (USB), parallel, or other wired or wireless (e.g., infrared (IR), near field communication (NFC), etc.) connection to communicate or control one or more
30 peripheral devices (e.g., a printer, card reader, etc.).

[0053] The storage device 516 may include a machine readable medium 522 on which is stored one or more sets of data structures or instructions 524 (e.g., software) embodying or utilized by any one or more of the techniques or

functions described herein. The instructions 524 may also reside, completely or at least partially, within the main memory 504, within static memory 506, or within the hardware processor 502 during execution thereof by the machine 500. In an example, one or any combination of the hardware processor 502, the main
5 memory 504, the static memory 506, or the storage device 516 may constitute machine readable media.

[0054] While the machine readable medium 522 is illustrated as a single medium, the term "machine readable medium" may include a single medium or multiple media (e.g., a centralized or distributed database, and/or associated
10 caches and servers) configured to store the one or more instructions 524.

[0055] The term "machine readable medium" may include any medium that is capable of storing, encoding, or carrying instructions for execution by the machine 500 and that cause the machine 500 to perform any one or more of the techniques of the present disclosure, or that is capable of storing, encoding or
15 carrying data structures used by or associated with such instructions. Non-limiting machine readable medium examples may include solid-state memories, and optical and magnetic media. Specific examples of machine readable media may include: non-volatile memory, such as semiconductor memory devices (e.g., Electrically Programmable Read-Only Memory (EPROM), Electrically
20 Erasable Programmable Read-Only Memory (EEPROM)) and flash memory devices; magnetic disks, such as internal hard disks and removable disks; magneto-optical disks; Random Access Memory (RAM); and CD-ROM and DVD-ROM disks. In some examples, machine readable media may include non-transitory machine readable media. In some examples, machine readable
25 media may include machine readable media that is not a transitory propagating signal.

[0056] The instructions 524 may further be transmitted or received over a communications network 526 using a transmission medium via the network interface device 520 utilizing any one of a number of transfer protocols (e.g.,
30 frame relay, internet protocol (IP), transmission control protocol (TCP), user datagram protocol (UDP), hypertext transfer protocol (HTTP), etc.). Example communication networks may include a local area network (LAN), a wide area network (WAN), a packet data network (e.g., the Internet), mobile telephone

networks (e.g., cellular networks), Plain Old Telephone (POTS) networks, and wireless data networks (e.g., Institute of Electrical and Electronics Engineers (IEEE) 802.11 family of standards known as Wi-Fi®, IEEE 802.16 family of standards known as WiMax®, IEEE 802.15.4 family of standards, a Long Term Evolution (LTE) family of standards, a Universal Mobile Telecommunications System (UMTS) family of standards, peer-to-peer (P2P) networks, among others. In an example, the network interface device 520 may include one or more physical jacks (e.g., Ethernet, coaxial, or phone jacks) or one or more antennas to connect to the communications network 526. In an example, the network interface device 520 may include a plurality of antennas to wirelessly communicate using at least one of single-input multiple-output (SIMO), multiple-input multiple-output (MIMO), or multiple-input single-output (MISO) techniques. In some examples, the network interface device 520 may wirelessly communicate using Multiple User MIMO techniques. The term “transmission medium” shall be taken to include any intangible medium that is capable of storing, encoding, or carrying instructions for execution by the machine 500, and includes digital or analog communications signals or other intangible medium to facilitate communication of such software.

Example UE Description

[0057] As used herein, the term "circuitry" may refer to, be part of, or include an Application Specific Integrated Circuit (ASIC), an electronic circuit, a processor (shared, dedicated, or group), and/or memory (shared, dedicated, or group) that execute one or more software or firmware programs, a combinational logic circuit, and/or other suitable hardware components that provide the described functionality. In some embodiments, the circuitry may be implemented in, or functions associated with the circuitry may be implemented by, one or more software or firmware modules. In some embodiments, circuitry may include logic, at least partially operable in hardware.

[0058] Embodiments described herein may be implemented into a system using any suitably configured hardware and/or software. FIG. 6 illustrates, for one embodiment, example components of a User Equipment (UE) device 600. In some embodiments, the UE device 600 may include application circuitry 602,

baseband circuitry 604, Radio Frequency (RF) circuitry 606, front-end module (FEM) circuitry 608 and one or more antennas 610, coupled together at least as shown.

[0059] The application circuitry 602 may include one or more application processors. For example, the application circuitry 602 may include circuitry such as, but not limited to, one or more single-core or multi-core processors. The processor(s) may include any combination of general-purpose processors and dedicated processors (e.g., graphics processors, application processors, etc.). The processors may be coupled with and/or may include memory/storage and may be configured to execute instructions stored in the memory/storage to enable various applications and/or operating systems to run on the system.

[0060] The baseband circuitry 604 may include circuitry such as, but not limited to, one or more single-core or multi-core processors. The baseband circuitry 604 may include one or more baseband processors and/or control logic to process baseband signals received from a receive signal path of the RF circuitry 606 and to generate baseband signals for a transmit signal path of the RF circuitry 606. Baseband processing circuitry 604 may interface with the application circuitry 602 for generation and processing of the baseband signals and for controlling operations of the RF circuitry 606. For example, in some embodiments, the baseband circuitry 604 may include a second generation (2G) baseband processor 604a, third generation (3G) baseband processor 604b, fourth generation (4G) baseband processor 604c, and/or other baseband processor(s) 604d for other existing generations, generations in development or to be developed in the future (e.g., fifth generation (5G), 6G, etc.). The baseband circuitry 604 (e.g., one or more of baseband processors 604a-d) may handle various radio control functions that enable communication with one or more radio networks via the RF circuitry 606. The radio control functions may include, but are not limited to, signal modulation/demodulation, encoding/decoding, radio frequency shifting, etc. In some embodiments, modulation/demodulation circuitry of the baseband circuitry 604 may include Fast-Fourier Transform (FFT), precoding, and/or constellation mapping/demapping functionality. In some embodiments, encoding/decoding circuitry of the baseband circuitry 604 may include convolution, tail-biting

convolution, turbo, Viterbi, and/or Low Density Parity Check (LDPC) encoder/decoder functionality. Embodiments of modulation/demodulation and encoder/decoder functionality are not limited to these examples and may include other suitable functionality in other embodiments.

5 **[0061]** In some embodiments, the baseband circuitry 604 may include elements of a protocol stack such as, for example, elements of an evolved universal terrestrial radio access network (EUTRAN) protocol including, for example, physical (PHY), media access control (MAC), radio link control (RLC), packet data convergence protocol (PDCP), and/or radio resource control
10 (RRC) elements. A central processing unit (CPU) 604e of the baseband circuitry 604 may be configured to run elements of the protocol stack for signaling of the PHY, MAC, RLC, PDCP and/or RRC layers. In some embodiments, the baseband circuitry may include one or more audio digital signal processor(s) (DSP) 604f. The audio DSP(s) 604f may be include elements for
15 compression/decompression and echo cancellation and may include other suitable processing elements in other embodiments. Components of the baseband circuitry may be suitably combined in a single chip, a single chipset, or disposed on a same circuit board in some embodiments. In some embodiments, some or all of the constituent components of the baseband circuitry 604 and the
20 application circuitry 602 may be implemented together such as, for example, on a system on a chip (SOC).

[0062] In some embodiments, the baseband circuitry 604 may provide for communication compatible with one or more radio technologies. For example, in some embodiments, the baseband circuitry 604 may support communication
25 with an evolved universal terrestrial radio access network (EUTRAN) and/or other wireless metropolitan area networks (WMAN), a wireless local area network (WLAN), a wireless personal area network (WPAN). Embodiments in which the baseband circuitry 604 is configured to support radio communications of more than one wireless protocol may be referred to as multi-mode baseband
30 circuitry.

[0063] RF circuitry 606 may enable communication with wireless networks using modulated electromagnetic radiation through a non-solid medium. In various embodiments, the RF circuitry 606 may include switches, filters,

amplifiers, etc. to facilitate the communication with the wireless network. RF circuitry 606 may include a receive signal path which may include circuitry to down-convert RF signals received from the FEM circuitry 608 and provide baseband signals to the baseband circuitry 604. RF circuitry 606 may also
5 include a transmit signal path which may include circuitry to up-convert baseband signals provided by the baseband circuitry 604 and provide RF output signals to the FEM circuitry 608 for transmission.

[0064] In some embodiments, the RF circuitry 606 may include a receive signal path and a transmit signal path. The receive signal path of the RF
10 circuitry 606 may include mixer circuitry 606a, amplifier circuitry 606b and filter circuitry 606c. The transmit signal path of the RF circuitry 606 may include filter circuitry 606c and mixer circuitry 606a. RF circuitry 606 may also include synthesizer circuitry 606d for synthesizing a frequency for use by the mixer circuitry 606a of the receive signal path and the transmit signal path. In
15 some embodiments, the mixer circuitry 606a of the receive signal path may be configured to down-convert RF signals received from the FEM circuitry 608 based on the synthesized frequency provided by synthesizer circuitry 606d. The amplifier circuitry 606b may be configured to amplify the down-converted signals and the filter circuitry 606c may be a low-pass filter (LPF) or band-pass
20 filter (BPF) configured to remove unwanted signals from the down-converted signals to generate output baseband signals. Output baseband signals may be provided to the baseband circuitry 604 for further processing. In some embodiments, the output baseband signals may be zero-frequency baseband signals, although this is not a requirement. In some embodiments, mixer
25 circuitry 606a of the receive signal path may comprise passive mixers, although the scope of the embodiments is not limited in this respect.

[0065] In some embodiments, the mixer circuitry 606a of the transmit signal path may be configured to up-convert input baseband signals based on the synthesized frequency provided by the synthesizer circuitry 606d to generate RF
30 output signals for the FEM circuitry 608. The baseband signals may be provided by the baseband circuitry 604 and may be filtered by filter circuitry 606c. The filter circuitry 606c may include a low-pass filter (LPF), although the scope of the embodiments is not limited in this respect.

[0066] In some embodiments, the mixer circuitry 606a of the receive signal path and the mixer circuitry 606a of the transmit signal path may include two or more mixers and may be arranged for quadrature downconversion and/or upconversion respectively. In some embodiments, the mixer circuitry 606a of the receive signal path and the mixer circuitry 606a of the transmit signal path may include two or more mixers and may be arranged for image rejection (e.g., Hartley image rejection). In some embodiments, the mixer circuitry 606a of the receive signal path and the mixer circuitry 606a may be arranged for direct downconversion and/or direct upconversion, respectively. In some embodiments, the mixer circuitry 606a of the receive signal path and the mixer circuitry 606a of the transmit signal path may be configured for super-heterodyne operation.

[0067] In some embodiments, the output baseband signals and the input baseband signals may be analog baseband signals, although the scope of the embodiments is not limited in this respect. In some alternate embodiments, the output baseband signals and the input baseband signals may be digital baseband signals. In these alternate embodiments, the RF circuitry 606 may include analog-to-digital converter (ADC) and digital-to-analog converter (DAC) circuitry and the baseband circuitry 604 may include a digital baseband interface to communicate with the RF circuitry 606.

[0068] In some dual-mode embodiments, a separate radio IC circuitry may be provided for processing signals for each spectrum, although the scope of the embodiments is not limited in this respect.

[0069] In some embodiments, the synthesizer circuitry 606d may be a fractional-N synthesizer or a fractional N/N+1 synthesizer, although the scope of the embodiments is not limited in this respect as other types of frequency synthesizers may be suitable. For example, synthesizer circuitry 606d may be a delta-sigma synthesizer, a frequency multiplier, or a synthesizer comprising a phase-locked loop with a frequency divider.

[0070] The synthesizer circuitry 606d may be configured to synthesize an output frequency for use by the mixer circuitry 606a of the RF circuitry 606 based on a frequency input and a divider control input. In some embodiments, the synthesizer circuitry 606d may be a fractional N/N+1 synthesizer.

[0071] In some embodiments, frequency input may be provided by a voltage controlled oscillator (VCO), although that is not a requirement. Divider control input may be provided by either the baseband circuitry 604 or the applications processor 602 depending on the desired output frequency. In some

5 embodiments, a divider control input (e.g., N) may be determined from a look-up table based on a channel indicated by the applications processor 602.

[0072] Synthesizer circuitry 606d of the RF circuitry 606 may include a divider, a delay-locked loop (DLL), a multiplexer and a phase accumulator. In some embodiments, the divider may be a dual modulus divider (DMD) and the

10 phase accumulator may be a digital phase accumulator (DPA). In some embodiments, the DMD may be configured to divide the input signal by either N or N+1 (e.g., based on a carry out) to provide a fractional division ratio. In some example embodiments, the DLL may include a set of cascaded, tunable, delay elements, a phase detector, a charge pump and a D-type flip-flop. In these

15 embodiments, the delay elements may be configured to break a VCO period up into N_d equal packets of phase, where N_d is the number of delay elements in the delay line. In this way, the DLL provides negative feedback to help ensure that the total delay through the delay line is one VCO cycle.

[0073] In some embodiments, synthesizer circuitry 606d may be configured

20 to generate a carrier frequency as the output frequency, while in other embodiments, the output frequency may be a multiple of the carrier frequency (e.g., twice the carrier frequency, four times the carrier frequency) and used in conjunction with quadrature generator and divider circuitry to generate multiple signals at the carrier frequency with multiple different phases with respect to

25 each other. In some embodiments, the output frequency may be a LO frequency (f_{LO}). In some embodiments, the RF circuitry 606 may include an IQ/polar converter.

[0074] FEM circuitry 608 may include a receive signal path which may include circuitry configured to operate on RF signals received from one or more

30 antennas 610, amplify the received signals and provide the amplified versions of the received signals to the RF circuitry 606 for further processing. FEM circuitry 608 may also include a transmit signal path which may include circuitry

configured to amplify signals for transmission provided by the RF circuitry 606 for transmission by one or more of the one or more antennas 610.

[0075] In some embodiments, the FEM circuitry 608 may include a TX/RX switch to switch between transmit mode and receive mode operation. The FEM circuitry may include a receive signal path and a transmit signal path. The receive signal path of the FEM circuitry may include a low-noise amplifier (LNA) to amplify received RF signals and provide the amplified received RF signals as an output (e.g., to the RF circuitry 606). The transmit signal path of the FEM circuitry 608 may include a power amplifier (PA) to amplify input RF signals (e.g., provided by RF circuitry 606), and one or more filters to generate RF signals for subsequent transmission (e.g., by one or more of the one or more antennas 610).

[0076] In some embodiments, the UE device 600 may include additional elements such as, for example, memory/storage, display, camera, sensor, and/or input/output (I/O) interface.

Description of Embodiments

[0077] In a 4G core network, referred to as the Evolved Packet Core (EPC), protocols and reference points (i.e., interfaces) are defined for entities such as a Mobility Management Entity (MME), a Serving Gateway (S-GW), and a Packet Data Network Gateway (P-GW). In a 5G or next generation network, protocols and reference points (i.e., interfaces) are defined for Network Functions (NFs), where an NF can be implemented either as a network element on a dedicated hardware, a software instance running on a dedicated hardware, or as a virtualized function instantiated on an appropriate platform such as a cloud infrastructure.

[0078] Fig. 7 illustrates the non-roaming architecture of a 5G network according to some embodiments that is composed of NFs and reference points connecting NFs. The core network (CN) is divided into control plane functions and user plane functions that communicate via a reference point designated as NG4. The control plane NFs may include an access and mobility function (AMF), a session management function (SMF), a policy control function (PCF), an application function (AF), an

authentication server function (AUSF), and a unified data management (UDM) function. The user plane comprises one or more user plane functions (UPFs). Fig. 7 shows control plane functions 740 that communicate with a user plane function (UPF) 730. A user equipment (UE) 710 is connected to an Access Network (AN) 720 via a radio interface where the AN represents a generalized base station that may be a 4G evolved Node B, a next generation evolved Node B (gNB), or a non-3GPP base station such as a WiFi access point. The UE 710 includes processing circuitry 711 and a radio transceiver 712, and the AN 720 includes processing circuitry 721 and a radio transceiver 722. The AN 720 also includes a network interface 723 for communication with a user plane function (UPF) 730 over an interface or reference point designated as NG3. The UPF 730 includes processing circuitry 731 and a network interface 733. The UPF 730 communicates with a data network (DN) 750 (e.g., the Internet) via the NG6 reference point to transmit and receive user plane data packets. UPF 730 and AN720 communicate with the control plane functions 740 via the NG4 and NG2 reference points, respectively. UE 710 communicates with the control plane functions via the NG1 reference point where the NG1 protocol is a non-access stratum (NAS) protocol, meaning that the NG1 protocol does not terminate in the AN 720 and uses the NG2 protocol as a transport protocol.

[0079] Fig. 8 illustrates the user plane protocol stacks of the UE 710, AN 720, and UPF 730. The UPF 730 and AN 720 transmit and receive user plane packets via the NG3 protocol that, in some embodiments, may be a general packet radio service tunneling protocol (GTP). NG3 encapsulated packets are further encapsulated by an IP/UDP transport layer, a link layer, and a physical layer for transporting the packets between the UPF 730 and AN 720. The IP header provided by the protocol stacks of the AN 720 and UPF 730 may be referred to as a transport layer protocol header or as an outer IP header. AN 720 and UE 710 transmit and receive user plane packets via a radio protocol stack whose layers include a service data application protocol (SDAP) layer, a packet data convergence protocol (PDCP) layer, a radio link control (RLC) layer, a medium access control (MAC) layer, and a physical (PHY) layer.

[0080] As noted above, the 5G QoS model is a QoS flow based framework that supports both QoS flows that require guaranteed bit rate and QoS flows that do not require guaranteed bit rate. The 5G QoS model also supports reflective QoS in which uplink (UL) packets from a UE are afforded the same QoS as the downlink (DL) packets in a particular QoS flow that are received by the UE. The QoS flow is the finest granularity of QoS differentiation within PDU session. A QoS Flow ID (QFI) is used to identify a QoS flow is carried in within an NG3 encapsulation header. The QFI is also referred to herein as a flow priority indicator (FPI). The NG3 encapsulation header may also contain a reflective QoS indicator (RQI) when reflective QoS is enabled by the network. Upon receipt of a DL user plane packet from the data network, the UPF maps the packet to a particular QoS flow in accordance with information received from control plane functions and marks the packet with the corresponding QFI in the NG3 encapsulation header. When the AN receives the NG3 encapsulated user plane packet, it notes the QoS flow that packet belongs to. The packet is then mapped to a data radio bearer (DRB) specific for that QoS flow by the SDAP. For each DRB, a PDCP entity and an RLC entity specific for that DRB are instantiated by both the UE and the AN. The packet is then successively encapsulated by the PDCP, RCL, and MAC layers before processing by the PHY layer as a transport block to be transmitted to the UE.

[0081] With multi-cell aggregation technology such as Dual-Connectivity (DC), and LTE-WLAN Aggregation (LWA), it is possible to support higher throughput by having the UE be simultaneously connected to two cells (i.e., two ANs) and combining the resource available in both cells. Fig. 7 illustrates such a scenario in which the UE 710 is shown as connected to both an AN 720 and a secondary AN 725 that communicate with one another via an X_n interface. In what is known as bearer splitting, a single PDCP entity is created by AN 720 for a DRB designated as a split bearer, and RLC entities are created in both AN 720 and secondary AN 725. The PDCP entity of AN 720 communicates with the RLC entity of secondary AN 725 over the X_n interface. The UE creates PDCP and RLC entities to receive packets over the split DRB from the AN 720 and an RLC entity to receive packets from the secondary AN 725.

[0082] Data aggregation and re-ordering operations are required at the UE when it receives DL packets over a split DRB to ensure that all the packets are delivered in sequence to upper layer even if the individual links with AN 720 and secondary AN 725 have different available bandwidths and latencies.

5 In the case of DC or LWA, such data aggregation and re-ordering is done in the PDCP layer using PDCP sequence numbers contained in the PDCP header that are managed per DRB. SDFs from different application with potentially different latency constraints, however, may be transmitted in the same bearer. As result, data from one SDF may be pending in the re-ordering window

10 waiting for the reception of the data of another SDF on another link leading to unnecessary latency. For example, with a real-time application such as a Skype call, high throughput may be less of a concern, compared to latency and jitter. In that case, it may be better to use the link with less latency and jitter, instead of sending over both links. For non-real-time applications such

15 as FTP, on the other hand, throughput is more important and data aggregation over both links is beneficial. It is therefore beneficial to support flow-based PDCP sequencing so that individual SDFs can be processed independently. Also, by separating a bearer into multiple SDFs, the lower layers (e.g., RLC and MAC) can support multiple queues for different SDFs of a same bearer,

20 and provide better QoS for different applications.

[0083] To deal with the above issues, a flow-based sequencing scheme is implemented for a particular SDF when a flow classification rule for that SDF is activated. The SDF classification rule may be provisioned by UE or the network through additional control signaling. When an SDF classification

25 rule is activated that covers a particular SDF, flow-specific PDCP entities are created in the UE and the AN to process and sequence DL user plane (UP) packets carrying the SDF. A flow-specific PDCP entity is separate from any PDCP entity or entities that used to process packets that carry SDFs not covered by the SDF classification rule and that are mapped to the same DRB. In an

30 example scenario, a DRB is created by the AN, and a default PDCP entity is created to process all packets of the DRB. When an SDF classification rule is activated, both the AN and the UE create a flow-specific PDCP entity that will be used to process the SDF, and all other packets of the DRB will

still be processed by the default PDCP entity. There may be multiple flow-specific PDCP entities per DRB, which together with the default PDCP entity will be associated to the same RLC entity of the DRB. As a result, all traffic of the same DRB are still processed as the same bearer at the lower-layer protocols (e.g., RLC and MAC).

5 [0084] To assist the AN in identifying SDFs carried by UP packets received from the UPF, a new packet marking is introduced. The UPF is configured to identify the service data flow (SDF) carried by a UP packet received from a data network and encapsulate the UP packet with NG3 and transport layer protocol
10 headers. The NG3 header and/or transport layer header is then made to include the QFI that indicates a QoS flow to be applied to the UP packet and, in addition, a flow identifier (FI) that indicates the identified SDF. The SDF covered by an SDF classification rule or identified by the FI may be an internet protocol (IP) flow, an Ethernet flow, or an unstructured protocol flow. The FI may identify
15 one more SDFs that belong to the same QoS flow. The SDF identified by the FI may be, for example, an internet protocol (IP) flow specified by any combination of the members of an IP-tuple that includes a source address, a destination address, protocol type, source port value, or destination port value or specified by an IP-tuple that includes a range of source and destination addresses.

20 [0085] In one embodiment, the flow-specific PDCP entity of the AN encapsulates the UP packet with a PDCP encapsulation header that includes the FI before conveying the packet to the RLC entity specific for the DRB. In the case where the DRB is a split bearer, such that PDCP-encapsulated UP packets are to be conveyed to one or both of an RLC entity specific for the DRB located
25 in the AN and an RLC entity specific for the DRB located in a secondary AN, the FI may also be used by the AN in selecting which RLC entity or entities to send the packet.

[0086] FIG. 9 shows an example of a CN-assisted flow-based bearer splitting call-flow procedure using the FI as described above. Stages of the
30 call-flow are numbered 1 through 7 and are described in the following paragraphs. For simplicity, it is assumed that reflective QoS is always supported so that no RQI is necessary. The flow priority indicator (FPI) is equivalent to the QFI discussed above.

[0087] At stage 1, the UPF receives a downlink IP packet from the data network. At stage 2, the UPF determines the FPI (FPI_1 in the figure) to apply as packet marking over NG3 based on the QoS of the packet. The FPI packet marking is placed in the NG3 encapsulation header, and possibly also (or instead of) in a transport-layer header. In addition, the UPF may determine the Flow Identification (FI) based on, for example, the IP header 5-tuple. As a result, multiple packets sharing the same FPI may be marked with different FIs (FI_1 and FI_2 in the figure) if they belong to different IP flows or SDFs. Similar to the FPI, the FI may be supported in the NG3 encapsulation header and/or a transport-layer marking.

[0088] At stage 3, upon reception of the NG3 packet the AN uses the FPI marking to determine the packet handling on the radio interface. In the case of bearer splitting operation in DC or LWA, the AN uses the FI marking to identify individual SDFs or IP flows and triggers per-flow PDCP sequencing flow-based bearer splitting if a flow classification rule for the SDF is activated. In this example, the UE is attached to the AN via two links (designated as #1 and #2), and the AN decides to send the FI_1 packets over the link #1, and the FI_2 packets over the link #2. At stage 4, upon reception of the radio packet, the UE takes a note of the received information (FPI) and, with reflective QoS, handles all corresponding uplink flows with the same FPI (i.e., FPI_1). Given that the QoS handling of this flow was initiated by the network, FPI_1 does not need to be part of a pre-authorized FPI set.

[0089] At stage 5, an application client in the UE provides an uplink packet for transmission to the lower layers. Based on internal configuration, the UE maps the uplink packet into one of the pre-authorized FPIs (FPI_2 in the figure) and proceeds with transmission in the uplink. If the UE currently has no corresponding DRB for FPI_2, the UE creates a new DRB for FPI_2 using in-band means. The UE includes the selected FPI (FPI_2) in the radio packet header. Similarly, the FI in the downlink PDCP packet as described above can assist the UE in detecting and identifying different SDFs sharing the same FPI (or DRB), and may then handle all corresponding uplink packets the same way as the downlink. Alternatively, the UE may identify UL flows itself,

independent of DL flows. In the case of UL bearer splitting, the UE may decide how to distribute UL flows across multiple links.

[0090] At stage 6, upon reception of the radio packet the AN verifies whether FPI_2 is part of the pre-authorised FPI set. In the affirmative case the AN copies the received FPI in the NG3 encapsulation header, and possibly uses FPI_2 to determine any transport-layer marking over NG3. Otherwise, the AN discards the packet. It is not necessary to include FI marking for uplink traffic over the NG3 interface. At stage 7, upon reception of the NG3 packet, the UPF performs validation of the FPI (FPI_2), and forwards the uplink IP packet towards the data network.

Additional Notes and Examples

[0091] In Example 1, an apparatus for an access network (AN), comprises memory and processing circuitry; wherein the processing circuitry is to: decode a downlink (DL) user plane (UP) packet received from a user plane function (UPF) to identify a quality of service (QoS) flow to be applied to the UP packet as indicated by a QoS flow identifier (QFI) carried by an encapsulation header of the UP packet; map the UP packet to a data radio bearer (DRB) corresponding to the identified QoS flow; decode the UP packet to obtain a flow identification (FI) carried by the encapsulation header of the UP packet that identifies a service data flow (SDF) carried by a data portion of the UP packet; when an SDF classification rule is activated that covers the identified SDF, process and sequence the UP packet with a flow-specific packet data convergence protocol (PDCP) entity that is separate from any PDCP entity or entities used to process packets that carry SDFs not covered by the SDF classification rule and that are mapped to the same DRB.

[0092] In Example 1a, an apparatus for an access network (AN), comprises memory and processing circuitry; wherein the processing circuitry is to: identify a quality of service (QoS) flow to be applied to a user plane (UP) packet received from a user plane function (UP) as indicated by a QoS flow identifier (QFI) carried by an encapsulation header of the UP packet; map the UP packet to a data radio bearer (DRB) corresponding to the identified QoS flow; obtain a

flow identification (FI) carried by the encapsulation header of the UP packet that identifies a service data flow (SDF) carried by a data portion of the UP packet; and, encapsulate the UP packet with a PDCP encapsulation header that includes the FI before conveying the packet to a radio link control (RLC) entity specific

5 for the DRB.

[0093] In Example 1b, the subject matter of Example 1a or any of the Examples herein may optionally include wherein the processing circuitry is to, when an SDF classification rule is activated that covers the identified SDF, process and sequence the UP packet with a flow-specific packet data convergence protocol (PDCP) entity that is separate from any PDCP entity or entities used to process packets that carry SDFs not covered by the SDF classification rule and that are mapped to the same DRB.

[0094] In Example 1c, an apparatus for a user plane function (UPF), comprises memory and processing circuitry; wherein the processing circuitry is to: identify a service data flow (SDF) in a downlink (DL) user plane (UP) packet received from a data network (DN); encapsulate the UP packet with an NG3 protocol, where NG3 designates a reference point or interface between the UPF and an access network (AN) to which the UP packet is to be sent; encapsulate the NG3-encapsulated packet with a transport layer protocol for transporting the UP packet to the AN; wherein an NG3 or transport layer header includes a quality of service (QoS) flow identifier (QFI) that indicates a QoS flow to be applied to the UP packet and a flow identifier (FI) that indicates the identified SDF.

[0095] In Example 2, the subject matter of any of the Examples herein may optionally include wherein the FI is carried by an NG3 encapsulation header of an NG3 protocol packet, where NG3 designates a reference point or interface between the UPF and the AN.

[0096] In Example 3, the subject matter of any of the Examples herein may optionally include wherein the FI is carried by a transport layer protocol header that encapsulates an NG3 protocol packet, where NG3 designates a reference point or interface between the UPF and the AN.

[0097] In Example 4, the subject matter of any of the Examples herein may optionally include wherein the NG3 protocol is a general packet radio service

tunneling protocol (GTP) that is encapsulated by an internet protocol (IP) transport layer that conveys packets from the UPF to the AN.

[0098] In Example 5, the subject matter of any of the Examples herein may optionally include wherein the flow-specific PDCP entity encapsulates the UP packet with a PDCP encapsulation header that includes the FI before conveying the packet to a radio link control (RLC) entity specific for the DRB.

[0099] In Example 6, the subject matter of any of the Examples herein may optionally include wherein the DRB is a split bearer such that PDCP-encapsulated UP packets are to be conveyed to one or both of an RLC entity specific for the DRB located in the AN and an RLC entity specific for the DRB located in a secondary AN, wherein the RLC entities of the AN and secondary AN encapsulate UP packets for DL transmission to a user equipment (UE) dually connected to the AN and the secondary AN.

[00100] In Example 6a, the subject matter of Example 6 may optionally include wherein the processing circuitry of the AN is to use the FI to select which RLC entity or entities to send a UP packet from the flow-specific PDCP entity.

[00101] In Example 7, the subject matter of any of the Examples herein may optionally include wherein the flow classification rule covers one or more SDFs that belong to the same QoS flow.

[00102] In Example 8, the subject matter of any of the Examples herein may optionally include wherein the FI identifies one more SDFs that belong to the same QoS flow.

[00103] In Example 9, the subject matter of any of the Examples herein may optionally include wherein the SDF covered by the SDF classification rule or identified by the FI is an internet protocol (IP) flow, an Ethernet flow, or an unstructured protocol flow.

[00104] In Example 10, the subject matter of any of the Examples herein may optionally include wherein the SDF covered by the SDF classification rule or identified by the FI is an internet protocol (IP) flow specified by any combination of the members of an IP-tuple that includes a source address, a destination address, protocol type, destination port value, or source port value or

specified by an IP-tuple that includes a range of source and destination addresses.

5 [00105] In Example 11, the subject matter of any of the apparatus Examples herein may optionally include a network interface for communicating with next generation network functions.

[00106] In Example 12, the subject matter of any of the AN apparatus Examples herein may optionally include a radio transceiver for communication with a user equipment (UE) over an air interface.

10 [00107] In Example 12a, the subject matter of any of the AN or UPF apparatus Examples here may optionally include wherein the memory is to store the UP packet received from the UPF or DN.

[00108] In Example 13, a method for operating an AN comprises performing the functions of the memory and/or processing circuitry as set forth by any of the AN apparatus Examples herein.

15 [00109] In Example 14, a method for operating a UPF comprises performing the functions of the memory and/or processing circuitry as set forth by any of the UPF apparatus Examples herein.

[00110] In Example 15, an apparatus for an AN comprises means for performing a method as set forth by Example 13.

20 [00111] In Example 16, an apparatus for a UPF comprises means for performing a method as set forth by Example 14.

[00112] In Example 17, a computer-readable medium comprises instructions to cause an AN or a UPF, upon execution of the instructions by the processing circuitry of the AN or UPF, to perform the functions of the memory and/or processing circuitry as recited by any of the Examples herein

25 [00113] In Example 18, the subject matter of any of the Examples herein may optionally include a radio transceiver having one or more antennas connected to the processing circuitry.

30 [00114] In Example 19, a method for operating comprises performing any of the functions of the processing circuitry and/or radio transceiver as recited by any of the Examples herein.

[00115] In Example 20, an apparatus for comprises means for performing any of the functions of the processing circuitry and/or radio transceiver as recited by any of the Examples herein.

[00116] In Example 21, an apparatus for a user equipment (UE) comprises:
5 memory and processing circuitry; wherein the processing circuitry is to: decode a UP packet received from an access network (AN) over a data radio bearer (DRB) corresponding to a particular QoS flow; decode the UP packet further to obtain a flow identification (FI) carried by a packet data convergence protocol (PDCP) encapsulation header of the UP packet that identifies a service data flow
10 (SDF) carried by a data portion of the UP packet; when an SDF classification rule is activated that covers the identified SDF, process and sequence uplink (UL) packets with a flow-specific packet data convergence protocol (PDCP) entity that is separate from a PDCP entity used to process packets that carry UL SDFs not covered by the SDF classification rule and that are mapped to the same
15 DRB.

[00117] In Example 22, the subject matter of any of the UE apparatus Examples herein may optionally include wherein the processing circuitry is to convey PDCP-encapsulated UL packets to one or both of an RLC entity specific for the DRB that encapsulates packets for UL transmission to the AN and an
20 RLC entity specific for the DRB that encapsulates packets for UL transmission to a secondary AN, the DRB being a split bearer in the UL.

[00118] In Example 23, the subject matter of any of the UE apparatus Examples herein may optionally include wherein the memory is to store the received UP packet.

[00119] The above detailed description includes references to the accompanying drawings, which form a part of the detailed description. The drawings show, by way of illustration, specific embodiments that may be practiced. These embodiments are also referred to herein as “examples.” Such examples may include elements in addition to those shown or described. However, also contemplated are examples that include the elements shown or described. Moreover, also contemplate are examples using any combination or permutation of those elements shown or described (or one or more aspects

thereof), either with respect to a particular example (or one or more aspects thereof), or with respect to other examples (or one or more aspects thereof) shown or described herein.

[00120] Publications, patents, and patent documents referred to in this document are incorporated by reference herein in their entirety, as though individually incorporated by reference. In the event of inconsistent usages between this document and those documents so incorporated by reference, the usage in the incorporated reference(s) are supplementary to that of this document; for irreconcilable inconsistencies, the usage in this document controls.

[00121] In this document, the terms “a” or “an” are used, as is common in patent documents, to include one or more than one, independent of any other instances or usages of “at least one” or “one or more.” In this document, the term “or” is used to refer to a nonexclusive or, such that “A or B” includes “A but not B,” “B but not A,” and “A and B,” unless otherwise indicated. In the appended claims, the terms “including” and “in which” are used as the plain-English equivalents of the respective terms “comprising” and “wherein.” Also, in the following claims, the terms “including” and “comprising” are open-ended, that is, a system, device, article, or process that includes elements in addition to those listed after such a term in a claim are still deemed to fall within the scope of that claim. Moreover, in the following claims, the terms “first,” “second,” and “third,” etc. are used merely as labels, and are not intended to suggest a numerical order for their objects.

[00122] The embodiments as described above may be implemented in various hardware configurations that may include a processor for executing instructions that perform the techniques described. Such instructions may be contained in a machine-readable medium such as a suitable storage medium or a memory or
5 other processor-executable medium.

[00123] The embodiments as described herein may be implemented in a number of environments such as part of a wireless local area network (WLAN), 3rd Generation Partnership Project (3GPP) Universal Terrestrial Radio Access Network (UTRAN), or Long-Term-Evolution (LTE) or a Long-Term-Evolution
10 (LTE) communication system, although the scope of the disclosure is not limited

in this respect. An example LTE system includes a number of mobile stations, defined by the LTE specification as User Equipment (UE), communicating with a base station, defined by the LTE specifications as an eNodeB.

[00124] Antennas referred to herein may comprise one or more directional or
5 omnidirectional antennas, including, for example, dipole antennas, monopole antennas, patch antennas, loop antennas, microstrip antennas or other types of antennas suitable for transmission of RF signals. In some embodiments, instead of two or more antennas, a single antenna with multiple apertures may be used. In these embodiments, each aperture may be considered a separate antenna. In
10 some multiple-input multiple-output (MIMO) embodiments, antennas may be effectively separated to take advantage of spatial diversity and the different channel characteristics that may result between each of antennas and the antennas of a transmitting station. In some MIMO embodiments, antennas may be separated by up to 1/10 of a wavelength or more.

15 [00125] In some embodiments, a receiver as described herein may be configured to receive signals in accordance with specific communication standards, such as the Institute of Electrical and Electronics Engineers (IEEE) standards including IEEE 802.11-2007 and/or 802.11(n) standards and/or proposed specifications for WLANs, although the scope of the disclosure is not
20 limited in this respect as they may also be suitable to transmit and/or receive communications in accordance with other techniques and standards. In some embodiments, the receiver may be configured to receive signals in accordance with the IEEE 802.16-2004, the IEEE 802.16(e) and/or IEEE 802.16(m) standards for wireless metropolitan area networks (WMANs) including
25 variations and evolutions thereof, although the scope of the disclosure is not limited in this respect as they may also be suitable to transmit and/or receive communications in accordance with other techniques and standards. In some embodiments, the receiver may be configured to receive signals in accordance with the Universal Terrestrial Radio Access Network (UTRAN) LTE
30 communication standards. For more information with respect to the IEEE 802.11 and IEEE 802.16 standards, please refer to "IEEE Standards for Information Technology -- Telecommunications and Information Exchange between Systems" - Local Area Networks - Specific Requirements - Part 11

- “Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY), ISO/IEC 8802-11: 1999”, and Metropolitan Area Networks - Specific Requirements – Part 16: “Air Interface for Fixed Broadband Wireless Access Systems,” May 2005 and related amendments/versions. For more information
- 5 with respect to UTRAN LTE standards, see the 3rd Generation Partnership Project (3GPP) standards for UTRAN-LTE, release 8, March 2008, including variations and evolutions thereof.

[00126] The above description is intended to be illustrative, and not restrictive. For example, the above-described examples (or one or more aspects thereof) may be used in combination with others. Other embodiments may be used, such as by one of ordinary skill in the art upon reviewing the above description. The Abstract is to allow the reader to quickly ascertain the nature of the technical disclosure, for example, to comply with 37 C.F.R. §1.72(b) in the United States of America. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims. Also, in the above Detailed Description, various features may be grouped together to streamline the disclosure. However, the claims may not set forth every feature disclosed herein as embodiments may feature a subset of said features. Further, embodiments may include fewer features than those disclosed in a particular example. Thus, the following claims are hereby incorporated into the Detailed Description, with a claim standing on its own as a separate embodiment. The scope of the embodiments disclosed herein is to be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

CLAIMS

1. An apparatus for an access network (AN), comprising:

memory and processing circuitry;

wherein the processing circuitry is to:

decode a downlink (DL) user plane (UP) packet received from a user
5 plane function (UPF) to identify a quality of service (QoS) flow to be applied to
the UP packet as indicated by a QoS flow identifier (QFI) carried by an
encapsulation header of the UP packet;

map the UP packet to a data radio bearer (DRB) corresponding to the
identified QoS flow;

10 decode the UP packet to obtain a flow identification (FI) carried by the
encapsulation header of the UP packet that identifies a service data flow (SDF)
carried by a data portion of the UP packet;

when an SDF classification rule is activated that covers the identified
SDF, process and sequence the UP packet with a flow-specific packet data
15 convergence protocol (PDCP) entity that is separate from a PDCP entity used to
process packets that carry SDFs not covered by the SDF classification rule and
that are mapped to the same DRB.
2. The apparatus of claim 1 wherein NG3 designates a reference point or
20 interface between the UPF and the AN using an NG3 protocol and wherein the
FI is carried by an NG3 encapsulation header of an NG3 protocol packet.
3. The apparatus of claim 1 wherein NG3 designates a reference point or
interface between the UPF and the AN using an NG3 protocol and wherein the
25 FI is carried by a transport layer protocol header that encapsulates an NG3
protocol packet.

4. The apparatus of claim 2 or 3 wherein the NG3 protocol is a general packet radio service tunneling protocol (GTP) that is encapsulated by an internet protocol (IP) transport layer that conveys packets from the UPF to the AN.

5

5. The apparatus of claim 1 wherein the flow-specific PDCP entity encapsulates the UP packet with a PDCP encapsulation header that includes the FI before conveying the packet to a radio link control (RLC) entity specific for the DRB.

10

6. The apparatus of claim 5 wherein the DRB is a split bearer such that PDCP-encapsulated UP packets are to be conveyed to one or both of an RLC entity specific for the DRB located in the AN and an RLC entity specific for the DRB located in a secondary AN, wherein the RLC entities of the AN and
15 secondary AN encapsulate UP packets for DL transmission to a user equipment (UE) dually connected to the AN and the secondary AN.

7. The apparatus of claim 1 wherein the SDF classification rule covers one or more SDFs that belong to the same QoS flow.

20

8. The apparatus of claim 1 wherein the FI identifies one more SDFs that belong to the same QoS flow.

9. The apparatus of claim 1 wherein the SDF covered by the SDF
25 classification rule or identified by the FI is an internet protocol (IP) flow, an Ethernet flow, or an unstructured protocol flow.

10. The apparatus of claim 1 wherein the SDF covered by the SDF classification rule or identified by the FI is an internet protocol (IP) flow specified by an IP-tuple that includes a source address and a destination address or specified by an IP-tuple that includes a range of source and destination
5 addresses.
11. The apparatus of claim 1 wherein the memory is to store the UP packet received from the UPF.
- 10 12. An apparatus for a user plane function (UPF), the apparatus comprising:

memory and processing circuitry;

wherein the processing circuitry is to:

identify a service data flow (SDF) in a downlink (DL) user plane (UP) packet received from a data network (DN);

15 encapsulate the UP packet with an NG3 protocol, where NG3 designates a reference point or interface between the UPF and an access network (AN) to which the UP packet is to be sent using the NG3 protocol;

encapsulate the NG3-encapsulated packet with a transport layer protocol for transporting the UP packet to the AN;

20 wherein an NG3 or transport layer header includes a quality of service (QoS) flow identifier (QFI) that indicates a QoS flow to be applied to the UP packet and a flow identifier (FI) that indicates the identified SDF.
13. The apparatus of claim 12 wherein the NG3 protocol is a general packet
25 radio service tunneling protocol (GTP) that is encapsulated by an internet protocol (IP) transport layer that conveys packets from the UPF to the AN.

14. The apparatus of claim 12 wherein the FI identifies one more SDFs that belong to the same QoS flow.
- 5 15. The apparatus of claim 12 wherein the SDF identified by the FI is an internet protocol (IP) flow, an Ethernet flow, or an unstructured protocol flow.
16. The apparatus of claim 12 wherein the SDF identified by the FI is an internet protocol (IP) flow specified by any combination of the members of an
10 IP-tuple that includes a source address, a destination address, protocol type, source port value, or destination port value or specified by an IP-tuple that includes a range of source and destination addresses.
17. The apparatus of any of claims 12 through 16 wherein the memory is to
15 store the UP packet received from the DN.
18. An apparatus for a user equipment (UE), the apparatus comprising:
memory and processing circuitry;
wherein the processing circuitry is to:
20 decode a UP packet received from an access network (AN) over a data radio bearer (DRB) corresponding to a particular QoS flow;
decode the UP packet further to obtain a flow identification (FI) carried by a packet data convergence protocol (PDCP) encapsulation header of the UP packet that identifies a service data flow (SDF) carried by a data portion of the
25 UP packet;

when an SDF classification rule is activated that covers the identified SDF, process and sequence uplink (UL) packets with a flow-specific packet data convergence protocol (PDCP) entity that is separate from a PDCP entity used to process packets that carry UL SDFs not covered by the SDF classification rule
5 and that are mapped to the same DRB.

19. The apparatus of claim 18 wherein the processing circuitry is to convey PDCP-encapsulated UL packets to one or both of an RLC entity specific for the DRB that encapsulates packets for UL transmission to the AN and an RLC entity
10 specific for the DRB that encapsulates packets for UL transmission to a secondary AN, the DRB being a split bearer in the UL..

20. The apparatus of claim 19 wherein the processing circuitry is to store the received UP packet in memory.

15

21. A computer-readable storage medium comprising instructions to cause processing circuitry of an access network (AN), upon execution of the instructions by processing circuitry of the AN, to:

20 decode a downlink (DL) user plane (UP) packet received from a user plane function (UPF) to identify a quality of service (QoS) flow to be applied to the UP packet as indicated by a QoS flow identifier (QFI) carried by an encapsulation header of the UP packet;

map the UP packet to a data radio bearer (DRB) corresponding to the identified QoS flow;

25 decode the UP packet to obtain a flow identification (FI) carried by the encapsulation header of the UP packet that identifies a service data flow (SDF) carried by a data portion of the UP packet;

when an SDF classification rule is activated that covers the identified SDF, process and sequence the UP packet with a flow-specific packet data convergence protocol (PDCP) entity that is separate from any PDCP entity or entities used to process packets that carry SDFs not covered by the SDF
5 classification rule and that are mapped to the same DRB.

22. The medium of claim 21 wherein NG3 designates a reference point or interface between the UPF and the AN using an NG3 protocol and wherein the FI is carried by an NG3 encapsulation header of an NG3 protocol packet..

10

23. The medium of claim 21 wherein NG3 designates a reference point or interface between the UPF and the AN using an NG3 protocol and wherein the FI is carried by a transport layer protocol header that encapsulates an NG3 protocol packet.

15

24. The medium of claim 22 or 23 wherein the NG3 protocol is a general packet radio service tunneling protocol (GTP) that is encapsulated by an internet protocol (IP) transport layer that conveys packets from the UPF to the AN.

20 25. The medium of claim 21 wherein the flow-specific PDCP entity encapsulates the UP packet with a PDCP encapsulation header that includes the FI before conveying the packet to a radio link control (RLC) entity specific for the DRB.

25

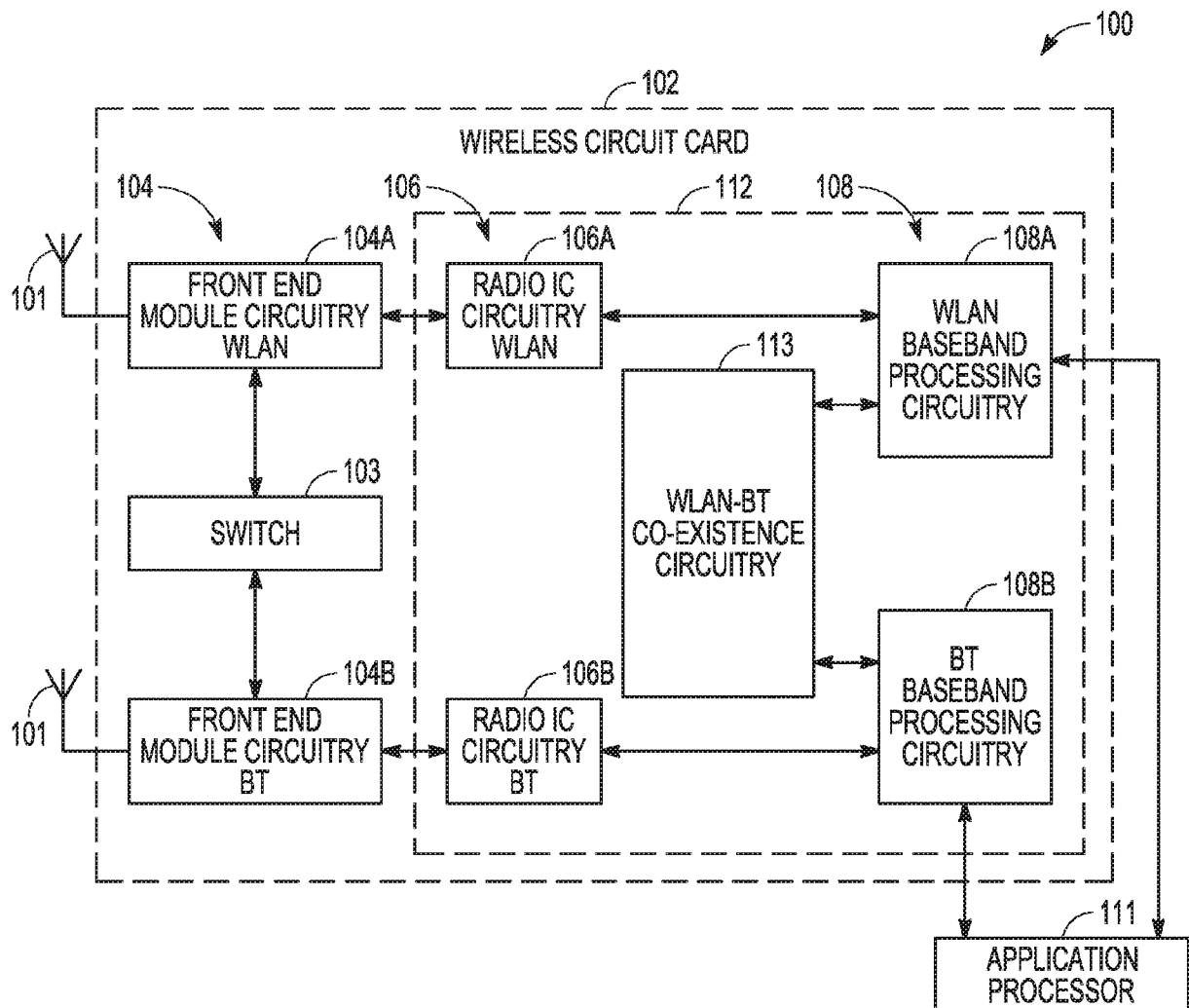


FIG. 1

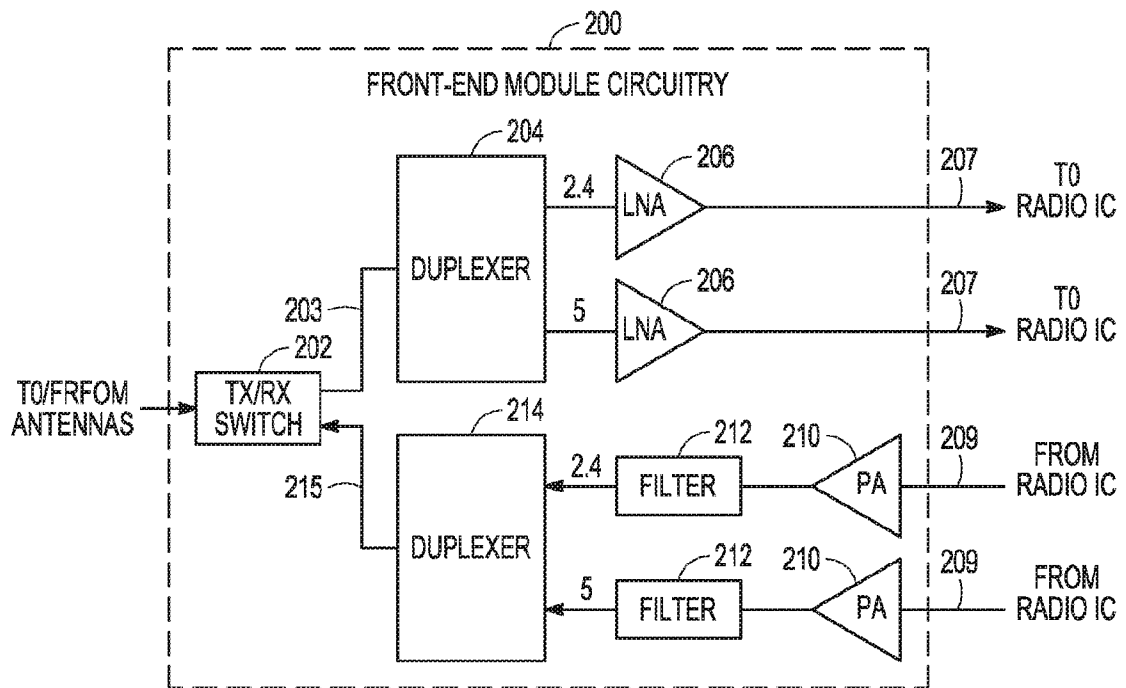


FIG. 2

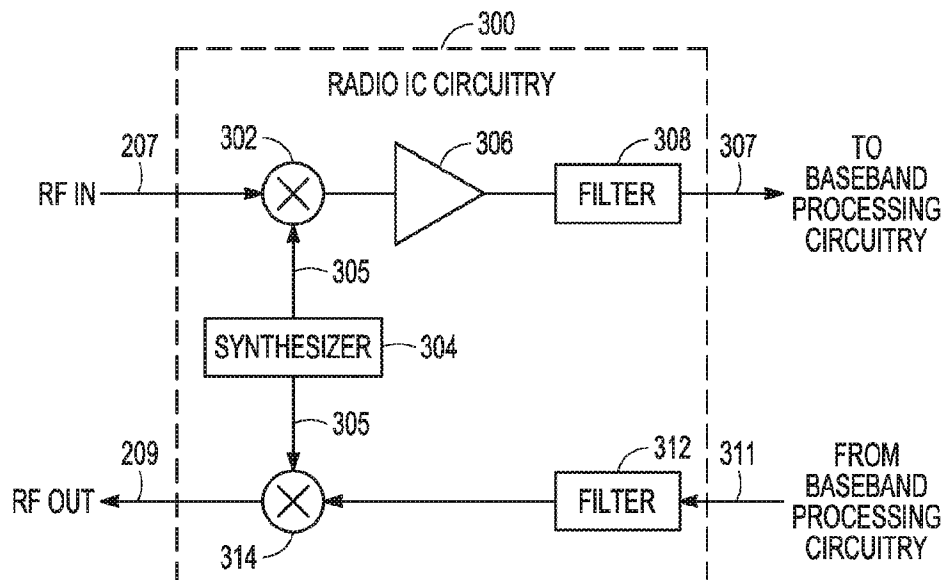


FIG. 3

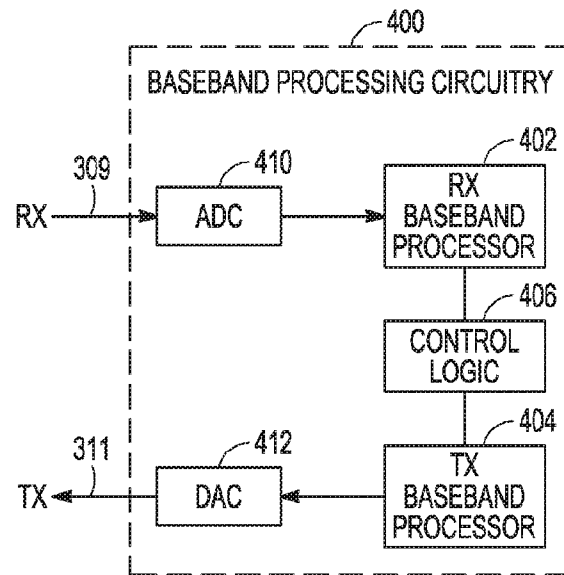
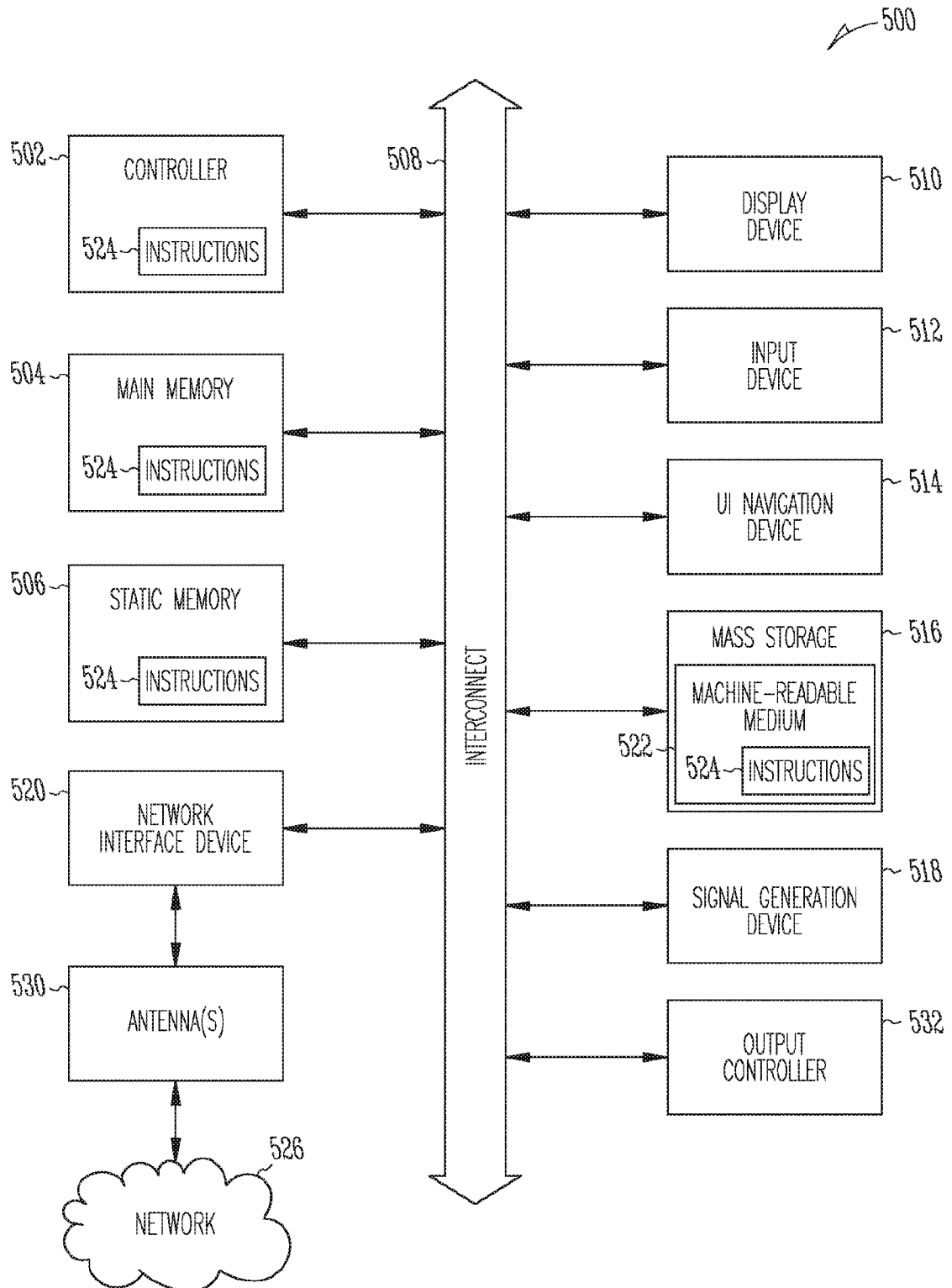
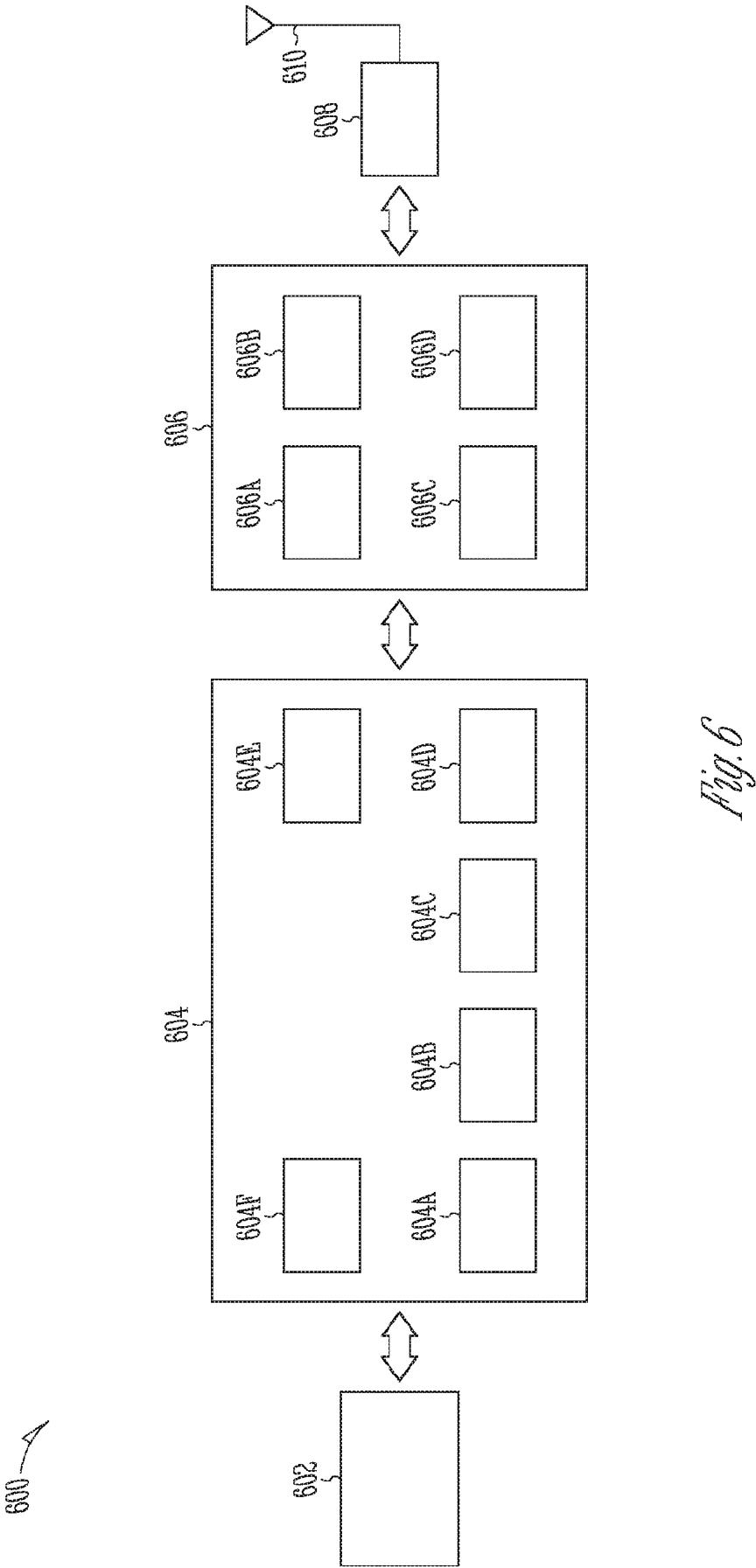


FIG. 4

*Fig. 5*



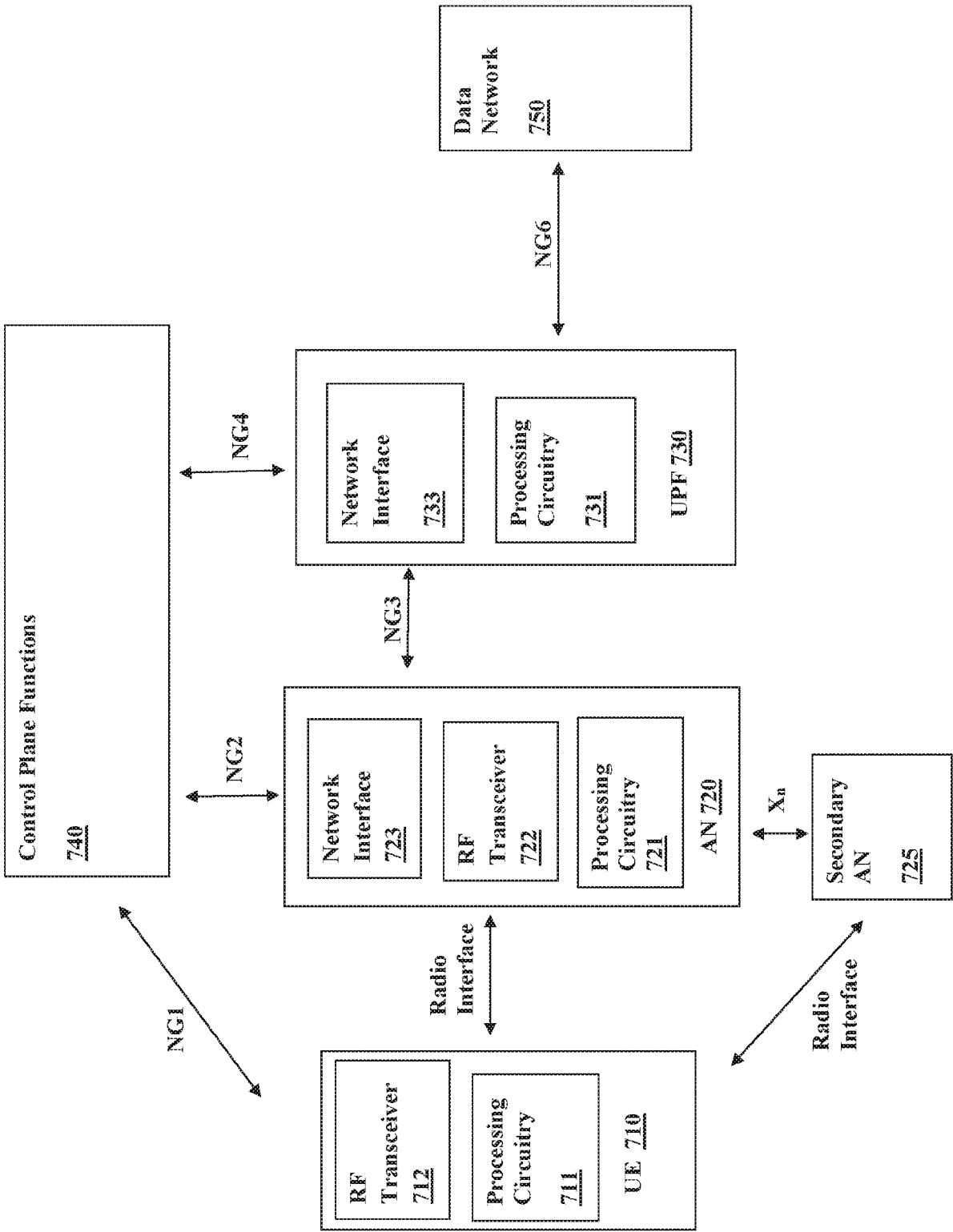


FIG. 7

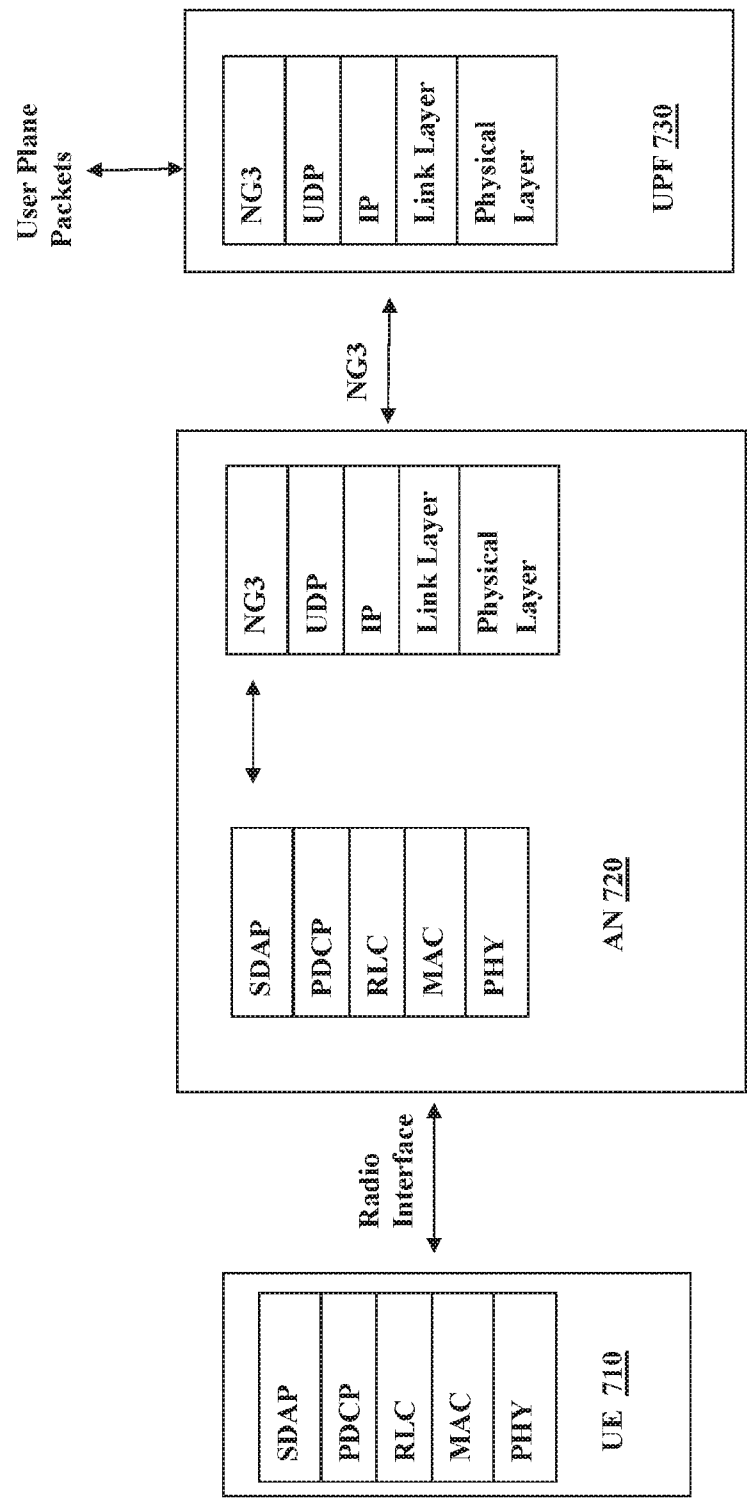


FIG. 8

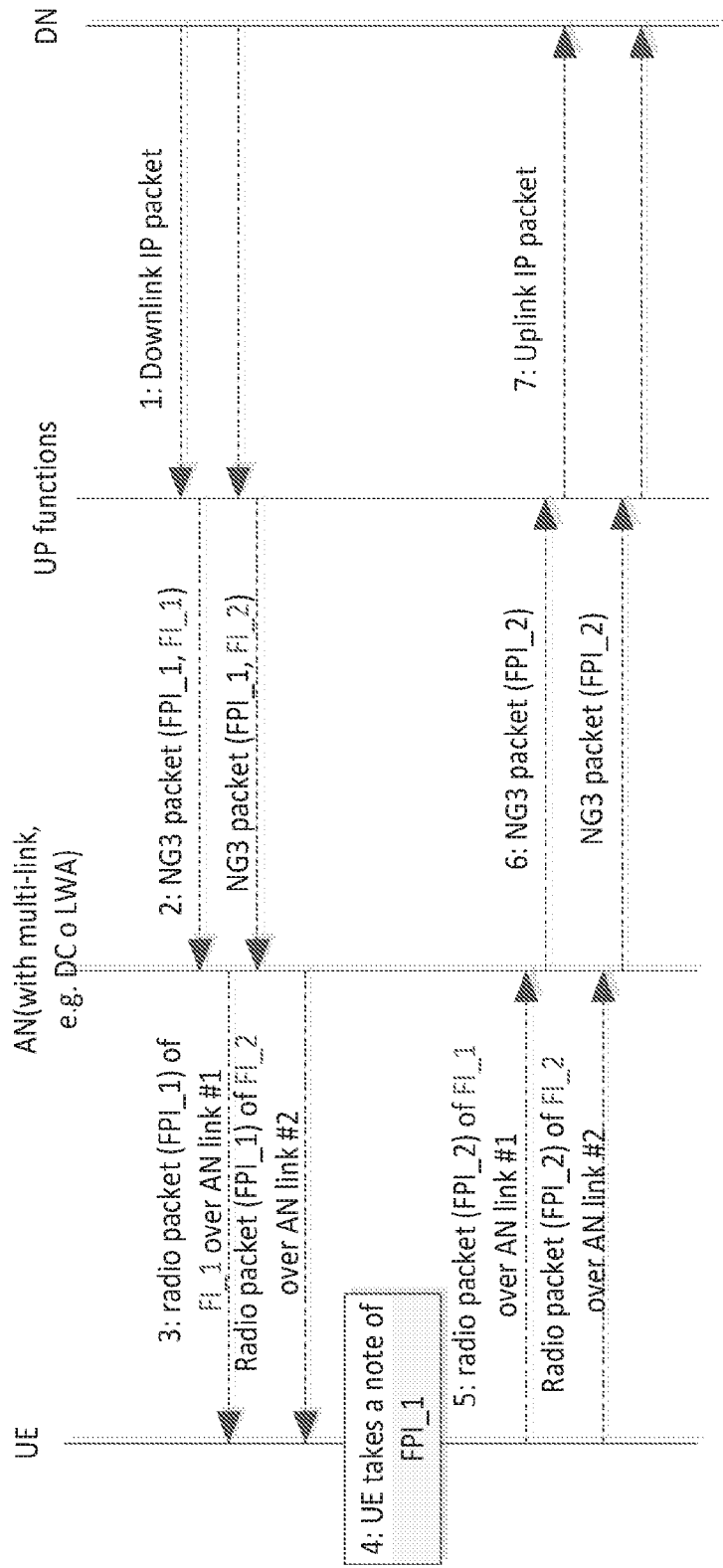


FIG. 9