

[54] MULTICELLED DISPLAY/MEMORY GAS DISCHARGE DEVICE HAVING INTEGRAL CELL INTERCONNECTIONS

[75] Inventor: Jerry D. Schmerhorn, Swanton, Ohio

[73] Assignee: Owens-Illinois, Inc., Toledo, Ohio

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[51] Int. Cl. H01l 61/00

[58] Field of Search..... 313/188, 217, 220

[56] References Cited

UNITED STATES PATENTS

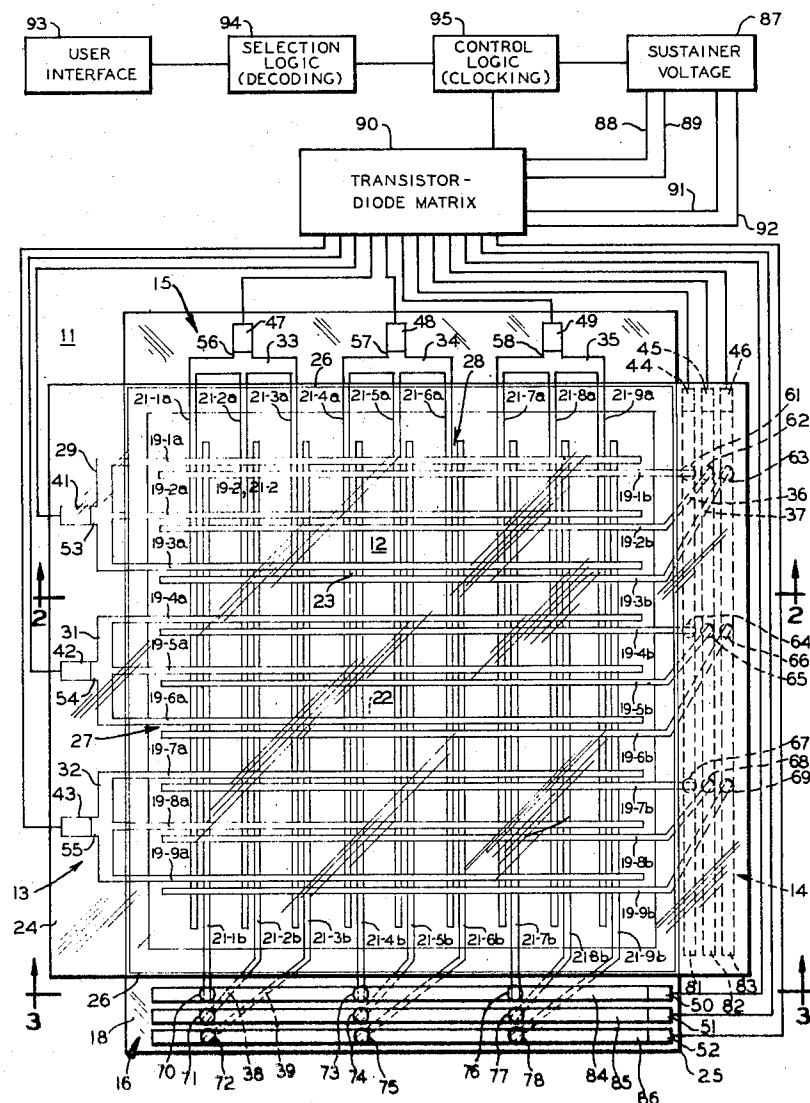
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Primary Examiner—Herman Karl Saalbach
Assistant Examiner—Darwin R. Hostetter
Attorney, Agent, or Firm—Donald Keith Wedding

[57] ABSTRACT

A multicelled gas discharge device in which individual cells are made up of spatial discharge transfer related discharge sub sites is provided with interconnections between conductors which are integral with the device. Sub sites have their conductor portions interconnected in both series and parallel relationships by connecting array conductor lines in parallel with display connector lines of conductive material integral with the device in combinations such that each cell has a group of discharge sub sites uniquely connected to terminals to external circuitry. These connections are made on the non-conductive surface supporting the array and on a dielectric layer overlying portions of the conductors and apertured in registry with the conductors to admit portions of display connector lines on the dielectric layer to engage the conductors. Paralleling connections to the array conductors are made at one side of the array and both sides of the array. They connect the conductors at one or both ends. Various geometries are proposed including those for monolithic display devices.

19 Claims, 10 Drawing Figures



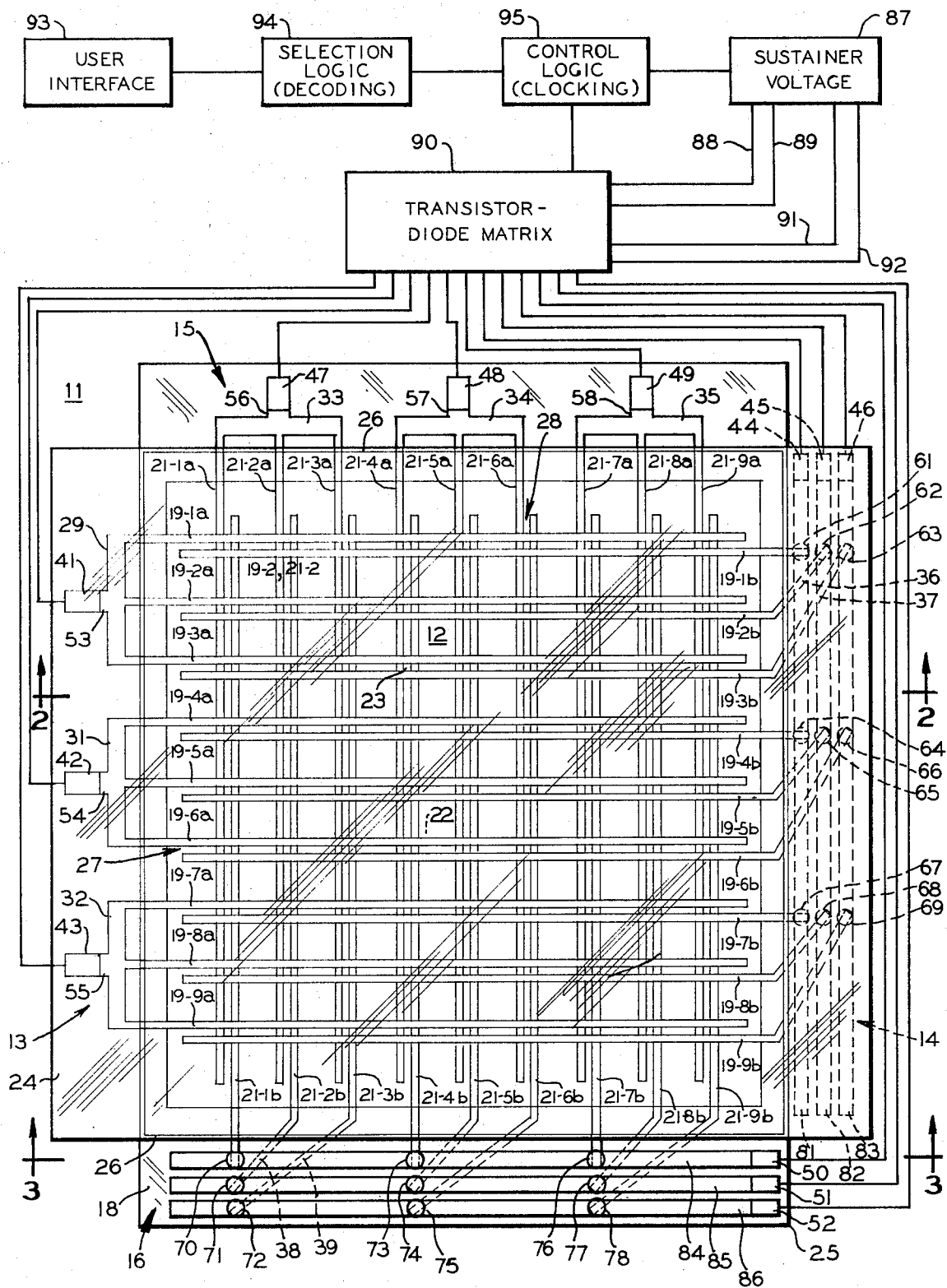


FIG. 1

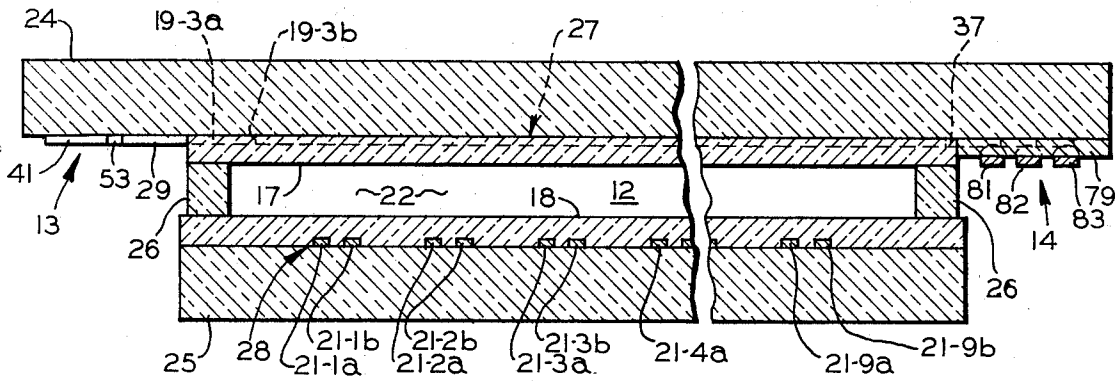


FIG. 2

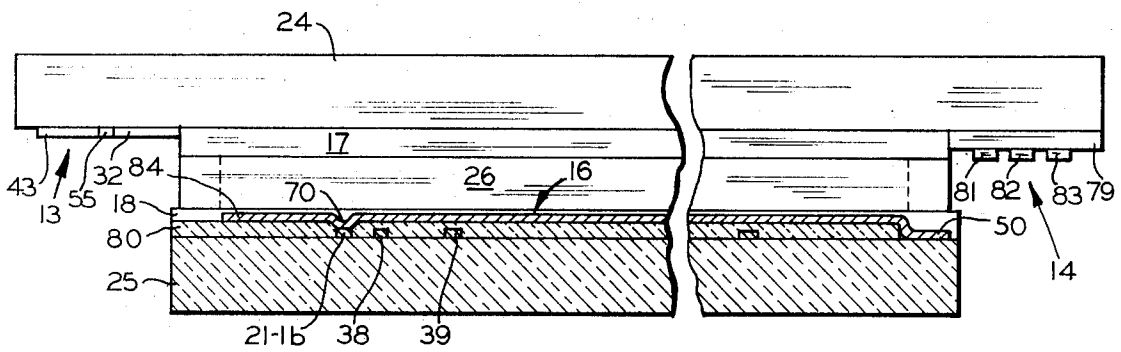


FIG. 3

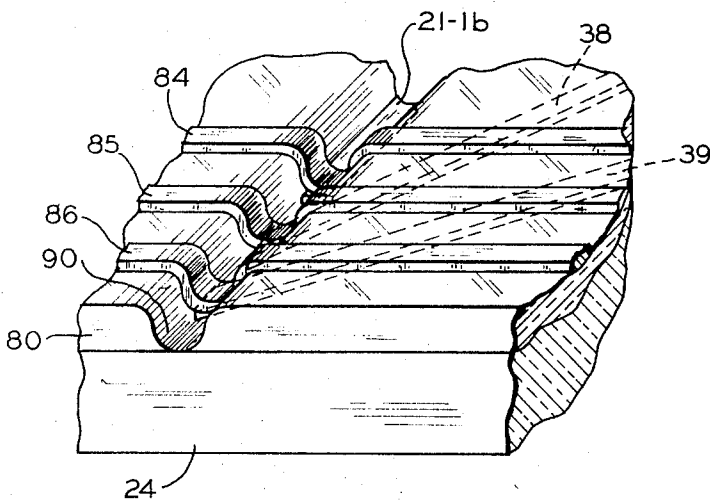


FIG. 4

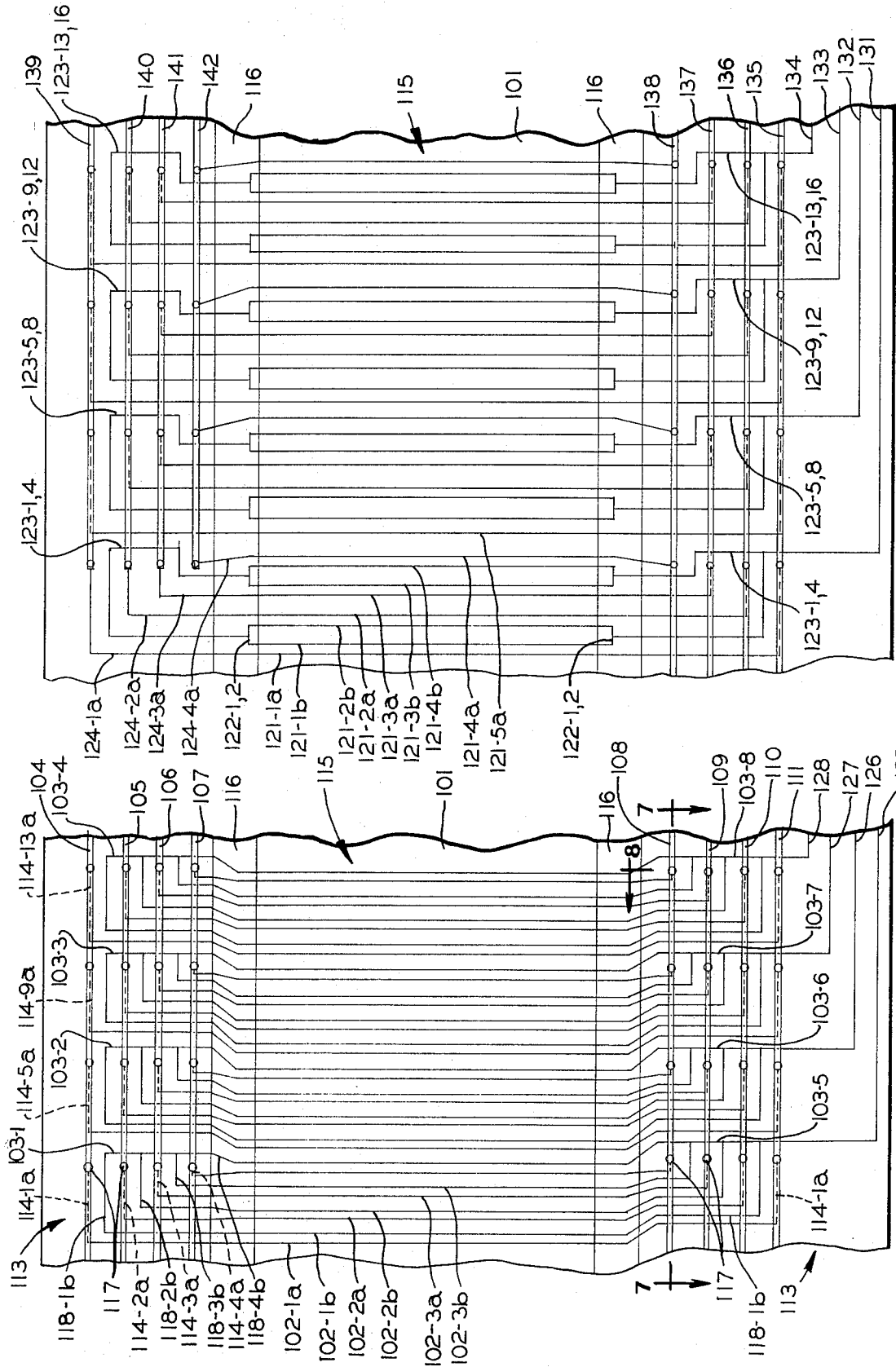


FIG. 6

FIG. 5

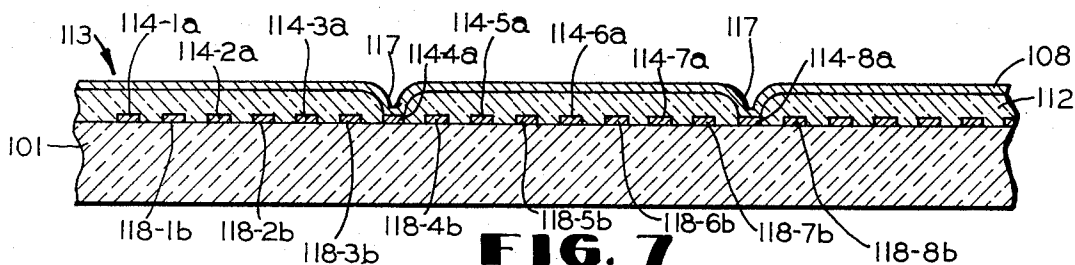


FIG. 7

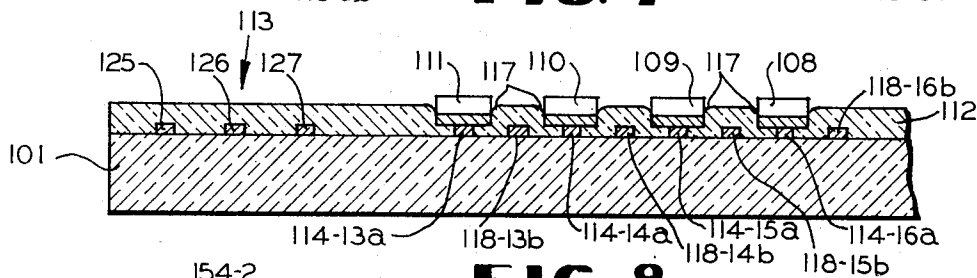


FIG. 8

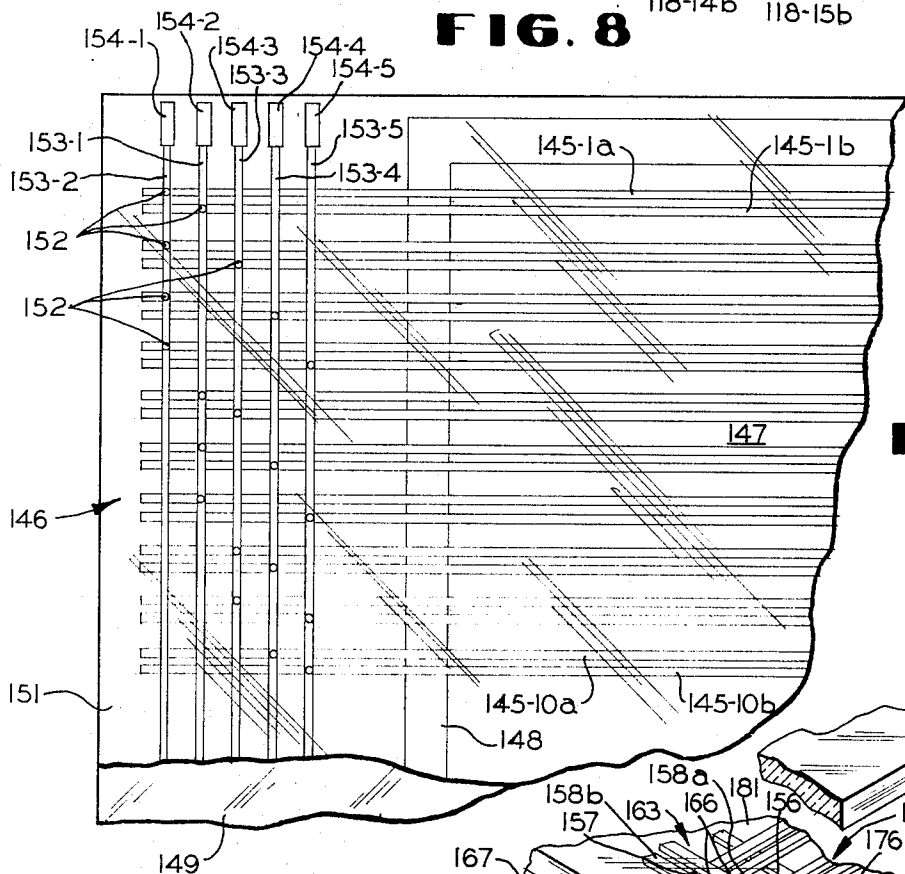


FIG. 9

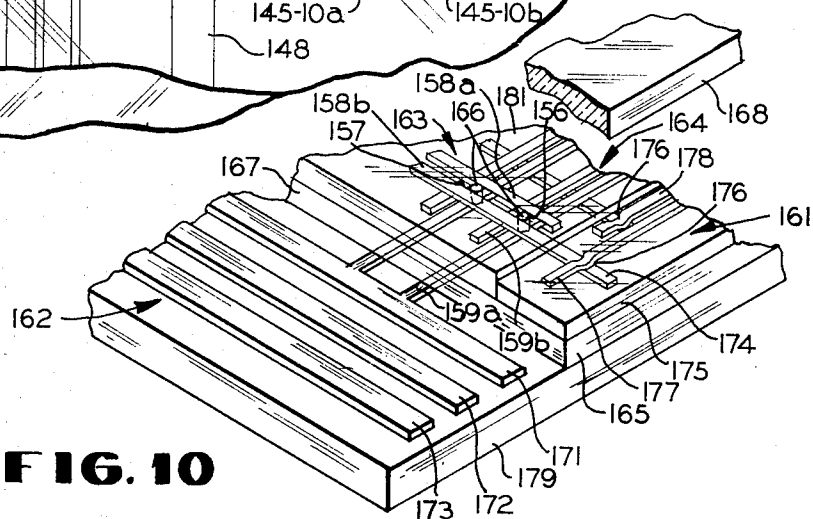


FIG. 10

MULTICELLED DISPLAY/MEMORY GAS DISCHARGE DEVICE HAVING INTEGRAL CELL INTERCONNECTIONS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is related to the U.S. Pat. Applications of Jerry D. Schermerhorn for "Spatial Discharge Transfer Gaseous Discharge Display/Memory Panel," Ser. No. 372,730, filed June 22, 1973; and "Method of and System for Introducing Logic Into Display/Memory Gaseous Discharge Panels by Spatial Discharge Transfer" Ser. No. 372,542, filed June 22, 1973 both of which were filed herewith.

BACKGROUND OF THE INVENTION

This invention relates to gaseous discharge display/memory devices of the multicelled type wherein selected cells in a matrix of cells are placed in a discharge state to display and/or store information and more particularly to those type of devices wherein cells are made up of grouped discharge sub sites which have the characteristic that the institution of an on state of discharge in one sub site of a cell causes any other sub site of that cell to enter an on state of discharge.

In the aforementioned related patent applications gaseous discharge display/memory devices having at least two spaced arrays of conductors between cooperating opposed pairs of which a gaseous discharge can be developed selectively are arranged with conductors in sufficient proximity that the discharge sites they define interact, when an "on state" of discharge is established in one of them, by placing the "off state" sites in an "on state." The matrices of cells made up of such spatially related discharge sites have grouped conductors in one or both of the opposed conductor arrays with conductive lines extending beyond the display area of the array and device for connection to external terminals.

Prior art display panels have been made up of five hundred and twelve individual conductive lines in each array orthogonally related when viewed along common perpendiculars to the opposed arrays. Thus five hundred and twelve connections were required to each axis of the panel. In the case of a spatial discharge panel where each line of cells along an axis has two conductors the number of connections doubles to one thousand-twenty-four. Lines of cells have frequently been arranged with a center-to-center spacing of about 16 mils. Typically, spatial discharge cell sub sites have three mil wide conductors spaced three mils for paired conductors in an array with the pairs spaced sixteen mils center-to-center. These close spacings dictate close tolerances in the dense connections for external circuitry to the discharge devices.

In the application "Method of and System for Introducing Logic Into Display/Memory Gaseous Discharge Panels by Spatial Discharge Transfer" it has been shown that the number of driving circuits for that type of panel can be reduced at least an order of magnitude by taking advantage of the internal logic functions of the devices. This has been accomplished by employing erase-writing techniques and combining the discharge sub site control circuits in unique combinations for each cell. In the case of a cell made up of four discharge sub sites and thus having two proximate conductor portions in the cell region of each conductor array, each cell has a unique combination of four "erase"

or "turn off" circuits to control its discharge state. Each of these four "turn off" circuits can be associated with other discharge sub sites. Thus the remaining sub sites in each axis which include the selected cell as coordinates would be subject to erase signals issued by those circuits by virtue of the serial connection of its conductor portions along the length of the conductors of the array. Where array conductors are connected in parallel to a common display connector line, each sub site having as one of its proximate conductor portions a portion of such a connector line is also subjected to the turn off signal addressed to a cell comprised in part of one such conductor portion. Thus, a number of sub sites will have but one conductor portion subjected to a discharge state manipulating signal without lasting effect either because its conductor portion in the opposite array is not subject to such a signal or because one or more of the sub sites with which it is associated in a discharge cell maintains control of the cell.

While the number of discharge state manipulating signal sources is greatly reduced by the internal logic accomplished employing the spatial discharge transfer phenomenon, the connection of those sources to a discharge display/memory device is complicated by the increased number of array conductors for each cell of the device or panel.

An object of the present invention is to improve gas discharge display/memory devices.

Another object is to reduce the number of connections required between external circuits and gas discharge display/memory devices having a given number of discharge cells.

A further object is to increase the reliability of signal transmission of signals to the conductive elements of discharge sites in a gas discharge display/memory device.

A fourth object is to reduce the expense of manufacture of gas discharge display/memory devices.

A fifth object is to reduce manufacturing tolerances required for conductor arrays of gas discharge display/memory devices.

SUMMARY OF THE INVENTION

In accordance with the above objects, a feature of this invention resides in interconnecting the conductors of an array for a gas discharge display/memory device within the structure of the device. Advantageously some interconnections between discrete sub site conductors can be made simultaneously with the formation of those conductors as by forming conductive strips in patterns on a dielectric substrate. Where conductive strips cross in the pattern a dielectric layer can be formed over the substrate mounted conductive strips with apertures in registry with those strips at desired connection points. Conductive strips can be formed on the dielectric overcoat to intersect with the apertures and electrically connect to the underlying conductive strip connection points. External connections need be made only from the signal sources to the display connector lines providing the array supported interconnections.

Another feature involves interconnecting both ends of array conductors in parallel arrangements whereby a break or discontinuity in a conductor is bypassed through its paralleled conductors to its opposite end so that signals are fed up to the break from both sides.

This interconnection arrangement increases the manufacturing yield of conductor arrays.

A third feature comprises cross connections between array conductors of adjacent lines of discharge cells each having two or more conductors whereby the density of conductor branches from the device discharge display area to the display connector lines is reduced. A broader tolerance in manufacture of the conductor arrays is achieved with this reduced conductor density.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagrammatic plan view of a gas discharge display/memory device in the form of a panel, typical of the type to which this invention applies, together with a block diagram of interface, sustainer and addressing circuitry which can be coupled to the panel;

FIGS. 2 and 3 are broken sections of the panel of FIG. 1 taken along lines 2—2 and 3—3 respectively of FIG. 1, enlarged but not to proportional scale since the thickness of the gas volume, dielectric and conductor arrays have been enlarged for purposes of illustration;

FIG. 4 is a sectioned perspective, enlarged in a manner similar to FIGS. 2 and 3, to illustrate a portion of the terminal strip region of a modified array for the panel of FIG. 1 wherein grooves in a dielectric are employed to expose connection areas instead of individual cavities;

FIG. 5 is a diagrammatic plan representation of a fragment of another form of conductor array having integral terminal strips on either side of the display area in a form which can be incorporated in a panel of the type shown in FIG. 1;

FIG. 6 is a fragment of an array showing another form of interconnection of the conductors;

FIGS. 7 and 8 are cross sections of the array terminal strip region of FIG. 5 taken along lines 7—7 and 8—8 respectively;

FIG. 9 is a diagrammatic plan view of a fragment of another form of array showing a scheme of interconnections to achieve the maximum number of unique circuit combinations for a given number of array terminals taken two at a time; and

FIG. 10 is a fragmentary perspective of a monolithic panel structure having the integral conductor interconnections of this invention for the two arrays formed on a dielectric layered monolith.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A multicelled gas discharge display/memory device 11 in the form of a panel having a display area 12 and terminal strip regions 13, 14, 15 and 16 is shown in FIG. 1. As in prior art devices the panel is basically in the form of a pair of opposed dielectric charge storage members, layers 17 and 18, which are backed by electrodes 19 and 21, the electrodes being so formed and oriented with respect to an ionizable gaseous medium 22 as to define a plurality of discrete gas discharge sites 23. More particularly, the electrodes 19 are arranged in an array, which in the orthogonal relationship chosen for illustration of the invention, comprises straight, parallel bands of conductive material, designated x conductors of an x array and the electrodes 21 are similar y conductors of a y array. While only a single charge storage member such as a dielectric layer 17

separating one array from the ionizable gas 22 is required for operation, it is common to provide such a layer for each array.

The gas volume 22 is thin, usually under 10 mils and typically about 4 to 6 mils in thickness. It is of a nature to produce a copious supply of charges (ions and electrons). These charges are alternately collectable on the surface of the dielectric members at opposed or facing elemental or discrete areas defined by the conductor arrays on the non-gas contacting sides of the dielectric layers 17 and 18.

The electrically operative members, dielectric layers 17 and 18, electrodes 19 and 21, and gas 22, are all relatively thin (being exaggerated in thickness in the drawings). They are formed on and supported by rigid, non-conducting support members 24 and 25 respectively. One or both of the non-conductive support members pass light produced by discharges in the discharge sites in the gas volume unless only the memory function is utilized, in which case they can be opaque. Advantageously, members 24 and 25 are transparent glass, typically about one-eighth to one-fourth inch thick.

The display area 12 of the panel is ordinarily hermetically sealed to enclose the gas volume by a wall which also establishes the volume thickness as a spacer 26 which may be of the same glass material as dielectric layers 17 and 18, and may be an integral rib or bead formed on one of the layers or directly on the support member 24 or 25 and fused to the other layer or member.

Conductor arrays 27 and 28 may be formed in situ on support members 24 and 25 for the x and y arrays respectively, for example as individual conductor strips about 8,000 angstroms thick, and may be transparent, semitransparent, or opaque conductive material such as tin oxide, gold or aluminum. In the illustrated arrays at least one array is made up of grouped, parallel, straight conductors, typically 3 mils wide spaced 3 mils apart in the group and 7 mils apart between groups. Specifically, the conductor ribbons 19 and 21 have been shown as paired in their groupings in a manner to provide spatial discharge transfer in the panel. The dimensions of the conductors, their intragroup spacing and their intergroup spacing are not restricted to the above values since there is a range of such dimensions which is dependent upon the gas thickness, composition and pressure as well as the conductor dimensions in order to achieve spatial discharge transfer between discharge sites grouped, by virtue of conductor groupings, into cells. The spatial discharge transfer is attributed to fringing of the discharge effects beyond the shadow area of the conductor cross points between the x and y arrays when viewed along a common perpendicular to each of the arrays. One form of display panel having a neon-krypton or neon-argon gas atmosphere, with neon about 99.7 percent by weight, at about atmospheric pressure and a thickness of 4.5 to 4.7 mils exhibits spatial discharge transfer between conductors of an array spaced up to 5 mils apart without interaction between conductors 7 mils apart, depending somewhat on the size of the conductors and the thickness of the dielectric overcoat.

A lower limit exists for conductor spacing in an array if useful turn off characteristics of grouped discharge sites are to be realized. When the conductor edges are too close, the discharge region of one extends into the

region of influence of its grouped companion sites whereby an erase signal imposed on less than all sites of a group draws enough charge from the walls of those sites not subject to erase signals to transfer them to an "off state" of discharge. Discharge sites grouped to provide spatial discharge transfer are treated as discrete cells and the sites which make-up those cells are termed sub sites. In the arrays employing paired conductors the conductors in a pair should be conductively isolated from each other, and so spaced from each other and the sub site electrode areas of the one or more conductors of the opposite array as to be adapted to initiate an "on state" of discharge in a discharge sub site including one of the first and second conductors of the pair which is in an "off state" of discharge in response to an "on state" of discharge in the discharge sub site of the other of the first and second conductors. Those conductors should be spaced from each other sufficiently so that their sub sites will maintain an "on state" of discharge when other sub sites of the group are transferred to an "off state" of discharge.

Discharge device 11 is operated by applying an alternating sustainer voltage between the x array 27 and the y array 28. A range of voltage differences exist in which cells placed in the "on state" of discharge remain in that state and cells in the "off state" of discharge remain in the "off state." This is attributed to the development, for a discharge site in the "on state," of a wall voltage on the surface of the dielectric layers 17 and 18 by virtue of charge collected on those areas in the general area of the cross point of conductors of opposed arrays when viewed along a common perpendicular to the arrays. That wall charge is of a neutralizing polarity as it develops, hence, on reversal of the applied voltage it augments the sustainer voltage to a level causing a discharge, thereby providing a memory of the "on state" and the emission of light.

A matrix of cells can be inverted in its discharge state by a shift in the sustainer level. The inverting shift involves placing the sustainer voltage at a level relative to the wall charge voltage of the cells which were in an "off state" of discharge such that the voltage of that wall charge augments the sustainer voltage to impose sufficient voltage across the cells to ignite a discharge. The sustainer shift should be in a direction to place the wall voltage of cells in an "on state" of discharge at an "off state" voltage level relative to the new sustainer voltage.

As disclosed in greater detail in the afore-noted patent applications, spatial discharge transfer between sub sites of a discharge cell having proximate conductor portions in one or both of its opposed conductor arrays lends itself to logic functions internal of the device. Such logic functions can be achieved by inverting the device cell matrix discharge state and turning "on" cells "off." A coincidence of "off" manipulating signals must be imposed on all sub sites of a cell to turn off that cell if it is arranged for spatial discharge transfer. If any of a cell's sub sites remains in an "on state" of discharge, that sub site will initiate an "on state" in the remainder of the cell sub sites. This coincidence requisite for turn off is employed and an AND function in the addressing of cells in the matrix with a resultant reduction in the number of manipulating signal sources required to address selected cells. That is, a manipulating signal source can be connected to a number of parallel array conductors which provide by their portions proximate

with similar portions of other conductors in their array and in the opposed array the effective electrodes of the discharge sub sites of each cell. Such parallel connections can be combined so that each cell is controlled by a unique combination of manipulating signal sources and thus by appropriate selection and control logic can be individually addressed.

A common cell matrix is made up of an orthogonal array of the cross points of 512 lines in each coordinate. Thus, it required 1,024 manipulating signal sources individually connected to the 1,024 lines. A spatial discharge transfer type of matrix of the same number of cells requires at least twice the 512 lines in one coordinate. A preferred two by two sub site cell form employs two conductors in each array for each of the 512 lines of cells. This suggests 2,048 connections to the device from external circuitry.

According to the present invention the device is formed in the manufacture of its conductor arrays with interconnections to groups of those conductors connected in parallel for control from a single discharge signal manipulating source integral with the device. Such interconnections can be formed on terminal strip regions 13, 14, 15 and 16 at the ends of the conductors of the respective arrays 27 and 28. As shown in FIGS. 1, 2 and 3 the device 15 is a panel made up of paired x conductors 19 of array 27 and paired y conductors 20 of array 28 in a nine line by nine line cell matrix. Each conductor pair has been designated by a numbering system originating in the upper left corner of the array with the paired lines designated as 19-1 ... 19-9 for x conductors 19 and 21-1 ... 21-9 for y conductors 21. In addition, each conductor is considered as an *a* set or *b* set conductor so that the cell which is in the second *x* and *y* line is 19-2, 21-2 and its sub sites are designated by their proximate conductor portions as 19-2a, 21-2a; 19-2b, 21-2a; 19-2a, 21-2b; and 19-2b, 21-2b.

Parallel connections are made to sets of conductors of adjacent pairs in groups of three, in the example, and to sets of conductors of every third pair in each array. In the x array 27 the *a* sets are parallel by display connector lines 29, 31 and 32 for 19-1a, 19-2a and 19-3a; 19-4a, 19-5a and 19-6a; and 19-7a, 19-8a and 19-9a respectively. Adjacent pairs have their *a* conductors paralleled in the y array 28 by display connector lines 33, 34 and 35. The other sets of conductors of each array are connected through cross overs provided to extensions of the array lines which are aligned parallel to the length of the conductors by a linear extension of one conductor and oblique extensions 36 and 37 of the other two in the x array and 38 and 39 in the y array.

Panel edge terminals 41 through 46 and 47 through 52 provide means for connecting twelve discharge state manipulating signal sources to the conductors of the array. Conductive strips coupling sections 53 through 58 of the display connector lines formed on the substrates 24 and 25 with the display connector lines 29, 31 and 32 and 33, 34 and 35 couple those lines to terminals 41, 42 and 43 and 47, 48 and 49 respectively. In practice, the display connector lines interconnecting sections, strip coupler sections of the lines, and terminals can be formed at the same time the conductive lines of the array are formed, for example by vacuum deposition of a conductive film through suitable masks. It is desirable that the current carrying capacity of display connector lines and strip coupler sections be ade-

quate and accordingly they are made wider than the conductors in the array, typically about three times as wide or 9 mils.

The substrates 24 and 25 with their conductive elements thereon are then covered with a dielectric layer 17 and 18 at least in the display area 12. This dielectric layer can also be extended over the terminal strip regions 13, 14, 15 and 16, particularly the region of the display connector lines, both in the array conductor interconnection and terminal coupler sections. The terminals 41 through 52 should be free of dielectric to facilitate connection to external circuits. The terminals can have additional elements in the form of metal foil overlays (not shown) applied to protect the deposited film and make a more rugged connection.

In the case of the conductors which are not interconnected on the surface of the substrate due to the requirement that a system of cross-overs be provided to produce a unique combination of each pair of array conductors, the oblique extensions of the array conductors are covered with a dielectric layer such as layers 79 and 80 if layers 17 and 18 are not applied in those areas. Apertures 61 through 78 in the dielectric layers located in registry with the conductor extensions across the terminal strip region of the substrates 24 and 25 afford access to those extensions for electrical connections in the form of conductive strips 81, 82 and 83 for the b conductors of the x array and 84, 85 and 86 for the b conductors of the y array. Conductive strips 81 to 86 can be formed in situ by suitable deposition techniques such as vacuum deposition through masks such that the strips form continuously along the walls of the apertures 61 through 78 to conductively engage the array conductor extensions. Apertures 61 through 78 can be formed by localized photoetching and/or chemical etching of the dielectric layer. Other techniques of forming apertures through layers 79 and 80 or 17 and 18 to the conductor extensions include masking the dielectric as it is applied in a powder or thick slurry which is fired in situ, or the layers can be machined by means of a laser beam, sonic source or like energy means.

Terminals 44, 45 and 46 for the x array and 50, 51 and 52 for the y array are provided on the ends of cross connecting conductive strips 81, 82 and 83 and 84, 85 and 86 respectively. As in the case of terminals such as 41 these terminals can be formed with the cross connectors during their deposition; however, in order to increase their adaptability to external connections a sheet metal or foil overlay (not shown) can be superimposed on this region. An overcoat of dielectric (not shown) can be applied to the terminal strip regions 14 and 16 if it is deemed warranted for protection. Such a layer can be laid down as a powder or thick slurry, leaving the terminal faces free for electrical connections, and can be fired either separately or in conjunction with the assembly of the opposed substrate 24 and 25 into the display device 11.

A convenient construction for the device is to form array sub assemblies as described, join them together with proper spacing to define the desired gas volume thickness, fill the unit with gas and seal it. Dielectric layers such as 17 and 18 are formed of an inorganic material as adherent films or coatings which are not chemically or physically affected by elevated temperatures. One such material is a solder glass such as Kimble SG-68 manufactured and commercially available from

the assignee of the present invention. This glass has a thermal expansion characteristic substantially matching the thermal expansion characteristics of certain soda-lime glasses suitable, when in plate form for support members 24 and 25. Dielectric layers 17 and 18 in the display area 12 must be smooth and have a dielectric strength of about 1,000 volts per mil and be electrically homogenous on a microscopic scale (i.e. no cracks, bubbles, crystals, dirt, surface films or other irregularities). Also, the surfaces of dielectric layers 17 and 18 in the display area should be good photoemitters of electrons to enable priming or conditioning of the cells for transfer to an "on state" of discharge. Alternatively, dielectric layers 17 and 18 may be overcoated with materials designed to produce good electron emission, as in U.S. Pat. No. 3,634,719 issued to Roger E. Ernsthausen.

Spacer 26 provides a hermetic seal for the volume containing gas 22. It can be formed as a bead enclosing display area 12 on one of dielectric layers 17 and 18 or directly on one of substrate 24 and 25. The bead 26 can directly contact portions of conductors 19 and 21 where no overlying dielectric layer is present. In assembling the x and y arrays into a display panel the bead 26 is fused to the opposed face, usually in a baking process. A tubulation (not shown) is provided through the spacer bead 26 to enable the interior of the panel to be flushed and filled with an appropriate ionizable gas. After filling, the tubulation is closed to seal the display area 12.

Utilization of the device 11 as a display panel having inherent memory involves connecting its conductors to suitable circuitry generally represented in FIG. 1. In operation the device is continuously subject to an alternating sustainer voltage from sustainer voltage source 87 through pull-up and pull-down busses 88 and 89 and 91 and 92 for the x and y arrays respectively. This sustainer is applied through a transistor-diode matrix 90 to x and y conductors at terminals 41 through 52.

According to one form of operation employing cell matrix inversion of discharge states by shift of the sustainer level, one component of the sustainer voltage applied to one array has a smaller transition between extremes than the sustainer component applied to the other array. For example, the y conductors might normally have a sustainer component pulsating at regular periods between a reference level V_G and a voltage V_H above V_G while the x conductor sustainer component would pulsate between a value V_L below the reference level V_G and V_H above the reference level V_G . In such an arrangement $(V_H - V_G) + (V_H - V_L) = 2 V_s$ or about 220 volts. Typically V_H is 70 volts above V_s and V_L is 110 volts below V_G .

Inversion of a cell matrix discharge state energized by a sustainer of the above type is by an interchange of sustainer components between the arrays so that the y array is pulsed periodically between a value V_L below reference V_G and a value V_H above the reference while the x array is periodically shifted between V_H and V_G . Such sustainer pulsations can be applied at a frequency of 50 kilohertz for both normal and inversion producing levels. The inversion shift places the wall voltage of "off" cells at a sustainer augmenting value sufficient to initiate discharges in those cells and places the wall voltage of "on" cells at an "off state" level relative to the shifted sustainer.

Selective manipulation of discharge states for the cells is achieved by superimposing voltages on the sustainer components in proper synchronism with those components. Discharge terminating manipulations can be employed with the described assymetric sustainer components in a system arranged for inversion of the cell matrix. Such manipulations involve opposing the sustainer components, as by pulling the addressed discharge site conductors in each array to or toward the reference level V_G so that an "on state" of discharge is terminated by discharging the wall charge to an "off state." A sub site can be written by an erase signal addressed to it while it is inverted by cell matrix inversion to the "on state" and can be erased by an erase signal addressed to it while it is written and is operating in its normal sustainer operating mode.

The manipulation of the sub sites is selectively controlled from the user interface 93, which may be a computer or other suitable source of information to be displayed, through selection logic 94 which decodes the information to cell location and the type of cell manipulation desired, and to control logic 95 which clocks manipulating signals in proper synchronism with its clocking of the sustainer voltage. The manipulating signals termed "partial select signals" can be developed by normally open switches such as transistors in the transistor-diode matrix 90 arranged so that p-n-p transistors pull up an addressed conductor in the array then subjected to a sustainer voltage below the reference level and n-p-n transistors pull down an addressed conductor in the array subject to a sustainer voltage above the reference level. A pull-up and pull-down erase pulser is coupled to each of terminals 41 through 52 from transistor diode matrix 90.

While the connectors coupling a plurality of conductors in an array in parallel pass the erase partial select pulse for a cell to be manipulated to sub sites of all other sub sites having a portion of one of those conductors as an electrode, only one cell will transfer its state in response to operation of any given combination of four erase pulsers.

The effect of interconnecting the conductors in each array in sets enables a unique combination of an x a , x b , y a and y b pulser to be established for each cell in the matrix of cells of the panel. If the array conductors are assigned numbers 19-1a through 19-9b through 19-9b, 21-1a through 21-9a and 21-1b through 21-9b and are connected with the x a and y a conductors of three adjacent paired conductors and the x b and y b conductors of every third conductor pair in parallel, six pulsers are employed to uniquely select nine lines in each axis and twelve pulsers select eighty-one unique cell sites. Where a nine bit binary input provides 512 distinct signals and that number of lines are provided in a coordinate of a display panel, the two set system employing two conductors per line conveniently decodes with 32 pulsers each connected through display connector lines to 16 panel conductors for one set and with 16 pulsers each connected to 32 panel conductors for the other set.

The number of pulsers and paralleled conductors required to produce a given number of unique conductor pairs can be reduced further where all possible combinations of the conductors in an array are utilized. Effectively in the illustrated structure each of the three pulsers for the a set of conductors should have their conductors uniquely paired and each of the conductors

in the b set should similarly be combined. If there are N_x coordinate locations in the x dimension and N_y coordinate locations in the y dimension in the display and double conductors are employed for each location, there will be $2 N_x$ x conductors and $2 N_y$ y conductors in the display/memory panel grouped in pairs for each axis. With n voltage pulse sources per axis, the maximum number of lines L per axis which can be uniquely selected is $n(n-1)/2 = L$, i.e., the number of combinations of n things taken two at a time. In FIG. 1 n is six and 15 unique pairs of conductors could have been illustrated as lines in both the x and y axes, had all possible pairings been employed and had space permitted. This would have afforded 225 unique cells in the matrix addressed by 12 pulsers. Where 512 unique paired conductor lines were desired, the minimum number of pulsers and display connector lines to the array is 33. It should be noted that these reductions in the number of pulsers lead to more complex encoding and decoding for addressing purposes.

In actuating x a , x b , y a and y b pulsers for a unique four discharge sub site cell of the matrix a number of cell sub sites will be subject to the erase signals without altering the state of a cell in the "on state" since at least one of their sub sites will not be erased and will reignite the entire cell in the next half sustainer cycle. Thus there will be some coordinate locations which have one, two and three sub sites of the four that could be erased or transferred to an "off state" of discharge, leaving at least one which is not and is effective as a control sub site to reignite to the "on state" those which were erased. As described above, where this writing of a unique cell by addressing the matrix through the pulsers for the four conductors unique to the cell is practiced in a normally "off" field of cells, the matrix of cells is inverted to place the field of "off" cells in an "on state," the addressed cell is erased, and the matrix is reinverted so that the addressed cell is in an "on state" with the other originally "off" cells returned to their "off" state.

It is to be recognized that the number of conductors over each coordinate location of any array can be more than two and need not be equal in each array. That is there could be three or more conductors having portions so proximate each other and at least one conductor in the opposed array that spatial discharge transfer is realized between the sub sites defined by each pair of proximate conductor portions in opposed arrays. For example each cell can be formed with an x array conductor portion and three or more y array conductor portions, or each cell can be formed with three or more proximate conductor portions in each array.

The combinations of discharge sub sites to achieve spatial discharge transfer can be with a single conductor in one array and grouped conductors in the other array as where the discharge cells are in alignment along the single conductor as paired sub sites where the second array has paired proximate conductor portions as the conductor groupings. More commonly the cells are in a matrix having width and length where plural conductors are in each array. Again while only one array need have grouped conductors forming proximate conductor portions for spatial discharge transfer within the cell it is advantageous to have both arrays so arranged. Each conductor can have a plurality of regions spaced along its length in its array providing proximate conductor portions forming the electrodes of dis-

charge sub sites. Cell electrodes or proximate conductor portions can be connected in electrical parallel as well as series connections in the cross point or grid matrices shown and maintain unique discharge sub site combinations for individual cell control where erase writing techniques are utilized.

Since coincident erasure of all sub sites of a cell is necessary to erase a cell, unique writing of a cell is accomplished by inverting the discharge state of the matrix, as by actuating control logic 95 to interchange the sustainer component waveforms applied to the x and y arrays of conductors to shift the resultant sustainer level to "turn on" those cells normally "off" without loss of memory of previously written cells since they are turned "off" by the inversion. The coincident erase signals are then applied to the selected cell as determined by selection logic 94 and synchronized with sustainer voltage transitions in control logic 95 to activate the two pull up pulsers for the two conductors of the cell for the array at a low potential, V_L in the illustration, and the two pull down pulsers for the two conductors of the cell for the array at the high potential V_H whereby all four sub sites of the selected cell are erased. As noted above other sub sites made up from portions of the conductors of the erased cell sub sites will also be erased by these functions however since an "on" memory is retained in those other cells by the retention of at least one sub site in an "on state" those cells will be reignited in the next half sustainer cycle. Reinversion of the matrix places the newly erase written cell in an "on state" and returns any previously written cells to an "on state" while returning the background cells to an "off state."

FIG. 4 shows a modification of the structure of FIG. 1 where a trough or groove 96 in the dielectric overcoats 79 and 80 for the terminal strip regions 14 and 16 extends across and intersects with conductor extensions 36 and 37 or 38 and 39 in place of the individual apertures 61 through 78. Grooves 96 extend through the thickness of overcoats 79 and 80 to expose the conductor extensions and provide contact regions therewith by conductive strips 81 through 86. A convenient arrangement is to form grooves 96 in the same manner as the apertures and in the same alignment as, for example on terminal strip region 16, three grooves each coincident with aperture groups 70, 71 and 72; 73, 74 and 75; and 76, 77 and 78.

Conductors of the arrays are shown interconnected in parallel at each end in the structures of FIGS. 5 through 8. Only a portion of one array is represented in these Figures therefore it is to be understood that another array, assembled as illustrated in FIGS. 1 through 3, is required to complete the device. In FIG. 5 the substrate 101 has paired conductors 102 in a and b sets with the b sets connected in parallel on the substrate by jumpers 103 and the a set connected in parallel by cross-connectors 104 through 111 overlying a dielectric overcoat 112 on the terminal strip portions 113 and the underlying jumpers 103 and conductor extensions 114 of the a set of conductors 102. The display area 115 of the panel is within the bounds of the seal bead spacer 116 which generally separates the display area 115 from the terminal strip portions 113. The dielectric overcoat 112 on the terminal strip portions is required on both ends of the array since there are conductive cross-overs required at each end in the illustrated pattern. As in the case of the arrays of FIGS. 1 through 4

the extensions of the conductors in the terminal strip portion are offset from their alignment in the display area to facilitate their fan-out for interconnection.

Connection of cross-overs is by means of apertures in the dielectric overcoat 112 either as individual apertures 117 or as a groove (not shown) extending along each alignment of apertures transverse of the extensions 114. Cross-connectors 104 through 111 when deposited or otherwise applied to the overcoat extend through the overcoat 112 at the apertures to connect the a conductor 102 of every fourth pair of conductors along the array as at extensions 114-1a, 114-5a, 114-9a and 114-13a for connectors 104 and 111.

The parallel conductors in adjacent conductor pairs, conductors 102b have their terminal extension portions 118 extending beyond the apertures at which connections are made to the a conductors 102. These extensions 118 permit jumpers 103 to be formed around the terminal ends of the a conductors. The number of such embracing jumpers can be reduced by the conductor pattern shown in FIG. 6 wherein adjacent paired conductors 121 have their b conductors adjacent each other instead of alternating with the a set conductors. This permits a jumper 122 to couple b conductors of adjacent conductor pairs in the vicinity of the display area 115 so that one interconnecting jumper 123 is required to extend around the terminal ends of a conductor extensions 124 for each pair of b conductors. As a result, the manufacturing tolerances in the terminal strip portions can be further reduced.

An advantage of the double end connection of parallel conductors 102 and 121 resides in the double ended feed to each conductor provided by the jumpers and cross connections even though only a single external connection is made to the panel for each parallel conductor grouping. Jumpers 103-1, 103-2, 103-3 and 103-4 connect the ends of the b conductors 102 remote from the connection to circuits external of the device. Main feed lines 125, 126, 127 and 128 for the b set of conductors 102 are formed on substrate 101 as extensions of jumpers 103-5, 103-6, 103-7 and 103-8 respectively and can have terminals (not shown) as discussed with respect to FIGS. 1 through 4 for external connection. Cross connectors 104, 105, 106 and 107 connect the ends of the a conductors remote from the external terminal connections while cross connectors 108, 109, 110 and 111 extend to such terminals for feeding signals to the a conductors. Each conductor in the array thus provides a parallel feed to each end of every other conductor with which it is paralleled so that a break in any one conductor does not render the portion of that conductor beyond its feed end inoperative. Consideration of the arrangement of FIG. 6 in this regard reveals the same alternate feed paths from the main signal input at substrate engaged main feed lines 131 through 134 which are continuations of jumpers 123-1,4; 123-5,8; 123-9,12 and 123-13,16 respectively for the b conductors 121, and, in the case of the a conductors, cross connectors 135 through 138 function as main feed lines while cross connectors 139 through 142 are bind ended to merely provide the alternate signal feeds.

FIG. 9 illustrates another pattern of cross connections to achieve the maximum number of unique combinations of paired conductors 145 for a given number of inputs by providing all possible combinations of inputs taken two at a time. In the example, five inputs are

coupled in 10 unique combinations. Only a single terminal strip region 146 is employed although such a strip with the same pattern of interconnections could be provided at the opposite ends of conductors 145 if parallel interconnections between conductors are desired. The first input is combined with each of the other four in the first four pairs, the second input is combined with the remaining three in the next three pairs, etc. In this array construction the interconnections are all made from one end of the array conductors hence each connection is shown as a cross-over. Terminal strip region 146 is separated from display area 147 by a spacer-seal bead 148. The conductors 145 are extended from display area 147 to terminal strip 146 as straight, parallel ribbons or wires applied on substrate 149. A dielectric overcoat 151 applied over the conductors 145 is apertured in registry with the conductors 145, as represented by the connecting dots 152, and cross connecting conductive strips 153 are deposited on the dielectric 151 and across the apertures 152 to electrically engage only the conductors to be interconnected as 145-1a, 145-2a, 145-3a and 145-4a for cross-connecting strip 153-1. Terminals 154 are provided for each cross connecting strip 153 for connection to external circuitry.

A monolithic, multi-celled gas discharge display/memory panel is represented in FIG. 10. The illustrated broken away perspective shows two cells 156 and 157 having the spatial discharge transfer characteristic with four grouped discharge sub sites per cell. Each array line is made up of paired conductors, 158 and 159 for the x and y arrays respectively, which in plan can be interconnected in any of the terminal region patterns of FIGS. 1 through 9 and for discussion purposes will be assumed to be connected in pattern of FIG. 1. The terminal region 161 and 162 for the b set of x conductors and for the a set of y conductors, respectively, are fragmentarily illustrated.

The x and y conductor arrays 163 and 164 are on opposite faces of a dielectric layer 165 and a cavity 166 formed in dielectric layer 165 in each cell site. While not essential to operation, a dielectric overcoat 167 can be applied to the y array. The panel has a gas enclosure above the y array which can be formed by an overlying glass plate 168 sealed to the monolithic structure by a spacer bead (not shown) as previously described.

Terminal strip 162 is in the same plane as the y array 164 and has display connector lines 171, 172 and 173 formed with the array. Extensions 174 of the b conductors of the x array 163 are in the plane of that array and are overcoated with a dielectric 175 in the terminal strip region 161 such that apertures 176 in overcoat 175 afford access for electrical contact of the cross-connecting ribbons 177 and 178 with those conductors. In a similar manner the display connector lines for a conductors of the x array (not shown) are formed with and in the plane of the x array on the terminal strip region opposite 161 and the b conductors of the y array are paralleled with cross connecting display connector lines on a dielectric overcoat for extensions of those conductors into a terminal strip region opposite region 162 (not shown).

A monolithic structure can be formed on a glass plate substrate 179. The y array of conductors 159 and display connector lines 171, 172 and 173 are deposited on substrate 179. Dielectric layer 165 is applied over the region to receive the x array and its terminal strip re-

gions, as 161. The x array 163 and its integral display connector lines and conductor extensions 174 are deposited on fired layer 165. Any dielectric overcoats as 167 and 175 are then applied over the x array and is fired. Cavities 166 for the discharge sites and 176 for the cross connections on terminal strip region 161 can be formed either by masking the dielectric as it is applied and prior to firing or by etching, or machining the fired layers. Seal beading is then applied around display area 181 and the enclosing plate 168 secured. The atmosphere desired is placed in the space beneath plate 168 and cavities 166 to complete the display panel fabrication.

The conductor patterns proposed can be varied as by mixing patterns as can the display connector line patterns integral with the device. Thus the monolithic structure can have display connector lines at but one terminal strip region of each of its conductor arrays, it can be double ended, or it can have a mixture of the patterns with some conductors connected in parallel at each end and others connected at only one end. Accordingly, it is to be understood that the above disclosure is illustrative and is not to be read in a limiting sense.

What is claimed is:

1. A conductor array for a gaseous discharge display/memory panel comprising a non-conductive substrate; a plurality of closely spaced lines of conductive material on said substrate; a display area of said substrate mounted lines adapted to be enclosed; a terminal strip region of said substrate and said substrate mounted lines extending beyond said display area; a dielectric layer over said substrate mounted lines in said terminal strip region, said layer having apertures through its thickness which are in registry with and intersect with predetermined ones of said lines along predetermined paths which cross a plurality of said lines; and display connector lines formed as continuous strips of conductive material extending along said predetermined paths and into the apertures intersected by said paths to conductively engage said lines of conductive material on said substrate.

2. A conductor array according to claim 1 wherein said closely spaced lines are grouped in a plurality of groups with the intragroup line spacing such as to provide spatial discharge transfer between discharge sites defined by adjacent segments of said lines when incorporated in a discharge panel and with the intergroup line spacing such that discharges in discharge sites defined by portions of lines in one group have no effect on the discharge state of discharge sites defined by portions of lines in another group.

3. A conductor array according to claim 2 wherein said substrate is essentially planar and said conductive lines are straight and parallel in said display area.

4. A conductive array according to claim 2 wherein said apertures are arranged in a pattern in which each group of conductive lines is connected with a unique combination of display connector lines.

5. A conductive array according to claim 1 including second terminal strip region of said substrate and said substrate mounted lines extending beyond said display area.

6. A conductive array according to claim 3 wherein said terminal strip region is at one end of said straight and parallel conductive lines.

7. A conductive array according to claim 6 including a second terminal strip region of said substrate and said substrate mounted lines extending from the end of said straight and parallel conductive lines opposite said one end and external of said display area.

8. A conductive array according to claim 2 including display connector lines on said substrate between sets of conductors individual to a plurality of groups of conductors.

9. A conductive array according to claim 8 wherein said groups are contiguous to each other.

10. A conductive array according to claim 7 including display connector lines on said substrate in said second terminal region and electrically coupling a conductor of each of a plurality of contiguous groups of conductors, the remaining conductors of said contiguous groups being terminated on said substrate short of said display connector lines.

11. A conductive array according to claim 2 including a second terminal strip region of said substrate, including substrate mounted lines portions spaced from said first mentioned terminal strip region external of said display area and display connector lines between individual conductive lines of each of a plurality of conductive line groups adjacent each end of said lines on said first mentioned and second terminal strip regions.

12. A conductive array according to claim 2 including conductive connections on said substrate interconnecting contiguous conductive lines of separate contiguous groups of conductive lines.

13. A conductive array according to claim 12 wherein said conductive connections are adjacent each end of said conductive lines.

14. A conductive array according to claim 11 including a dielectric layer over said substrate mounted lines in said second terminal strip region, said layer having apertures through its thickness which intersect with predetermined ones of said lines along predetermined paths which cross a plurality of said lines, and display connector lines formed on said second terminal strip region as continuous strips of conductive material extending along said predetermined paths and into the apertures intersected by said paths to conductively engage said lines of conductive material on said substrate.

15. A combination according to claim 14 wherein said apertures and said display connector lines are so positioned on said second terminal strip region as to connect the same conductor lines as are connected by said display connector lines on said first mentioned terminal strip region.

16. A combination according to claim 1 wherein said

apertures are grooves extending across a plurality of conductive lines.

17. A combination according to claim 3 wherein at least some of said lines have portions continuous with said display area portions which extend in a direction offset from said straight display area portions, said cavities being in registry with and intersect said offset portions.

18. The structure defined in claim 2 a dielectric member on said display area; a cooperating second conductor array on the surface of said dielectric member opposite said display area and said first mentioned plurality of closely spaced lines of conductive material the conductors in said arrays defining cooperating conductor pairs; said dielectric member having a plurality of gas-filled cavities in one cavity juxtaposed to each cooperating conductor pair; and a terminal strip region of said dielectric member having conductors of said second array extending thereon beyond said display area; a second dielectric layer over said dielectric member and said conductors on said dielectric member terminal strip region, said second layer having apertures through its thickness which are in registry with and intersect with predetermined ones of said conductors along predetermined paths which cross a plurality of said conductors of said second array; and display connector lines formed on said dielectric member terminal strip region as continuous strips of conductive material extending along said predetermined paths and into the apertures intersected by said conductors to conductively engage said conductors.

19. The structure according to claim 1 having a second non-conductive substrate; a second plurality of closely spaced lines of conductive material on said second substrate; a display area of said second substrate mounted lines adapted to be enclosed; a terminal strip region of said second substrate and said substrate mounted lines extending beyond said display area of said second substrate mounted lines; a dielectric layer over said second substrate mounted lines in said terminal strip region, said layer having apertures through its thickness which are in registry with and intersect with predetermined ones of said lines along predetermined paths which cross a plurality of said lines; display connector lines formed as continuous strips of conductive material extending along said predetermined paths and into the apertures intersected by said paths to conductively engage said lines of conductive material on said second substrate; and means joining said second substrate to said first substrate with said first and second plurality of conductive lines in face to face spaced relationship.

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