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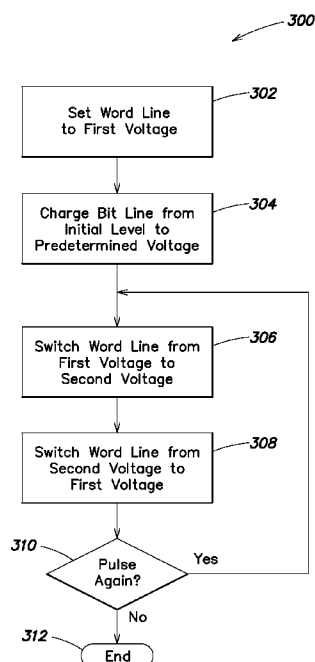
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(54) Title: CREATING SHORT PROGRAM PULSES IN RRAM WHEREIN THE BITLINES ARE LONGER THAN THE WORDLINES



(57) Abstract: The present invention provides methods and apparatus for adjusting voltages of bit and word lines to create short programming pulses to program a memory cell. The invention may include setting a first line connected to a memory cell to a first voltage from a first line standby voltage, charging a second line connected to the memory cell to a predetermined voltage from a second line standby voltage, switching the first line from the first voltage to a second voltage, and switching the first line from the second voltage to the first voltage. The voltage difference between the first voltage and the predetermined voltage is such that a safe voltage results that does not program the memory cell. A voltage difference between the second voltage and the predetermined voltage is such that a programming voltage operative to program the memory cell results. The switching operations together may create a first pulse.

FIG. 3



SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, —
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CREATING SHORT PROGRAM PULSES IN RRAM WHEREIN THE BITLINES ARE LONGER THAN THE
WORDLINES

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REFERENCE TO RELATED APPLICATIONS

This application claims priority from U.S. Patent
Application Serial No. 12/551,546, filed August 31, 2009,
15 and titled "Creating Short Program Pulses in Asymmetric
Memory Arrays," which is incorporated by reference herein
in its entirety for all purposes.

The present application is related to the following
patent applications, which are hereby incorporated by
20 reference herein in their entirety for all purposes:

U.S. Patent Application Serial No. 12/551,548,
filed August 31, 2009, and entitled "Reducing Programming
Time Of A Memory Cell;" and

U.S. Patent Application Serial No. 12/551,553,
25 filed August 31, 2009, and entitled "Flexible Multi-Pulse
Set Operation For Phase-Change Memories."

FIELD OF THE INVENTION

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The present invention relates generally to
integrated circuits containing memory arrays, and more
particularly, to creating short program pulses in such
arrays.

35

BACKGROUND OF THE INVENTION

Program pulses may be used to program a memory cell. In using program pulses, shorter (and faster) program pulses may be desirable. The maximum speed (and
5 minimum duration) of such pulses may be improved by using better quality metals for bit lines and word lines leading to memory cells, shortening the length of the bit lines, and adding switches to memory arrays to reduce capacitance on the bit lines. However, these previous approaches may
10 not be possible or desirable for all types of memory arrays including 3D memory arrays (e.g., diode matrix arrays). Thus, what are needed are methods and apparatus for creating short program pulses in memory arrays.

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SUMMARY OF THE INVENTION

In a first aspect of the invention, a method of programming a two terminal memory cell may be provided.
20 The method may include setting a first line connected to the memory cell to a first voltage from a first line standby voltage, charging a second line connected to the memory cell to a predetermined voltage from a second line standby voltage, switching the first line from the first
25 voltage to a second voltage, and switching the first line from the second voltage to the first voltage. The voltage difference between the first voltage and the predetermined voltage is such that a safe voltage results that does not program the memory cell. The voltage difference between
30 the second voltage and the predetermined voltage is such that a programming voltage operative to program the memory cell results. The switching operations together may create a first pulse.

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In a second aspect of the invention, a method of programming a two terminal memory cell, may be provided. The method may include setting a first line connected to the memory cell to a first voltage from a first line standby voltage; charging a second line connected to the memory cell to a predetermined voltage from a second line standby voltage; switching the first line connected to the memory cell from the first voltage to a second voltage; determining whether the memory cell has successfully programmed; and switching the first line connected to the memory cell from the second voltage to the first voltage in response to the determining operation. The voltage difference between the first voltage and the predetermined voltage is such that a safe voltage results that does not program the memory cell. The voltage difference between the second voltage and the predetermined voltage is such that a programming voltage operative to program the memory cell results. The switching operations together may create a first pulse.

In a third aspect of the invention, a method of programming a two terminal memory cell may be provided. The method may include connecting to a control circuit, a first line connected to the memory cell; setting via the control circuit the first line to a first voltage from a first line standby voltage; connecting to a sense amplifier, a second line connected to the memory cell; charging via the sense amplifier the second line to a predetermined voltage from a second line standby voltage; switching via the control circuit the first line connected to the memory cell from the first voltage to a second voltage; and switching via the control circuit the first line connected to the memory cell from the second voltage

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to the first voltage. The voltage difference between the first voltage and the predetermined voltage is such that a safe voltage results that does not program the memory cell. The voltage difference between the second voltage and the predetermined voltage is such that a programming voltage operative to program the memory cell results. The switching operations together may create a first pulse.

In a fourth aspect of the invention, a method of programming a two terminal memory cell may be provided. The method may include connecting to a control circuit, a first line connected to the memory cell; setting via the control circuit the first line to a first voltage from a first line standby voltage; connecting to a sense amplifier, a second line connected to the memory cell; charging via the sense amplifier the second line to a predetermined voltage from a second line standby voltage; switching via the control circuit the first line connected to the memory cell from the first voltage to a second voltage; determining via the sense amplifier whether the memory cell has successfully programmed; and switching via the control circuit the first line connected to the memory cell from the second voltage to the first voltage in response to the determining operation. The voltage difference between the first voltage and the predetermined voltage is such that a safe voltage results that does not program the memory cell. The voltage difference between the second voltage and the predetermined voltage is such that a programming voltage operative to program the memory cell results. The switching operations together may create a first pulse.

In a fifth aspect of the invention, a method of programming a two terminal memory cell may be provided.

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The method may include providing the memory cell; providing a first line connected to the memory cell; providing a first line driver connected to the first line; providing a first line select configured to control the first line driver; providing a control circuit selectively connected to the first line through the first line driver when the first line select is enabled, the control circuit configured to set the first line to a first voltage from a first line standby voltage; providing a second line connected to the memory cell; providing a second line driver connected to the second line; providing a second line select to control the second line driver; and providing a sense amplifier selectively connected to the second line through the second line driver when the second line is enabled, the sense amplifier configured to charge the second line to a predetermined voltage from a second line standby voltage. The control circuit switches the first line from the first voltage to the second voltage. The control circuit may switch the first line from the second voltage to the first voltage. The voltage difference between the first voltage and the predetermined voltage is such that a safe voltage results that does not program the memory cell. The voltage difference between the second voltage and the predetermined voltage is such that a programming voltage operative to program the memory cell results. The switches together may create a first pulse.

In a sixth aspect of the invention, a control circuit and sense amplifier combination operative to program a two terminal memory cell may be provided. The control circuit and sense amplifier combination may include a first line connection outputting a first voltage; and a

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second line connection outputting a predetermined voltage. The first line connection may be switched to output a second voltage. The first line connection may then be switched to output the first voltage. The voltage
5 difference between the first voltage and the predetermined voltage is such that a safe voltage results that does not program the memory cell. The voltage difference between the second voltage and the predetermined voltage is such that a programming voltage operative to program the memory
10 cell results. The switching the first line connection to output the second voltage and the switching the first line connection to a first voltage together may create a first pulse.

In a seventh aspect of the invention, a memory
15 array including a two terminal memory cell may be provided. The memory array may include a memory cell; a first line connected to the memory cell being set to a first voltage from a first line standby voltage; and a second line connected to the memory cell being charged to a
20 predetermined voltage from a second line standby voltage. The first line may be switched from the first voltage to a second voltage. The first line may then be switched from the second voltage to the first voltage. The voltage difference between the first voltage and the predetermined
25 voltage is such that a safe voltage results that does not program the memory cell. The voltage difference between the second voltage and the predetermined voltage is such that a programming voltage operative to program the memory cell results. The switching of the first line to the
30 second voltage and the switching of the first line to the first voltage together may create a first pulse.

In accordance with an eighth aspect of the invention, a memory array including a two terminal memory cell may be provided. The memory array may include the memory cell; a first line connected to the memory cell; a first line driver connected to the first line; a first line select configured to control the first line driver; a control circuit selectively connected to the first line through the first line driver when the first line select is enabled, the control circuit configured to set the first line to a first voltage from a first line standby voltage; a second line connected to the memory cell; a second line driver connected to the second line; a second line select configured to control the second line driver; and a sense amplifier selectively connected to the second line through the second line driver when the second line select is enabled, the sense amplifier configured to charge the second line to a predetermined voltage from a second line standby voltage. The control circuit may switch the first line from the first voltage to a second voltage. The control circuit may then switch the first line from the second voltage to the first voltage. The voltage difference between the first voltage and the predetermined voltage is such that a safe voltage results that does not program the memory cell. The voltage difference between the second voltage and the predetermined voltage is such that a programming voltage operative to program the memory cell results. The switching the first line from the first voltage to the second voltage and from the second voltage to the first voltage together may create a first pulse.

Other features and aspects of the present invention will become more fully apparent from the following detailed

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description, the appended claims and the accompanying drawings.

5 BRIEF DESCRIPTION OF THE FIGURES

FIG. 1 is a schematic representation of an electronic device according to an embodiment of the present invention.

10 FIG. 2A is a schematic representation of a memory array.

FIG. 2B is a schematic representation of a sense amplifier.

15 FIG. 3 is a flowchart of a first exemplary open-loop method of creating short program pulses.

FIG. 4 is a schematic representation of voltages of a bit line and a word line according to an embodiment of the present invention.

20 FIG. 5 is a flowchart of a second open-loop method of creating short program pulses.

FIG. 6 is a flowchart of an exemplary closed-loop method of creating short program pulses.

25 FIG. 7 is a schematic representation of voltages of a bit line, a word line, and a sense amplifier according to an embodiment of the present invention.

DETAILED DESCRIPTION

30 Reference will now be made in detail to embodiments of the present invention, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to the like elements throughout. The embodiments are described below to explain the present
35 invention by referring to the figures.

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As used herein, the terms "a," "an" and "the" may refer to one or more than one of an item. The terms "and" and "or" may be used in the conjunctive or disjunctive and will generally be understood to be equivalent to "and/or."

5 For brevity and clarity, a particular quantity of an item may be described or shown while the actual quantity of the item may differ.

Initially, it should be noted that the term voltage as used throughout this specification including the claims,
10 should be broadly interpreted to include the phrase "programming energy."

In accordance with embodiments of the present invention, voltages of both a bit line and a word line may be adjusted to create short programming pulses to program a
15 memory cell. Voltages of the bit line and the word line may initially be at standby voltages. A word line may be switched from a first voltage to a second voltage and then back to the first voltage. The first voltage (e.g., 3 volts) may be such that relative to a voltage applied to
20 the bit line (e.g., 8 volts), a net voltage (e.g., 5 volts) results that is less than a voltage needed to program the memory cell. That is, the first voltage may result in a safe voltage that does not cause the cell to be programmed. Using the voltage of the word line to adjust the net
25 voltage to be less than a voltage that may program the memory cell is counter-intuitive in that conventionally the voltage of the bit line is used to control the net voltage. The second voltage (e.g., 0 volts) may be such that relative to a voltage applied to the bit line (e.g., 8
30 volts), a net voltage (e.g., 8 volts) results that is effective to program the memory cell. That is, the second voltage may result in a programming voltage that does cause

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the cell to be programmed. The switching from the first voltage to the second voltage and then back to the first voltage may create a short programming pulse. Multiple short programming pulses may be created (*i.e.*, the voltage of the word line may be modulated). By switching from the safe voltage to the programming voltage (*e.g.*, instead of switching from the standby voltage to the programming voltage), a much smaller voltage change may be used during programming that does not require the current to be limited.

FIG. 1 is a schematic representation of an electronic device 100 according to an embodiment of the present invention. The electronic device 100 may include an integrated circuit 102. The integrated circuit 102 may include a memory array 104. The memory array 104 may include a memory cell 106. The memory cell 106 is shown as part of the memory array 104 which is shown as part of the integrated circuit 102 which is shown as part of the electronic device 100. However, the electronic device 100 may otherwise access memory cells 106.

The electronic device 100 may include any of a variety of known or later-developed electronic devices that include or access memory cells 106. For example and not by way of limitation, the electronic device 100 may include a flash drive, a digital audio player, or a portable computer.

FIG. 2A is a schematic representation of a memory array 200, such as the memory array 104 of FIG. 1. The memory array 200 may include a memory cell 202, a bit line 204, a bit line driver 206, a bit line select 208, a sense amplifier 210, a word line 220, a word line

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driver 222, a word line select 224, a control circuit 226, and a capacitor 230.

The memory cell 202 may be formed of any of a variety of known or later-developed materials. For example
5 and not by way of limitation, the memory cell 202 may be formed of chalcogenide/PVM or chalcogenide-type materials. The memory cell 202 may be a two-terminal memory cell. The memory cell 202 may include an isolation unit. The isolation unit may include a diode including an anode and a
10 cathode. The anode side may be sensed. The cathode side may be controlled. Alternatively, the anode side may be controlled, and the cathode side may be sensed.

The memory cell 202 may be connected to the bit line 204. The bit line 204 may be on the anode side of the
15 memory cell 202. That is, the bit line may be on the sensed side. The bit line 204 may be long relative to the word line 220. The bit line 204 may be connected to the bit line driver 206. The bit line driver 206 may be controlled by the bit line select 208. When the bit line
20 select 208 is enabled, the bit line 204 may be connected to the sense amplifier 210. The bit line driver 206 may be enabled or disabled based on a charge of the capacitor 230.

The memory cell 202 may be connected to the word line 220. The word line 220 may be on the cathode side of
25 the memory cell 202. That is, the word line may be on the side that is controlled. The word line 220 may be connected to the word line driver 222. The word line driver 222 may be controlled by the word line select 224. When the word line select 224 is enabled, it may connect
30 the word line 220 to the control circuit 226. The word line 220 may be shorted together with another word line so that word lines are shared.

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The sense amplifier 210 may be a write sense amplifier. As will be described further below, the sense amplifier 210 may control programming of the memory cell 202 in conjunction with the control circuit 226.

5 The control circuit 226 may include a dedicated regulator (e.g., a MUX). The control circuit 226 may control the amount of voltage applied to the word line 220. The control circuit 226 may switch between two voltages.

 It should be noted that the word line and bit line
10 may be switched between more than two voltages, such as from standby voltages to, for example, a first voltage and to a second voltage. Examples of standby voltages are described in U.S. Patent Nos. 6,822,903 and 6,963,504, both to Scheuerlein and Knall, and both entitled "Apparatus And
15 Method For Disturb-Free Programming Of Passive Element Memory Cells," both of which are incorporated by reference herein in their entirety for all purposes. In these examples, first and second array lines may be driven to selected bias voltages. Then, the first and second array
20 lines may be driven to unselected bias voltages. The timing of when the first and second array lines may be driven to selected bias voltages and when the first and second array lines may be driven to unselected bias voltages may be adjusted relative to one another (i.e., the
25 first array line relative to the second array line), for example, to prevent unintended programming of cells located near target cells in an array. It should be appreciated that in the present disclosure, such standby voltages should not be confused with the first voltage (i.e., as
30 discussed below, the voltage that, when coupled with the voltage applied to the bit line, results in a safe voltage).

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The first voltage (e.g., 3 volts) may be high enough that when coupled with voltage applied to the bit line 204 (e.g., 8 volts), may result in a net voltage (e.g., 5 volts) that may be less than a voltage that may
5 program the memory cell 202. That is, the first voltage may result in a safe voltage. The second voltage (e.g., 0 volts) may be low enough that when coupled with voltage applied to the bit line 204 (e.g., 8 volts), may result in a net voltage (e.g., 8 volts) effective to program the
10 memory cell 202. That is, the second voltage may result in a programming voltage.

Alternatively, the control circuit 226 may include a diode connected NMOS device and a bypass path. The diode connected NMOS device may provide the first voltage (i.e.,
15 the safe voltage). The bypass path, when selected, may provide the second voltage (resulting in the programming voltage).

The actual value of the first and second voltages may be determined based upon multiple considerations. One
20 consideration may be that the difference between the two voltages should be sufficient to distinguish between programming and not programming. Another consideration may be that the smaller the difference between the two voltages is, the faster the programming of the memory cell 202 may
25 be.

FIG. 2B is a schematic representation of a sense amplifier 250, such as the sense amplifier 210 of FIG. 2A. The sense amplifier 250 may be a write sense amplifier. The sense amplifier 250 may control programming of the
30 memory cell 202 in conjunction with the control circuit 226. The sense amplifier 250 may include a

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voltage 252, a current limiter 254, a node 256, a PMOS device 258, and a voltage reference 260.

The voltage 252 may flow through the current limiter 254, the node 256, and the PMOS device 258. The current limit may limit to a predetermined amount (e.g., 1 microamp). The voltage 252 may be compared with the voltage reference 260. Once the memory cell 202 programs, the voltage 252 flowing through the node 256 may fall.

The operation of the memory array 200 is now described with reference to FIGS. 3 - 7, which illustrate, inter alia, exemplary methods of creating short program pulses.

FIG. 3 is a flowchart of a first exemplary open-loop method 300 of creating short program pulses. FIG. 4 is a schematic representation of voltages 400 of a bit line 204 and a word line 220 according to an embodiment of the present invention.

In operation 302, the word line 220 may be set to a first voltage 406. For example and not by limitation, the voltage of the word line 220 may be set to 3 volts. The word line select 224 may be enabled thereby connecting the word line 220 through the word line driver 222 to the control circuit 226.

In operation 304, the bit line 204 may be charged from an initial level 402 to a predetermined voltage 404. For example and not by limitation, the bit line 204 may be charged from an initial level of 0 volts to a predetermined voltage of 8 volts. The bit line 204 may be charged from the initial level 402 to the predetermined voltage 404 quickly and without limitation (e.g., without limiting the amount of current flow). The bit line select 208 may be

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enabled thereby connecting the bit line 204 through the bit line driver 206 to the sense amplifier 210.

The first voltage 406 of the word line (e.g., 3 volts) may be high enough that when the cell is coupled to the first voltage 406 and the predetermined voltage 404 of the bit line 204 (e.g., 8 volts), a net voltage (e.g., 5 volts) may result that is less than a voltage needed to program the memory cell 202. That is, the first voltage 406 may result in a safe voltage.

In operation 306, the word line 220 may be switched from the first voltage 406 to a second voltage 408. The second voltage (e.g., 0 volts) may be low enough that when the second voltage and the predetermined voltage 404 applied to the bit line 204 (e.g., 8 volts) are coupled to the memory cell a net voltage (e.g., 8 volts) operative to program the memory cell 202 may result. That is, the second voltage 408 may result in a programming voltage. The control circuit 226 may switch between the first voltage 406 and the second voltage 408.

As noted above, the bit line 204 may be long relative to the word line 220. Thus, the switching of the word line 220 may be faster than if the bit line 204 were switched or otherwise controlled.

In operation 308, the word line 220 may be switched from the second voltage 408 to the first voltage 406. Operations 306 and 308 therefore together may create a short programming pulse.

In operation 310, a determination may be made whether to again create a short programming pulse. If it is determined that a short programming pulse should again be created, the open-loop method 300 may return to operation 306, and proceed through operations 306 and 308

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to create a short programming pulse. This process may be repeated to create an appropriate number of short programming pulses. If, during operation 310, it is determined that a short programming pulse should not again
5 be created, the open-loop method 300 may proceed to operation 312 and end.

It should be noted that although FIG. 3 shows the determination of whether to again create a short programming pulse after the previous creation of a short
10 programming pulse, the determination, like other operations, may be made at a different point during the open-loop method 300. However, for brevity and clarity, operation 310 is shown as following operation 308.

FIG. 5 is a flowchart of a second open-loop
15 method 500 of creating short program pulses.

In operation 502, the word line 220 may be set to a first voltage 406. For example and not by limitation, the voltage of the word line 220 may be set to 3 volts.

In operation 504, the bit line 204 may be charged
20 from an initial level 402 to a predetermined voltage 404. For example and not by limitation, the bit line 204 may be charged from an initial level of 0 volts to a predetermined voltage of 8 volts. The bit line 204 may be charged from the initial level 402 to the predetermined voltage 404
25 quickly and without limitation.

In operation 506, the word line 220 may be switched from the first voltage 406 to a second voltage 408.

In operation 508, the word line 220 may be switched from the second voltage to the first voltage 406.
30 Operations 506 and 508 therefore together may create a short programming pulse.

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In operation 510, a determination may be made whether to again create a short programming pulse. If it is determined that a short programming pulse should again be created, the open-loop method 500 may return to
5 operation 506, and proceed through operations 506 and 508 to create a short programming pulse. If during operation 510, it is determined that a short programming pulse should not again be created, the open-loop method 500 may proceed to operation 512.

10 In operation 512, a determination may be made whether the memory cell 202 has been successfully programmed. If it is determined that the memory cell 202 has not been successfully programmed, the open-looped method 500 may return to operation 506, and proceed through
15 operations 506 and 508 to create a short programming pulse. If, during operation 512, it is determined that the memory cell 202 has been successfully programmed, the open-looped method 500 may proceed to operation 514 and end.

It should be noted that although FIG. 5 shows the
20 determinations of whether to again create a short programming pulse and whether the memory cell has been successfully programmed after the previous creation of a short programming pulse, the determinations, like other operations, may be made at a different point during the
25 open-loop method 500, and differently relative to one another. However, for brevity and clarity, operations 510 and 512 are shown as following operation 508.

FIG. 6 is a flowchart of an exemplary closed-loop method 600 of creating short program pulses. FIG. 7 is a
30 schematic representation of voltages 700 of a bit line 204, a word line 220, and a sense amplifier 210 according to an embodiment of the present invention.

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In operation 602, the word line 220 may be set to a first voltage (e.g., first voltage 406 in FIG. 4). For example and not by limitation, the voltage of the word line 220 may be set to 3 volts.

5 In operation 604, the bit line 204 may be charged from an initial level (e.g., initial level 402 in FIG. 4) to a predetermined voltage 704. For example and not by limitation, the bit line 204 may be charged from an initial level of 0 volts to a predetermined voltage of 8 volts.
10 The bit line 204 may be charged from the initial level 402 to the predetermined voltage quickly and without limitation.

In operation 606, the word line 220 may be switched from the first voltage to a second voltage 708.

15 In operation 608, a determination may be made whether the memory cell 202 has been successfully programmed. The determination of operation 608 may be made based on a switch from a first voltage 712 of the sense amplifier 210 to a second voltage 710. Upon this switch,
20 predetermined voltage 704 may drop 703. If it is determined that the memory cell 202 has not been successfully programmed, the closed-loop method 600 may return to operation 608 and proceed to determine whether the memory cell 202 has been successfully programmed. If,
25 during operation 608 it is determined that the memory cell 202 has been successfully programmed, the closed-loop method 600 may proceed to operation 610.

In operation 610, the word line 220 may be switched from the second voltage 708 to the first voltage 706.

30 In operation 612, the closed-looped method 600 may end.

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The foregoing description discloses only exemplary embodiments of the invention. Modifications of the above-disclosed embodiments of the present invention of which fall within the scope of the invention will be readily apparent to those of ordinary skill in the art. For instance, although in some embodiments, certain operations are shown as occurring at particular times relative to other operations, the operations may occur at other times.

Accordingly, while the present invention has been disclosed in connection with exemplary embodiments thereof, it should be understood that other embodiments may fall within the spirit and scope of the invention as defined by the following claims.

15

THE INVENTION CLAIMED IS:

1. A method of programming a two terminal memory cell, comprising:

5 setting a first line connected to the memory cell to a first voltage from a first line standby voltage;

 setting a second line connected to the memory cell to a predetermined voltage from a second line standby voltage;

10 switching the first line connected to the memory cell from the first voltage to a second voltage; and

 switching the first line connected to the memory cell from the second voltage to the first voltage,

 wherein a difference between the first voltage and
15 the predetermined voltage results in a safe voltage that does not program the memory cell,

 wherein a difference between the second voltage and the predetermined voltage results in a programming voltage operative to program the memory cell, and

20 wherein the switching operations together create a first pulse.

2. The method of claim 1, further comprising, after the switching operations, determining whether to repeat the
25 switching operations to create a second pulse.

3. The method of claim 2, further comprising repeating the switching operations after the determining operation to create the second pulse in response to the determining
30 operation.

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4. The method of claim 1, further comprising, after the switching operations, determining whether the memory cell successfully programmed.

5 5. The method of claim 4, further comprising repeating the switching operations after the determining operation to create a second pulse in response to the determining operation.

10 6. The method of claim 4, wherein the determining operation includes reading the memory cell to confirm whether the memory cell successfully programmed.

15 7. The method of claim 2, further comprising, after the switching operations, determining whether the memory cell successfully programmed.

8. The method of claim 7, further comprising:
repeating the switching operations after the
20 determining whether to repeat the switching operations operation to create the second pulse in response to the determining operation; and
repeating the switching operations after the
determining whether the memory cell successfully programmed
25 operation to create a third pulse in response to the determining operation.

9. The method of claim 8, wherein the operation of repeating the switching operations after determining
30 whether to repeat the switching operations occurs before the operation of repeating the switching operations after

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the determining whether the memory cell successfully programmed operation.

10. The method of claim 1, wherein the first line
5 comprises a word line and the second line comprises a bit line.

11. The method of claim 1, wherein the first voltage is higher than the second voltage.

10

12. The method of claim 1, wherein a difference between the safe voltage and the programming voltage is operative to maximize programming speed and operative to distinguish between programming and not programming.

15

13. The method of claim 1, wherein setting the second line to the predetermined voltage includes charging the second line to the predetermined voltage without limitation.

20

14. The method of claim 1, wherein the switching from the first voltage to the second voltage includes a VT drop.

15. A method of programming a two terminal memory cell,
25 comprising:

setting a first line connected to the memory cell to a first voltage from a first line standby voltage;

setting a second line connected to the memory cell to a predetermined voltage from a second line standby
30 voltage;

switching the first line connected to the memory cell from the first voltage to a second voltage;

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determining whether the memory cell has successfully programmed; and

switching the first line connected to the memory cell from the second voltage to the first voltage in

5 response to the determining operation,

wherein a difference between the first voltage and the predetermined voltage results in a safe voltage that does not program the memory cell,

10 wherein a difference between the second voltage and the predetermined voltage results in a programming voltage operative to program the memory cell, and

wherein the switching operations together create a first pulse.

15 16. The method of claim 15, further comprising, after the switching operations, determining whether to repeat the switching operations to create a second pulse.

17. The method of claim 16, further comprising
20 repeating the switching operations after the determining whether to repeat operation to create the second pulse in response to the determining whether to repeat operation.

18. The method of claim 15, wherein the determining
25 whether the memory cell has successfully programmed comprises determining when a sense amplifier voltage switches voltage.

19. The method of claim 15, wherein the first line
30 comprises a word line and the second line comprises a bit line.

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20. The method of claim 15, wherein the first voltage is higher than the second voltage.

21. The method of claim 15, wherein a difference
5 between the safe voltage and the programming voltage is operative to maximize programming speed and operative to distinguish between programming and not programming.

22. The method of claim 15, wherein the setting of the
10 second line to the predetermined voltage includes charging the second line to the predetermined voltage without limitation.

23. The method of claim 15, wherein the switching from
15 the first voltage to the second voltage comprises a VT drop.

24. A method of programming a two terminal memory cell, comprising:
20 connecting a control circuit to a first line connected to the memory cell;
setting the first line to a first voltage via the control circuit from a first line standby voltage;
connecting to a sense amplifier, a second line
25 connected to the memory cell;
charging via the sense amplifier the second line to a predetermined voltage from a second line standby voltage;
switching via the control circuit the first line connected to the memory cell from the first voltage to a
30 second voltage; and

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switching via the control circuit the first line connected to the memory cell from the second voltage to the first voltage,

wherein a difference between the first voltage and
5 the predetermined voltage results in a safe voltage that does not program the memory cell,

wherein a difference between the second voltage and the predetermined voltage results in a programming voltage operative to program the memory cell, and

10 wherein the switching operations together create a first pulse.

25. The method of claim 24, further comprising, after the switching operations, determining via the control
15 circuit whether to repeat the switching operations to create a second pulse.

26. The method of claim 25, further comprising repeating the switching operations after the determining
20 operation to create the second pulse in response to the determining operation.

27. The method of claim 24, further comprising, after the switching operations, determining via the control
25 circuit whether the memory cell successfully programmed.

28. The method of claim 27, further comprising repeating the switching operations after the determining
operation to create a second pulse in response to the
30 determining operation.

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29. The method of claim 27, wherein the determining operation includes reading the memory cell to confirm whether the memory cell successfully programmed.

5 30. The method of claim 25, further comprising, after the switching operations, determining via the control circuit whether the memory cell successfully programmed.

31. The method of claim 30, further comprising:
10 repeating the switching operations after the determining whether to repeat the switching operations operation to create the second pulse in response to the determining operation; and
 repeating the switching operations after the
15 determining whether the memory cell successfully programmed operation to create a third pulse in response to the determining operation.

32. The method of claim 31, wherein the operation of
20 repeating the switching operations after determining whether to repeat the switching operations occurs before the operation of repeating the switching operations after the determining whether the memory cell successfully programmed operation.

25 33. The method of claim 24, wherein the first line comprises a word line and the second line comprises a bit line.

30 34. The method of claim 24, wherein the first voltage is higher than the second voltage.

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35. The method of claim 24, wherein a difference between the safe voltage and the programming voltage is operative to maximize programming speed and operative to distinguish between programming and not programming.

5

36. The method of claim 24, wherein the charging of the second line to the predetermined voltage is without limitation.

10 37. The method of claim 24, wherein the switching from the first voltage to the second voltage comprises a VT drop.

15 38. A method of programming a two terminal memory cell, comprising:

connecting a first line to a control circuit wherein the first line is connected to the memory cell; setting via the control circuit the first line to a first voltage from a first line standby voltage;

20 connecting a second line to a sense amplifier, wherein the second line is connected to the memory cell; charging the second line to a predetermined voltage via the sense amplifier from a second line standby voltage;

switching via the control circuit the first line connected to the memory cell from the first voltage to a second voltage;

25 determining via the sense amplifier whether the memory cell has successfully programmed; and

switching via the control circuit the first line connected to the memory cell from the second voltage to the first voltage in response to the determining operation,

30

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wherein a difference between the first voltage and the predetermined voltage results in a safe voltage that does not program the memory cell,

wherein a difference between the second voltage and
5 the predetermined voltage results in a programming voltage operative to program the memory cell, and

wherein the switching operations together create a first pulse.

10 39. The method of claim 38, further comprising, after the switching operations, determining via the control circuit whether to repeat the switching operations to create a second pulse.

15 40. The method of claim 39, further comprising repeating the switching operations after the determining whether to repeat operation to create the second pulse in response to the determining whether to repeat operation.

20 41. The method of claim 38, wherein the determining whether the memory cell has successfully programmed comprises determining when the sense amplifier voltage switches voltage.

25 42. The method of claim 38, wherein the first line comprises a word line and the second line comprises a bit line.

30 43. The method of claim 38, wherein the first voltage is higher than the second voltage.

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44. The method of claim 38, wherein a difference between the safe voltage and the programming voltage is operative to maximize programming speed and operative to distinguish between programming and not programming.

5

45. The method of claim 38, wherein the charging of the second line to the predetermined voltage is without limitation.

10 46. The method of claim 35, wherein the switching from the first voltage to the second voltage comprises a VT drop.

15 47. A method of programming a two terminal memory cell, comprising:

providing the memory cell;

providing a first line connected to the memory cell;

20 providing a first line driver connected to the first line;

providing a first line select configured to control the first line driver;

25 providing a control circuit selectively connected to the first line through the first line driver when the first line select is enabled, the control circuit configured to set the first line to a first voltage from a first line standby voltage;

providing a second line connected to the memory cell;

30 providing a second line driver connected to the second line;

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providing a second line select to control the second line driver; and

providing a sense amplifier selectively connected to the second line through the second line driver when the second line is enabled, the sense amplifier configured to
5 charge the second line to a predetermined voltage from a second line standby voltage,

wherein the control circuit switches the first line from the first voltage to the second voltage,

10 wherein the control circuit switches the first line from the second voltage to the first voltage,

wherein a difference between the first voltage and the predetermined voltage results in a safe voltage that does not program the memory cell,

15 wherein a difference between the second voltage and the predetermined voltage results in a programming voltage operative to program the memory cell, and

wherein the switches together create a first pulse.

20 48. The method of claim 47, wherein, after the control circuit switches the first line from the first voltage to the second voltage and from the second voltage to the first voltage, the control circuit determines whether to again switch the first line from the first voltage to the second
25 voltage and from the second voltage to the first voltage to create a second pulse.

49. The method of claim 48, wherein the control circuit switches the first line from the first voltage to the
30 second voltage and from the second voltage to the first voltage to create the second pulse.

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50. The method of claim 47, wherein, after the control circuit switches the first line from the first voltage to the second voltage and from the second voltage to the first voltage, the control circuit determines whether the memory
5 cell successfully programmed.

51. The method of claim 50, wherein the control circuit switches the first line from the first voltage to the second voltage and from the second voltage to the first
10 voltage to create a second pulse.

52. The method of claim 50, wherein the control circuit determines whether the memory cell successfully programmed by reading the memory cell to confirm whether the memory
15 cell successfully programmed.

53. The method of claim 48, wherein, after the control circuit switches the first line from the first voltage to the second voltage and from the second voltage to the first
20 voltage, the control circuit determines whether the memory cell successfully programmed.

54. The method of claim 53, wherein, the control circuit switches the first line from the first voltage to the second voltage and from the second voltage to the first
25 voltage to create the second pulse, and the control circuit switches the first line from the first voltage to the second voltage and from the second voltage to the first voltage to create a third pulse.

30

55. The method of claim 54, wherein the control circuit switches the first line from the first voltage to the

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second voltage and from the second voltage to the first voltage to create the second pulse before the control circuit switches the first line from the first voltage to the second voltage and from the second voltage to the first
5 voltage to create the third pulse.

56. The method of claim 47, wherein the first line comprises a word line and the second line comprises a bit
10 line.

57. The method of claim 47, wherein the first voltage is higher than the second voltage.

58. The method of claim 47, wherein a difference
15 between the safe voltage and the programming voltage is operative to maximize programming speed and operative to distinguish between programming and not programming.

59. The method of claim 47, wherein the charging of the
20 second line to the predetermined voltage is without limitation.

60. The method of claim 47, wherein the switching from the first voltage to the second voltage comprises a VT
25 drop.

61. The method of claim 47, wherein the sense amplifier is further configured to detect whether the memory cell has successfully programmed, wherein the control circuit
30 switches the first line from the second voltage to the first voltage in response to the sense amplifier

determining that the memory cell has been successfully programmed.

62. The method of claim 61, wherein, after the control
5 circuit switches the first line from the first voltage to
the second voltage and from the second voltage to the first
voltage, the control circuit determines whether to again
switch the first line from the first voltage to the second
voltage and from the second voltage to the first voltage to
10 create a second pulse.

63. The method of claim 62, wherein the control circuit
switches the first line from the first voltage to the
second voltage and from the second voltage to the first
15 voltage to create the second pulse.

64. The method of claim 61, wherein the sense amplifier
determines that the memory cell has been successfully
programmed by detecting when a sense amplifier voltage
20 switches voltage.

65. A control circuit and sense amplifier combination
operative to program a two terminal memory cell,
comprising:
25 a first line connection outputting a first voltage;
and
a second line connection outputting a predetermined
voltage;
wherein the first line connection is switched to
30 output a second voltage,
wherein the first line connection is then switched
to output the first voltage,

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wherein a difference between the first voltage and the predetermined voltage results in a safe voltage,

wherein a difference between the second voltage and the predetermined voltage results in a programming voltage,

5 and

wherein the switching the first line connection to output the second voltage and the switching the first line connection to a first voltage together create a first pulse.

10

66. The control circuit and sense amplifier combination of claim 65, wherein, after the first line connection is switched from outputting the first voltage to output the second voltage and from outputting the second voltage to output the first voltage, the control circuit and sense amplifier combination determines whether to again switch the first line connection from outputting the first voltage to output the second voltage and from outputting the second voltage to output the first voltage to create a second

15
20 pulse.

67. The control circuit and sense amplifier combination of claim 66, wherein the control circuit and sense amplifier combination switches the first line connection from outputting the first voltage to output the second voltage and from outputting the second voltage to outputting the first voltage to create the second pulse.

25
30 68. The control circuit and sense amplifier combination of claim 65, wherein after the first line connection is switched from outputting the first voltage to output the second voltage and from outputting the second voltage to

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output the first voltage, the control circuit and sense amplifier combination determines whether a memory cell successfully programmed.

5 69. The control circuit and sense amplifier of claim 68, wherein the control circuit and sense amplifier combination switches the first line connection from outputting the first voltage to output the second voltage and from outputting the second voltage to outputting the
10 first voltage to create a second pulse.

70. The control circuit and sense amplifier of claim 68, wherein the control circuit and sense amplifier combination determines whether the memory cell successfully
15 programmed by reading the memory cell to confirm whether the memory cell successfully programmed.

71. The control circuit and sense amplifier combination of claim 66, wherein after the first line connection is
20 switched from outputting the first voltage to output the second voltage and from outputting the second voltage to output the first voltage, the control circuit and sense amplifier combination determines whether a memory cell successfully programmed.

25

72. The control circuit and sense amplifier combination of claim 71, wherein the control circuit and sense amplifier combination switches the first line connection from outputting the first voltage to output the second
30 voltage and from outputting the second voltage to output the first voltage to create a third pulse.

73. The control circuit and sense amplifier combination of claim 72, wherein the control circuit and sense amplifier combination switches the first line connection from outputting the first voltage to output the second
5 voltage and from outputting the second voltage to outputting the first voltage to create the second pulse before the control circuit and sense amplifier combination switches the first line output from outputting the first voltage to output the second voltage and from outputting
10 the second voltage to output the first voltage to create the third pulse.

74. The control circuit and sense amplifier combination of claim 65, wherein the first line connection includes a
15 word line connection and the second line connection includes a bit line connection.

75. The control circuit and sense amplifier combination of claim 65, wherein the first voltage is higher than the
20 second voltage.

76. The control circuit and sense amplifier combination of claim 65, wherein the switching from the first voltage to the second voltage comprises a VT drop.
25

77. The control circuit and sense amplifier combination of claim 65, wherein the control circuit and sense amplifier comprises a dedicated regulator.

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78. The control circuit and sense amplifier combination of claim 65, wherein the control circuit and sense amplifier includes:

- 5 a diode connected NMOS device; and
- a bypass path.

79. The control circuit and sense amplifier combination of claim 65, wherein the control circuit and sense amplifier is configured to detect whether the memory cell
10 has successfully programmed, wherein the first line connection is switched to output the first voltage in response to the control circuit and sense amplifier combination detecting that a memory cell has successfully
programmed.

15

80. The control circuit and sense amplifier combination of claim 79, wherein, after the control circuit and sense amplifier combination switches the first line connection from outputting the first voltage to outputting the second
20 voltage and from outputting the second voltage to output the first voltage, the control circuit and sense amplifier combination determines whether to again switch the first line connection from outputting the first voltage to output the second voltage and from outputting the second voltage
25 to output the first voltage to create a second pulse.

81. The control circuit and sense amplifier combination of claim 80, wherein the control circuit and sense amplifier combination switches the first line connection
30 from outputting the first voltage to output the second voltage and from outputting the second voltage to output the first voltage to create the second pulse.

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82. The control circuit and sense amplifier combination of claim 79, wherein the control circuit and sense amplifier combination determines that the memory cell has been successfully programmed by detecting when a sense
5 amplifier voltage switches voltage.

83. A memory array including a two terminal memory cell, comprising:

the memory cell;
10 a first line connected to the memory cell being set to a first voltage from a first line standby voltage; and
a second line connected to the memory cell being charged to a predetermined voltage from a second line standby voltage;
15 wherein the first line is switched from the first voltage to a second voltage,
wherein the first line is then switched from the second voltage to the first voltage,
wherein a difference between the first voltage and
20 the predetermined voltage results in a safe voltage that does not program the memory cell,
wherein a difference between the second voltage and the predetermined voltage results in a programming voltage operative to program the memory cell, and
25 wherein the switching of the first line to the second voltage and the switching of the first line to the first voltage together create a first pulse.

84. The memory array of claim 83, wherein, after the
30 first line is switched from the first voltage to the second voltage and from the second voltage to the first voltage, a control circuit determines whether the first line is again

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switched from the first voltage to the second voltage and from the second voltage to the first voltage to create a second pulse.

5 85. The memory array of claim 84, wherein the first line is switched from the first voltage to the second voltage and from the second voltage to the first voltage to create the second pulse.

10 86. The memory array of claim 83, wherein, after the first line is switched from the first voltage to the second voltage and from the second voltage to the first voltage, a sense amplifier determines whether the memory cell successfully programmed.

15 87. The memory array of claim 86, wherein the first line is switched from the first voltage to the second voltage and from the second voltage to the first voltage to create a second pulse.

20 88. The memory array of claim 86, wherein sense amplifier determines whether the memory cell successfully programmed by reading the memory cell to confirm whether the memory cell successfully programmed.

25 89. The memory array of claim 85, wherein, after the first line is switched from the first voltage to the second voltage and from the second voltage to the first voltage, a sense amplifier determines whether the memory cell
30 successfully programmed.

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90. The memory array of claim 89, wherein the first line is switched from the first voltage to the second voltage and from the second voltage to the first voltage to create a third pulse.

5

91. The memory array of claim 90, wherein the first line is switched from the first voltage to the second voltage and from the second voltage to the first voltage to create the second pulse before the first line is switched from the first voltage to the second voltage and from the second voltage to the first voltage to create a third pulse.

10

92. The memory array of claim 83, wherein the first line includes a word line and the second line includes a bit line.

15

93. The memory array of claim 83, wherein the first voltage is higher than the second voltage.

20

94. The memory array of claim 83, wherein the switching from the first voltage to the second voltage comprises a VT drop.

95. The memory array of claim 83, further comprising a control circuit including a dedicated regulator.

25

96. The memory array of claim 83, further comprising a control circuit, wherein the control circuit includes:
a diode connected NMOS device; and
a bypass path.

30

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97. The memory array of claim 83, wherein a sense amplifier is configured to detect whether the memory cell has successfully programmed, wherein the first line is switched from the second voltage to the first voltage in response to the sense amplifier detecting that the memory cell has successfully programmed.

98. The memory array of claim 97, wherein after the first line is switched from the first voltage to the second voltage and from the second voltage to the first voltage, the first line is switched from the first voltage to the second voltage and from the second voltage to the first voltage to create a second pulse.

99. The memory array of claim 97, wherein the sense amplifier is configured to determine whether the memory cell has successfully programmed by detecting when a sense amplifier voltage switches voltage.

100. The memory array of claim 83, wherein the second line is longer than the first line.

101. The memory array of claim 83, wherein the memory cell comprises chalcogenide.

102. A memory array including a two terminal memory cell, comprising:
the memory cell;
a first line connected to the memory cell;
a first line driver connected to the first line;
a first line select configured to control the first line driver;

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a control circuit selectively connected to the first line through the first line driver when the first line select is enabled, the control circuit configured to set the first line to a first voltage from a first line standby voltage;

a second line connected to the memory cell;
a second line driver connected to the second line;
a second line select configured to control the second line driver; and

a sense amplifier selectively connected to the second line through the second line driver when the second line select is enabled, the sense amplifier configured to charge the second line to a predetermined voltage from a second line standby voltage,

wherein the control circuit switches the first line from the first voltage to a second voltage,

wherein the control circuit then switches the first line from the second voltage to the first voltage,

wherein a difference between the first voltage and the predetermined voltage results in a safe voltage that does not program the memory cell,

wherein a difference between the second voltage and the predetermined voltage results in a programming voltage operative to program the memory cell, and

wherein the switching the first line from the first voltage to the second voltage and from the second voltage to the first voltage together create a first pulse.

103. The memory array of claim 102, wherein the second line is longer than the first line.

104. The memory array of claim 102, wherein the memory cell comprises chalcogenide.

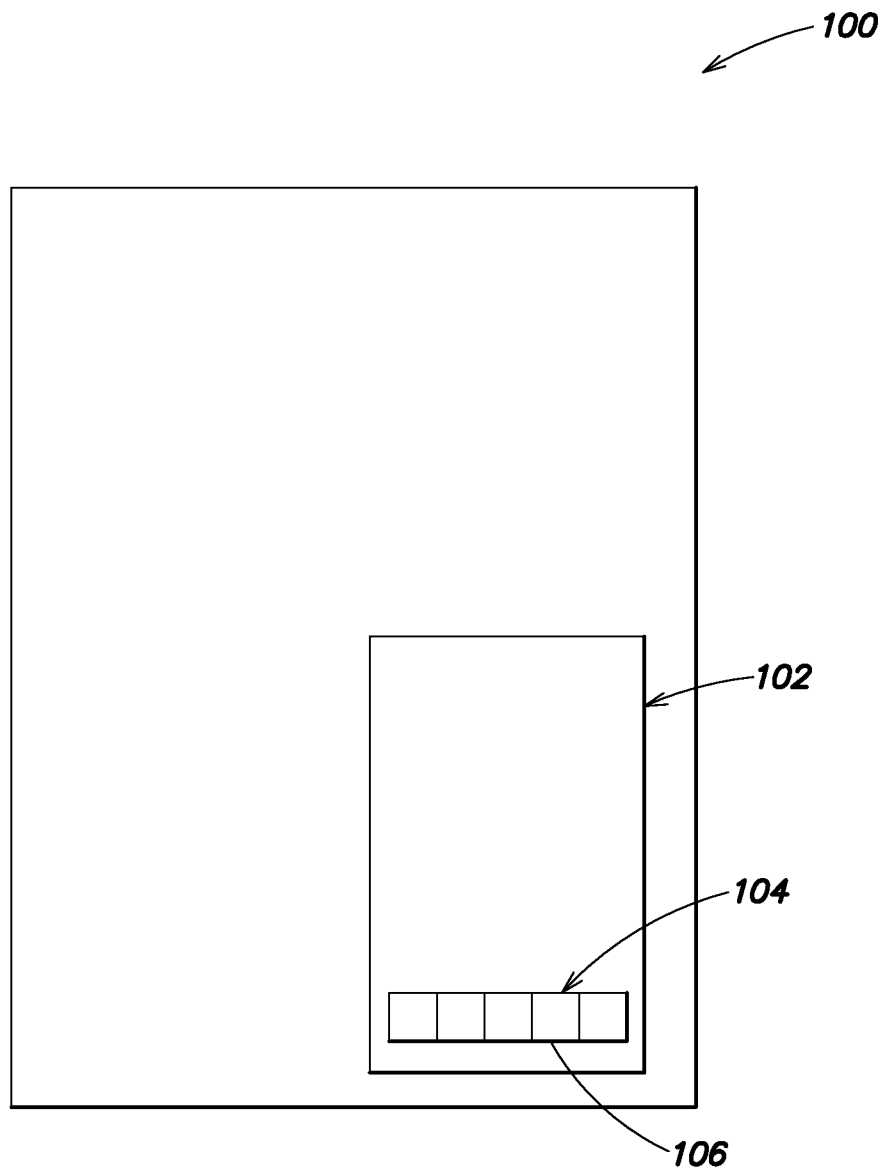
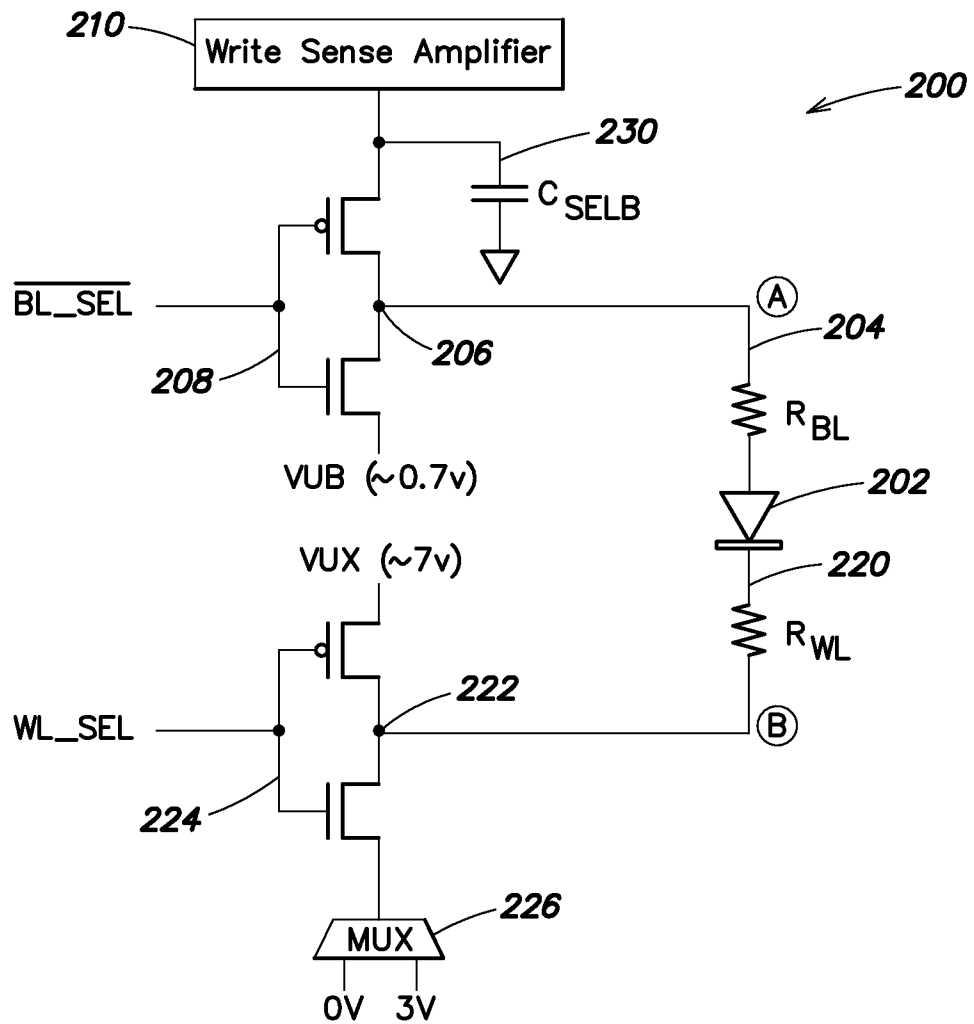
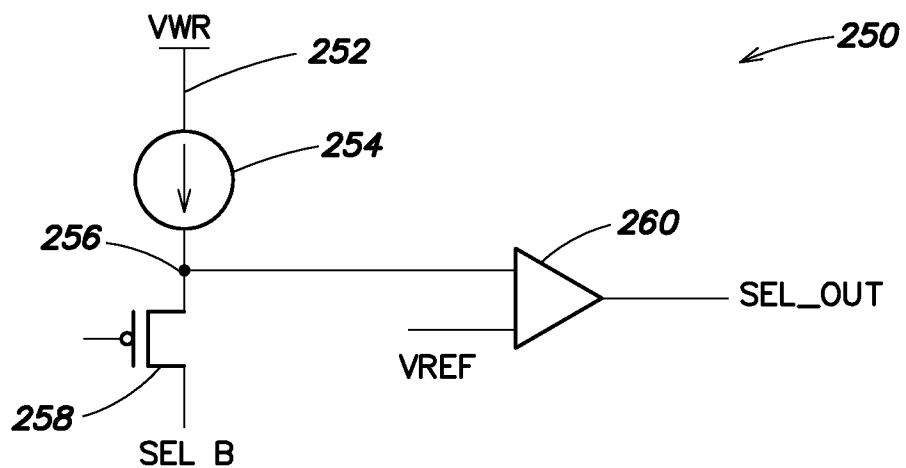
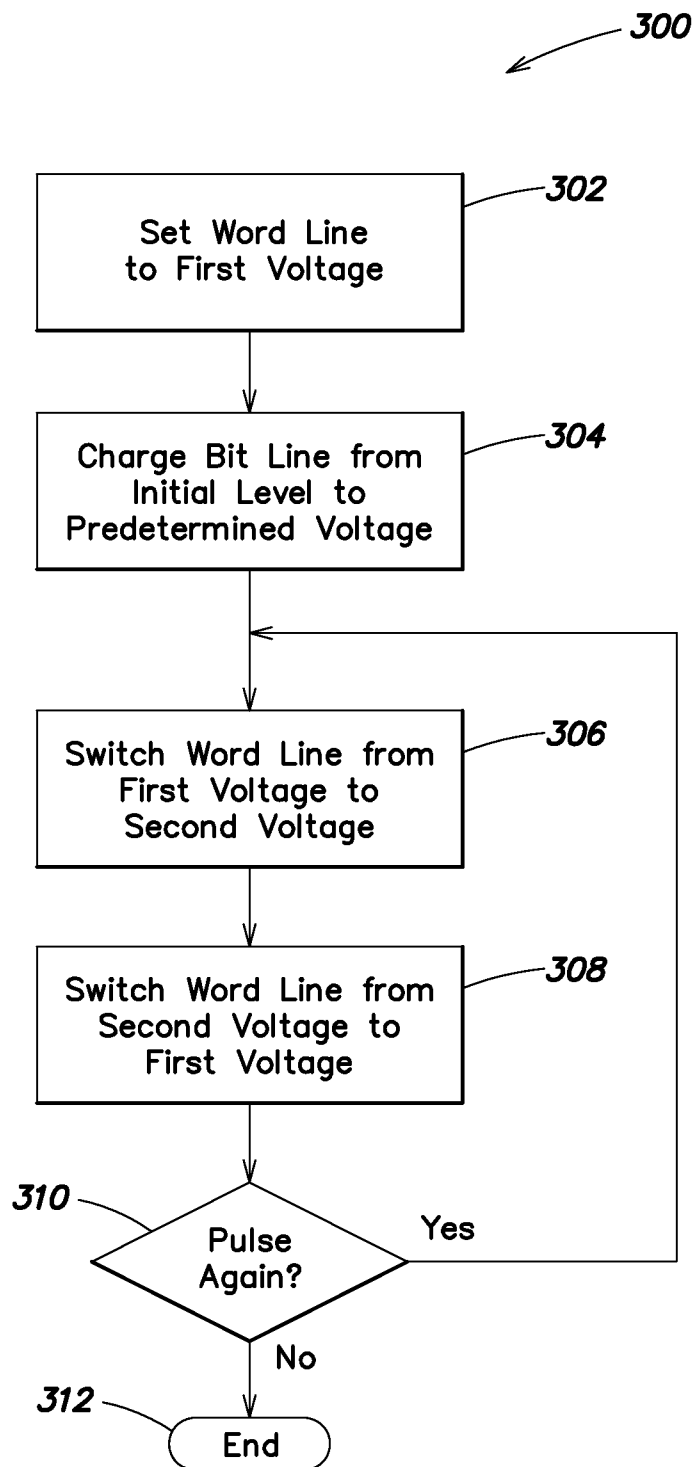
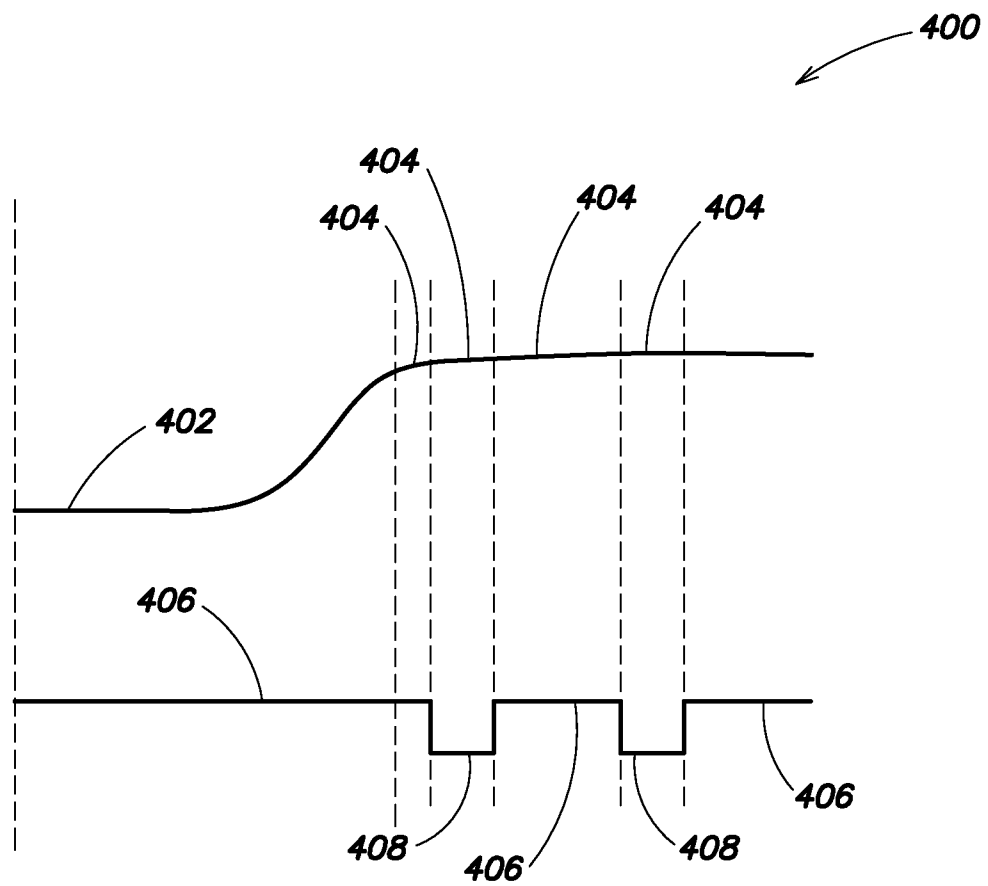
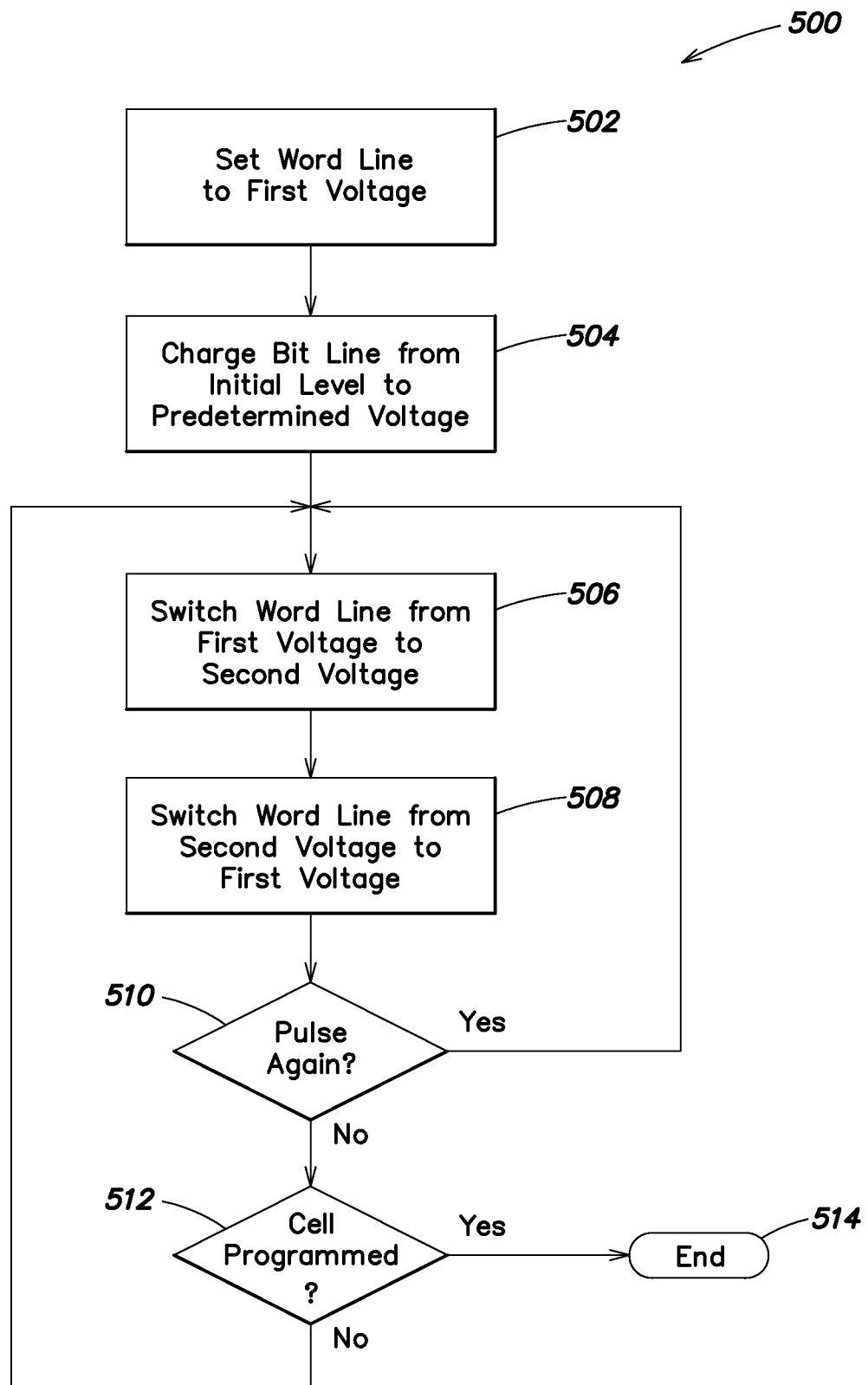


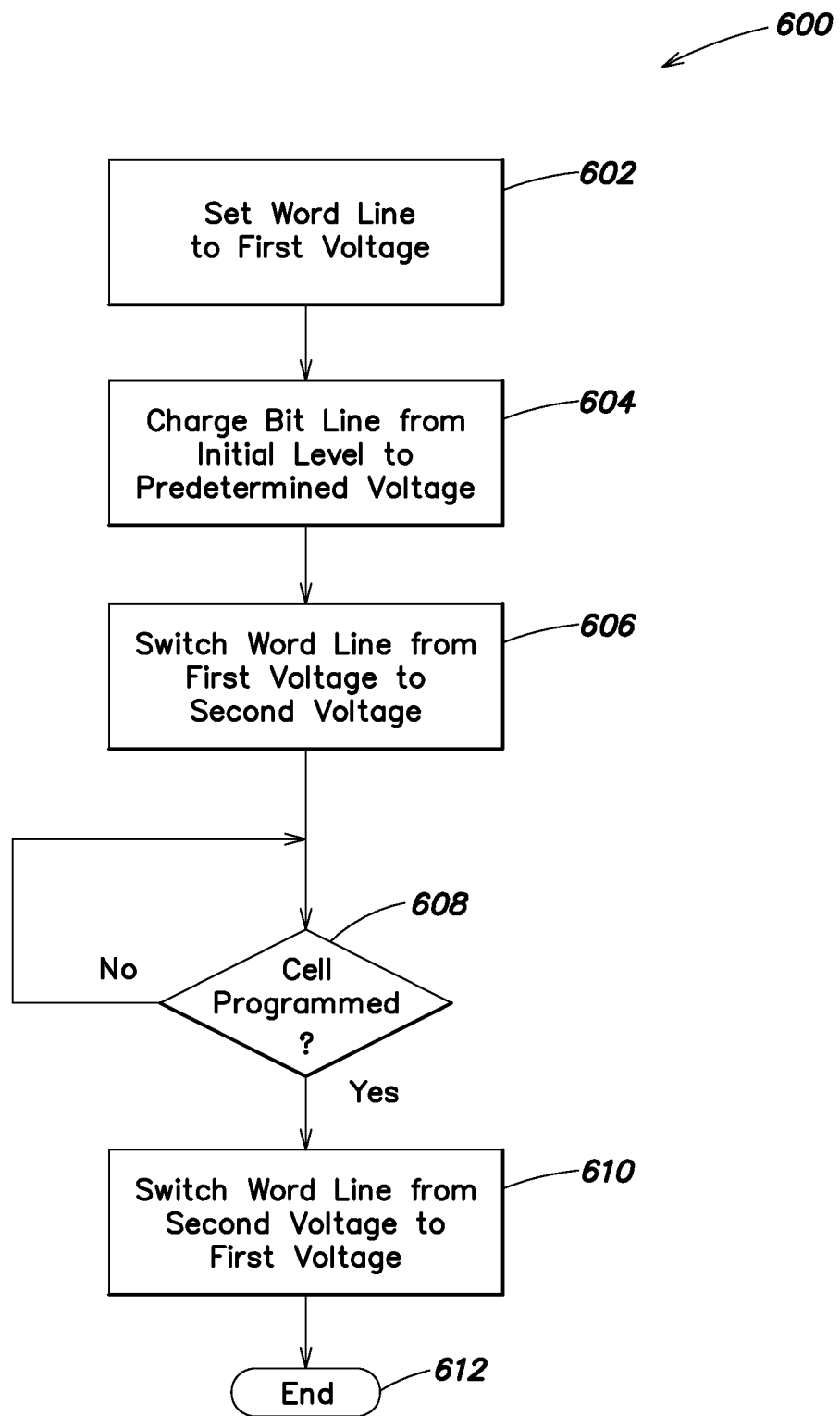
FIG. 1

**FIG. 2A****FIG. 2B**

**FIG. 3**

**FIG. 4**

**FIG. 5**

**FIG. 6**

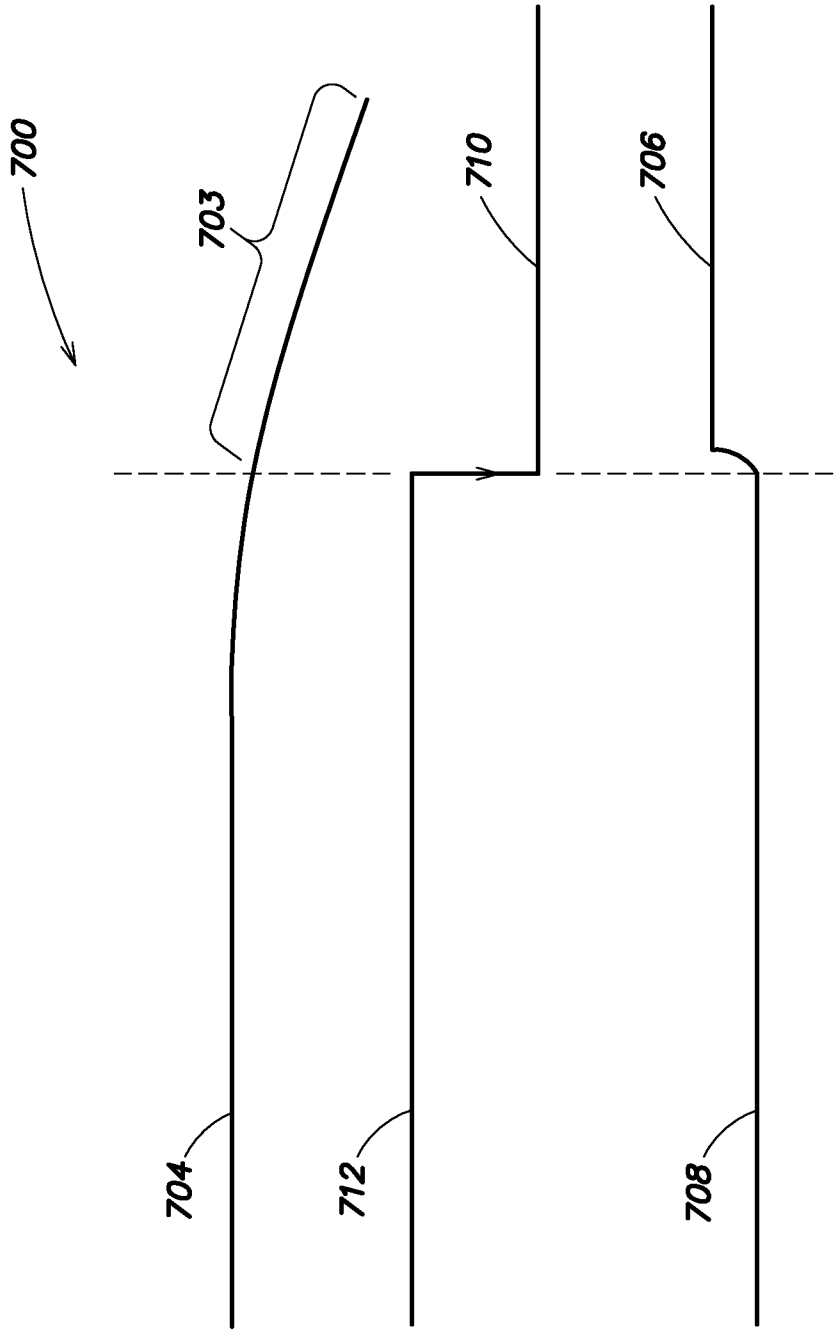


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2010/045684

A. CLASSIFICATION OF SUBJECT MATTER
INV. G11C13/02 G11C16/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, COMPENDEX, INSPEC, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009/052227 A1 (EDAHIRO TOSHIAKI [JP] ET AL) 26 February 2009 (2009-02-26)	1,10,11, 13,14, 24,33, 34,36, 37,47, 56,57, 59,60, 65, 74-77, 83, 92-95, 100-104
Y	figures 1, 6-7,8, 10 ----- -/-	2-9, 25-32, 48-55, 66-73, 84-91

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

5 November 2010

Date of mailing of the international search report

31/01/2011

Name and mailing address of the ISA/

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/045684

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-11, 13, 14, 24-34, 36, 37, 47-57, 59, 60, 65-77, 83-95, 100-104

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2010/045684

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 545 898 B1 (SCHEUERLEIN ROY E [US]) 8 April 2003 (2003-04-08)	1,10,65, 74,77, 83,92, 95,100, 101
Y	figures 4,8	2-9, 66-73, 84-91
Y	----- US 2006/166455 A1 (GORDON GEORGE [US] ET AL) 27 July 2006 (2006-07-27)	2,3,25, 26,48, 49,66, 67,84,85
Y	----- US 2009/207647 A1 (MAEJIMA HIROSHI [JP] ET AL) 20 August 2009 (2009-08-20)	2-9, 25-32, 48-55, 66-73, 84-91
Y	----- WO 2008/013619 A2 (CSWITCH CORP [US]; CHAN VEI-HAN [US]; KORDUS LOUIS C II [US]; DERHACOB) 31 January 2008 (2008-01-31)	2-9, 25-32, 48-55, 66-73, 84-91
	figure 11 -----	

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2010/045684

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2009052227 A1	26-02-2009	JP 4410272 B2 JP 2008282499 A	03-02-2010 20-11-2008
US 6545898 B1	08-04-2003	NONE	
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US 2009207647 A1	20-08-2009	JP 2009193629 A	27-08-2009
WO 2008013619 A2	31-01-2008	US 2008025080 A1	31-01-2008

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-11, 13, 14, 24-34, 36, 37, 47-57, 59, 60, 65-77, 83-95, 100-104

Fast programming pulse with the application of further programming pulses in response to the determination that other programming pulses are required

2. claims: 12, 35, 58, 78, 96

Fast programming pulse with diode connected NMOS device providing the first voltage and a bypass path providing, when selected, the second programming voltage

3. claims: 15-23, 38-46, 61-64, 79-82, 97-99

Fast programming pulse with verifying while programming
