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[54] SEQUENTIAL GATING CIRCUIT 5 Claims, 3 Drawing Figs.

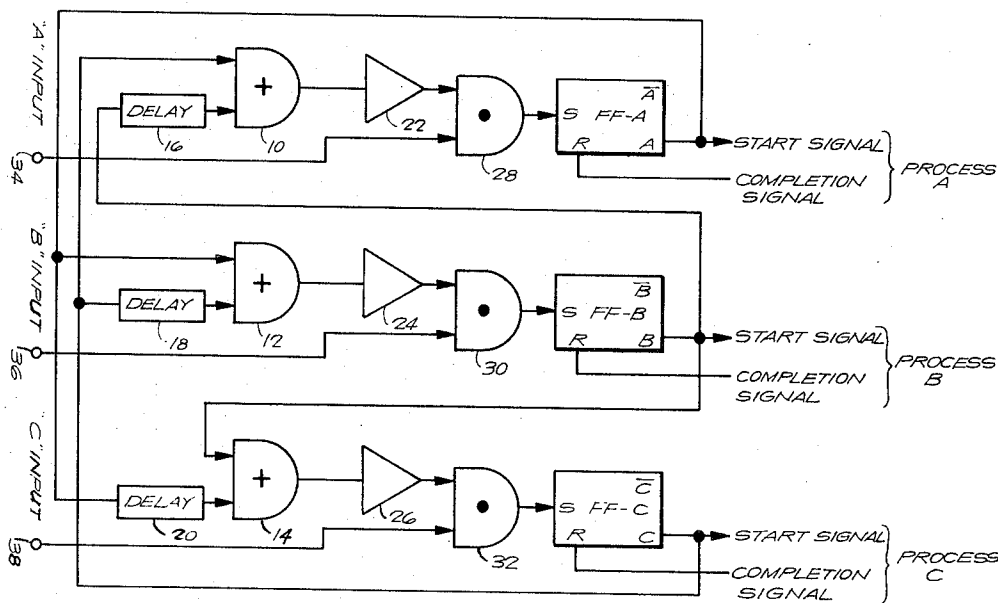
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 340/146.2
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 152, 75; 307/217, 218, 242, 247; 340/146.2

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ABSTRACT: A gating circuit for sequentially initiating a plurality of different processes or events in accordance with a predetermined preferential sequence of activation. A plurality of gates are provided, each of which receives an independent input signal for initiating the corresponding process or event. The output signal of each gate circuit is fed back to all of the other gate circuits as an inhibiting signal to prevent any two of the gates from being activated at the same time. The inhibiting signals are applied to the other gates through a plurality of different delay lines which establish a preferential time sequence of gate activation. When one gate has been activated, it inhibits all of the other gates until the corresponding process or event has been completed, at which time the inhibiting signal to the other gates is removed. Due to the difference in delay time, however, the removal of the inhibiting signal occurs in a time sequence which establishes a preferential sequence of gate activation for the remaining gates.



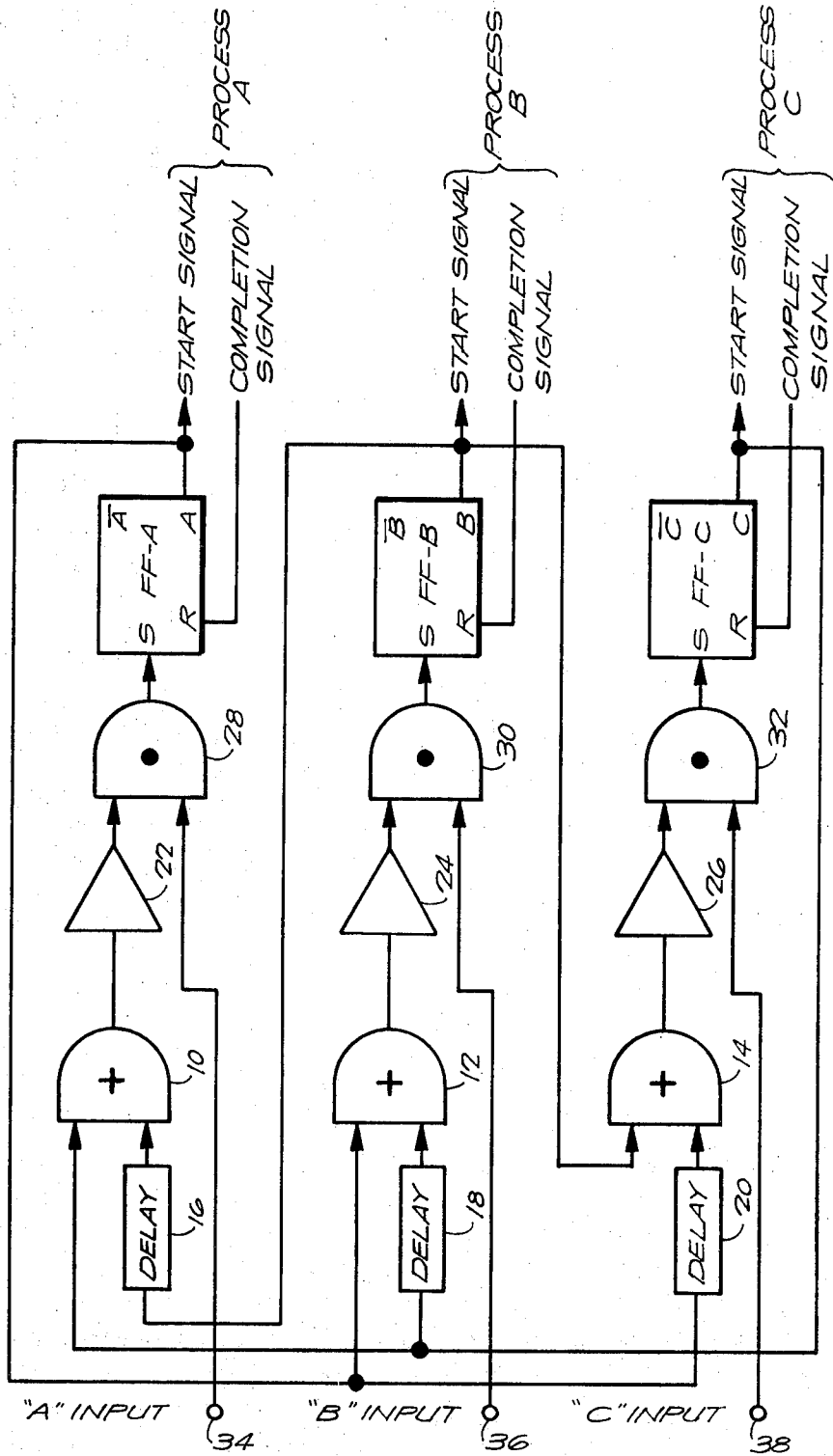


FIG 1

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[Signature]

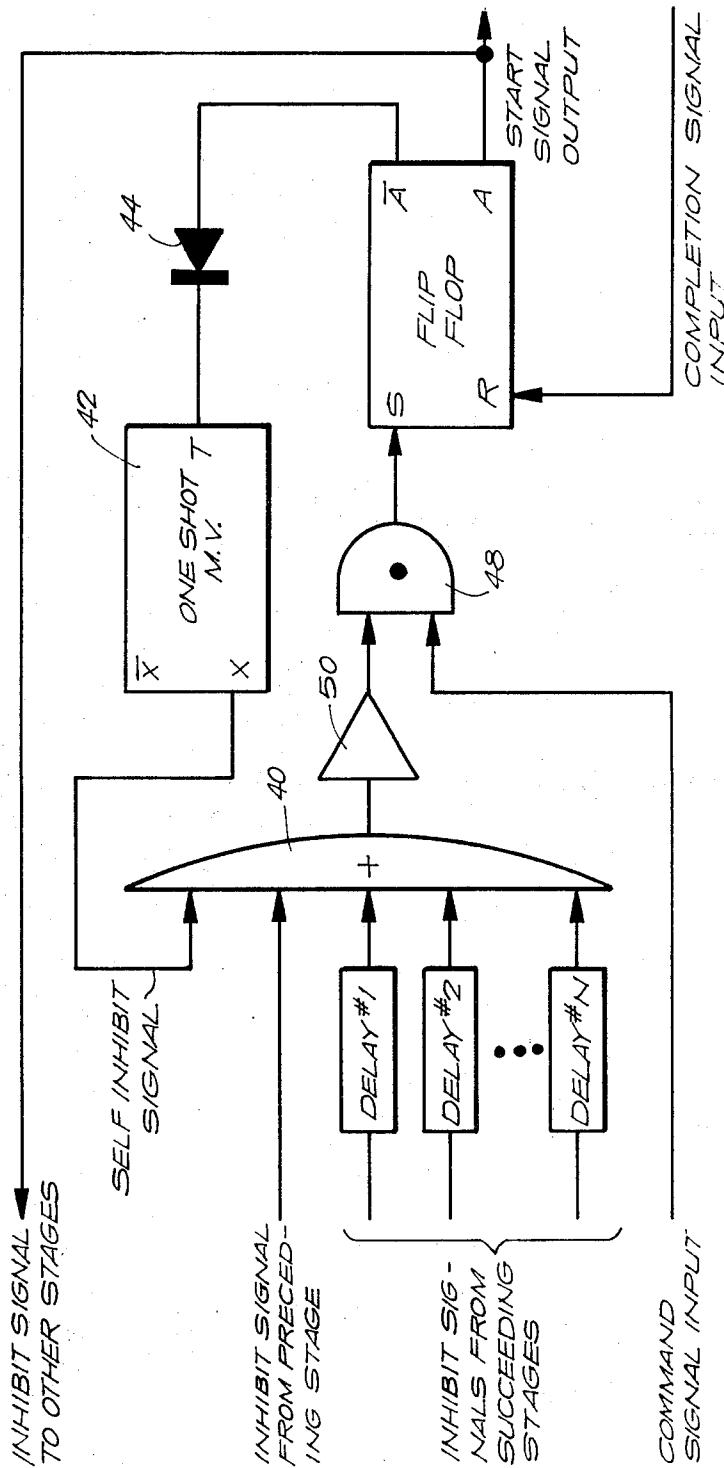


FIG 2

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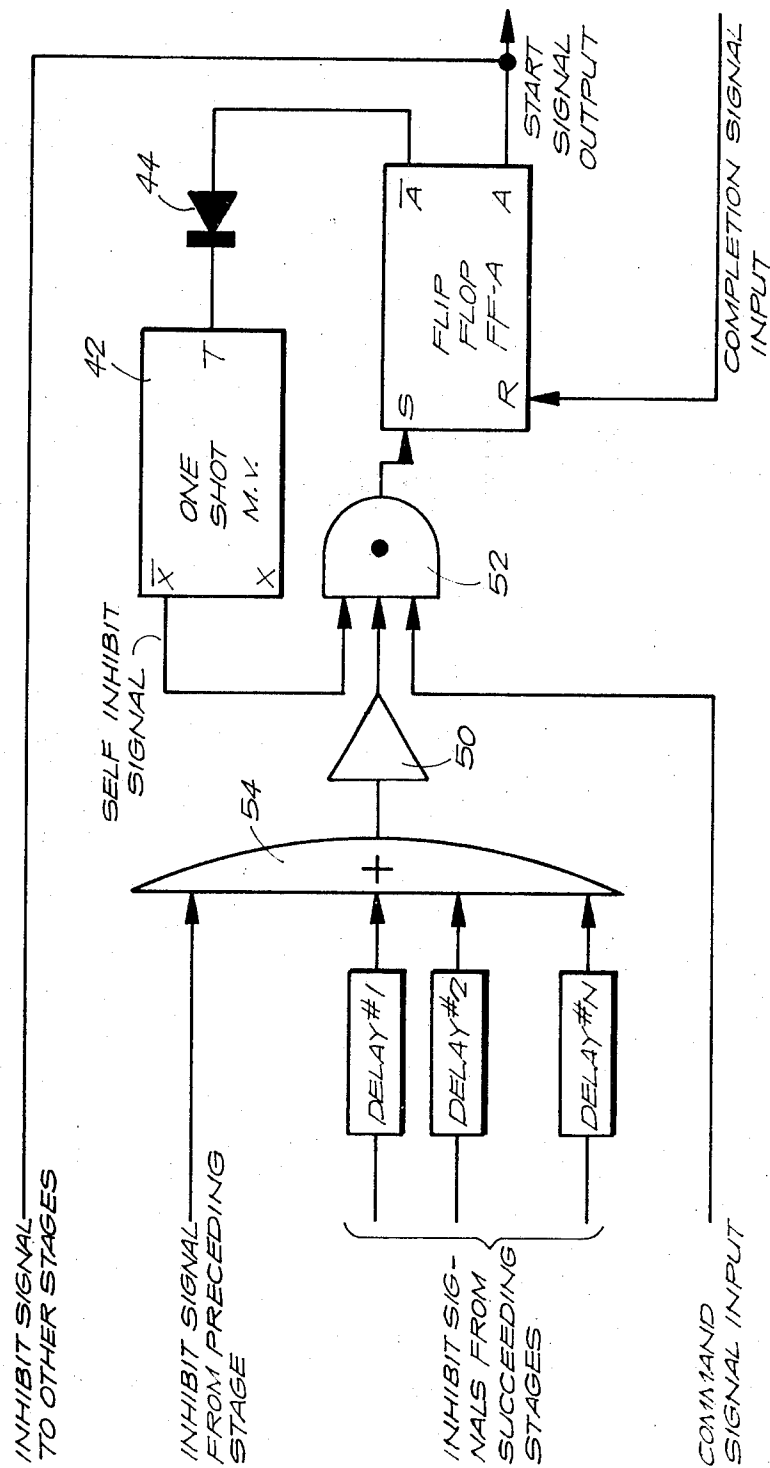


Fig 3

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SEQUENTIAL GATING CIRCUIT

BACKGROUND OF THE INVENTION

Sequential gating circuits have been used in the past to sequentially activate many different types of processes or events in which a predetermined sequence must be followed. In most cases, however, these prior art sequential gating circuits have used ring counters or shift registers to define the preferential sequence, and this has limited the performance of these prior art circuits because it is not possible to advance a ring counter or shift register from one state to a nonadjacent state without passing through the intervening states. In other words, if the sequence A, B, C, D is defined by a ring counter or shift register, it is not possible to advance from the state A to state D without first passing through states B and C. Since passing through operational states unnecessarily can involve substantial waste of time and money in many sequential processes, it is, therefore, highly desirable to provide a sequential gating circuit which has the capability of advancing directly from one state to a nonadjacent state when it is desirable to do so without altering the normal sequence of states. The principal object of this invention is to provide a sequential gating circuit which has the above-noted capability. In addition, these prior art sequential gating circuits were relatively complex in structure, and it is an additional object of this invention to provide a sequential gating circuit which is simpler than those heretofore known in the art.

SUMMARY OF THE INVENTION

In accordance with this invention, the above-noted objects are achieved by using a plurality of different delay lines as a means of establishing the preferential sequence of gate activation. Each gate, when it is activated, applies inhibiting signals to all of the other gates to prevent two gates from being activated at the same time. The inhibiting signals, however, are applied to the other gate circuits through a plurality of delay lines, with a different delay line being used for each gate. Therefore, when the activated gate is deactivated, the inhibiting signals will be removed from the other gates in a time sequence which is dependent on the difference of delay times. This establishes a preferential sequence of gate activation in such a way that the sequence can be moved from one state to a nonadjacent state without activating the intervening states and yet without disturbing the normal sequence of states. In addition, the delay line circuit is much simpler than the ring counters and shift registers that have been used in the past.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of one illustrative gating circuit of this invention for establishing a preferential sequence of activation for three different processes.

FIG. 2 is a block diagram of a generalized gating circuit of this invention which is adapted for use in connection with $N \pm 2$ different processes.

FIG. 3 is a block diagram of a second generalized gate circuit of this invention which is adapted for use in connection with $N+2$ different processes.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 shows one illustrative embodiment of the invention for assigning a predetermined preferential sequence of activation to three processes which are designated by the letters A, B and C. In this embodiment of the invention, three flip-flops FF-A, FF-B, and FF-C are provided as control elements for their respective processes. When any one of these flip-flops is switched to its "set" state by an input signal applied to its S terminal, a "start" signal will be applied to the control circuitry for the corresponding process, which will then be activated until it is completed, at which time the corresponding flip-flop will be reset by a "completion" signal from the corresponding process control circuitry. The "start" signal or each process is also applied to the input of the other gate cir-

cuits as an inhibiting signal to prevent any two of the processes from being activated at the same time. The inhibiting signals are applied to OR-gates 10, 12, and 14 either directly or through delay lines 16, 18, and 20, which establish a preferential sequence of gate activation. The output of OR-gates 10, 12, and 14 are applied through inverting amplifiers 22, 24, and 26 to one input of AND-gates 28, 30, and 32 to inhibit the AND gates when any one of the inhibiting signals is present. The command input signals for activating the three processes in question are applied to the other input terminals of AND-gates 28, 30, and 32. Command input signals applied to terminals 34, 36, and 38 will pass through their corresponding AND gate and "set" the corresponding flip-flop if no inhibiting signals are present on the other input of the AND gate but they will be blocked when the corresponding AND gate is inhibited by an inhibiting signal on its other input terminal. The detailed operation of this circuit can be best explained by tracing through several illustrative operating cycles thereof.

Let us assume for purposes of explanation that the above-described gating circuit is in its initial condition with all of the flip-flops reset and no input signals applied. Under these conditions, an input signal on any one of the three input terminals 34, 36, or 38 will pass directly through the corresponding AND-gates 28, 30, or 32 and trigger the corresponding flip-flop. Thus, in the initial condition, any one of the three input signals will immediately activate the corresponding process without any regard to its position in the sequence. For purposes of explanation, let us assume that an input signal occurs first on the B input terminal 36. This signal would pass through AND-gate 30 and trigger flip-flop FF-B to its "set" condition to initiate the process B. When flip-flop FF-B switches to its "set" condition, a "start" signal is applied to the control circuitry for process B and simultaneously an inhibiting signal is applied to the other two gates to prevent processes A or C from being initiated until process B has been completed. The inhibiting signal for the next process in the sequence (process C) is applied directly to OR-gate 14, but the inhibiting signal for the next preceding process in the sequence (process A) is applied through delay line 16 to OR-gate 10. The delay line establishes a preferential sequence of gate activation for the other two gates after process B has been completed.

After the process B has been initiated, input signals to the A- and C-input terminals will be ineffective until the B process has been completed. When the B-process has been completed, flip-flop FF-B will be reset by a "completion" signal received from the process B control circuitry, and at this time, the inhibiting signals will be removed from the other two gate circuits. Due to the use of the delay lines, however, the inhibiting signals will be removed in a preferential time sequence rather than being removed at the same time. The inhibiting signal on the succeeding stage in the sequence (process C) will be removed immediately but the inhibiting signal on the preceding stage in the sequence (process A) will be delayed by the amount of time set in time delay circuit 16. Therefore, if the A- and C-stages are both triggered by an input signal when the B-process is completed, the C-process will be activated first in preference to the A-process due to the preferential delay in the removal of the inhibiting signal. In this case, as soon as the C-process is initiated, a new inhibiting signal will be applied directly to the A-stage through OR-gate 10 to hold the A-process inhibited until the C-process has been completed. In this manner, a preferential sequence of activation ABC is established by the delay lines after one of the stages has been initially activated.

Since the preferential sequence of this invention is established by means of a delay circuit rather than by a ring counter or shift register, the circuit can move from one stage to a nonadjacent stage without switching through the intervening stages. For example, assume that it is desired to activate processes A and C but not the intervening process B. After the process A has been completed, the next process in the preferential sequence would normally be process B, but if no input signal is applied to the B-input terminal 36, the circuit

will move directly to the C-process after a short delay interval without any switching of the B-process.

In the case of three processes to be controlled, it is only necessary to have one delayed input for each of the gates. When more than three processes are involved, however, it is necessary to add an additional delayed input for each additional process, with each additional delay being longer than the others. FIGS. 2 and 3 show two different generalized gate circuits which can be used for applications involving $N+2$ different processes. Referring to FIG. 2, a sequence of delay lines No. 1 through No. N are provided at the input to OR-gate 40, which also receives one undelayed inhibit signal and a self-inhibit signal. The undelayed input signal to OR-gate 40 is applied from the preceding stage in the sequence and the delayed inputs are applied from the succeeding stages in the sequence in order, with the next stage in the sequence being applied to delay No. 1, and the stage after that being applied to delay No. 2, and so on to delay No. N. Each of the delays is longer than the preceding delays in numerical sequence. The gate circuits shown in FIGS. 2 and 3 also include an additional self-inhibiting signal which is applied to OR-gate 40 from a one-shot multivibrator 42 to prevent the corresponding process from being reactivated after it has been completed for a delay time which is greater than the longest delay for all of the other stages. This ensures that the other processes in the sequence will all have an opportunity to be initiated next before any one of the processes are reactivated. The input to one-shot multivibrator 42 is applied through a diode 44 which prevents the self-inhibit signal from being generated when the flip-flop FF-A is triggered to its "set" state. The diode 44 only passes positive going transitions to the trigger terminal of one-shot multivibrator 42, which means that one-shot multivibrator 42 will only be triggered when the flip-flop FF-A is reset by a "completion" signal input after the corresponding process has been completed. The remaining portions of the gate circuit are similar to those disclosed in FIG. 1, with a two input AND-gate 48 being used for the input to the S-terminal of flip-flop FF-A and an inverting amplifier 50 being used to invert the output of OR-gate 40.

The circuit of FIG. 3 is identical to the circuit of FIG. 2 except that the self-inhibit signal is applied to a three input AND-gate 52 instead of being applied to the OR-gate 54, which has one input terminal fewer than the OR-gate 40 shown in FIG. 2. The basic operation of the circuit is not, however, altered by this slight difference in circuit configuration.

The exact delay times chosen for the delay lines No. 1 through No. N and for the one-shot multivibrator 42 will depend upon the specific components employed in the gate circuit and on the switching requirements of the particular processes involved. In general, terms, however, the time difference between the various delay lines should be larger than the switching time for the flip-flops to insure that the next inhibiting signal will be applied to the out-of-sequence gates before the previous inhibit signal is removed to prevent two gates from being activated at the same time. In other words, in the sequence ABC, if input signals are applied to both gates A and C when gate B is deactivated, it is necessary for the inhibit signal from gate C to be applied to gate A before the delayed inhibit signal from gate B is removed therefrom. This requires that the difference of time delay between stages A and C must be greater than the time required for flip-flop C to switch from its "reset" to its "set" state. In most cases, this lower limit of time difference will be so small as to present no problem, but it will have to be taken into account in applications which utilize relatively slow relay flip-flops instead of high-speed transistorized flip-flops. The upper limit of the time difference depends upon the switching requirements of the processes involved and upon the total delay that can be tolerated between the deactivation of one process and the activation of the next process. This presents no problem when all of the processes are activated in sequence, since there is no time delay between any one gate and the next gate in the preferential sequence, but when some of the gates are skipped and delay time must

be taken into account. In general terms, the time delay of the longest delay line should be shorter than the maximum switching delay that can be tolerated when the processes are triggered by random input signals.

With regard to the detailed structure of the gate circuit, any suitable circuit components can be used which perform the desired gating functions. The AND gates and OR gates can be diode gates or transistor gates or any other type of gate that fits the requirements of a particular application. In this connection it should be noted that NOR gates could be used in place of the OR gates if desired or that NAND gates could be used in place of the AND gates. Either of these two modifications would have the advantage of incorporating the inverter circuits into the gate circuitry and thus would be desirable in applications that utilize transistor gates. It should also be noted that the flip-flops, or equivalent control elements, will be a part of the process control circuitry in many applications, and therefore it should be understood that these elements are not essential to the basic operation of the invention. In some applications of the invention, the output signal of the AND gates will serve as the "start" signal for the corresponding process or event and the inhibit signals will be fed back to the other gates from the process control circuitry. These and many other modifications of the disclosed circuits will be apparent to those skilled in the art and it should be understood that this invention includes all modifications falling within the scope of the following claims.

We claim:

1. A gating circuit for sequentially initiating a plurality of different processes or events in accordance with a predetermined preferential time sequence, comprising: a plurality of AND gates each having one output and at least two inputs, means for coupling the output of each AND gate to the control means of a corresponding one of said processes for initiating the process, means coupled to a first input of each AND gate for receiving an input signal to activate the corresponding AND gate, and feedback means coupled between the output of each AND gate and a second input of all of the other AND gates, said feedback means being operable when any one of the AND gates is activated to apply inhibiting signals to all of the remaining AND gates to prevent any two of the gates from being activated at the same time, each of said inhibiting signals being applied through time delay means for establishing a predetermined time sequence with respect to the termination of the inhibiting signals, each of said time delay means delaying inhibiting signals passing therethrough for an increment of time differing from that of all other said time delay means thereby establishing a predetermined preferential time sequence of initiation for the corresponding processes or events.

2. A gating circuit as defined in claim 1 wherein said feedback means includes a plurality of multiple-input OR gates each having one output and a plurality of inputs, the output of each OR gate being coupled to said second input of a corresponding one of said AND gates, means coupling each of said OR gate inputs to the output of a different one of said AND gates, said time delay means each coupled in series with a different input of said OR gates for establishing a predetermined time sequence with respect to the termination of signals applied to the inputs of said OR gates, thereby establishing a predetermined preferential time sequence of activation for the corresponding process or events.

3. A gating circuit as defined in claim 2 and also including a plurality of flip-flops each having a "set" input and a "reset" input and at least one output, the "set" input of each flip-flop being coupled to the output of a corresponding one of said AND gates, the output of each of said flip-flops being coupled to the control means of a corresponding one of said processes for initiating the process, means coupled to the "reset" input of each flip-flop for resetting the flip-flop when the corresponding process has been completed and said feedback means being coupled to the output of each of said flip-flops.

5

4. A gating circuit as defined in claim 3 and also including a plurality of one-shot multivibrators each having an input and at least one output, each of said one-shot multivibrators being operable when triggered by an input signal to produce an output signal having a time duration which is longer than the longest of said time delay circuits, the input of each one-shot multivibrator being coupled to the output of a corresponding one of said flip-flops, and the output of each one-shot multivibrator

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tor being coupled to one input of the corresponding AND gate to inhibit said AND gate for a time delay which is longer than the delay time of the longest of said time delay circuits after the corresponding flip-flop has been reset.

5. A gating circuit as defined in claim 4 wherein the output of each one-shot multivibrator is coupled to the input of the corresponding AND gate via the corresponding OR gate.

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