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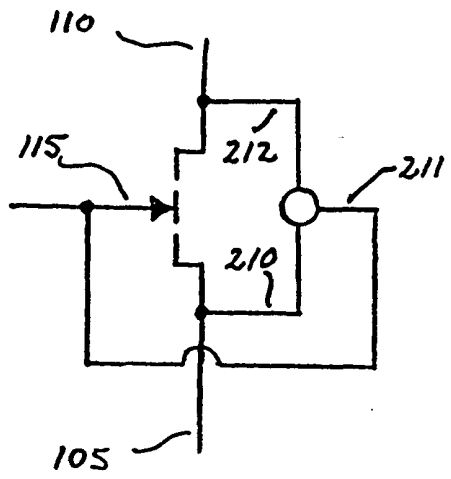

(57) Abstract: A semiconductor switching device or amplifier combined in parallel with one or more active devices defined as starter devices. A starter device is used to reduce the terminal voltage of a switching device or amplifier to a dc level below about 0.4 volts which will then allow the switching device to easily change between the on or conducting state and the off or non-conducting state. Three different starter devices are utilized. The first being a Bipolar Junction Transistor (BJT), the second a Metal Oxide Silicon Field Effect Transistor (MOSFET), and the third consisting of three normally off JFETs connected serially. Generally, a single starter device is coupled across the terminals of a semiconductor switching device or amplifier, but it is possible and sometimes advantageous to couple two or more starter devices in parallel. In a first case, a symmetrical, normally off or enhancement mode JFET is used as the switch or amplifier. A starter device coupled between source and drain of the JFET will allow operation at dc voltage levels above 0.4 volts. In a second case, an asymmetrical, normally off JFET is used as the switch or amplifier. A starter device coupled between source and drain of the JFET will allow operation at dc voltage levels above 0.4 volts. In a third case, a normally off MESFET is used as the switch or amplifier. A starter device coupled between source and drain of the MESFET will allow operation at dc voltage levels above 0.4 volts.

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STARTER DEVICE FOR NORMALLY OFF FETS

BACKGROUND

Related Applications

The following copending U.S. patent application Serial No. 091430,500, "NOVEL JFET STRUCTURE AND MANUFACTURE METHOD FOR LOW ON RESISTANCE AND *LOW VOLTAGE* APPLICATIONS", Ho-Yuan Yu, filed 2 December, 1999, is incorporated herein by reference for all purposes. The following copending U.S. provisional patent application Serial No. 60/167,959, "STARTER DEVICE FOR NORMALLY "OFF" JFETS", Ho-Yuan Yu, filed 29 November, 1999, is incorporated herein by reference for all purposes.

FIELD

The present disclosure relates generally to the field of active semiconductor devices. More specifically, the present disclosure relates to novel semiconductor device structures useful in low voltage and high current density applications. More particularly, the present disclosure relates to active semiconductor devices referred to as normally off Field Effect Transistors (FET), which specifically include Junction Field Effect Transistors (JFET) as well as Metal Semiconductor Field Effect Transistors (MESFET).

RELATED ART

The increasing trend toward lower supply voltages for active semiconductor devices and Integrated Circuits (IC's) has accelerated the search

for more efficient low voltage power sources. Conventional power supplies utilizing silicon diode rectifiers are unacceptable in low voltage applications due to the excessive voltage drop across the forward biased diode terminals. Power loss in the diodes becomes excessive when they are used as rectifiers in a direct current (dc) power supply designed for a terminal voltage as low as 3.0 volts.

Semiconductor diodes are combined with active devices to form circuits capable of producing low value dc supply voltages, but such circuits are generally not capable of handling the large currents frequently required. They usually exhibit a fairly large internal resistance and as such are very inefficient power sources. Furthermore, the number and complexity of steps required in the processing of this type of circuit as an IC also increases with the number of devices included.

Active semiconductor devices are used as switches in circuit arrangements producing dc power supply voltages, as for example in switched mode power supplies. Junction Field Effect Transistors (JFET) can be used as switches because they are easily switched between an on or conducting state and an off or non-conducting state. Most importantly, the current carriers in a JFET are all majority carriers which results in short switching times. However, when operated at lower voltages, JFETs exhibit an internal resistance in the on state that make them unsatisfactory and inefficient in applications requiring large currents.

In U.S. Patent 4,523,111 entitled "Normally-Off Gate-Controlled Electric Circuit with Low On-Resistance", Baliga disclosed a JFET serially connected to an Insulated Gate Field Effect Transistor (IGFET). The on resistance of this circuit is the sum of the JFET resistance and the IGFET resistance. As a result, the on resistance is too large and therefore unsatisfactory for low voltage operations requiring large currents.

In a similar invention disclosed in U.S. Patent 4,645,957 entitled "Normally Off Semiconductor Device with Low On-Resistance and Circuit Analogue" by Baliga, a JFET is serially connected to a Bipolar Junction Transistor (BJT). The on resistance is the sum of the JFET and the BJT which is again too large for low voltage applications requiring large currents.

The previously cited U.S. patent application Serial No. 09/430/500, "NOVEL JFET STRUCTURE AND MANUFACTURING METHOD FOR LOW ON RESISTANCE AND LOW VOLTAGE APPLICATIONS", Ho-Yuan Yu, filed December 2, 1999, discloses the basic structure for novel semiconductor devices useful for switching high level currents in ac circuit applications. These novel semiconductor devices have very low on resistance, and could be useful as switches in circuit arrangements producing dc power supply voltages, as for example in switched mode power supplies. Furthermore, the current carriers in these devices are all majority carriers which would result in short switching times. However, in dc circuit applications at voltage levels greater than

approximately 0.4 volts, the normally off JFET disclosed will not easily switch between an on or conducting state and an off or non-conducting state. The normally off JFET wil not easily used as an amplifier under dc bias above o.4 volts. Therefore a need of starter device to assist normally off JFET to be used as a switch or an amplifier under dc bias above 0.4 volt.

SUMMARY

Accordingly, what is needed is a semiconductor circuit that can efficiently supply the dc currents required in both discrete and integrated circuits being operated at low dc supply voltages. What is also needed is a semiconductor switching device or an amplifier that has a very low on or current conducting resistance. What is needed yet is a semiconductor switching device or an amplifier that can be easily switched between an on or current conducting state and an off or non-current conducting state with the smallest possible switching time. What is further needed is a circuit or method that will allow the use of a normally off FET in dc circuit applications at dc voltage levels greater than approximately 0.4 volts. The present invention provides these advantages and others not specifically mentioned above but described in the sections to follow.

A semiconductor switching device or an amplifier combined in parallel with one or more active devices defined as a starter device. A starter device is used to reduce the terminal voltage of a switching device to a dc level below about 0.4 volts which will then allow the switching device to transition between the on or conducting state and the off or non-conducting state. The starter device also allows normally off JFET to be used as an amplifier under dc bias greater than 0.4 volt. Three different starter devices are utilized. The first being a Bipolar Junction Transistor (BJT), the second a Metal Oxide Silicon Field Effect Transistor (MOSFET), and the third consisting of three normally off JFETs connected serially. In general, a single starter device is coupled with the

terminals of a semiconductor switching device, but it is possible and sometimes advantageous to couple two or more starter devices in parallel. In a first case, a symmetrical, normally off or enhancement mode JFET is used as the semiconductor switching device. One or more starter devices coupled between source and drain of the JFET will allow switching at dc voltage levels greater than 0.4 volts. In a second case, an asymmetrical, normally off JFET is used as the switching device. One or more starter devices coupled between source and drain of the JFET will allow switching at dc voltage levels greater than 0.4 volts. In a third case, a normally off MESFET is used as the switching device. One or more starter devices coupled between source and drain of the MESFET will allow switching at dc voltage levels greater than 0.4 volts.

More specifically, an embodiment of the present invention includes a symmetrical, enhancement mode JFET as the switching device or an amplifier device. In a first case, a BJT acting as the starter device is coupled between source and drain of the JFET. This BJT can be designed along with enhancement mode JFET or use the prasitic BJT of JFET as the starter device. In a second case, a normally off MOSFET acting as the starter device is coupled between source and drain of the JFET. In a third case, three normally off JFETs connected serially as a starter device are then coupled between source and drain of the JFET. Further cases include two or more starter devices coupled between source and drain of the JFET. Each of the resulting structures provide high current carrying capacity at low voltage levels, and will easily switch

between states at dc voltage levels greater than 0.4 volts or used as an amplifier at dc voltage levels greater than 0.4 volt.

A second embodiment of the present invention includes an asymmetrical, enhancement mode JFET as the switching device or an amplifier device. In a first case, a BJT acting as the starter device, either by added structure or use its parasitic BJT structure, is coupled between source and drain of the JFET. In a second case, a normally off MOSFET acting as the starter device is coupled between source and drain of the JFET. In a third case, three normally off JFETs connected serially as a starter device are then coupled between source and drain of the JFET. Further cases include two or more starter devices coupled between source and drain of the JFET. Each of the resulting structures provide high current carrying capacity at low voltage levels, and will easily switch between states at dc voltage levels greater than 0.4 volts.

A third embodiment of the present invention includes a symmetrical, enhancement mode MESFET as the switching device or an amplifier device. In a first case, a BJT acting as the starter device by added structure is coupled between source and drain of the MESFET. In a second case, a normally off MOSFET acting as the starter device is coupled between source and drain of the MESFET. In a third case, three normally off JFETs connected serially as a starter device are then coupled between source and drain of the MESFET. Further cases include two or more starter devices coupled between source and drain of the MESFET. Each of the resulting structures provide high current

carrying capacity at low voltage levels, and will easily switch between states at dc voltage levels greater than 0.4 volts.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1a shows the electronic symbol used in the present invention to represent an n-channel, symmetrical, normally off JFET.

Figure 1b shows the electronic symbol used in the present invention to represent an n-channel, asymmetrical, normally off JFET.

Figure 1c shows the electronic symbol used in the present invention to represent an n-channel, symmetrical, normally off MESFET.

Figure 2a shows the electronic symbol used in the present invention to represent a starter device.

Figure 2b shows the electronic symbol used in prior art to represent a BJT.

Figure 2c shows the electronic symbol used in prior art to represent a normally off MOSFET.

Figure 2d shows the electronic symbol used in the present invention to represent three, n-channel, symmetrical, normally off JFETs connected in series to form a starter device.

Figure 3 shows the electronic symbol used in the present invention to represent an n-channel, symmetrical, normally off JFET coupled to a starter device.

Figure 4 shows the electronic symbol used in the present invention to represent an n-channel, asymmetrical, normally off JFET coupled to a starter device.

Figure 5 shows the electronic symbol used in the present invention to represent an n-channel, symmetrical, normally off MESFET coupled to a starter device.

Figure 6 is an exemplary cross-sectional view showing the construction of an n-channel, symmetrical, normally off JFET coupled to a normally off MOSFET starter device according to the present invention.

DETAILED DESCRIPTION

In the following detailed description of the present invention, starter device for normally off FETs, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be obvious to one skilled in the art that the present invention may be practiced without these specific details. In other instances well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

Figure 1 shows the electronic symbols used in the present invention to represent three different normally off FETs 100. Figure 1a is the electronic symbol used to represent an n-channel, symmetrical, normally off JFET. The gate lead 115 is spaced equidistant between the source lead 105 and the drain lead 110 which identifies this as a symmetrical device. The direction of the arrow on the gate lead signifies an n-channel JFET. The broken line 116 between source and drain denotes a normally off or enhancement mode device. Since the device is symmetrical, the source and drain leads are interchangeable. A dc voltage that will forward bias both the p-n junction between gate and source and the p-n junction between gate and drain will switch the normally off JFET into the on state which will allow a dc current between source and drain. However, it is not possible to simultaneously forward bias both p-n junctions with the existence of a dc voltage between drain and source greater than approximately 0.4 volts. Therefore, switching the normally off JFET into a

current conducting state with a dc drain to source voltage greater than about 0.4 volts requires the use of a starter device to initially forward bias both p-n junctions.

Figure 1b is the electronic symbol used to represent an n-channel, asymmetrical, normally off JFET. The gate lead 135 is directly across from the source lead 125 which identifies this as an asymmetrical device. The direction of the arrow on the gate lead signifies an n-channel JFET. The broken line 136 between source and drain 130 denotes a normally off or enhancement mode device. A dc voltage that will forward bias both the p-n junction between gate and source and the p-n junction between gate and drain will switch the normally off JFET into the on state which will allow a dc current between source and drain. Again, it is not possible to simultaneously forward bias both p-n junctions with the existence of a dc voltage between drain and source greater than approximately 0.4 volts. Therefore, switching the normally off JFET into a current conducting state or use of the normally off JFET as an amplifier with a dc drain to source voltage greater than about 0.4 volts requires the use of a starter device to initially forward bias both p-n junctions.

Figure 1c is the electronic symbol used to represent an n-channel, symmetrical, normally off MESFET. The gate lead 155 is spaced equidistant between the source lead 145 and the drain lead 150 which identifies this as a symmetrical device. The direction of the arrow on the gate lead signifies an n-channel JFET. The broken line 156 between source and drain denotes a

normally off or enhancement mode device. The angular center section 157 of the broken line denotes a Schottky diode as the gate structure. A dc voltage that will forward bias both the Schottky barrier between gate and source and the Schottky barrier between gate and drain will switch the normally off MESFET into the on state which will allow a dc current between source and drain. With this device, it is not possible to simultaneously forward bias both Schottky barriers with the existence of a dc voltage between drain and source greater than approximately 0.4 volts. Therefore, switching the MESFET into a current conducting state with a dc drain to source voltage greater than about 0.4 volts or use of MESFET as an amplifier requires the use of a starter device to initially forward bias both Schottky barriers.

Figure 2 shows the electronic symbols used in the present invention to represent starter devices 200. Figure 2a is a generic three terminal symbol that is used in the present invention to represent one or more devices coupled to form a starter device. Terminals 210 and 212 are coupled between the source and drain of an FET switching device, and a control signal is applied to terminal 211 to switch the starter device between conducting and non-conducting states.

Figure 2b is the prior art symbol used to represent an npn BJT. The emitter lead 220 corresponds to terminal 210 of the generic symbol, the base lead 221 corresponds to terminal 211 of the generic symbol and the collector lead 222 corresponds to terminal 212 of the generic symbol. This kind of BJT

can be designed in with normally off JFET, using parasitic npn structure of JFET or simply connecting a discrete BJT to a JFET.

Figure 2c is the prior art symbol used to represent an n-channel MOSFET. The source lead 230 corresponds to terminal 210 of the generic symbol, the gate lead 231 corresponds to terminal 211 of the generic symbol and the drain lead 232 corresponds to terminal 212 of the generic symbol.

Figure 2d is the symbol used in the present invention to represent three n-channel JFETs coupled in series and having the three gate leads connected together. Lead 240 corresponds to terminal 210 of the generic symbol, lead 241 corresponds to terminal 211 of the generic symbol and lead 242 corresponds to terminal 212 of the generic symbol.

Figure 3 shows the electronic symbol used 300 in the present invention to represent an n-channel, symmetrical, normally off JFET coupled to a starter device. Lead 210 of the starter device is connected to the source lead 105 of the JFET, lead 212 of the starter device is connected to the drain lead 110 of the JFET and lead 211 of the starter device is connected to the gate lead 115 of the JFET. In dc circuit applications where the dc voltage between source and drain is greater than about 0.4 volts, a starter device which will initially forward bias both the p-n junction between gate and source and the p-n junction between gate and drain is required to switch the normally off JFET into the current conducting state or us the normally off JFET as an amplifier under dc bias above 0.4 volts.

In a first case, the starter device is an npn BJT coupled to the JFET with emitter 210 connnected to source 105, base 211 connected to gate 115 and collector 212 connected to drain 110. A dc voltage applied which will forward bias the gate-source p-n junction will also forward bias the base-emitter junction of the BJT. The BJT will thus switch into a current conducting state and the voltage collector to emitter will reduce to around 0.4 volts dc. The source to drain voltage of the JFET is simultaneously reduced to around 0.1 volts dc which forward biases both p-n junctions of the JFET. The JFET is thus switched on or used as an amplifier and will then conduct current between source and drain. A dc voltage applied which will forward bias the gate-drain p-n junction will also forward bias the base-collector junction of the BJT. The BJT will thus switch in the inverse mode into a current conducting state and the voltage collector to emitter will reduce to around 0.1 volts dc. The source to drain voltage of the JFET is again reduced to around 0.1 volts dc which forward biases both p-n junctions of the JFET. The JFET is thus switched on or used as an amplifier and will then conduct current between source and drain. This BJT can be individually designed along with JFET or use the parasitic npn structure of JFET as the starter device.

In a second case, the starter device is an n-channel, normally off MOSFET coupled to the JFET with source 210 connected to source 105, drain 212 connected to drain 110 and gate 211 connected to gate 115. A dc voltage applied to the gate of the JFET that will forward bias either the JFET gate to

source p-n junction or the JFET gate to drain p-n junction will switch the normally off MOSFET into a current conducting state which will reduce the drain to source voltage of both FETs to around 0.1 volts or less. Thus both p-n junctions of the JFET will be forward biased and the JFET will switch on and will then conduct current between source and drain.

In a third case, the starter device consists of three normally off, symmetrical, n-channel JFETs connected in series and having their gate leads connected together to form a three terminal device as illustrated in Figure 2d. The starter device is coupled to the JFET with source 210 connected to source 105, drain 212 connected to drain 110 and gate 211 connected to gate 115. A dc voltage applied to the gate of the JFET that will forward bias either the JFET gate to source p-n junction or the JFET gate to drain p-n junction will switch the normall off starter device into a current conducting state which will reduce the drain to source voltage of the JFET to around 0.1 volts or less. Thus both p-n junctions of the JFET will be forward biased and the JFET will switch on and will then conduct current between source and drain.

Figure 4 shows the electronic symbol used 400 in the present invention to represent an n-channel, asymmetrical, normally off JFET coupled to a starter device. Lead 210 of the starter device is connected to the source lead 125 of the JFET, lead 212 of the starter device is connected to the drain lead 130 of the JFET and lead 211 of the starter device is connected to the gate lead 135 of the JFET. In dc circuit applications where the dc voltage between source and drain

is greater than about 0.4 volts, a starter device which will initially forward bias both the p-n junction between gate and source and the p-n junction between gate and drain is required to switch the normally off JFET into the current conducting state.

In a first case, the starter device is an npn BJT coupled to the JFET with emitter 210 connnected to source 125, base 211 connected to gate 135 and collector 212 connected to drain 130. A dc voltage applied which will forward bias the gate-source p-n junction will also forward bias the base-emitter junction of the BJT. The BJT will thus switch into a current conducting state and the voltage collector to emitter will reduce to around 0.1 volts dc. The source to drain voltage of the JFET is simultaneously reduced to around 0.1 volts dc which forward biases both p-n junctions of the JFET. The JFET is thus switched on and will then conduct current between source and drain. A dc voltage applied which will forward bias the gate-drain p-n junction will also forward bias the base-collector junction of the BJT. The BJT will thus switch in the inverse mode into a current conducting state and the voltage collector to emitter will reduce to around 0.1 volts dc. The source to drain voltage of the JFET is again reduced to around 0.1 volts dc which forward biases both p-n junctions of the JFET. The JFET is thus switched on and will then conduct current between source and drain. This BJT can be individually designed along with JFET or use the parasitic npn structure of JFET as the starter device.

In a second case, the starter device is an n-channel, normally off MOSFET coupled to the JFET with source 210 connected to source 125, drain 212 connected to drain 130 and gate 211 connected to gate 135. A dc voltage applied to the gate of the JFET that will forward bias either the JFET gate to source p-n junction or the JFET gate to drain p-n junction will switch the normally off MOSFET into a current conducting state which will reduce the drain to source voltage of both FETs to around 0.1 volts or less. Thus both p-n junctions of the JFET will be forward biased and the JFET will switch on and will then conduct current between source and drain.

In a third case, the starter device consists of three normally off, symmetrical, n-channel JFETs connected in series and having their gate leads connected together to form a three terminal device as illustrated in Figure 2d. The starter device is coupled to the JFET with source 210 connected to source 125, drain 212 connected to drain 130 and gate 211 connected to gate 135. A dc voltage applied to the gate of the JFET that will forward bias either the JFET gate to source p-n junction or the JFET gate to drain p-n junction will switch the normall off starter device into a current conducting state which will reduce the drain to source voltage of the JFET to around 0.1 volts or less. Thus both p-n junctions of the JFET will be forward biased and the JFET will switch on and will then conduct current between source and drain.

Figure 5 shows the electronic symbol used 500 in the present invention to represent an n-channel, symmetrical, normally off MESFET coupled to a starter

device. Lead 210 of the starter device is connected to the source lead 145 of the MESFET, lead 212 of the starter device is connected to the drain lead 150 of the MESFET and lead 211 of the starter device is connected to the gate lead 155 of the MESFET. In dc circuit applications where the dc voltage between source and drain is greater than about 0.4 volts, a starter device which will initially forward bias both the Schottky barrier between gate and source and the Schottky barrier between gate and drain is required to switch the normally off MESFET into the current conducting state.

In a first case, the starter device is an npn BJT coupled to the MESFET with emitter 210 connnected to source 145, base 211 connected to gate 155 and collector 212 connected to drain 150. A dc voltage applied which will forward bias the gate-source Schottky barrier will also forward bias the base-emitter junction of the BJT. The BJT will thus switch into a current conducting state and the voltage collector to emitter will reduce to around 0.1 volts dc. The source to drain voltage of the MESFET is simultaneously reduced to around 0.1 volts dc which forward biases both Schottky barriers of the MESFET. The MESFET is thus switched on and will then conduct current between source and drain. A dc voltage applied which will forward bias the gate-drain Schottky barrier will also forward bias the base-collector junction of the BJT. The BJT will thus switch in the inverse mode into a current conducting state and the voltage collector to emitter will reduce to around 0.1 volts dc. The source to drain voltage of the MESFET is again reduced to around 0.1 volts dc which forward biases both

Schottky barriers of the MESFET. The MESFET is thus switched on and will then conduct current between source and drain.

In a second case, the starter device is an n-channel, normally off MOSFET coupled to the MESFET with source 210 connected to source 145, drain 212 connected to drain 150 and gate 211 connected to gate 155. A dc voltage applied to the gate of the MESFET that will forward bias either the MESFET gate to source p-n junction or the MESFET gate to drain p-n junction will switch the normally off MOSFET into a current conducting state which will reduce the drain to source voltage of both FETs to around 0.1 volts or less. Thus both Schottky barriers of the MESFET will be forward biased and the MESFET will switch on and will then conduct current between source and drain.

In a third case, the starter device consists of three normally off, symmetrical, n-channel JFETs connected in series and having their gate leads connected together to form a three terminal device as illustrated in Figure 2d. The starter device is coupled to the MESFET with source 210 connected to source 145, drain 212 connected to drain 150 and gate 211 connected to gate 155. A dc voltage applied to the gate of the MESFET that will forward bias either the MESFET gate to source Schottky barrier or the MESFET gate to drain Schottky barrier will switch the normally off starter device into a current conducting state which will reduce the drain to source voltage of the MESFET to around 0.1 volts or less. Thus both Schottky barriers of the MESFET will be

forward biased and the MESFET will switch on and will then conduct current between source and drain.

Figure 6 is an exemplary cross-sectional view 600 showing the construction of an n-channel, symmetrical, normally off JFET coupled to a normally off MOSFET starter device according to the present invention. The substrate 610 serves as the structural base on which the FETs are formed. The n+ symbol in the substrate region shows an elevated n-type doping density necessary to form good ohmic contact with the metal electrode 615. This metal electrode serves as the contact for the drain lead of the JFET 110 as well as the drain lead of the MOSFET 232.

The epitaxial region adjacent to the substrate 620 is doped n-type with a doping density less than that of the substrate as signified by the letter n located within the epitaxial region. A region signified by the symbol n+ and having an elevated n-type doping density 640 is formed on the upper surface of the epitaxial layer in order to form good ohmic contact with the metal JFET source electrode 105.

Elements of the grill-like gate structure of the JFET 630 are exemplary rectangular areas doped p-type and distributed throughout the mid-section of the epitaxial region. Electrical contact to the JFET gate is by means of the metal region 115.

The n-type region on the upper surface of the epitaxial layer 660 serves as the source of the MOSFET, and the metal area 230 is the electrical contact

for this region. The p-type region 670 surrounding the MOSFET source produces a depletion region between source and drain of the MOSFET, thereby creating a normally off device. The metal region 231 then acts as the gate lead for the MOSFET. The four metal electrodes on the upper surface are isolated electrically by oxide regions 650.

The metal area 615 acts as the single electrical contact connecting the JFET drain and the MOSFET drain. Electrical connections between JFET source and MOSFET source, and JFET gate and MOSFET gate are not shown here.

Likewise, this invention also applies to p-channel normally off JFET with pnp BJT or p-channel MOSFET. This invention also applies to other semiconductor materials such as germanium, gallium arsenide, heterojunction materials as sell as semiconductor on insulator (SOI) materials.

The preferred embodiment of the present invention, starter device for normally off FETs, is thus described. While the present invention has been described in particular embodiments, it should be appreciated that the present invention should not be construed as limited by such embodiments, but rather construed according to the below claims.

CLAIMS

What is Claimed is:

1. A current switch or an amplifier consisting of:

a) at least one normally off Field Effect, Transistor (FET), and

b) a starter device coupled to said FET.

2. A current switch or an amplifier according to Claim 1 wherein said starter device is a series coupling of at least two normally off Junction Field Effect Transistors (JFET).

3. The current switch or amplifier of Claim 1 wherein the FET is a Junction Field Effect Transistor (JFET)

4. The switch or amplifier of Claim 3 wherein the JFET is symmetrical.

5. The switch or amplifier of Claim 3 wherein the JFET is asymmetrical.

6. The current switch or amplifier according to Claim 3,4 or 5 wherein said starter device is a Bipolar Junction Transistor (BJT).

7. The current switch or amplifier of Claim 1 wherein the FET is a symmetrical, Metal Silicon Field Effect Transistor (MESFET).

8. A current switch or amplifier according to Claim 1 or 7 wherein said starter device is a Bipolar Junction Transistor (BJT) including:

a) a BJT connected externally;

b) a BJT designed along with said JFET, and

c) a BJT as a device parasitic to said JFET.

9. The current switch or amplifier according to Claim 1, 3, 4, 5 or 7 wherein said starter device is a Metal Oxide Silicon Field Effect Transistor (MOSFET).

10. A current switch or an amplifier according to Claim 3, 4, 5 or 7 wherein said starter device is a series coupling of three normally off Junction Field Effect Transistors (JFET).

11. A current switch or an amplifier according to Claim 1, 3, 4, 5 or 7 wherein said, starter device is a parallel coupling of at least two of said BJT and said MOSFET and said series coupling of three normally off JFETs.

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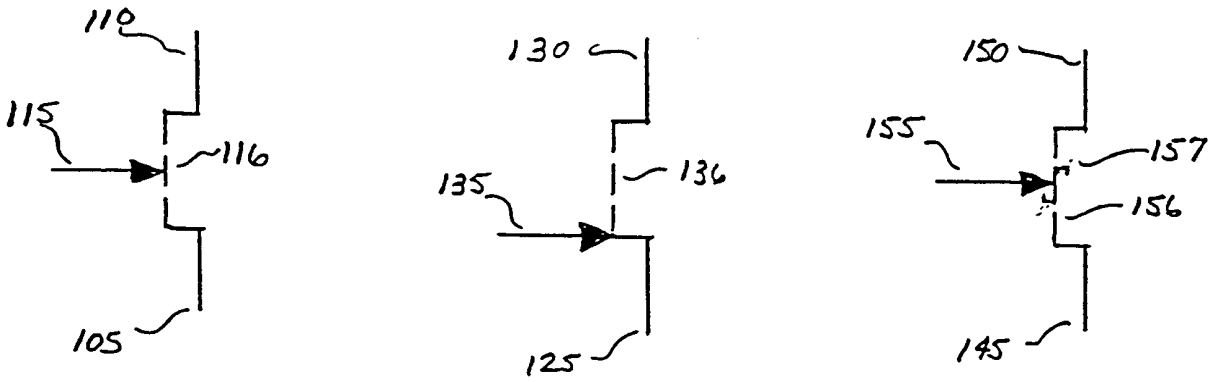
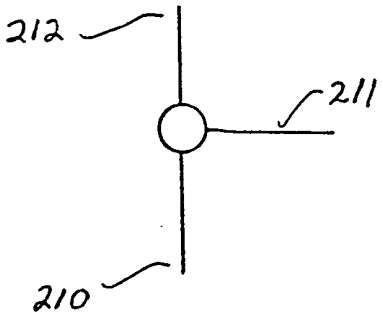


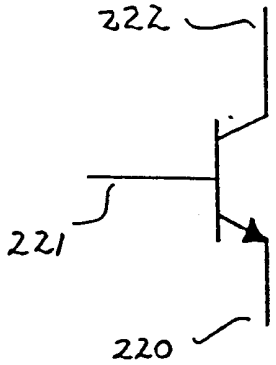
a) b) c)

FIGURE 1

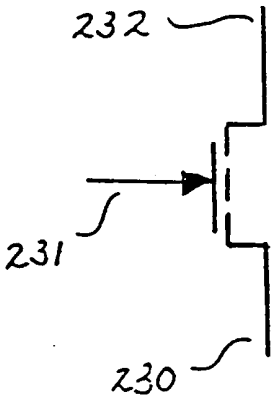
200



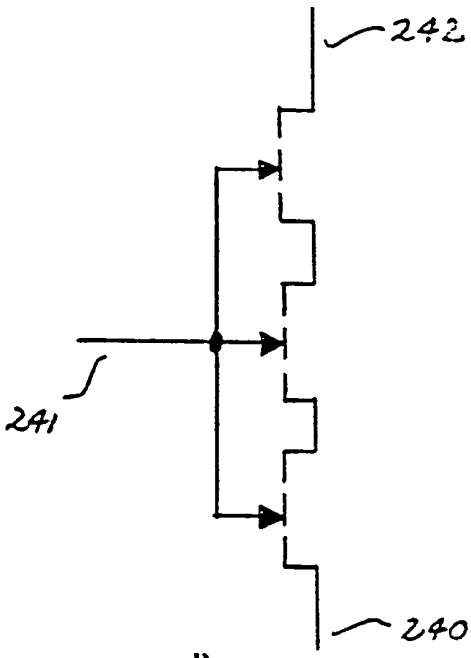
a)



b) prior art



c) prior art



d)

FIGURE 2

300

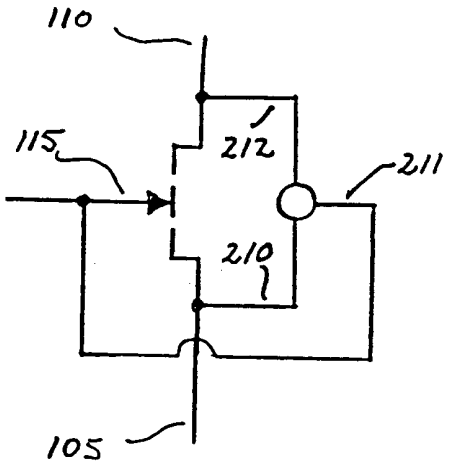


FIGURE 3

400

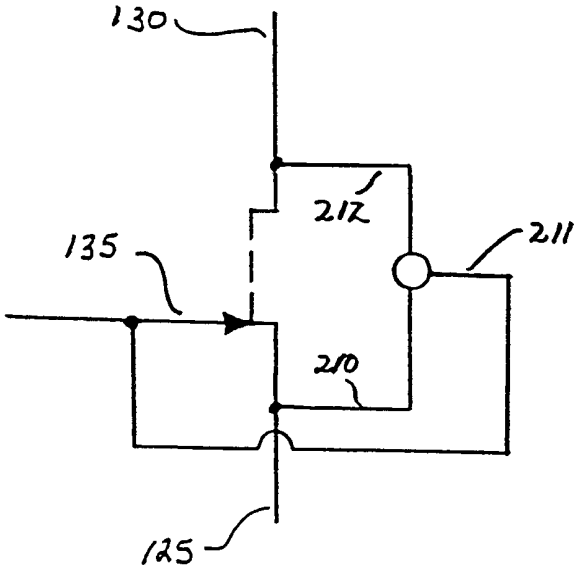


FIGURE 4

500

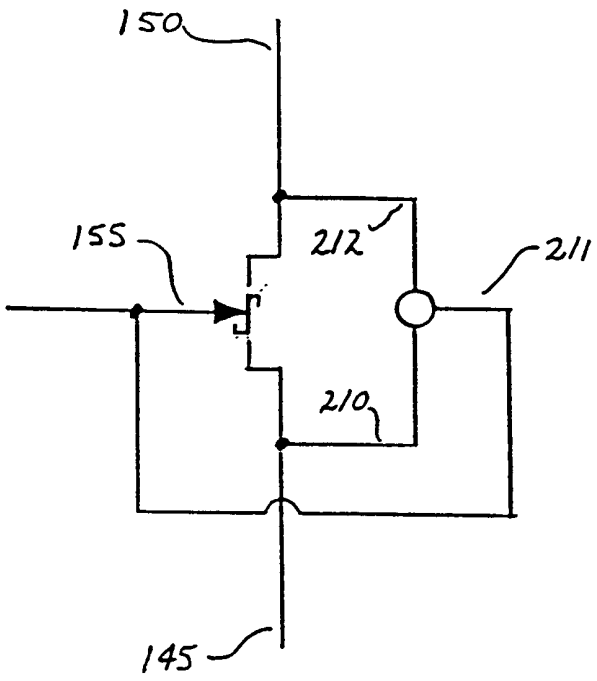


FIGURE 5

600

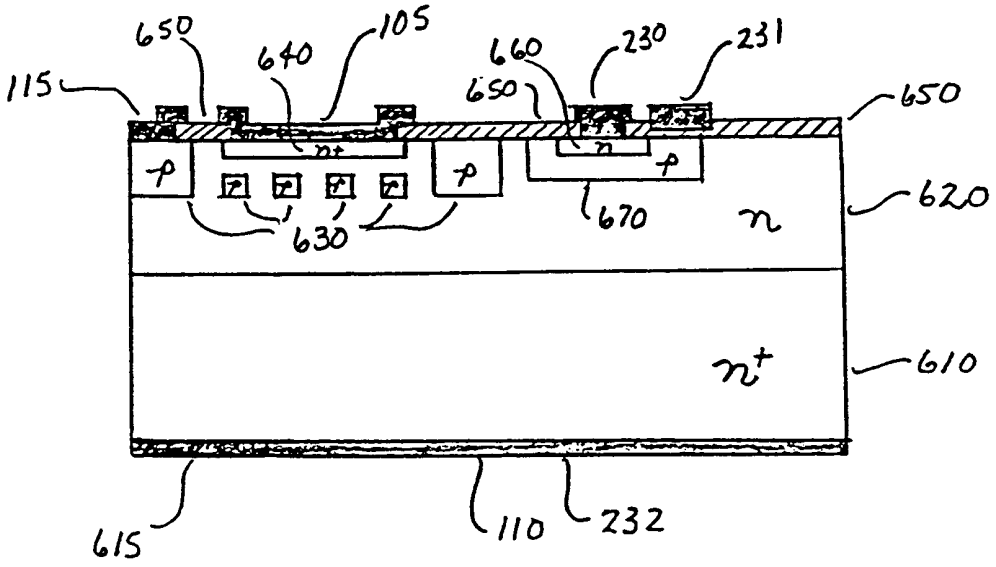

650
640
105
660
230
231
115
650
650
p
n+
p
n
p
620
630
670
n
n+
610
615
110
232

FIGURE 6

INTERNATIONAL SEARCH REPORT

Inte onal Application No
PCT/US 00/42244

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03K17/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
WPI Data, EPO-Internal, IBM-TDB, INSPEC, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 739 094 A (MATSUSHITA ELECTRIC IND CO LTD) 23 October 1996 (1996-10-23) column 6, line 17 - line 47; figures 3,4	1
A	US 4 523 111 A (BALIGA BANTVAL J) 11 June 1985 (1985-06-11) cited in the application the whole document	1
A	US 4 645 957 A (BALIGA BANTVAL J) 24 February 1987 (1987-02-24) cited in the application the whole document	1
A	US 5 396 085 A (BALIGA BANTVAL J) 7 March 1995 (1995-03-07) column 6, line 50 -column 9, line 32; figure 5	1,9

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
4 May 2001	14/05/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Feuer, F

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte onal Application No
PCT/US 00/42244

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