

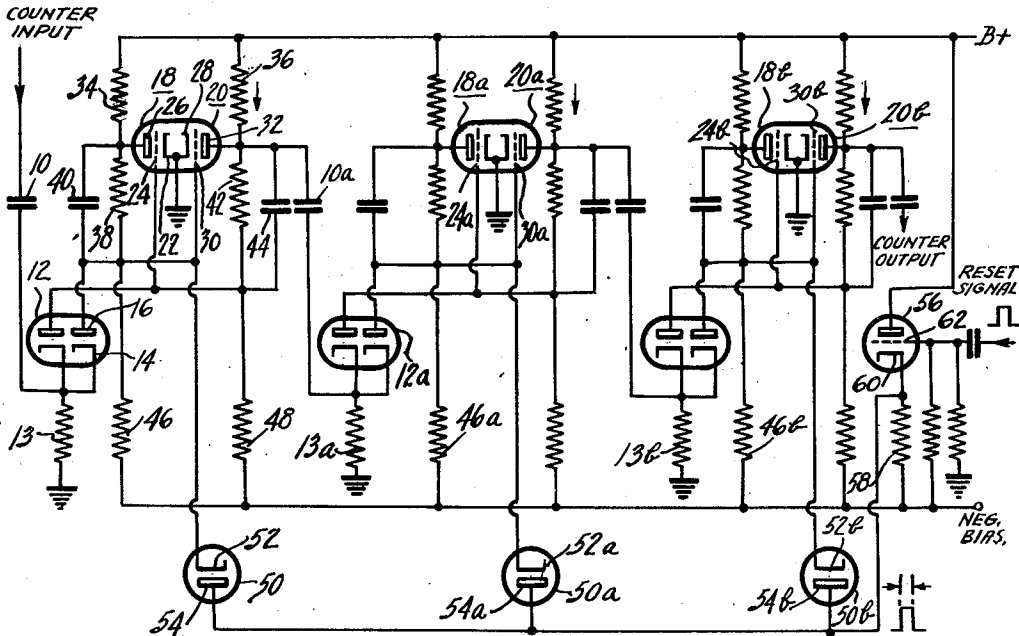
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I. E. GROSDOFF

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RESET CIRCUIT FOR ELECTRONIC COUNTERS

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INVENTOR
Igor E. Grosdoff
BY *Marion Rabin*
ATTORNEY

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RESET CIRCUIT FOR ELECTRONIC
COUNTERSIgor E. Grosdoff, Princeton, N. J., assignor to
Radio Corporation of America, a corporation
of Delaware

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The present invention relates to electronic counting systems and more particularly is an improved resetting system for electronic counter systems.

Electronic counting systems in general, use as a basis a chain or cascade of trigger circuits each of which is capable of assuming either of two conditions of stability. The basic trigger circuit with which the present invention is illustrated as being utilized is the trigger circuit of the general type described in "Theory and Application of Vacuum Tubes" by Herbert J. Reich, published in 1944. In one of its simplest forms, this trigger circuit includes two triodes in which the grid of the first triode is coupled to the anode of the second triode through a network comprising a parallel connected resistor and capacitor, and the grid of the second triode is similarly coupled to the anode of the first triode through a similar coupling network. The cathodes of both triodes are grounded. Grid and anode potentials are applied to the respective electrodes through separate resistors.

In operation, if a negative voltage is applied to the grid of the first triode, the anode current of the triode will be reduced and the anode potential will become more positive. Due to the connection through the coupling resistor, the grid potential of the second triode will become more positive, causing an increase in the anode current of the second triode, with a resultant decrease in the second triode anode potential. This decrease in anode potential will, in turn, cause the grid potential of the first triode to become more negative. This action will continue until the anode current of the first triode is cut off. The first triode will remain cut off, and the second triode will remain conducting, until a negative potential is applied to the grid of the second triode. The tubes' operating conditions are thereby reversed and the first triode becomes conducting and the anode current of the second triode is cut off.

For the purposes of counting, a pulse is usually applied to the first trigger circuit in the chain to transfer conduction from one tube to the other. The next pulse, applied to the first trigger circuit, transfers conduction back to the first tube and at the same time a pulse is generated by the first trigger circuit which is applied to the second trigger circuit to cause a transfer in conduction from one of its tubes to the other. Two more pulses must be applied to the first trigger circuit before it generates another pulse which is applied to the second trigger circuit to restore it to its starting condition. This latter action in turn

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generates a pulse which is applied to a third trigger circuit to cause it to transfer conduction. As many trigger circuits as are required for obtaining a desired count may be used. By the use of feedback between trigger circuits, a counter may complete a cycle of counting with fewer applied pulses than are required without feedback.

Regardless of the feedback connections between trigger circuits, all counter circuits, at the beginning of a count, usually have some desired starting position with conduction in one of the triodes of each trigger circuit. To attain this starting position at the termination of a count, a resetting circuit is usually provided. This consists of a reset pulse source which is connected to a grid of one of the triodes in each of the trigger circuits. The reset pulse is applied with a polarity to return or retain conduction in the tube in each trigger circuit which represents the desired starting condition. A "settling down" period is usually required after a counter is reset and before it can be used again for the next count. The reason for this is, that in being reset, a tube in a trigger circuit usually generates pulses which tend to drive the following trigger circuit and sometimes do. This reset and settling down period, or total reset time, seriously affects the speed of these types of counters and thus their application in situations requiring continuous rapid successions of counts is prevented or requires an alternate counter which can be switched on to allow time for reset.

It is therefore an object of the present invention to provide an improved reset circuit which permits a faster reset of an electronic counter than was possible heretofore.

It is a further object of the present invention to provide an improved reset circuit which dissipates pulses generated by the resetting action.

It is still another object of the present invention to provide a new and improved reset circuit for an electronic counter.

These and further objects are achieved, in accordance with the present invention, by coupling a diode or rectifier from the grid of the tube in each trigger circuit which it is desired to reset to the cathode of a cathode follower tube. A bias is applied to the diodes through the cathode load impedance so that there is no interference with the operation of the counter during a counting interval. When reset is desired, a reset pulse is applied to the cathode follower and through each of the diodes to the tubes being reset. Any generated pulse during reset which tends to drive a subsequent trigger circuit is bypassed through the

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low impedance path presented by the diodes and the cathode follower cathode impedance and is therefore rendered ineffective.

The novel features of the invention as well as the invention itself, both as to its organization and method of operation, will best be understood from the following description when read in connection with the accompanying drawing, which represents a circuit diagram of a preferred embodiment of the invention.

Three stages of a well-known binary type of counter are shown, each stage consisting of a trigger circuit which is connected to apply a pulse to the subsequent trigger circuit after it has had two pulses applied to its input.

The counter is arranged to be driven by negative pulses. The zero, or reset condition of the counter, is the one wherein current conduction is in the right hand tube of each trigger circuit, as shown by the arrows.

A negative input pulse is applied through a condenser 10 to the cathodes 14 of the double diode 12. Each of the anodes 16 of the double diode 12 are connected to a grid 24, 30 of each of the triodes 18, 20 of the trigger circuit comprising the first counter stage. A grid leak resistor 13 couples the diode cathodes to ground. The triodes 18, 20 have individual load resistors 34, 36 connecting each of their anodes 26, 32 to a source of anode potential. The left triode anode 26 is connected to the right triode grid 30 through a parallel connected resistor 38 and 40. The right triode anode 32 is also coupled to the left triode grid 24 by a parallel connected resistor 42-condenser 44 combination. Although the trigger circuits are shown as having triodes, multigrid electron discharge tubes may be substituted therefore in a manner which is well known to those skilled in the art. Each of the grids 24, 30 of the triodes 18, 20 are connected to a source of negative bias through a separate resistor 46, 48. The trigger circuit components and the applied bias have their values selected so that the trigger circuit has two stable states. One with conduction in the right triode 20 and the other with conduction in the left triode 18.

The first negative input pulse is applied through the double diode 12 to both grids 24, 30 of the first trigger circuit tubes. This has no effect on the left triode 18 which is already non-conducting, but the negative pulse causes the right triode 20 to go to cut-off. This causes a positive pulse to be generated at the right triode anode 32 which is applied to the left triode grid 24 causing the left triode 18 to become conductive.

The next negative pulse applied to the first trigger circuit through the double diode 12 causes a reversal of conduction from the left triode 18 to the right triode 20. In becoming conductive the right triode generates a negative pulse at its anode 32. Besides this pulse being applied to the left triode grid 24, it is also applied to the grids 24a, 30a of the next trigger circuit through a coupling condenser 10a and a double diode 12a connected to the grids 24a, 30a of the two triodes 18a, 20a included in the second trigger circuit. The connection and operation of the second trigger circuit is substantially the same as for the first trigger circuit. The third trigger circuit is also substantially the same in operation and connection as the first trigger circuit. Each trigger circuit goes from its initial or zero state to its second stable state and back to its zero state in response to two negative pulses being applied to it. Each trigger circuit supplies an output pulse to trigger

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the succeeding trigger circuit in returning from its second stable state back to its zero state. Therefore, one output pulse is received from the third trigger circuit in response to eight pulses being applied to the first trigger circuit.

If, at any time during a count, it is desired to reset the counter to its initial or zero condition with conduction in all the right triodes, a positive pulse, also known as a reset pulse, is applied to the right triode grids 30, 30a, 30b of the counter. This has the effect of causing all the right triodes 20, 20a, 20b being driven from a non-conducting to a conducting condition, to generate negative pulses. These negative pulses are applied through the coupling condensers and double diodes to the subsequent trigger circuit grids and tend to oppose the effects of the reset pulse. This causes the counter to be "jittery" and some time must be permitted for it to settle down before being used again.

These difficulties may be eliminated by coupling to the counter a reset circuit which is a preferred embodiment of the present invention. This includes a diode or rectifier 50, 50a, 50b for each triode that is being reset. A cathode follower tube 56 is also provided having a load impedance or resistance 58 connected to its cathode 60. Each diode cathode 52, 52a, 52b is connected to the grid of the triode being reset. In this instance, these are the right grids 30, 30a, 30b. Each diode anode 54, 54a, 54b is connected to the cathode 60 of the cathode follower tube. A negative bias is applied to the cathode follower grid 62 and to the anodes 54, 54a, 54b of the diodes 50, 50a, 50b through the load impedance 58 of the cathode follower tube 56. This serves the purpose of keeping the anodes of the diodes 50, 50a, 50b negative with respect to their cathodes even when negative pulses are applied to the grids to which the cathodes are connected. By this expedient the reset circuit does not interfere with the operation of the counter while counting. Effectively a high impedance is presented to the grids by the biased diodes.

When it is desired to reset the counter, a positive or reset pulse is applied to the grid 62 of the cathode follower. The signal on the cathode 60 follows the grid signal and thus a positive pulse is applied through the diodes 50, 50a, 50b to the respective triodes 20, 20a, 20b to cause them to be reset. Each of the right triodes which is reset generates a negative pulse which is applied to the subsequent trigger circuit as described above. But the reset diodes 50, 50a, 50b, the cathode follower cathode resistor 58, and the negative bias source present a low impedance path to such negative pulses during the time of application of the reset pulse. The negative pulses which could cause "jitter" are thereby dissipated without affecting the trigger circuit stability. The value of the cathode load resistor 58 of the cathode follower 56 is selected to be low when compared with the value of each of the grid resistors 13, 13a, 13b connecting the grids to ground or a point of fixed potential, or to the resistor 46, 46a, 46b through which negative bias is applied to the grids. The reset period is thereby considerably shortened to be the period of the duration of the reset pulse and the counter is available for a count immediately after the termination of the reset pulse. Thus, the biased diodes may be considered as unilateral impedances presenting a high impedance during the counting interval and a low impedance during the reset pulse interval.

From the foregoing description, it will be

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readily apparent that an improved reset circuit has been described which provides faster reset time than was heretofore possible. Although a single embodiment of the present invention has been shown and described, it should be readily apparent that many changes may be made in the particular embodiment herein disclosed, and that many other embodiments are possible, all within the spirit and scope of the invention. It will also be appreciated, by those skilled in the art, that the embodiment of the invention herein shown and described may be used with other types of electronic counters than binary counters. It is therefore desired that the foregoing description shall be taken as illustrative and not as limiting.

What is claimed is:

1. A circuit for resetting a chain of trigger circuits of the type wherein each trigger circuit has two stable conditions, one of which is a starting condition, an electron discharge tube having a grid electrode to which a voltage pulse is applied to reset said trigger circuit to its starting condition, and an impedance for coupling said grid electrode to a point of fixed potential, said reset circuit comprising an impedance the value of which is low when compared with the value of said grid coupling impedance, a plurality of unilateral impedances, each of said unilateral impedances being coupled between the grid of the tube in each of said trigger circuits to which it is desired to apply a reset pulse and said low value impedance, means to apply reset pulses to said low value impedance, and means to apply a bias to said unilateral impedances through said low value impedance to have said unilateral impedances and said low value impedance appear to said grids to have an impedance value which is high when compared to said grid coupling impedance and an impedance value which is low during reset.

2. A circuit for resetting a chain of trigger circuits of the type wherein each trigger circuit has two stable conditions one of which is a starting condition and each trigger circuit includes an electron discharge tube having a grid electrode to which a voltage pulse is applied to reset said trigger circuit to its starting condition and an impedance for coupling said grid electrode to a point of fixed potential, said reset circuit comprising an impedance the value of which is low when compared with the value of said grid coupling impedance, a plurality of rectifiers, each of said rectifiers being connected

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between the grid of a tube in each of said pair of tubes to which it is desired to apply a reset pulse and said low value impedance, means to apply reset pulses to said low value impedance, and means to apply a bias to said rectifiers to maintain said rectifiers non-conductive except during reset.

3. A circuit for resetting a chain of trigger circuits of the type wherein each trigger circuit has two stable conditions one of which is a starting condition, and an electron discharge tube having a grid electrode to which a voltage pulse is applied to reset said trigger circuit to its starting condition, said reset circuit comprising a cathode follower tube upon which reset pulses are impressed, a plurality of rectifiers, each of said rectifiers being connected between the grid of the tube in each of said pair of tubes to which it is desired to apply a reset pulse and the output of said cathode follower, and means to apply a bias to said cathode follower to maintain said rectifiers non-conductive except during reset.

4. A circuit for resetting a chain of trigger circuits of the type wherein each trigger circuit has two stable conditions, one of which is a starting condition, and an electron discharge tube having a grid electrode to which a voltage pulse is applied to reset said trigger circuit to its starting condition, said reset circuit comprising a cathode follower tube having grid, cathode and anode electrodes, a load impedance, connected to said cathode follower cathode, a plurality of diodes each having an anode and a cathode, said diodes' anodes being connected to said cathode follower cathode, each of said diodes' cathodes being connected to a grid of the one of each pair of tubes to which it is desired to apply a reset pulse, and means to apply a bias to said cathode follower cathode to maintain said diodes' anodes at a lower potential level than said diodes' cathodes, except during reset.

IGOR E. GROSDOFF.

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