US 20060170110A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2006/0170110 A1

Akram et al. (43) Pub. Date: Aug. 3, 2006

(54) THROUGH-SUBSTRATE INTERCONNECT STRUCTURES AND ASSEMBLIES

(76) Inventors: **Salman Akram**, Boise, ID (US); **Kyle K. Kirby**, Boise, ID (US)

Correspondence Address:
TRASK BRITT
P.O. BOX 2550
SALT LAKE CITY, UT 84110 (US)

(21) Appl. No.: **11/384,069**

(22) Filed: **Mar. 17, 2006**

Related U.S. Application Data

(62) Division of application No. 11/138,544, filed on May 26, 2005.

(60) Provisional application No. 60/606,355, filed on Aug. 31, 2004.

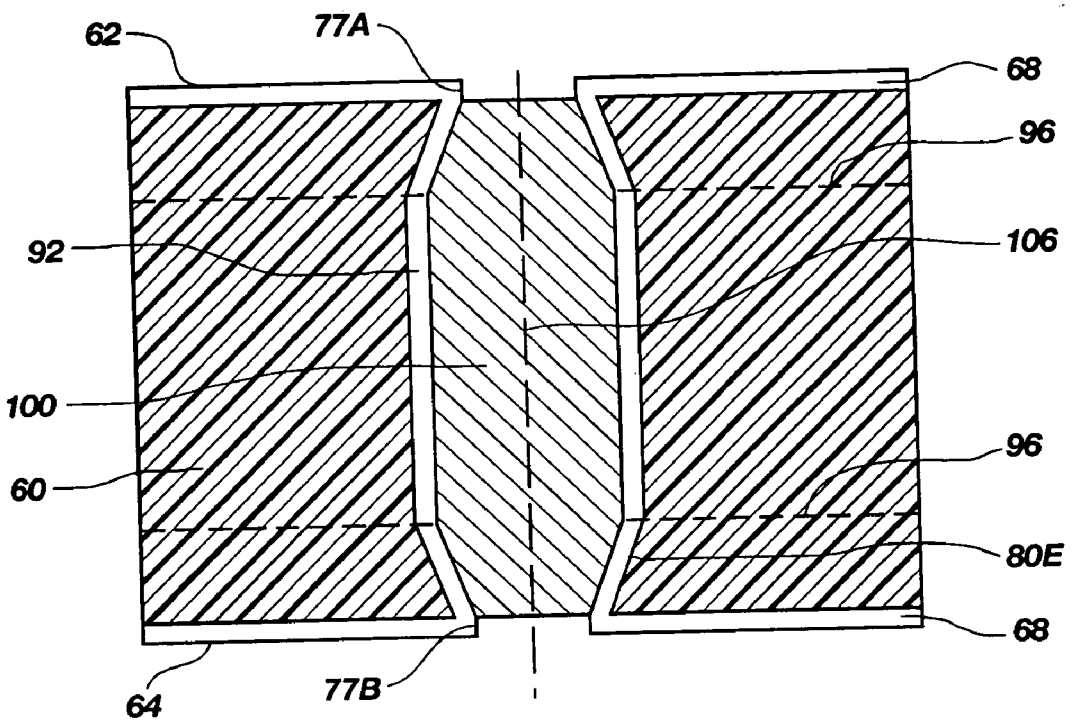
Publication Classification

(51) **Int. Cl.**
H01L 23/48 (2006.01)

(52) **U.S. Cl.** **257/774**; 257/E21

(57) **ABSTRACT**

Through-substrate interconnect structures and assemblies are disclosed. A substrate includes at least one via passing therethrough. The via may have an enlarged central portion, and one or more end portions which taper to smaller end surfaces. The one or more via end portions may be trapezoidal in shape. The one or more via end portions may have a rounded, i.e., frustoconical, shape. The shape is conducive to improved solder ball/bump attachment, and enables forming vias of very small diameter and pitch.



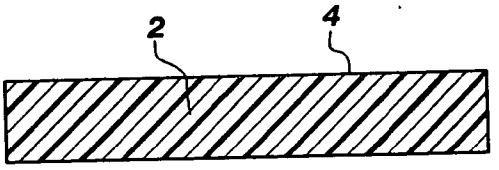


FIG. 1A
(PRIOR ART)

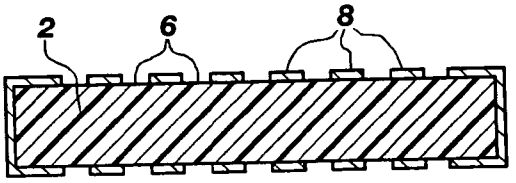


FIG. 1B
(PRIOR ART)

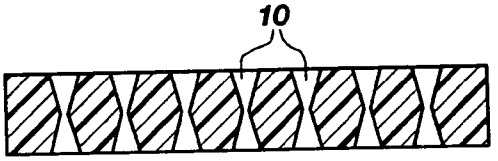


FIG. 1C
(PRIOR ART)

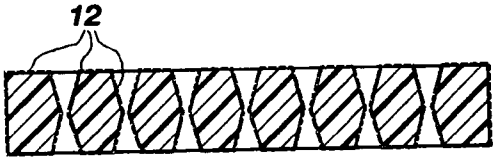


FIG. 1D
(PRIOR ART)

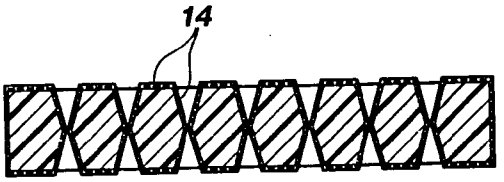


FIG. 1E
(PRIOR ART)

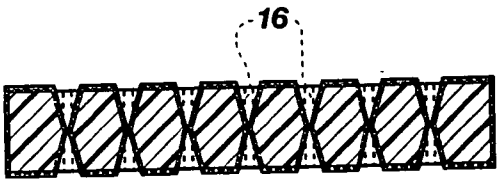


FIG. 1F
(PRIOR ART)

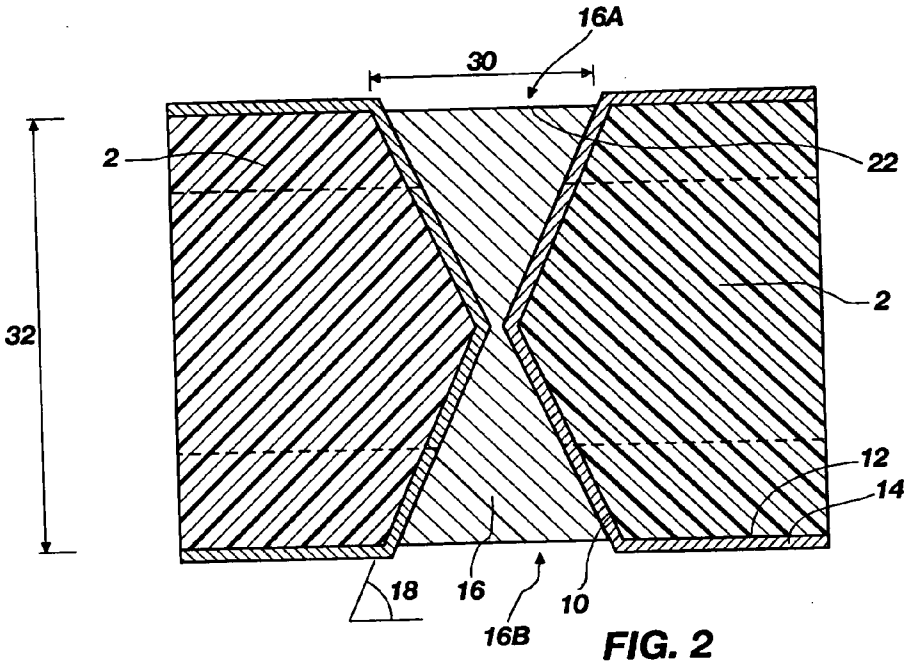


FIG. 2
(PRIOR ART)

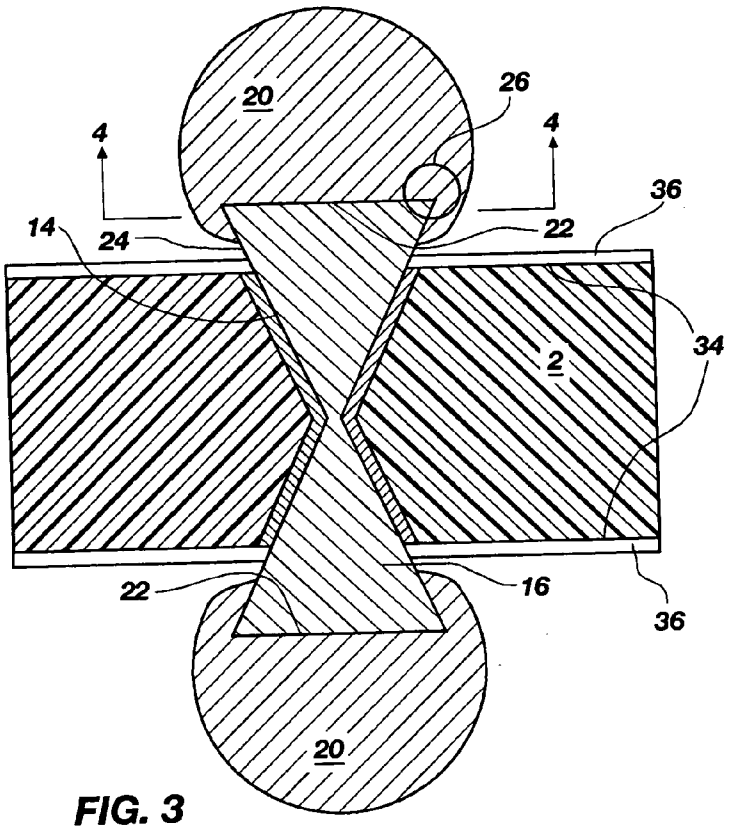


FIG. 3
(PRIOR ART)

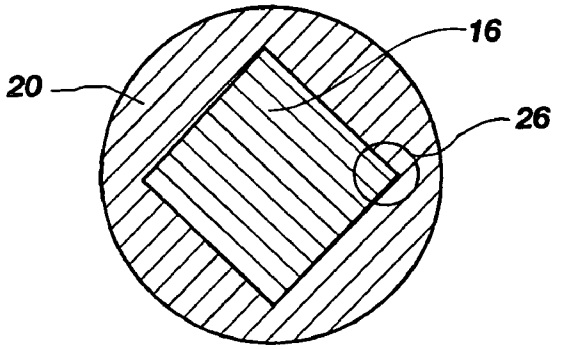


FIG. 4
(PRIOR ART)

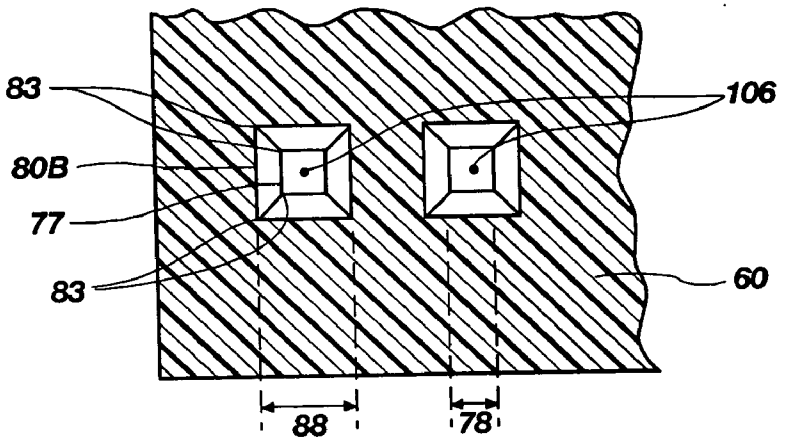


FIG. 10A

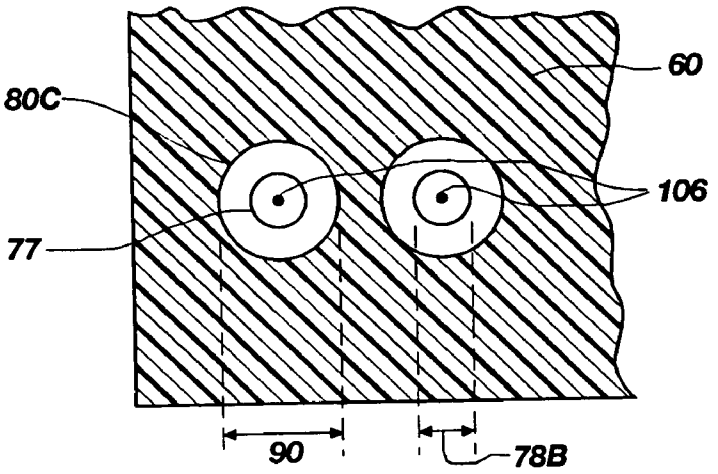


FIG. 11A

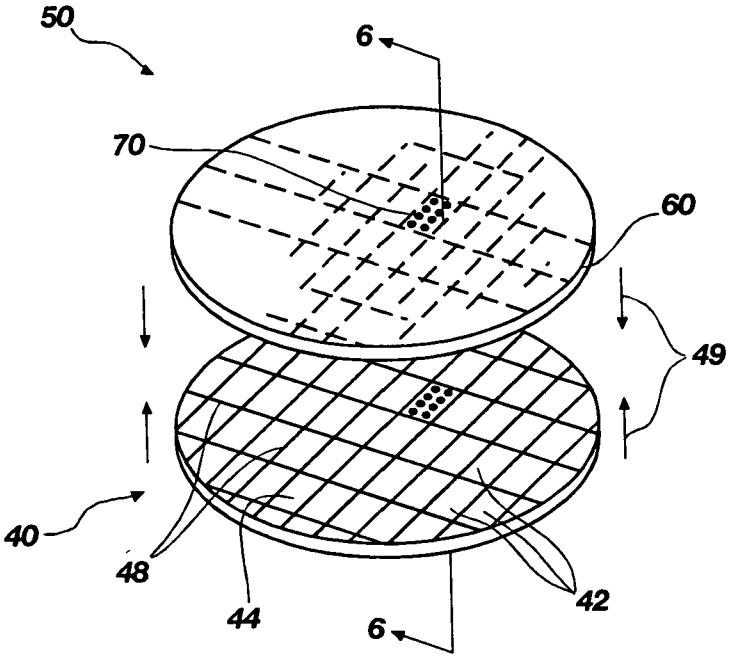


FIG. 5

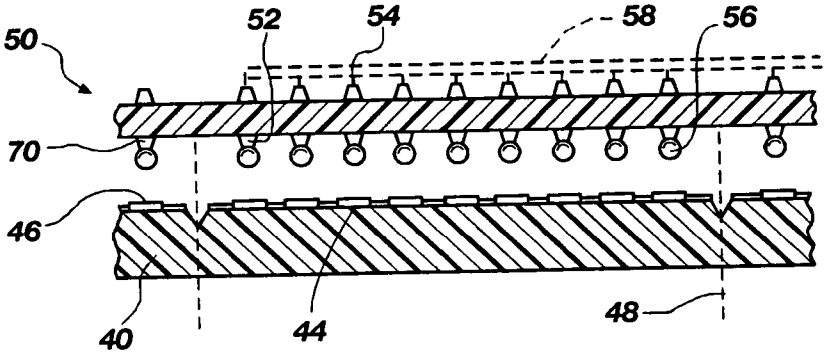


FIG. 6

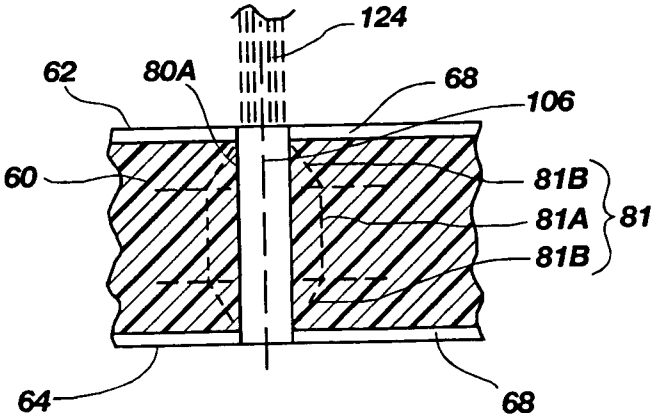


FIG. 9A

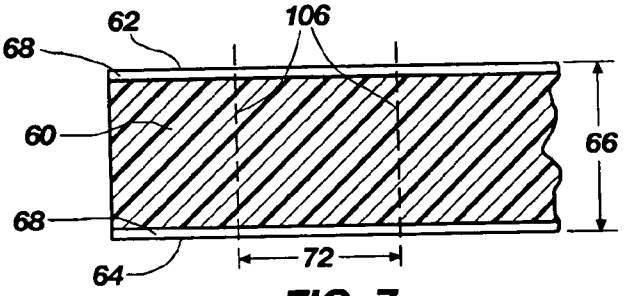


FIG. 7

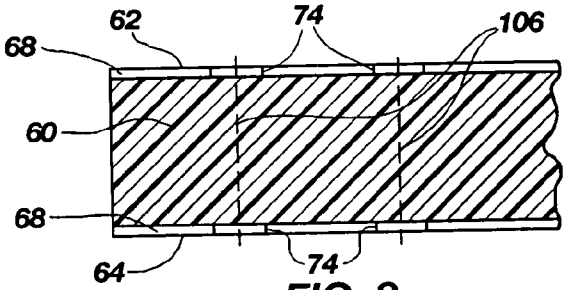


FIG. 8

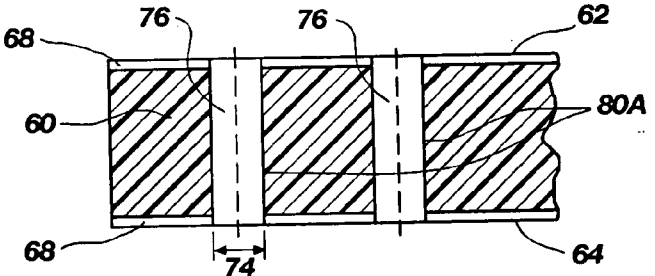


FIG. 9

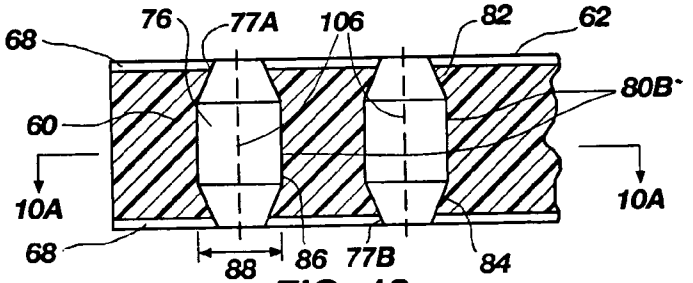


FIG. 10

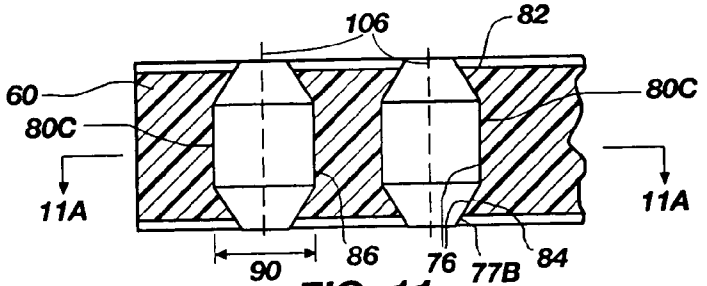


FIG. 11

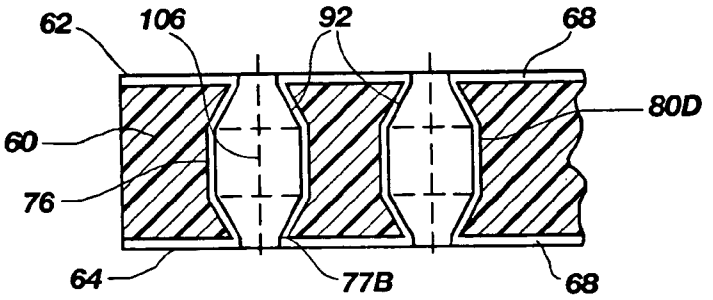


FIG. 12

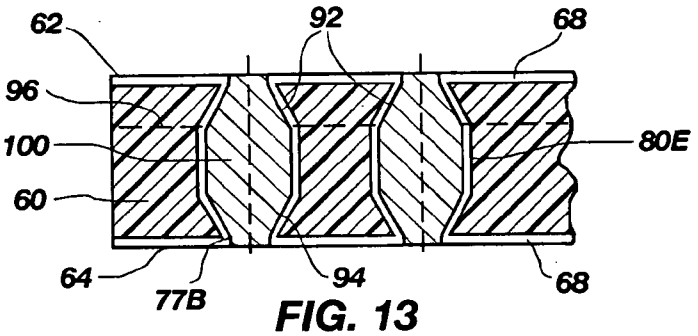


FIG. 13

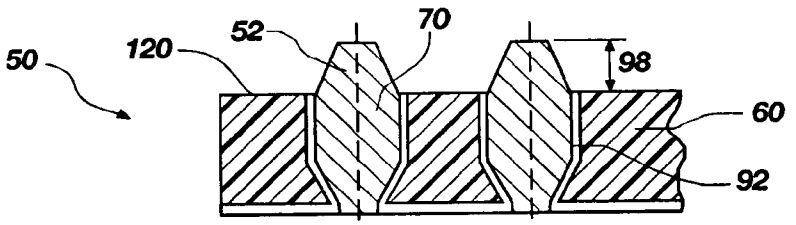


FIG. 14

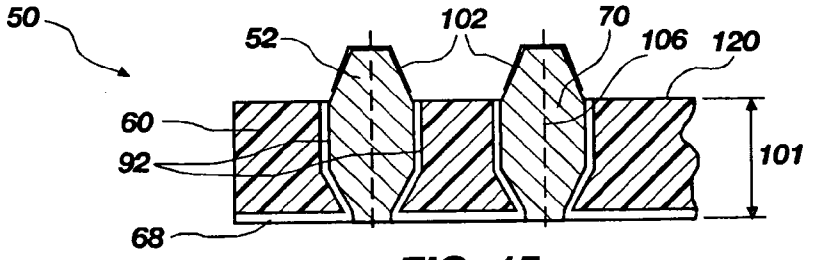


FIG. 15

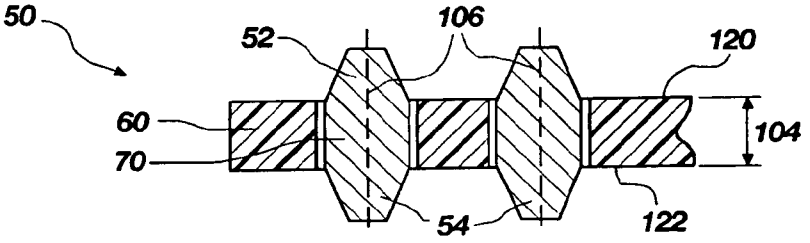


FIG. 16

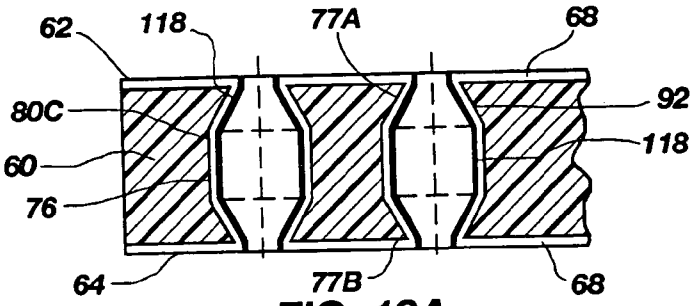


FIG. 13A

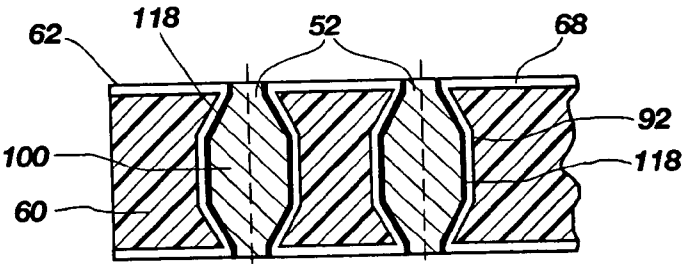


FIG. 13B

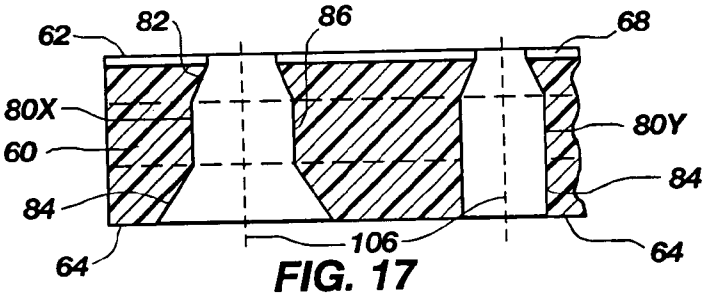


FIG. 17

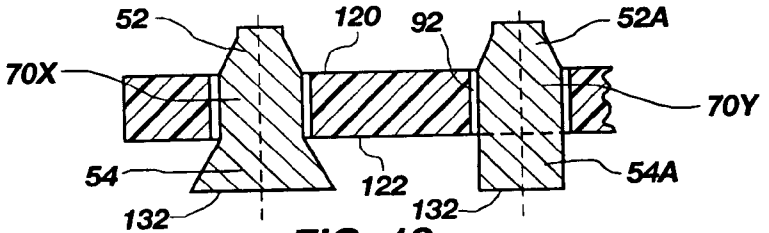


FIG. 18

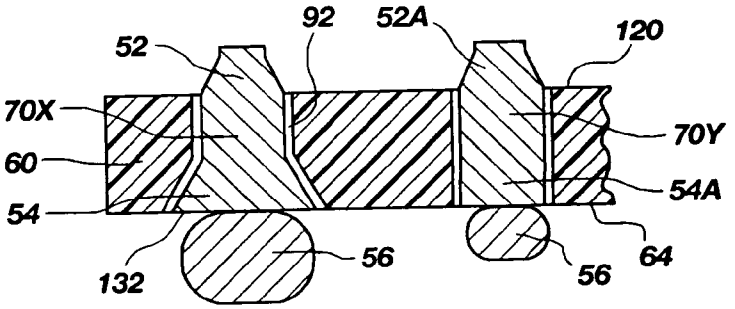


FIG. 19

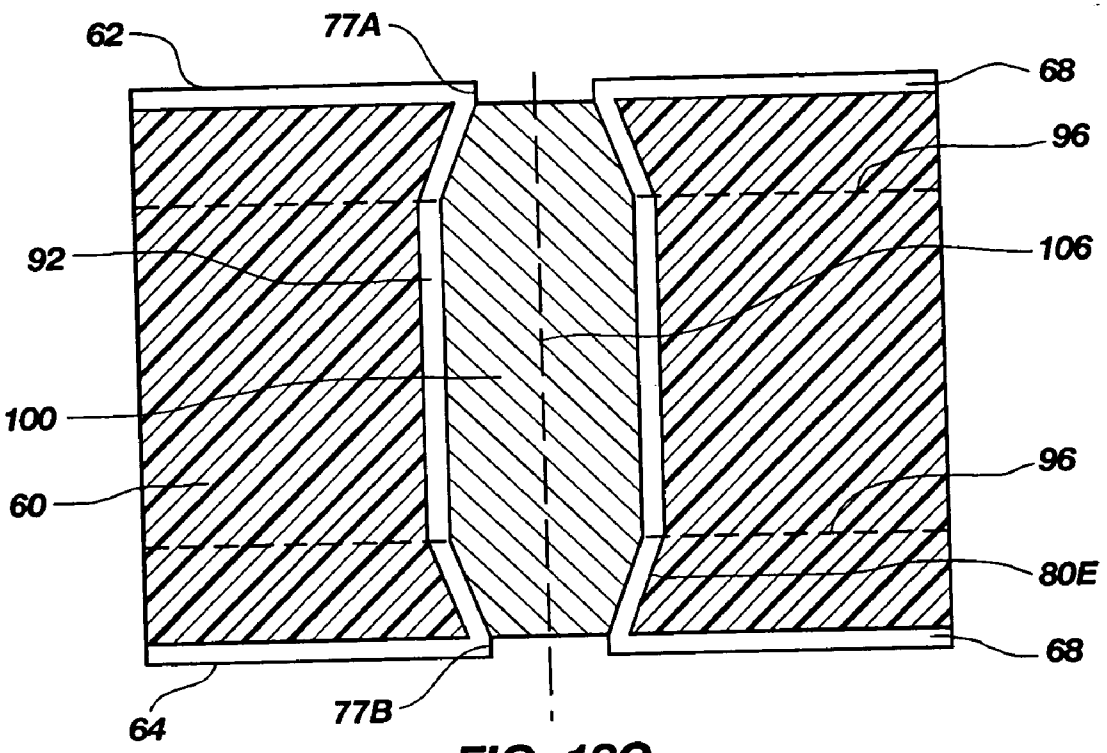


FIG. 13C

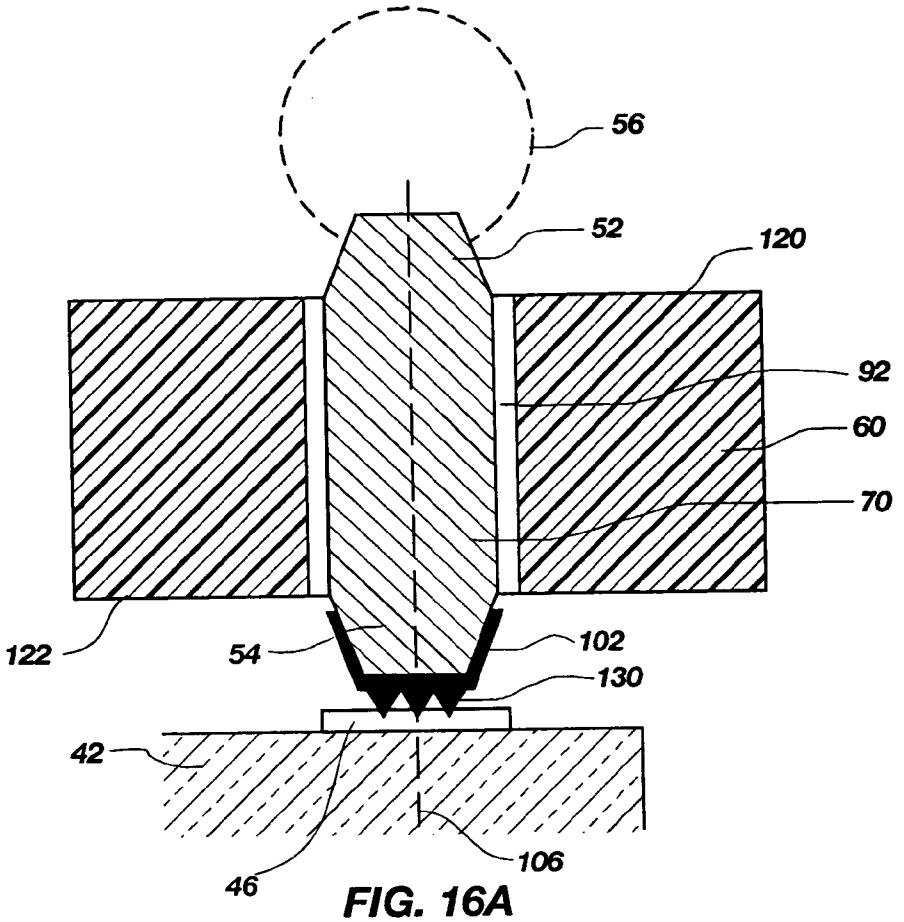


FIG. 16A

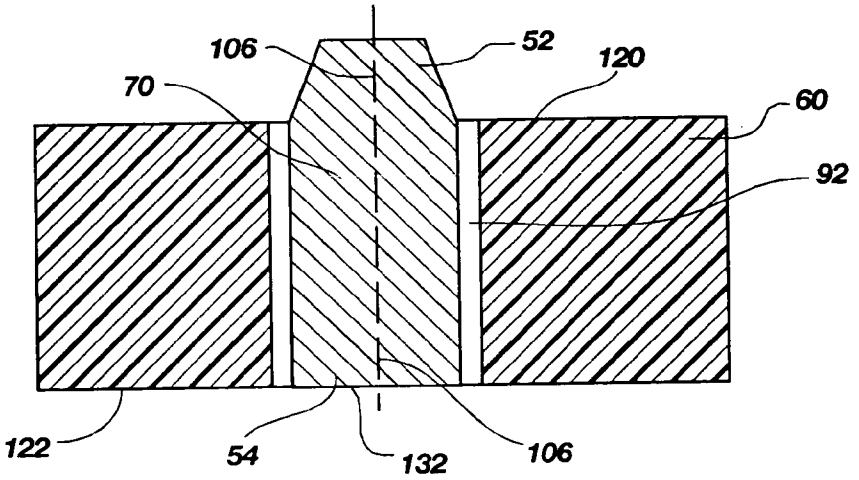


FIG. 16B

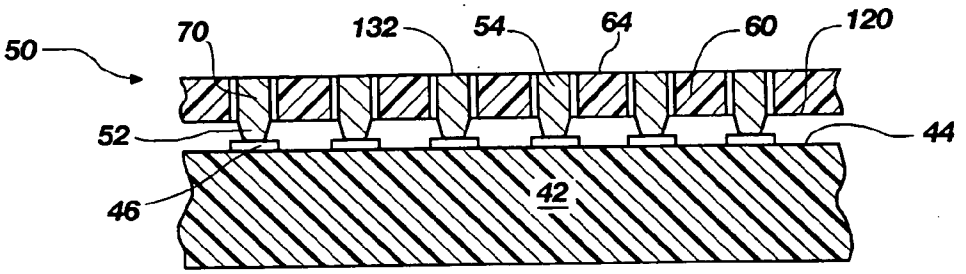


FIG. 20

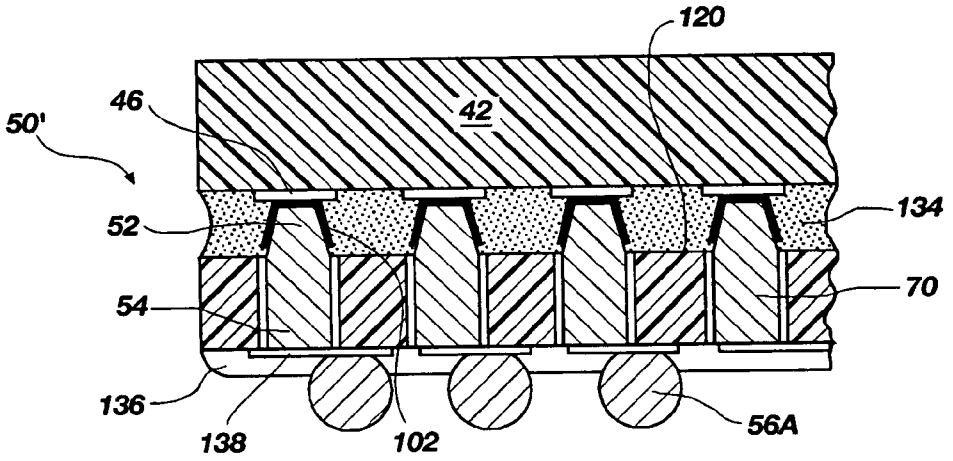


FIG. 21

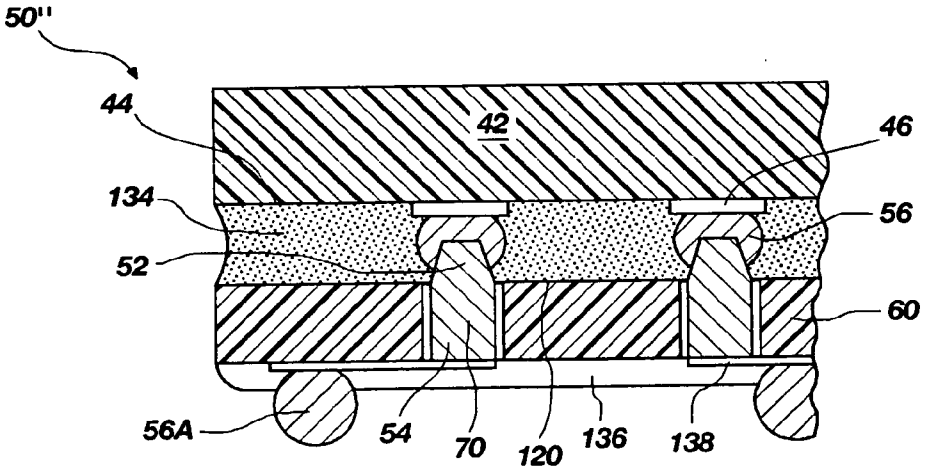


FIG. 22

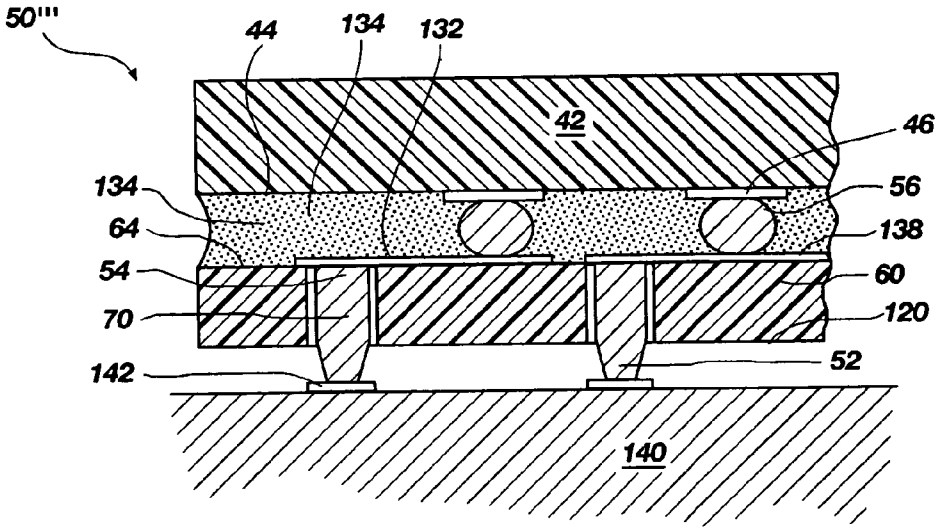

50'''
44
134
132
42
46
134
56
64
138
54
60
70
120
142
52
140

FIG. 23

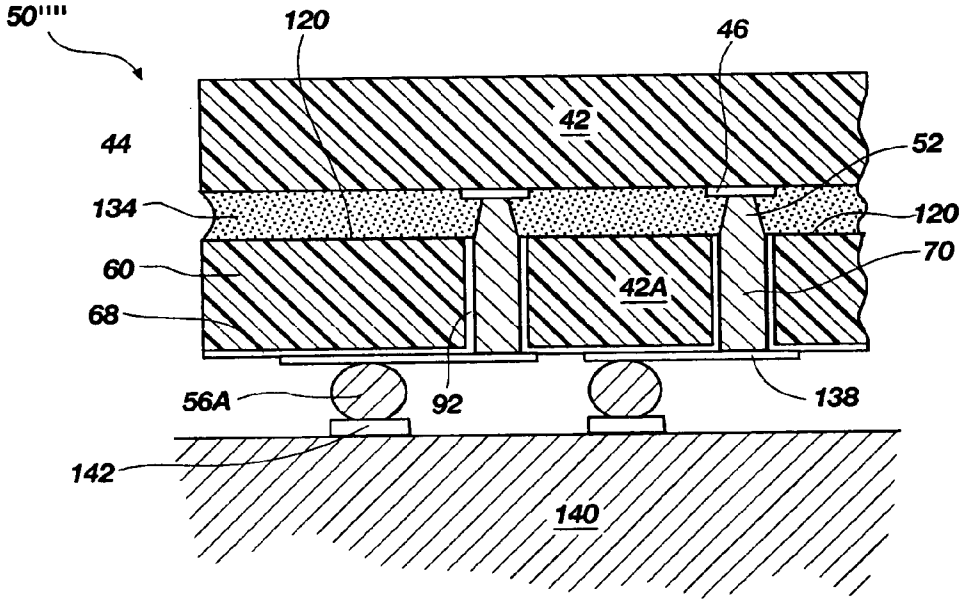

50''''
120
46
42
44
52
134
120
60
70
42A
68
56A
92
138
142
140

FIG. 24

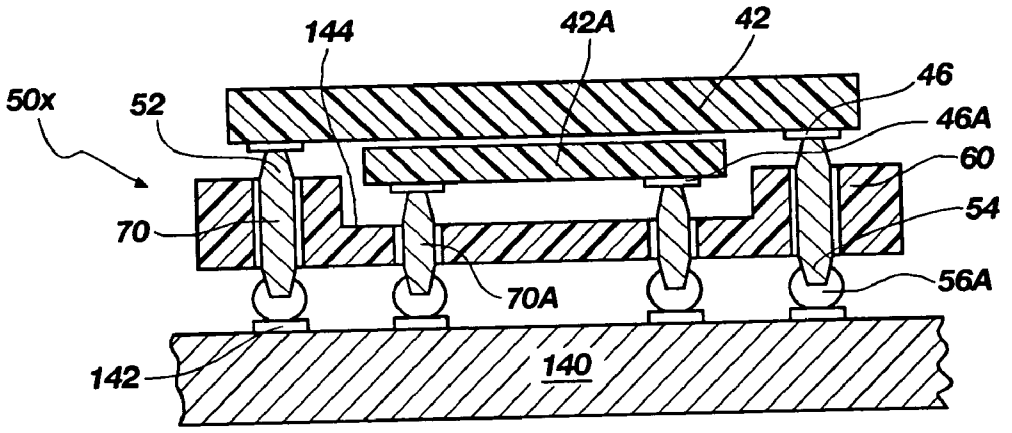


FIG. 25

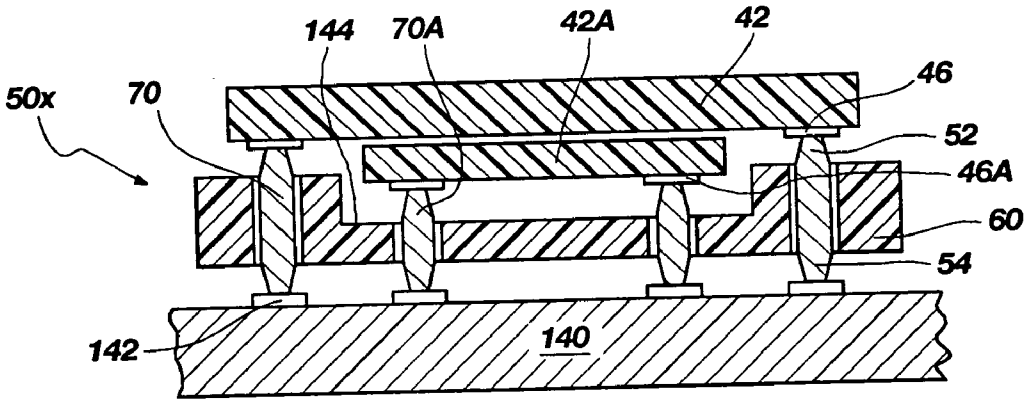


FIG. 26

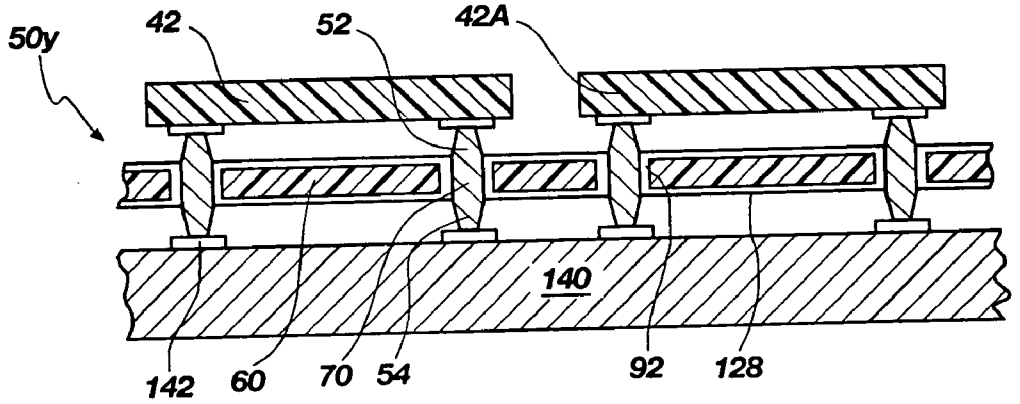


FIG. 27

THROUGH-SUBSTRATE INTERCONNECT STRUCTURES AND ASSEMBLIES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional of application Ser. No. 11/138,544, filed May 26, 2005, pending, which claims the benefit of Provisional Application Ser. No. 60/606,355, filed Aug. 31, 2004.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to methods for forming conductive vias and electrical contact terminals for substrates, such as semiconductor wafers or other bulk substrates or portions thereof, for use as contact cards, test carriers, package interposers and other substrates, and the like, and the resulting structures and assemblies.

[0004] 2. State of the Art

[0005] Semiconductor wafers and portions thereof are used for substrates for contact cards, test carriers, package substrates, and for other purposes. Typically, the portion of such a substrate has circuits formed on one or both sides for the mounting of one or more semiconductor dice thereon, for making electrical contact to active circuitry of semiconductor dice of a wafer to be tested, and for other purposes. Some portions of substrates, including semiconductor wafers, may have vias extending therethrough filled with conductive material for forming interconnects (commonly known as a through wafer interconnect, or TWI) for connecting circuitry on one side of a portion of the semiconductor wafer to circuitry on the other side thereof, or to external circuitry.

[0006] As used herein, a "via" refers to a hole or aperture having conductive material or a conductive member therein which extends through a substrate. The via may be used for electrically connecting a semiconductor device, a component, apparatus, or circuitry on one side of the substrate to a semiconductor device, a component, apparatus, or circuitry on the other side of the substrate. A via may typically be formed in a variety of substrates for a variety of uses, such as interposers for single die packages, interconnects for multi-die packages, and contact probe cards for temporarily connecting semiconductor dice to a test apparatus, for example. For example, a test apparatus is typically configured for temporary simultaneous connection of bond pads of a semiconductor die on a full or partial wafer to the test apparatus. A pattern of conductive vias passing through a substrate employed as a test interposer are designed on one side to match the bond pad patterns of the semiconductor dice on the wafer or portion of a wafer, and on the other side to be connected to the test apparatus.

[0007] Where a via is to be formed through a semiconductive material such as silicon, a prior method for constructing a via includes a first or precursor hole being typically formed by a so-called "trepan" process, whereby a very small router or drill is rotated while being moved radially to create the precursor hole. The precursor hole is larger in diameter than the desired completed via to be formed. Following precursor hole formation, an insulation (dielectric) layer is formed in the hole by either forming a thin silicon oxide layer on the hole's surface by exposure to an oxidizing atmosphere or by coating the hole with a insulative polymeric material after oxidizing the hole. When a polymeric insulative material coating is desired, a suitable polymer such as Parylene™ resin may be vapor deposited over the substrate including within each precursor hole while applying a negative pressure, i.e., vacuum, to the opposite end of the hole. Oxidation of the hole surfaces is required because adhesion of polymer to silicon is relatively poor while adhesion to the oxide is much improved. The insulative polymeric material is drawn into each primary hole to fill the hole. The polymer is then cured, and a small diameter via hole is drilled (by percussion drill or laser) or otherwise formed in the hardened insulative polymeric material. The via hole is then filled with a conductive material, typically a metal, metal alloy, or metal-containing material to provide a conductive path between the opposed surfaces of the substrate. The conductive material of the via is insulated from the substrate itself by the insulative polymeric material. In this method of forming vias, dense spacing of vias is difficult to achieve.

[0008] Another prior art method for forming vias in a semiconductor substrate is illustrated in drawing **FIG. 1A** through **FIG. 1F**. Such a method is also generally illustrated in U.S. Pat. No. 5,166,097 to Tanielian, U.S. Pat. No. 5,063,177 to Geller et al., and U.S. Pat. No. 6,400,172 to Akram et al. Illustrated in drawing **FIG. 1A**, a silicon wafer **2** is provided with a thin layer **4** of silicon dioxide on at least both major, opposing surfaces. A pattern **6** is then formed on the wafer **2** and a mask layer **8** is formed to prevent etching in non-via areas, as shown in drawing **FIG. 1B**. In drawing **FIG. 1C**, etchant has been applied to both major surfaces to form feedthroughs **10** which meet in the middle of the wafer. The wafer **2** is shown with the mask layer **8** removed. A dielectric layer **12** is then formed over the wafer surfaces including the feedthrough side walls, as shown in drawing **FIG. 1D**. In the next act, illustrated in drawing **FIG. 1E**, a metal layer **14** is formed over the dielectric layer **12**. The wafer is illustrated in drawing **FIG. 1F** as having a conductive material (shown in broken lines) placed in the feedthroughs **10** to complete the conductive vias **16**. It is noted that in order to isolate each via, the metal layer **14** must be configured to cover the feedthrough surfaces only, or be subsequently removed from the outer surfaces of the via and wafer.

[0009] As illustrated in U.S. Pat. No. 5,166,097 to Tanielian, in U.S. Pat. No. 5,063,177 to Geller et al., and in U.S. Pat. No. 6,400,172 to Akram et al., the cross-sectional shape of the feedthrough **10** and via **16** is generally that of an hour-glass, with the greatest cross-sectional dimension(s) located at the wafer surfaces. Illustrated in drawing **FIG. 2** is an enlarged portion of drawing **FIG. 1E**. In a preferred embodiment of Tanielian, each half-via **16**A, **16**B is pyramidal in shape, with a side angle **18** of about 54.7 degrees to the plane of wafer **2**. Thus, in this embodiment of Tanielian the minimal ratio of via dimension **30** (of surface **22**) to total via depth **32** (substrate thickness) will be in a range of about 0.45 to about 0.52, which is the reciprocal of the via's aspect ratio. As electronic components are becoming increasingly dense, it is necessary to decrease the lateral size or diameter as well as spacing or pitch of TWIs for increased TWI density. To achieve the desired feature densities for TWIs in future electronic components, the aspect ratio of depth **32** to dimension **30** must be considerably larger than about 2.0 for a given substrate thickness.

[0010] Illustrated in drawing **FIG. 3** is an interposer wherein a method for attaching solder balls/bumps to a via **16** requires that one or both wafer surfaces are mechanically or chemically-mechanically thinned to produce surfaces **34** defining thinned wafer **2**. The removal of material from wafer **2** results in exposure of the side surfaces **24** of the via **16**, to which a solder bump/ball **20** is wetted and bonded, and exposure of the substrate surface **34**. Reflow of a bump/ball **20** results in solder extending about side surfaces **24** of the via **16**. Inasmuch as the outer surfaces **22** of the via **16** significantly overlie the substrate surfaces **34**, the likelihood of inadvertent contact of solder from ball/bump **20** with the surface **34** increases, and shorting of the via **16** to wafer **2** may occur. It therefore becomes a requirement to provide a passivation layer **36** over surfaces **34** proximate solder/bumps/balls **20**, as shown.

[0011] In this type of via-to-bump connection, the bumps/balls **20** are susceptible to cracking, particularly at the corners **26** of the via **16**. Such cracking leads to break-off of solder from the via **16** due to failure of the via-to-bump adhesion. Without the application of a passivation layer **36** on the surface of the substrate, shorting failures are likely to occur.

[0012] In U.S. Pat. No. 6,355,181 to McQuarrie et al., a method is disclosed for making deep trenches having enlarged bottoms or bases. The method comprises applying a mask layer over a substrate, forming a hole in the mask layer and high energy plasma etching anisotropically to a desired depth. A protecting layer is then applied over the hole surfaces and mask layer. Selected portions of the protecting layer are removed from the base surface, and the base is etched to a desired shape.

[0013] It is desirable that the aforementioned disadvantages of the prior art be minimized.

BRIEF SUMMARY OF THE INVENTION

[0014] The present invention comprises methods for forming conductive vias, herein also known as through-wafer interconnects (TWIs), in substrates and resulting structures and assemblies.

[0015] Other features and advantages of the present invention will become apparent to those of skill in the art through consideration of the ensuing detailed description of the invention, the accompanying drawings, and the appended claims.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0016] In the drawings, which depict exemplary embodiments of various features of the present invention, and in which various elements are not necessarily to scale:

[0017] **FIG. 1A** is a cross-sectional depiction of a first act in the formation of conductive vias in a semiconductor substrate in accordance with the prior art;

[0018] **FIG. 1B** is a cross-sectional depiction of a second act in the formation of conductive vias in a semiconductor substrate in accordance with the prior art;

[0019] **FIG. 1C** is a cross-sectional depiction of a third act in the formation of conductive vias in a semiconductor substrate in accordance with the prior art;

[0020] **FIG. 1D** is a cross-sectional depiction of a fourth act in the formation of conductive vias in a semiconductor substrate in accordance with the prior art;

[0021] **FIG. 1E** is a cross-sectional depiction of a fifth act in the formation of conductive vias in a semiconductor substrate in accordance with the prior art;

[0022] **FIG. 1F** is a cross-sectional depiction of a sixth act in the formation of conductive vias in a semiconductor substrate in accordance with the prior art;

[0023] **FIG. 2** is an enlarged cross-sectional view of a conductive via in a semiconductor substrate in accordance with the prior art;

[0024] **FIG. 3** is an enlarged cross-sectional view of a conductive via in a semiconductor substrate according to **FIG. 2** following etchback of substrate surfaces and formation of solder bumps on the via ends;

[0025] **FIG. 4** is an enlarged cross-sectional view of a conductive via and solder bump attached thereto, as taken along line **4-4** of **FIG. 3**;

[0026] **FIG. 5** is a perspective view of a multi-die wafer and a wafer-size contactor card adapted for connecting the wafer bond pads to a test apparatus, in accordance with the present invention;

[0027] **FIG. 6** is a side view of a multi-die wafer and contactor card in accordance with the present invention;

[0028] **FIG. 7** is a cross-sectional view of a portion of a substrate used to form a contactor card in accordance with the invention;

[0029] **FIG. 8** is a cross-sectional view of a portion of a substrate following a primary etch act for via formation in a contactor card in accordance with an embodiment of the invention;

[0030] **FIG. 9** is a cross-sectional view of a portion of a substrate following the formation of precursor holes in a contactor card in accordance with an embodiment of the invention;

[0031] **FIG. 9A** is an enlarged cross-sectional view of a portion of a substrate with a laser-formed precursor aperture through a substrate in accordance with an embodiment of the invention;

[0032] **FIG. 10** is a cross-sectional view of a portion of a substrate following an aperture-enlarging shaping etch act in a contactor card in accordance with an embodiment of the invention;

[0033] **FIG. 10A** is a cross-sectional view of a portion of a substrate following a central aperture-shaping etch act in a contactor card, as taken along line **10A-10A** of **FIG. 10**;

[0034] **FIG. 11** is a cross-sectional view of a portion of a substrate following a rounding-etch act in shaped apertures of a contactor card in accordance with an embodiment of the present invention;

[0035] **FIG. 11A** is a cross-sectional view of a portion of a substrate following a rounding-etch act in shaped apertures in a contactor card, as taken along line **11A-11A** of **FIG. 11**;

[0036] **FIG. 12** is a cross-sectional view of a portion of a substrate following passivation of the surfaces of shaped/

rounded apertures in a contactor card in accordance with an embodiment of the invention;

[0037] **FIG. 13** is a cross-sectional view of a portion of a substrate following filling of the passivated shaped/rounded apertures in a contactor card with a conductive material to form conductive vias in accordance with an embodiment of the invention;

[0038] **FIG. 13A** is a cross-sectional view of a portion of a substrate following the application of a metal layer on the surfaces of passivation layers in shaped/rounded apertures in a contactor card in accordance with an embodiment of the invention;

[0039] **FIG. 13B** is a cross-sectional view of a portion of a substrate of **FIG. 13A** in which a conductive material has been deposited over the metal layers in the shaped/rounded apertures in a contact card in accordance with an embodiment of the invention;

[0040] **FIG. 13C** is an enlargement of a cross-sectional view of a portion of a substrate following filling of the passivated shaped/rounded apertures in a contactor card with a conductive material to form conductive vias in accordance with an embodiment of the invention;

[0041] **FIG. 14** is a cross-sectional view of a portion of a substrate following thinning of one side of a contactor card to expose the via ends in accordance with an embodiment of the invention;

[0042] **FIG. 14A** is an enlarged cross-sectional view of a portion of a substrate following thinning of one side of a contactor card to expose a via end in accordance with an embodiment of the invention, showing attachment to a solder ball/bump;

[0043] **FIG. 15** is a cross-sectional view of a portion of a substrate following the application of a metal to the via ends in a contactor card in accordance with an embodiment of the invention;

[0044] **FIG. 16** is a cross-sectional view of a portion of a substrate following two-sided thinning to expose via ends on both sides in a contactor card in accordance with an embodiment of the invention;

[0045] **FIG. 16A** is an enlarged cross-sectional view of a portion of a substrate following two-sided thinning to expose via ends on both surfaces of a contactor card, showing via end attachment to solder balls/bumps in accordance with an embodiment of the invention;

[0046] **FIG. 16B** is an enlarged cross-sectional view of a portion of a substrate following thinning of a first surface of a contactor card to expose one via end as a stud and in which the opposite via end is exposed as a surface generally coplanar with a second substrate surface according to an embodiment of the invention;

[0047] **FIG. 17** is a cross-sectional view of a portion of a substrate showing aperture formation for constructing a via having differing end configurations in accordance with the present invention;

[0048] **FIG. 18** is a cross-sectional view of a portion of a substrate showing vias with differing end configurations resulting from the aperture formations shown in **FIG. 17** and two-sided thinning, in accordance with embodiments of the present invention;

[0049] **FIG. 19** is a cross-sectional view of a portion of a substrate showing vias with differing end configurations resulting from the aperture formations shown in **FIG. 17** and one-sided thinning, in accordance with embodiments of the present invention;

[0050] **FIG. 20** is a cross-sectional side view of a portion of an exemplary probe card formed of a substrate through which a plurality of vias is constructed in accordance with the present invention;

[0051] **FIG. 21** is a cross-sectional side view of a portion of a single package interconnect or interposer through which a plurality of vias is constructed in accordance with the present invention;

[0052] **FIG. 22** is a cross-sectional side view of a portion of another single package interconnect or interposer through which a plurality of vias is constructed in accordance with the present invention;

[0053] **FIG. 23** is a cross-sectional side view of a portion of a further embodiment of a single package interconnect or interposer through which a plurality of vias is constructed in accordance with the present invention;

[0054] **FIG. 24** is a cross-sectional side view of a portion of a multiple-die interposer/interconnect having a plurality of vias constructed in accordance with the present invention;

[0055] **FIG. 25** is a cross-sectional side view of a portion of another multiple-die interposer/interconnect having a plurality of vias constructed in accordance with the present invention;

[0056] **FIG. 26** is a cross-sectional side view of a portion of an additional multiple-die interposer/interconnect having a plurality of vias constructed in accordance with the present invention; and

[0057] **FIG. 27** is a cross-sectional side view of a portion of a further embodiment of a multiple-die interposer/interconnect having a plurality of vias constructed in accordance with the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0058] In the present invention, semiconductor wafers or portions thereof and substrates and components in which vias are to be formed are identified herein as "substrates" regardless of the purpose of the via or material of construction of the substrate or via. Thus, for example, the term "substrate" is used in reference to semiconductor wafers, semiconductor wafer portions, other bulk semiconductor substrates, semiconductor devices, interposers, probe test cards, and the like. The invention will be illustrated as applied to construction of a silicon, wafer-scale test card, and methods of making such vias in a wide variety of components are described, as well as the resulting components so made and associated structures and assemblies. The vias made by methods of the present invention have via ends which may be configured to have projecting ends comprising mesas or pillars of reduced size, flared or enlarged ends, or a combination thereof.

[0059] One exemplary embodiment of the method of the invention may be generally described as comprising (a) providing a semiconductor substrate with a mask layer of

oxide or nitride on one or both major surfaces, (b) laser-drilling a precursor aperture completely through the substrate and mask layers, to provide a heat-affected zone of substrate material shielded by the overlying mask layer on one or both sides of the substrate, (c) subjecting the precursor aperture to shape etching, to remove the heat-affected material, leaving an aperture having an enlarged portion in the center of the substrate, tapering to at least one smaller aperture opening, and having a generally square cross-section, (d) lining the etched aperture with a passivation material, (e) filling the passivated aperture with a conductive via material to produce the conductive via, and (f) thinning the substrate on one or both sides to expose via end(s) having a generally trapezoidal shape. Optionally, an additional rounding etch act following the shaping etch rounds the corners of the shape-etched aperture, producing a via end with a frustoconical shape. The substrate may be thinned by etching, by a mechanical abrasion process or a chemical-mechanical polishing or planarization (CMP) process to expose the via end (contactor end or stud) to a desired standoff distance.

[0060] Optionally, the precursor hole may be formed by anisotropic etching from one or both surfaces of the substrate.

[0061] The shape etching may be conducted with a tetramethyl ammonium hydroxide (TMAH) solution, which results in a distinctive undercut of the opening in the mask layer. The precise shape of a resulting via end varies, depending upon laser strength and duration as well as etch strength and duration, and other factors.

[0062] The shaped aperture, or shaped-and-rounded aperture is filled with a conductive material which may comprise a metal, metal powder, a metal or alloy powder, a flowable conductive photopolymer, a thermoplastic conductive resin, resin-covered particulate metal material, or other suitable material which may be used to form a solid conductive via. The shaped aperture or shaped-and-rounded aperture may be filled with the conductive material or first coating the aperture walls with a metal, followed by filling of the aperture.

[0063] The method of the invention may be used to form via hole or aperture diameters of conventional size, i.e. about 17 μm to about 150 μm, as well as much smaller via holes or apertures applicable to enhanced miniaturization of the future. The via holes or apertures are formed to produce trapezoidal or frustoconical via ends which may be directly attached to bond pads or optionally to solder bumps/balls.

[0064] The method of the invention provides substantial advantages. First, very small diameter vias may be formed in a dense pattern in a semiconductor substrate. The vias may be rapidly and precisely formed. The shape of the via ends of the via holes or apertures is enhanced to enable direct attachment to small, finely pitched bond pads. If the via ends are employed with solder balls/bumps, the danger of ball cracking, solder shorts, etc. is much reduced in comparison to the state of the art. Inasmuch as a non-conductive layer may girdle the via ends, and solder wetting and bonding areas do not generally overlie the bare substrate, further passivation of the substrate area surrounding the vias is typically unnecessary.

[0065] The invention will be illustrated as applied to construction of a silicon wafer-scale test card having vias and methods of making such vias in a wide variety of components are described, as well as the resulting components so made. The vias made by methods of the present invention have via ends which may be configured as projecting or protruding ends comprising mesas or pillars of reduced size.

[0066] In the present invention, methods are illustrated for forming conductive TWIs (also known as vias and feedthroughs) in substrates of semiconductor material with improved configurations of their ends or contacts. As illustrated in drawing **FIGS. 5 and 6**, a wafer test contactor card **50**, also commonly termed a "probe" card, may be produced for the testing of a large number of integrated circuit or semiconductor dice **42** in, for example, a substrate comprising a silicon wafer **40**. The semiconductor dice **42** are fabricated in wafer **40** for subsequent separation along cut lines **48**. As illustrated in drawing **FIG. 6**, the contactor card **50** may have a large number of vias or TWIs **70** having first ends **52** which are aligned with corresponding bond pads **46** on the active surface **44** of each die **42** of the wafer **40**. The first ends **52** and second ends **54**, also called stud ends herein, are shown as having a generally truncated pyramidal or truncated conical shape, in contrast to the shape of prior art studs previously described. The first ends **52** of vias **70** may be configured to directly contact bond pads **46**, or to accommodate the attachment of solder or other metallic "balls" or "bumps"**56**, or to be joined to metal traces or wires or other types of conductive structures of semiconductor dice **42**. The second ends **54** as illustrated in drawing **FIG. 6** may be provided with metallization in the form of conductive lines **58** as shown in broken lines to connect to a test apparatus, not shown. Moving the contactor card **50** in the direction **49** to temporarily contact the metallic balls **56** with the bond pads **46** on the wafer's active surface **44** permits very rapid testing of each semiconductor die **42** on the wafer **40** for operability. Of course, first ends **52** may be employed to directly contact bond pads **46**.

[0067] Use of the methods of the invention enables small via diameter and pitch, i.e. spacing. Small via spacing may be achieved with high precision (accuracy) and with small feature dimensions, i.e. resolution with high repeatability. The end shape(s) of the vias **70** enables use of solder balls/bumps **56** thereon without the cracking problems with acute angled ends. Smaller solder connections may be used for permanent connections than is possible in the state of the art. Alternatively, the via ends **52** and/or **54** may be directly contacted with a bond pad **46** or other metallization, or bonded thereto, without using intervening solder balls/bumps **56**. Thus, the sizes of bond pads **46** may be significantly reduced, i.e., reduced to 5×5 microns or even as small as 2×2 microns, and the size of solder balls, if used, may be correspondingly reduced.

[0068] Generally illustrated in drawing **FIGS. 7 through 14**, are acts common to each of the embodiments of the inventions as illustrated herein, comprising (a) providing a substrate **60** of semiconductor material, (b) providing a dielectric etch mask layer **68** on at least one surface **62**, **64** of the substrate **60**, (c) forming a precursor aperture **80**A through the substrate **60** and etch mask layer(s) **68**, (d) conducting a shaping etching to form a shaped aperture **80**B with lateral enlargement in a central region **108** and sloped etch portions **110**, **112** extending from the central region **108** to terminate at an etch mask layer **68**, (e) optionally, con-

ducting a "rounding" etch to change the aperture's cross-sectional shape from square to rounded, (f) providing a passivation layer **92** over the side wall surfaces **76** of the shaped aperture **80**B or rounded aperture **80**C, (g) filling the passivated aperture with one or more conductive materials **100** to form a conductive via (TWI) **70**, and (h) thinning one or both surfaces **62**, **64** of the substrate **60** to expose the end(s) **52**, **54** of the conductive via **70**. In the manufacture of articles in the form of through wafer interconnects or vias **70** of the present invention, each of the acts (a) through (h) and modifications thereof of the various embodiments of inventions are discussed in further detail, infra. It is understood that the terms "upper" and "lower" are used herein to define opposed positions of a substrate surface, via ends, and the like, rather than the actual position thereof. Likewise, the terms "first" and "second" do not refer to a specific orientation.

[**0069**] Referring to drawing **FIG. 7**, a substrate **60** of a semiconductor material such as, for example, a silicon wafer is illustrated having a first surface **62** and a second surface **64**, both of which are covered with an etch mask layer **68** such as silicon dioxide or nitride. Depending upon the desired configuration of the via, one of the surfaces **62**, **64** may be left unmasked and unpassivated to produce a larger, even flared via end as described, infra. The substrate **60** is illustrated as a semiconductor wafer with total thickness **66** and configured for the creation of vias **70** having central axes **106** and pitch **72**. While the examples shown herein relate primarily to silicon or semiconductor wafers, the methods described herein may be used to form conductive vias **70** in other semiconductor materials.

[**0070**] As illustrated in **FIG. 9**, precursor apertures **80**A are formed in the substrate **60** and pass completely through the substrate about central axes **106**. In one embodiment, the precursor apertures **80**A are formed by laser cutting or ablation through the substrate **60** including outer etch mask layers **68** using a laser beam **124**, as illustrated in **FIG. 9A**. The apertures **80**A are shown in this embodiment of the invention having a generally uniform cross-section along axis **106**. The cross-sectional shape of the precursor apertures **70** may be generally square, oblong or circular. The laser power, duration and beam focus are controlled as known in the art to produce a generally uniform aperture **80**A of the desired shape. The width **78** of the resulting aperture openings **77** may be as narrow as obtainable by laser ablation. For example, aperture opening widths **78** as narrow as about 17 to about 30 μm may be precisely formed with current state-of-the-art laser equipment. However, the minimum usable opening width **78**A may be limited by the ability to effectively passivate the internal side wall surface **76** of the completed aperture and fill the aperture with electrically conductive material through a small opening, particularly when the aperture has a high depth-to-diameter ratio.

[**0071**] In an alternative embodiment of the invention, an act (see **FIG. 8**) prior to the structure depicted in **FIG. 9** replaces laser cutting with an etching act. As illustrated in drawing **FIG. 8**, guide holes **74** are first formed, e.g., etched in the etch mask layers **68** about axes **106**. The precursor aperture **80**A is then formed (**FIG. 9**) by dry anisotropic etching of silicon from one or both surfaces **62**, **64** of the substrate **60**. Dry anisotropic etching, commonly known as reactive ion etching (RIE), is well known in the art.

[**0072**] Whether the precursor aperture **80**A is formed by laser ablation or etching, the next major act, illustrated in drawing **FIG. 10**, comprises a shaping etch to remove silicon surrounding precursor aperture **80**A and laterally etch the precursor aperture **80**A. Where the precursor aperture **80**A is formed by laser, the substrate's silicon outside of the immediate aperture **80**A is heat-damaged (commonly termed a "heat-affected zone," or "HAZ") which may enhance removal of the material by etching. As illustrated in drawing **FIG. 9A**, the heat-affected zone **81** includes a central zone **81**A with substantially uniform cross-section and end zones **81** B between the central zone and the etch mask layers **68**, wherein the degree of undercutting of silicon is approximately proportional to the distance from the etch mask layer **68**.

[**0073**] A preferred method of using a shaping etch comprises the application of tetramethyl ammonium hydroxide (TMAH) as a 9:1 ratio of TMAH solution to deionized (DI) water. The TMAH solution is available as a six percent (6%) solution of TMAH in propylene glycol, which may be used without damage to wafer circuitry, as it does not degrade metallization. The etchant is applied by submersion of substrate **60** into a heated wet process tank full of the aforementioned TMAH and DI water solution. The cross-section of the shaped aperture **80**B so formed is generally square (see **FIG. 10A**) rather than circular, because the TMAH etchant solution is preferential to 100 or 011 crystallographic orientations of the silicon. The end portions **82**, **84** of the shaped aperture **80**B are thus generally trapezoidal in shape, with outer corners **83** and base width **88** (which also defines the width of central via portion **86**) and opening width **78**. Other etching systems may be alternatively used, including for example, dry "Bosch" style etching using an inductively coupled plasma for deep silicon etching and the aforementioned dry RIE process, as well as other known etch processes suitable for the material of substrate **60** such as, for example, the Advanced Silicon Etch process offered by Surface Technology Systems. HF solutions and KOH solutions as well as more concentrated TMAH solutions are suitable etchants for silicon, but may require masking of selected portions of substrate **60** to avoid damage to metallization. Aperture shapes will vary depending upon the etching system employed and the material and crystallographic orientation of the material of substrate **60**.

[**0074**] A shaped aperture **80**B may alternatively be formed by a variation of a method for forming enlarged aperture regions of a deep trench or hole. As described in U.S. Pat. No. 6,355,181 to McQuarrie, a masked substrate is etched using a fluorine-containing etchant gas or vapor in the absence of a plasma through an opening in the mask to a desired depth with a base. A layer of protecting material is applied to the base and surfaces of the hole and mask, then removed from the base of the hole. Further etching is conducted to enlarge the hole in the region of the base. This method may be used to selectively shape an aperture to a configuration of this invention. The disclosure of the U.S. Pat. No. 6,355,181 to McQuarrie is incorporated herein by reference.

[**0075**] Where a via end **52**, **54** is to have a discrete conductive element in the form of a solder ball/bump **56** bonded thereto, producing stress points at comers **83**, the shaped aperture **80**B may be subjected to a further rounding-etch act, producing a more circular via **70** and virtually

eliminating the comers. As illustrated in drawing **FIGS. 11 and 11**A, an isotropic etch results in a more circular aperture **80**C with rounded openings **77** of diameter **78**B and enlarged central portions **86** of diameter **90**. Various etchants may be utilized, including for example, a wet etch with a combination of ammonium fluoride, phosphoric acid, hydrogen peroxide and DI water. Other isotropic etchants may alternatively be used to achieve uniform etching in all directions, including a dry etch with either hydrobromic acid (HBr) or $HBrO_2SF_6$. Thus, substantially frustoconical via ends **52**, **54** may be produced.

[**0076**] In the next act illustrated in drawing **FIG. 12**, an insulative (passivation) layer **92** is deposited or formed on the side wall surfaces **76** of the shaped aperture **80**B or shaped and rounded aperture **80**C, creating passivated aperture **80**D in preparation for metallizing the aperture. The passivation layer **92** may comprise silicon oxide, silicon nitride, or another material, including one of a wide variety of organic (polymeric) materials which are available for passivation. The material may be applied by chemical vapor deposition (CVD) or other deposition method. An oxide layer may be formed by oxidation of the material of substrate **60**, or deposition. Any effective method for forming a thin passivation layer **92** on the aperture side wall surfaces **76** may be utilized. In general, it is unnecessary to passivate the substrate surfaces **62**, **64** after the aperture is formed, inasmuch as at least one surface is already passivated by the etch mask layer **68**, and subsequent removal of etch mask layer **68** in a thinning act renders the extra application act valueless. Furthermore, the passivation layer **92** extends to each end **52**, **54** of the aperture **80**B, **80**C of the unthinned substrate **60** to insulate the conductive material of via **70** which is to be formed.

[**0077**] As illustrated in drawing **FIG. 13**, the passivated aperture **80**D is then "metallized" by filling with a conductive material or materials **100**, forming a conductive pathway or via **70** spanning the thickness of the substrate **60**. The particular conductive material(s) **100** may vary, and the method of deposition may also vary. For example, the conductive filler material **100** may comprise a solder such as a tin/lead material, or copper, nickel, silver, tungsten, or other metal or alloy. Electroplating or electroless plating techniques may be used to fill passivated aperture **80**D. Copper, aluminum and other metals may also be deposited by a metalorganic chemical vapor deposition (MOCVD) process. Alternatively, the conductive material may comprise a conductive polymer or conductive material entrained in a polymer, such as conductive or conductor-filled epoxy. The polymer may be placed in a passivated aperture **80**D by needle dispenser, chemical vapor deposition (CVD) or other means known in the art, and cured to a solidified state. Nano-size particles of a metal, such as silver, in an organic carrier may also be placed in the aperture **80**D and converted to a cohesive solid by heating methods known in the art. Conductive material-filled aperture **80**E is depicted in **FIG. 13**.

[**0078**] Any appropriate method for filling a narrow aperture with the particular material **100** may be used. In one example, illustrated in drawing **FIG. 13A**, the surfaces **94** of passivation layer **92** are first coated with a thin layer of nickel, copper or tungsten as a "seed layer"**118** by an appropriate method such as chemical vapor deposition (CVD) or plasma-enhanced chemical vapor deposition (PECVD), and then (see **FIG. 13B**) the aperture is filled with a conductive material **100**, by an electroless deposition process, for example. Alternatively, a metal seed layer **118** may be deposited on surfaces **94** of the passivation layer **92** and a metallic filler conductive material **100** applied by electroplating within the aperture **80**D, or an electrode placed across one side of substrate **60** and electroplating effected thereon to fill passivated aperture **80**D from one end thereof.

[**0079**] The latter approach is especially suitable for probe cards, where the second via end **54** is to be generally coplanar with the second surface **64**, as the bottom aperture opening **77**B may be closed off with a conductive plate, not shown. A conductive metal filler material **100**, such as copper, is then electroplated from a solution entering top aperture opening **77**A upwardly from the bottom to fill passivated aperture **80**D.

[**0080**] Where the conductive material **100** is solder, dip or wave soldering may be employed to fill the passivated aperture **80**D. Further, a solder ball may be placed over each passivated aperture **80**D, heated to reflow and then drawn, as by a vacuum or by capillary action if passivated aperture **80**D is lined with a solder-wettable material, into apertures **80**D. Alternatively, a solder paste may be stenciled or squeegeed into the apertures **80**D followed by heating to reflow the solder and drive off organics and cooling to solidify the solder alloy. Illustrated in drawing **FIG. 13**, the degree to which the first surface **62** is to be thinned in a following act is indicated as thinning line **96**.

[**0081**] Turning now to drawing **FIG. 14**, the next act is seen to be a thinning of first substrate surface **62** (to thinning line **96** of **FIG. 13**) to expose the first ends **52** of vias **70** as studs projecting from bare thinned line **120**, resulting in a substrate thickness **101**. Thinning may be conducted by conventional methods such as etching, backgrinding or abrasive CMP techniques, as known in the art. The opposing substrate surface **54** may also be thinned to expose the second ends **54** of vias **70** as studs projecting from bare thinned surface **122**, as shown in **FIG. 16**. The substrate **60** itself is thus further thinned to a thickness **104**. While the via ends **52** are configured to produce an improved connection with solder balls/bumps, these structures may, alternatively, be used when substrate **60** is configured (for example) as a probe card for direct contact with a conductor e.g., bond pad or other metallization of a semiconductor die, provided that the standoff distance **98** (see **FIG. 14**) is sufficient. In the present state of the art, thinning a substrate surface **62** to produce a standoff distance **98** of about 300 μm meets the above criteria, enabling via end-to-bond pad contact without the presence of an intervening solder ball or solder bump.

[**0082**] Following via formation and substrate thinning, one or both of exposed, protruding via ends **52**, **54** may be coated with a metal overlay **102** such as copper, silver, gold, tungsten or nickel. Typically, nickel may be used to coat a via end **52**, **54** to be contacted with solder or a via end **52**, **54** comprising solder. A copper via end **52**, **54** may, for example, be plated with gold. Such a coating of via end **52** is illustrated in drawing **FIG. 15**. The particular overlay metal may be chosen and applied to provide an electrical connection which is of low resistance and ohmic, and which may enhance cohesion between a via end **52** or **54** and a bond pad **46** or metallization of a semiconductor die, not

shown in this figure. The via end **52**, **54** may, optionally, include at least one raised projection **130** configured to contact and/or penetrate bond pads **46**, as depicted in **FIG. 16A**. Such projections **130** may be formed on a via end **54**, for example, by methods described in U.S. Pat. No. 5,541,525 to Wood et al., assigned to the assignee of the present application, the disclosure of which is incorporated herein by reference thereto. For example, the raised projections **130** may comprise sharp spurs, rounded domes, or otherwise shaped projections which enhance connection to a bond pad or other metallization. In the example illustrated in drawing **FIG. 16A**, the opposite via end **52** is shown as being bare, i.e. without a metal overlay **102** or raised projections **130** thereon.

[**0083**] As illustrated in drawing **FIG. 14A**, a solder ball or bump **56** may be attached to a first projecting via end **52** for electrical connection to a bond pad or metallization of another component. The exposed portion of second, opposed via end **54** may be connected to a conductive member, not shown, such as a solder ball/bump, wire bond, etc. Because of passivation layer **92** about the periphery of via ends **52**, **54**, it may not be generally necessary to provide a further passivation layer **128** as shown in **FIG. 14A** on the thinned substrate line **120** and/or surface **122**. However, in particular applications where shorting is likely to occur, a passivation layer **128** may be applied to the thinned line **120** and/or surface **122** to prevent such shorting. It is further contemplated that passivation layer **92** may remain on projecting via ends as shown in broken lines to constrain the wetting of conductive member such as a solder ball/bump to the distal end surfaces of via ends **52**, **54**, so that a smaller solder ball/bump **56'** may lie over the end surfaces, again as shown in broken lines.

[**0084**] As illustrated in drawing **FIG. 16B**, one embodiment of the invention includes the full exposure of one via end **52**, and the opposite via end **54** may be leveled, typically during the substrate thinning as effected by planarization, to have an end surface **132** which is approximately co-planar with thinned surface **122**. Alternatively, thinning may be effected so that via end **54** exhibits a positive standoff less than would otherwise occur with full thinning to thinned surface **122**.

[**0085**] The methods of the invention may be used to produce via end configurations which are non-uniform, that is, one via end **52** differs from the opposite via end **54** in shape, size, standoff distance, composition or other configuration variable. Illustrated in drawing **FIG. 17** is a first shaped via aperture **80**X having a first end portion **82** configured as a reduced stud, and a second end portion **84** flared in accordance with the prior art. The shaped via aperture **80**X may be formed by a combination of laser cutting from both surfaces **62**, **64**, followed by etching to complete the internal via shape. Alternatively, etching of a substrate **60** having no aperture mouth constraining etch mask layer on surface **64** may be conducted to produce the indicated aperture shape. A semi-isotropic etch using TMAH for example, will produce an aperture resulting in a flared via end. The substrate may be left unthinned, or be thinned as previously described to produce a projecting via end portion **84**. The completed via ends **52**, **54** are illustrated in drawing **FIG. 18** with respect to via **70**X. In the second shaped via aperture **80**Y illustrated in drawing **FIG. 17**, the second via aperture end portion **84** has a "post" configuration of uniform cross-sectional dimensions, as formed by anisotropic etching from one or both surfaces **62**, **64** (without an etch mask layer **68** over surface **64**), or by laser cutting from via end **52** followed by etching, all without an etch mask layer **68** over surface **64**. The resulting via **70**Y having via ends **52**A and **54**A is depicted in **FIG. 18**. As already described in relation to drawing **FIG. 16B**, the via end **54** may be leveled or thinned in the thinning act of second substrate surface **64** to a reduced stand-off distance **98** (see **FIG. 14**).

[**0086**] The substrate surface **64** may alternatively be left unthinned, so that via ends **54** remain substantially within the substrate **60**, separated therefrom by passivation layer **92**. As shown in **FIG. 19**, the end surfaces **132** of the second ends **54**, **54**A are exposed for connection to solder balls/bumps **56** as shown, or to metallization layers or other connecting structures, not shown.

[**0087**] It is important to note that the various configurations of via ends **52** and **54** may be utilized in any combination in a substrate **60** to achieve a desirable connection result.

[**0088**] Illustrated in drawing **FIGS. 20 through 27** are various types of apparatus which may be formed by use of the via interconnections of the invention. These embodiments of the invention are not exhaustive in nature, but are merely examples.

[**0089**] Illustrated in drawing **FIG. 20**, the substrate **60** with vias **70** comprises an exemplary wafer test contactor, or probe, card **50** of the invention. The first ends **52** of the vias **70** comprise contactors of the invention for temporary direct contact with bond pads **46** on the active surface **44** of a semiconductor die **42**. The active surface **44** of semiconductor die **42** is generally parallel to the opposing thinned line **120** of the probe card **50**. The opposing via ends **54** are shown having exposed surfaces **132** generally coplanar with substrate surface **64**, for connection to a test circuit, not shown, via metallization traces, wire bonds, or the like. Although the via ends **54** are shown as being proximate an unthinned surface **64** of the substrate **60**, it is understood that the substrate surface **64** may be thinned to expose via ends **54** and achieve a similar projecting result as with via ends **52**, as illustrated in drawing **FIG. 16B**.

[**0090**] Illustrated in drawing **FIG. 21** is a single package application of the invention in which bond pads **46** of a semiconductor die **42** are directly joined to conductive via ends **52**, which may comprise a metal or alloy, of a substrate **60** of a package interconnect or interposer **50'**. The opposed ends **54** of the vias **70** are connected to metallization traces **138**, the distal ends of which are connected to discrete conductive elements in the form of, for example, solder balls **56**A, for attachment to terminals of a circuit board or the like. Substantially flat end surfaces of via ends **52** are shown with a metal overlay **102** to enhance contact with bond pads **46**, metal overlay **102** extending down a portion of the sides of via ends **52**. An insulating dielectric material **134** is placed in the space between the semiconductor die **42** and package interconnect or interposer **50'**. In addition, a polymeric packaging layer **136** is shown surrounding the external balls/bumps **56**A.

[**0091**] Illustrated in drawing **FIG. 22**, another form of a single package interconnect or interposer **50"** is shown

which differs from the embodiment of the invention illustrated in drawing **FIG. 21** in that the die bond pads **46** are connected to the via ends **52** through discrete conductive elements in the form of solder balls/bumps **56**. Like the package interconnect **50'** illustrated in drawing **FIG. 21**, discrete conductive elements in the form of external solder balls/bumps **56**A are connected to via ends **54** by metallization traces **138**.

[**0092**] A further variation of single package interconnect or interposer **50'''** is illustrated in drawing **FIG. 23**, having a substrate **60** with vias **70** passing therethrough. First via ends **52** are frustoconical or trapezoidal in shape, i.e. are mesa-shaped, as prepared by the method of this invention, and are shown directly impinging on contact sites **142** on a circuit board or other carrier substrate **140**. The second surface **64** of the substrate **60** is shown as being unthinned, whereby only the end surface **132** of each via **70** is accessible for metallization traces **138**. Discrete conductive elements in the form of solder balls or bumps **56** are bonded to the metallization traces **138** and bond pads **46** on the active surface **44** of semiconductor die **42**. As shown, a dielectric material **134** may be disposed in the volume between semiconductor die **42** and interposer **50'''**.

[**0093**] Another use of TWIs or vias **70** of the invention is illustrated in drawing **FIG. 24**, wherein the vias **70** pass through non-active regions of a second semiconductor die **42**A, connecting bond pads of a first semiconductor die **42** to conductive sites **142** on a circuit board **140**. The substrate **60** identified as a second semiconductor die **42**A may, alternatively, comprise an interconnect substrate or interposer **50''''**. The interconnect substrate or interposer **50'''** is shown in this embodiment as being inverted, when compared to the embodiment of the invention illustrated in drawing **FIG. 23**. Thus, first via ends **52** (frustoconical or trapezoidal) are shown as being in contact for temporary electrical connection to a semiconductor die **42** in a full-wafer or partial-wafer stage. Second via ends **54** are in contact with metallization traces **138**. As illustrated in drawing **FIG. 23**, the volume between semiconductor die **42** and substrate **60** is shown as having been filled with a dielectric material **134**.

[**0094**] Illustrated in drawing **FIGS. 25, 26** and **27** are three exemplary configurations of a multi-die interconnect or interposer **50***x*, and **50***y*, respectively, for connecting a first semiconductor die **42** and a second semiconductor die **42**A to a carrier substrate **140** such as a circuit board, etc. In **FIGS. 25 and 26**, a multi-level interconnect **50***x* has a further thinned, recessed region **144** for accommodating a second semiconductor die **42**A. Vias **70** and **70**A are provided for respective connection to bond pads **46** of the first semiconductor die **42** and bond pads **46**A of the second semiconductor die **42**A, and for direct connection or (as shown) discrete conductive element connection in the form of solder balls/bumps **56**A to a carrier substrate **140** such as a circuit board. The via ends **52**, **54** are uniformly shown as having the trapezoidal or frustoconical shapes. Optionally, some of the via ends **52**, **54** may be of the flared or post configuration as described previously. In drawing **FIGS. 25 and 26**, the semiconductor dice **42**, **42**A are superimposed or "stacked," while in drawing **FIG. 27**, the semiconductor dice **42**, **42**A are arranged to be substantially coplanar on interconnect **50***y*. In each of these embodiments, additional semiconductor dice may be accommodated by additional stacking or co-planar additions.

[**0095**] Other applications of an interconnect or interposer are contemplated, by use of variations in via end configurations, die orientation, numbers of dice, and the like.

[**0096**] The methods presented herein enable a small via aperture diameter to be formed, with a small pitch (spacing), high precision alignment and high resolution of features. Solder connections may be readily formed at dimensions smaller than currently used. It is believed that the invention enables the use of die bond pads as small as about 2×2 microns.

[**0097**] Although the foregoing description contains many specifics, these should not be construed as limiting the scope of the present invention, but merely as providing illustrations of some of the presently preferred embodiments. Similarly, other embodiments of the invention may be devised which do not depart from the spirit or scope of the present invention. Moreover, features from different embodiments of the invention may be employed in combination. The scope of the invention is, therefore, indicated and limited only by the appended claims and their legal equivalents, rather than by the foregoing description. All additions, deletions, and modifications to the invention, as disclosed herein, which fall within the meaning and scope of the claims are to be embraced thereby.

What is claimed is:

1. A through-wafer interconnect comprising a conductive via member passing through a wafer between a first surface and a second, opposing surface, the via member having a first exposed end and a second exposed end, the first end comprising one of a trapezoid shape and a frustoconical shape and the second end comprising one of a shape flaring out as it becomes more distal from the second surface and a post shape having a substantially constant lateral extent.

2. A through-wafer interconnect comprising a conductive via member passing through a wafer between a first surface and a second, opposing surface, the wafer being thinned from an initial thickness to expose a first end of the via member as one of a trapezoid shape and a frusto-conical shape, and the second surface of the wafer exposing only an end surface of a second end of the via member comprising one of a shape flaring out as it approaches the second surface and a post shape having a substantially constant lateral extent.

3. A through-wafer interconnect comprising a conductive via member passing through a wafer having a first surface and a second, opposing surface, the conductive via member having a first exposed end and a second exposed end, the first exposed end and the second exposed end each comprising one of a trapezoid shape and a frustoconical shape.

4. A via-containing member, comprising:

a substrate having a first surface and a second, opposing surface;

a pattern of vias in the substrate, each via passing through the substrate and having a first end and a second, opposing end, wherein the vias comprise:

a first end having at least one of a trapezoidal shape and a frustoconical shape and extending outwardly from one of the first surface and the second, opposing surface; and

a second via end having at least one of a flared-out shape and a post shape having a substantially constant lateral extent.

5. The via-containing member in accordance with claim 4, wherein the second via end having at least one of the flared-out shape and post shape extends outwardly from another of the first surface and the second, opposing surface.

6. A via-containing member comprising:

a substrate having first and second opposing surfaces; and

a pattern of vias on the substrate, each via passing through the substrate between a first end and an opposing second end, the first end and the second, opposing end each having one of a trapezoidal shape and a frusto-conical shape.

7. The via-containing member in accordance with claim 6, wherein the via-containing member comprises one of a wafer contact test card, a single die interposer, and a multi-die interconnect.

8. A semiconductor device assembly, comprising:

at least one semiconductor die having a plurality of bond pads on an active surface thereof; and

an interposer comprising a substrate having a plurality of conductive vias extending therethrough in alignment with bond pads of the plurality, the plurality of conductive vias each including a via end having a substantially flat end surface projecting from a substrate surface facing the at least one semiconductor die and in contact with a bond pad of the plurality, the via end tapering from a larger lateral extent proximate the substrate surface to a smaller lateral extent distal therefrom.

9. The semiconductor device assembly of claim 8, further including a dielectric material interposed between the active surface of the at least one semiconductor die and the surface of the substrate and surrounding the projecting via ends.

10. The semiconductor device assembly of claim 8, further including a metal overlay over at least the substantially flat end surface.

11. The semiconductor device assembly of claim 8, wherein ends of the plurality of vias opposite the projecting via ends lie substantially coplanar with another surface of the substrate, and further including:

conductive traces extending laterally across the another surface from the substantially coplanar via ends; and

discrete conductive elements disposed on distal ends of the conductive traces and projecting outwardly from the another surface.

12. The semiconductor device assembly of claim 11, further comprising a dielectric layer over the another surface and laterally surrounding the discrete conductive elements.

13. The semiconductor device assembly of claim 8, wherein the projecting via ends are in direct contact with the plurality of bond pads.

14. The semiconductor device assembly of claim 8, wherein the projecting via ends are in contact with the plurality of bond pads through intervening discrete conductive elements.

15. A semiconductor device assembly, comprising:

at least one semiconductor die having a plurality of bond pads on an active surface thereof; and

an interposer comprising a substrate having a plurality of conductive vias extending therethrough in alignment with bond pads of the plurality, the plurality of conductive vias each including a first via end having a substantially flat end surface projecting from a substrate surface opposite a substrate surface facing the at least one semiconductor die and tapering from a larger lateral extent proximate the substrate to a smaller lateral extent distal therefrom and a second via end substantially coplanar with the substrate surface facing the at least one semiconductor die and in contact with a bond pad of the plurality through a discrete conductive element projecting from the substrate.

16. The semiconductor device assembly of claim 15, further including a dielectric material interposed between the active surface of the at least one semiconductor die and the substrate and surrounding the discrete conductive elements.

17. The semiconductor device assembly of claim 15, further including:

conductive traces extending laterally across the surface of the substrate facing the at least one semiconductor die from the substantially coplanar via ends; and

wherein the discrete conductive elements lie at distal ends of the conductive traces.

18. A semiconductor device assembly, comprising:

at least one semiconductor die having a plurality of bond pads on an active surface thereof; and

at least another semiconductor die having a plurality of conductive vias extending therethrough in alignment with bond pads of the plurality of the at least one semiconductor die, the plurality of conductive vias each including a via end having a substantially flat end surface projecting from a surface of the at least another semiconductor die facing the at least one semiconductor die and in contact with a bond pad of the plurality, the via end tapering from a larger lateral extent proximate the surface of the at least another semiconductor die facing the at least one semiconductor die to a smaller lateral extent distal therefrom.

19. The semiconductor device assembly of claim 18, further including a dielectric material interposed between the active surface of the at least one semiconductor die and the at least another semiconductor die and surrounding the projecting via ends.

20. The semiconductor device assembly of claim 18, further including a metal overlay over at least the substantially flat end surface.

21. The semiconductor device assembly of claim 18, wherein ends of the plurality of vias opposite the projecting via ends lie substantially coplanar with another surface of the at least another semiconductor die, and further including:

conductive traces extending laterally across the another surface from the substantially coplanar via ends; and

discrete conductive elements disposed on distal ends of the conductive traces and projecting outwardly from the another surface.

22. The semiconductor device assembly of claim 21, further comprising a dielectric layer over the another surface and laterally surrounding the discrete conductive elements.

23. The semiconductor device assembly of claim 18, wherein the projecting via ends are in direct contact with the plurality of bond pads.

24. The semiconductor device assembly of claim 8, wherein the projecting via ends are in contact with the plurality of bond pads through intervening discrete conductive elements.

25. A semiconductor device assembly, comprising:

at least one semiconductor die having a plurality of bond pads on an active surface thereof, and

an interposer comprising a substrate having a plurality of conductive vias extending therethrough in alignment with bond pads of the plurality, the plurality of conductive vias each including a first via end having a substantially flat end surface projecting from a substrate surface facing the at least one semiconductor die and in contact with a bond pad of the plurality and a second via end projecting from a substrate surface facing away from the at least one semiconductor die, the first and second via ends tapering from a larger lateral extent proximate the substrate to a smaller lateral extent distal therefrom.

26. The semiconductor device assembly of claim 25, further including a dielectric material interposed between the active surface of the at least one semiconductor die and the surface of the substrate and surrounding the projecting first via ends.

27. The semiconductor device assembly of claim 25, further including a metal overlay over at least the substantially flat end surface.

28. The semiconductor device assembly of claim 25, wherein the second ends of the plurality of vias include discrete conductive elements disposed thereon.

29. The semiconductor device assembly of claim 25, wherein the at least one semiconductor die comprises a plurality of semiconductor dice mutually laterally adjacently disposed in substantially coplanar fashion over the substrate.

30. The semiconductor device assembly of claim 28, further comprising a dielectric layer over the another surface and laterally surrounding the discrete conductive elements.

31. The semiconductor device assembly of claim 25, wherein the projecting first via ends are in direct contact with the plurality of bond pads.

32. The semiconductor device assembly of claim 25, wherein the projecting first via ends are in contact with the plurality of bond pads through intervening discrete conductive elements.

33. The semiconductor device assembly of claim 25, wherein the substrate includes a recess therein facing the at least one semiconductor die and the at least one semiconductor die is aligned with the recess, and further including at least another semiconductor die having a plurality of bond pads on an active surface thereof superimposed over the at least one semiconductor die and in communication with the first via ends of vias of the plurality laterally adjacent the at least one semiconductor die and projecting at least beyond the active surface thereof.

34. The semiconductor device assembly of claim 33, wherein the substrate exhibits an increased thickness in a region surrounding the recess, and the vias of the plurality laterally adjacent the at least one semiconductor die extend through the region.

* * * * *