United States Patent

Chang

[15] **3,643,171**

[45] **Feb. 15, 1972**

[54] CORE MEMORY DELTA NOISE CANCELLATION

[72] Inventor: **Hua-Shan Chang**, South Pasadena, Calif.

[73] Assignee: **Lockheed Aircraft Corporation**, Burbank, Calif.

[22] Filed: **Nov. 6, 1970**

[21] Appl. No.: **87,541**

[52] **U.S. Cl.** **328/165**, 328/117, 307/231

[51] **Int. Cl.** **H04b 1/12**

[58] **Field of Search** 330/69; 307/231; 328/116, 117, 328/165, 163

[56] **References Cited**

UNITED STATES PATENTS

2,450,818	10/1948	Vermillion	325/467
3,328,704	6/1967	Wantland	328/117
2,534,264	12/1950	Hoeppner	328/117
3,119,070	1/1964	Seliger	328/114
3,387,221	6/1968	Arberman et al.	328/163
3,094,665	6/1963	Wildman	328/165

OTHER PUBLICATIONS

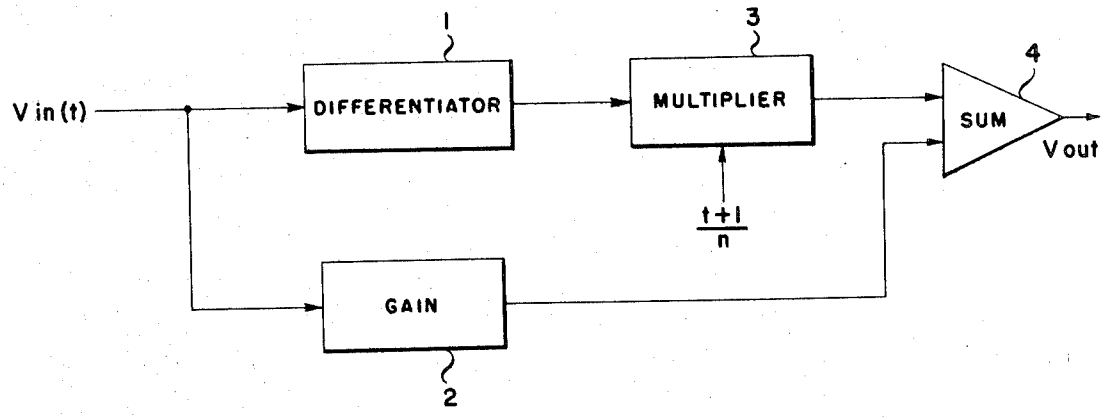
"Adaptive FSK Data Demodulator" by R. W. Calfee, IBM Technical Disclosure Bulletin, Vol. 5, No. 1, Apr. 1963, p. 76 (Copy in 328/116)

Primary Examiner—Donald D. Forrer
Assistant Examiner—Harold A. Dixon
Attorney—George C. Sullivan

[57] **ABSTRACT**

Method and means for delta noise cancellation for memory systems in which the delta noise decay function is combined electronically with a separately generated function derived from the delta noise decay function to cancel or reduce the delta noise amplitude in the decaying period to improve memory access time.

1 Claims, 4 Drawing Figures



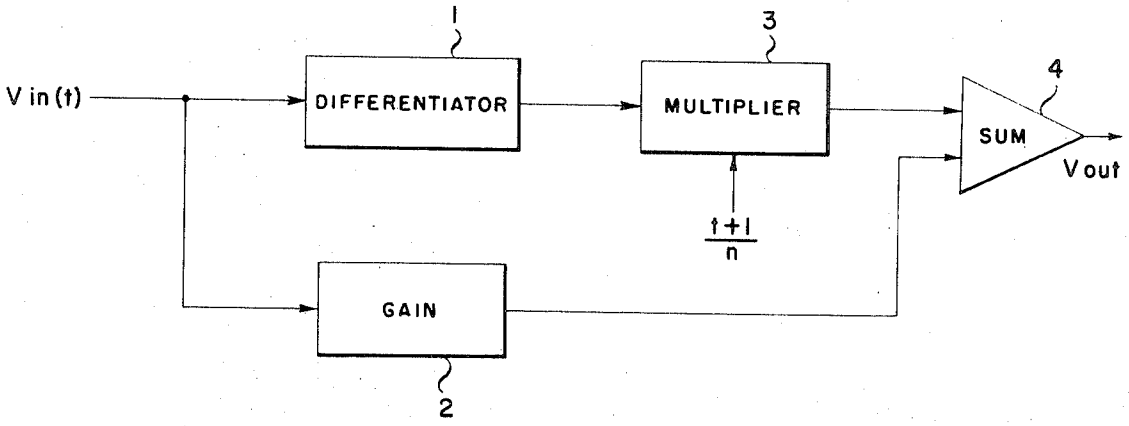


FIG. 1

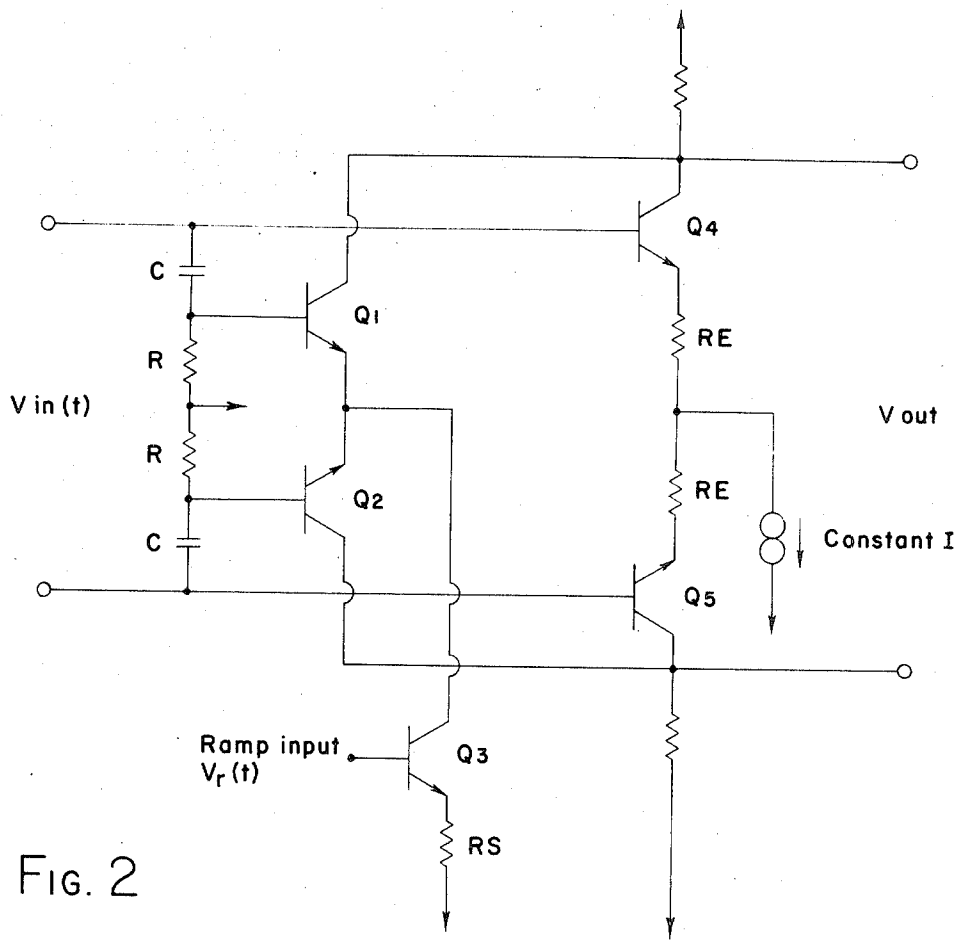


FIG. 2

INVENTOR.
HUA-SHAN CHANG
BY George C. Sullivan
Agent

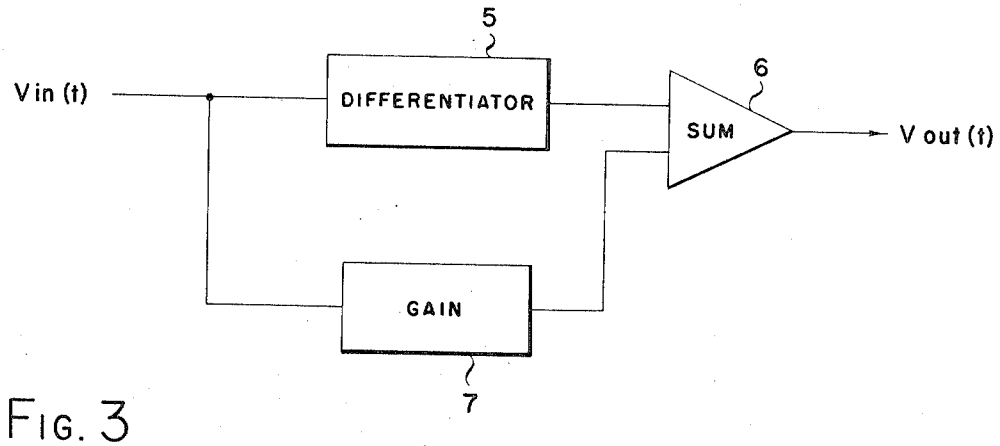


FIG. 3

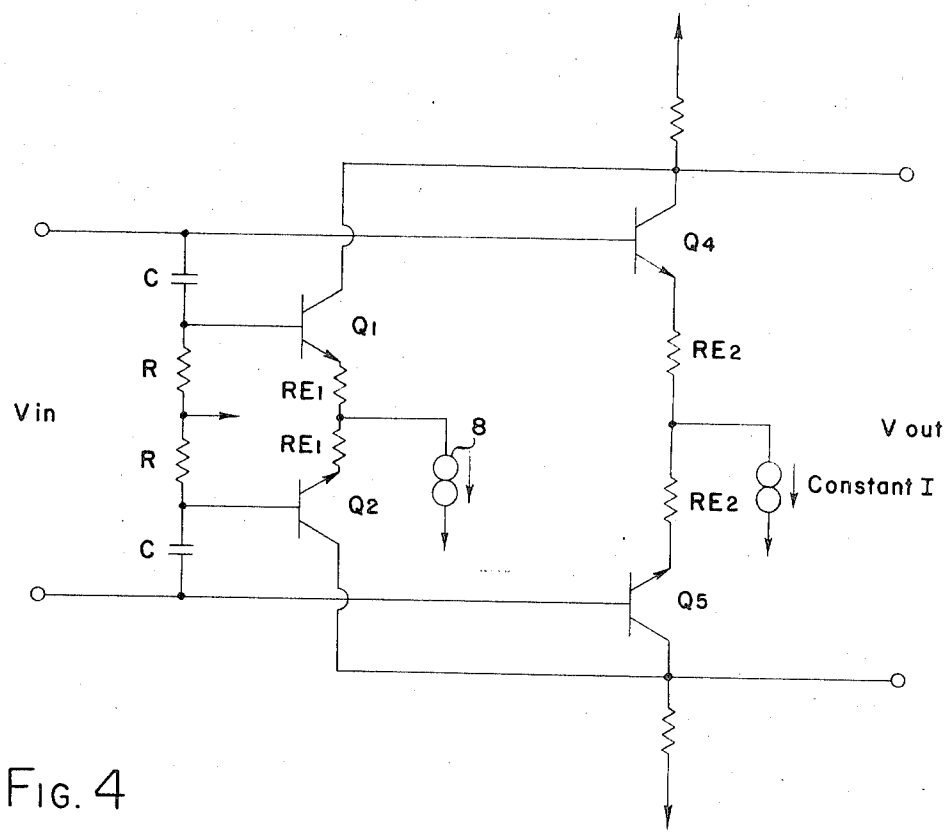


FIG. 4

INVENTOR.
HUA-SHAN CHANG
BY
Agent

CORE MEMORY DELTA NOISE CANCELLATION

This invention relates to noise cancellation and more particularly to delta noise cancellation to improve the core memory access time.

The inherent limitation on the access time of a large core memory usually lies in the slow decay of the delta noise in the sense lines. Normally, the delta noise decays according to an exponential function if the line is properly terminated. Previous attempts to differentiate the decay function with the hope that it will reduce to zero faster and be more predictable have been unsuccessful.

It is therefore an object of the present invention to provide an improved method for cancellation or reducing the delta noise amplitude.

Another object of the invention is to improve the memory access time.

These and other objects of the invention will become more apparent from the following description when taken with the accompanying drawings in which:

FIG. 1 is a block diagram of one embodiment of the invention;

FIG. 2 is a schematic showing a typical implementation of FIG. 1;

FIG. 3 is a block diagram of a second embodiment of the invention;

FIG. 4 is a schematic showing a typical implementation of FIG. 3.

The sense line in a memory system may be compared to a transmission line with the cores evenly spaced on the line. Analysis shows that after the current has reached the threshold of the minor wall displacement (on the hysteresis loop), the delta noise waveform follows the equation $a-b\exp(-t)$ up to $t=T$, where T is the total delay of the sense line. If the line is properly terminated, the delta noise will then decay exponentially. Otherwise, the decay of the delta noise can be approximated by the function $1/(t+1)^n$, where n can be determined from the length of the sense line and the reflection coefficient of the termination. The present invention utilizes the characteristics of the approximated decay function to cancel or substantially reduce the delta noise.

DIFFERENTIATION MULTIPLICATION

Referring to FIG. 1, a block diagram of this method is shown. This embodiment utilizes the distinctive characteristic of the delta noise decay function $1/(t+1)^n$. Observe that the product of its derivative and a ramp function is the original function. Thus, the block diagram represents the following equation:

$$Vout\ (t) = Vin\ (t) + \frac{(t+1)}{n} V'in(t) \qquad (1)$$

where $(t+1)/n$ is the ramp function and $V'\text{in}(t)$ is the derivative of $V\text{in}(t)$.

In FIG. 1, the input voltage $V\text{in}(t)$ is applied to differentiator 1 and the gain circuit 2. The differentiated output is applied to multiplier 3 and combined with the ramp function $(t+1)/n$. The output of the multiplier is one input to the summing amplifier 4 while the original signal is the other input.

Now where the original signal is the distinctive decay function $1/(t+1)^n$, then:

$$V'in(t) = \frac{-n}{(t+1)^{n+1}}$$

Substituting in equation (1), we have:

$$Vout\ (t) = \frac{1}{(t+1)^n} + \frac{(t+1)}{n}\left(\frac{-n}{(t+1)^{n+1}}\right) = 0$$

from which it is readily observed that the output is zero. The core turnover signal, which is represented by $\text{Sin}^2 w\ t$, will be partially differentiated in the output.

FIG. 2 represents a typical schematic to implement the block diagram of FIG. 1. The input signal is differentiated by the RC network and then multiplied with the ramp function by means of the transistor circuits Q_1–Q_2. Q_3 converts the ramp voltage to ramp current. The result is then added by Q_4–Q_5. Their emitter resistors RE determine the gain of the circuit. The resistors RE are connected to a constant current source. For the delta noise to be cancelled properly, the following relationship of the circuit elements and the ramp function should be:

Let

$$Vin\ (t) = 1/(t+1)^n$$

$$Vr\ (t = a(t+1)$$

Then

$$I_1 = \div n \frac{q}{KT} \frac{aRc}{2Rs} /(t+1)^n$$

$$I_2 = 1/(RE(t+1)^n)$$

Where KT/q=25 mv. at room temperature

The condition to cancel the delta noise is $I_1 = -I_2$, which gives the following equation:

$$\frac{RE}{2Rs}\ anRC = \frac{KT}{q}$$

Differentiation—Add

FIG. 3 shows a block diagram for this embodiment. Again, the delta noise decays exponentially. This circuit will implement the following equation:

$$V\text{out}(t) = V\text{in}(t) + V'\text{in}(t)$$

The noise is represented by $\exp(-t)$ and $V'\text{in}(t) = -\exp(-t)$

Then $V\text{out}(t) = \exp(-t) + [-\exp(-t)] = 0$

In FIG. 3, the differentiator 5 provides the differential and the summing circuit 6 combines the output with the original signal from the gain circuit 7.

FIG. 4 is a typical schematic for implementing the block diagram of FIG. 3.

The input signal is differentiated by the RC network. The differentiated output is applied to the bases Q_1 and Q_2. The emitter degeneration resistors RE determine the gain of the differentiator circuit. The input signal is simultaneously applied to Q_4 and Q_5 with their emitter degeneration resistors RE determining the gain of the circuit. The overall circuit is similar to FIG. 2 with the multiplier's ramp input current source replaced (Q_3 of FIG. 2) by a constant current source 8.

For the circuit to function properly, the following equation should be satisfied:

$$RC = RE1/RE2$$

What is claimed:

1. Means for delta noise cancellation for memory systems comprising an input signal including a delta noise signal. means for differentiating said input signal, multiplier means for multiplying the differentiated signal and a ramp function, a summing amplifier, means for applying the output of said multiplier means to said amplifier and means for applying the input signal to said amplifier.

* * * * *