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## (54) Electronic device and method for adjusting an internal clock

(57) The present invention relates to an electronic device and a method for adjusting an internal clock reference. An external clock reference is retrieved from a received external signal and the external clock reference is compared to an internal clock reference. The resulting difference value is employed to permanently compensate deviations of the internal clock reference.

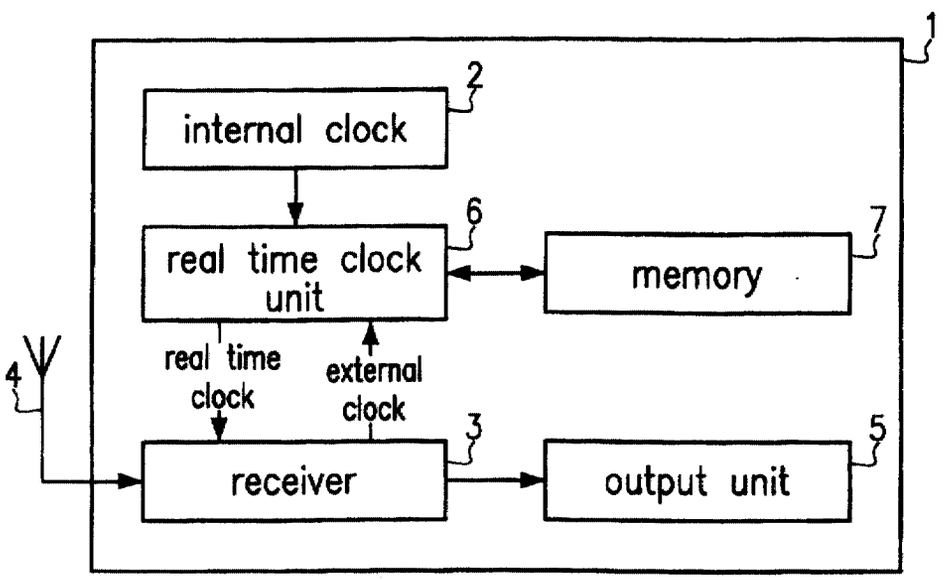


FIG. 2

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## Description

**[0001]** The present invention relates to a method for adjusting an internal clock in an electronic device and an electronic device including a circuit for adjusting an internal clock. In particular, the present invention relates to a television receiver comprising a circuit for adjusting an internal clock.

**[0002]** Today, many consumer devices use a real time clock. This clock signal is employed in order to control a start and/or end of operation. In particular, VCR's, satellite receivers, and radio alarm clocks may start an operation depending on a preset point of time. When an internal time value provided by an internal timer reaches a predetermined point of time a preselected operation is carried out.

**[0003]** Such electronic devices include an internal clock source. An internal time value is calculated based on the internal clock reference. Said internal clock is generated by means of a crystal having a predetermined resonance frequency. In order to achieve a high accuracy of the internal clock (and the internal time value) it is known to use a crystal having a low deviation. However, crystals having a low deviation generally are too expensive for use in consumer products.

**[0004]** It is an object of the present invention to provide a method for realizing a precise internal clock and an apparatus including a precise clock, both using a clock reference of low accuracy.

**[0005]** This object is achieved by the subject-matter of claim 1 for a method and by claim 12 for an electronic device.

**[0006]** Preferred embodiments are the subject-matter of dependent claims.

**[0007]** The present invention performs an alignment procedure in order to bring the internal clock in line with an external clock. This procedure is based on a comparison step of the internal clock signal with the external clock signal. The internal clock signal and the external clock signal are sampled simultaneously twice, having a predetermined period of time between both sampling steps. The first and second sampling of the clock signals generate first and second sample values. By evaluating the sample values a correction value for the internal clock reference is calculated.

**[0008]** First, differences are calculated between the sample values of each of the clock signals respectively, i.e. an internal difference value for the sample values of the internal clock and an external difference value for the sample values of the external clock. Second, an absolute difference value is calculated between the internal difference value and the external difference value. This absolute difference value represents a clock deviation of the internal clock with regard to the external clock reference. Third, a relative difference value is calculated. Such a relative difference value is independent of the period of time between both sampling steps and is employed as a correction value for the internal clock. The correction value (being the relative difference value) is stored in a non-volatile memory. This stored value may permanently be employed for compensating a deviation of the internal clock to be in line with said external clock reference.

**[0009]** Further, an electronic device using an internal clock reference may include a processing unit adapted to carry out the above described method. Such electronic devices are simpler in construction and, thus, easier to manufacture. The present invention allows to use internal clock references having a high deviation without adversely effecting the clock accuracy of the internal clock, in particular the accuracy of an internal real time value.

**[0010]** According to a preferred embodiment, the compensation procedure adds the calculated correction value each time a predetermined period of time is elapsed. Such a solution does not require a complex hardware realisation.

**[0011]** It is one of the particular advantages of the present invention that it is not necessary to further access an external clock reference after a correction value is calculated once. A repeated calculation of the compensation value, a further calibration procedure, may be carried out only in order to adjust variations due temperature changes or due to ageing of the used components.

**[0012]** Additionally, the electronic device may comprise an electronic timer providing a real time value based on the compensated internal clock. In a preferred embodiment, the absolute time calculated by an internal timer of the electronic device will be set in accordance with an external absolute time reference in predetermined time intervals. These time intervals may last for several weeks or months and an calibration procedure for calculating a new correction value will only be carried out during normal operation of the electronic device.

**[0013]** In the following, preferred embodiments of the present invention are described in conjunction with the accompanying drawings, which show:

figure 1, a simplified block diagram of a conventional prior art electronic device,

figure 2, a simplified block diagram of a preferred embodiment of an electronic device according to the present invention,

figure 3, a simplified block diagram of a compensation circuit included in an electronic device of figure 2, and

figure 4, a simplified block diagram of a digital TV receiver according to the present invention.

**[0014]** Today, many consumer devices include an internal clock which is used for controlling an internal processing of the consumer device, an example of which is shown in fig. 1, designated by reference numer-

al 1. The internal clock is further employed to provide a real time clock signal. Such an electronic device may be a television receiver, a VCR, a satellite receiver or a radio.

**[0015]** The electronic device 1 may comprise an internal clock 2, a receiver 3 receiving an external signal transmitted from an external source via an antenna 4 and an output unit 5. The receiving unit 3 is supplied with the internal clock reference in order to generate an internal real time clock.

**[0016]** When using an inexpensive internal clock source, e.g. a resonator having a high deviation, an accurate real time value can not be provided. Assuming the internal clock source has a deviation of 200ppm. Such a deviation results in a difference of about four minutes after elapse of two weeks. Thus, a time-based automated operation depending on the internal real time signal of the electronic device is not possible when the operation has to be in line with an external real time signal. In particular, when the operation, e.g. the recording operation of a VCR, has to be carried out corresponding to a program schedule of a broadcasting station.

**[0017]** According to the present invention, an undesirable high deviation of an internal clock is compensated. The compensation is achieved by means for calculating a correction value and performing a compensation operation. An example of an electronic device according to the present invention is shown in figure 2. Blocks which correspond to those of figure 1 are designated with the same reference numerals.

**[0018]** In general, the electronic device shown in figure 2 corresponds to the electronic device of figure 1. In addition, the electronic device of the present invention comprises a real time clock unit 6 and a memory 7. Further, the receiving unit 3 provides an external reference signal which is extracted from the signal received from the external source. The extracted external clock signal is supplied to the real time clock unit 6. In response, the real time clock unit 6 provides the receiving unit 3 with a compensated real time clock signal.

**[0019]** An example for a configuration of a real time clock unit 6 is shown in figure 3. The real time clock unit 6 receives an internal clock signal and an external clock signal. Both clock signals are sampled by a sampling unit 8. The operation of the sampling unit 8 is controlled by a processing unit 9. The processing unit 9 is supplied with the sampled values of the internal and external clock signals from the sampling unit 8. The processing unit 9 may store both sample values in a memory 7.

**[0020]** Based on the sampled clock values the processing unit 9 calculates a compensation value which is stored within memory 7 being a non-volatile memory unit. The compensation value which is calculated once may be accessed during the whole life-time of the electronic device from the non-volatile memory unit 7.

**[0021]** A compensation of the internal clock is carried out by a compensation unit 10 providing a real time clock signal to the receiving unit 3.

**[0022]** The compensation procedure is preferably implemented by software instructions which may also be stored within said memory unit 7 or within a separate memory. The procedure carried out by the processing unit 9 in conjunction with the sampling unit 8 is called a clock calibration routine. During the calibration phase, the electronic device needs access to an external clock reference. Such an external reference signal may be provided during normal operation of the electronic device, but may also be provided especially for the calibration procedure.

**[0023]** The calibration procedure will take a sample of the external clock reference $T_{ref,1}$ and, at the same time, a sample of the internal clock signal $T_{int,1}$. After a predetermined period of time, the length of which is depending on the accuracy of the external clock reference and that accuracy that the manufacturer of the electronic device wants to achieve, a second sample of the external clock $T_{ref,2}$ and the internal clock $T_{int,2}$ are taken. Thus, four sample values, two for each clock signal, are taken and stored in memory unit 7.

**[0024]** Subsequently, a difference between both sample values of a clock signal is calculated, separately for each clock signal. An internal difference value $\Delta T_{int}$ represents the difference between both sample values of the internal clock signal:

$$\Delta T_{int} = \Delta T_{int,1} - \Delta T_{int,2}$$

**[0025]** The difference of the external clock sample values is calculated as:

$$\Delta T_{ref} = \Delta T_{ref,1} - \Delta T_{ref,2}$$

**[0026]** The deviation of the internal clock is calculated as follows:

$$\Delta T = \Delta T_{int} - \Delta T_{ref}$$

**[0027]** Such a difference indicates an absolute deviation of the internal clock which has been accumulated during the time period between both sampling steps. A relative difference value may be calculated as follows:

$$\Delta T_R = \Delta T / \triangle T_{ref}$$

**[0028]** This relative difference value $\Delta T_R$ is an individual value for each electronic device. The value depends on the deviation of the used internal clock reference (i. e. the deviation of the used resonator). In order to make a permanent compensation of this deviation possible the difference value has to be stored permanently within a non-volatile memory 7.

**[0029]** A permanent compensation allows to bridge long unused periods of the electronic device without a significant deviation of the internal real time value. Thus, the present invention allows a precise start of normal operation by an automated procedure after long standby periods.

**[0030]** The above described calibration procedure may be carried out during a first set-up phase of the electronic device at the customer's home, or during manufacturing. Preferably, the calibration procedure is carried out during a short operation test during manufacturing. Neither the set-up procedure nor the manufacturing will be adversely effected since the calibration procedure may be automatically handled by software inside the electronic device and does not require any manual interaction input commands.

**[0031]** The external clock may be a real time clock signal. Generally, real time clock signals are generated with high accuracy using professional equipment or being derived from an officially broadcasted clock reference signal or from a GPS signal.

**[0032]** Depending on the kind of electronic device different external signals may be used as an external clock reference. Preferably these signals are received and processed during a normal operation mode of the electronic device. In case, the electronic device is a digital TV receiver (DTV receiver) or a VCR including a digital television receiver the DTV receiver may access during normal operation either the Program Clock Reference (PCR) or the Time Description Table (TDT) which are included in an MPEG2 Transport Stream. The Program Clock Reference is described in more detail in reference ISO/IEC 13818-1 and the Time Description Table in ETSI EN-300 468. The Time Description Table is part of the SI tables which are transmitted according to the digital video broadcasting standard (DVB). It contains the UTC time and date information having a resolution of one second. It is used to set the real time and date within digital TV receivers. The Program Clock Reference (PCR) is located in the adaptation field of the MPEG Transport Stream (TS) packet and has a resolution 1/27 MHz. It is transmitted at least every 100 ms and is used to synchronize an MPEG decoder of the DTV receiver with the transmitting device.

**[0033]** Analogue television receivers have access to videotext time information during normal operation. Details of the video time information are given in EBU-SPB 492.

**[0034]** Radio receivers may extract time information from the radio data system. Digital radio receivers (DAB receivers) using a crystal or resonator as external clock source may extract an external clock reference from the time information in the Fast Group of the Fast Information Channel (FIC). This information is described with more detail in ETS 300 401. Of course, an electronic device may extract an external clock from a different source. Preferably, the external clock signal is accessed during normal operation, but may also be provided separately.

**[0035]** When employing a method or an electronic device according to the present invention, the internal clock resonator still provides a clock frequency that does not correspond to a precise real time clock. But due to the known difference between the internal clock frequency and the real time clock frequency, the electronic device is able to compensate the difference and to calculate a correct real time value.

**[0036]** Such a compensation procedure may be repeatedly carried out within said electronic device in order to correct influences of slow temperature changes, e.g. to overcome differences between summer and winter temperatures, and/or to correct the influence of ageing effects of the employed components.

**[0037]** In the following, an example will be given for the operation of the present invention.

**[0038]** It is assumed that the internal clock source has a deviation of 200ppm. Further, the internal real time clock has a resolution of 1/100 second. It is desired that the internal real time clock keeps a precision of $\pm 2$ seconds per day. This value represents a maximum allowable deviation of the real time clock and corresponds to a deviation of 1/100 second per 7.2 minutes (corresponding to 432 seconds). Further, it is assumed that the external clock reference has a resolution of 1/1000 second.

**[0039]** Due to the given resolution of 1/100 second of the internal clock, the maximal allowable deviation of 1/100 second may first be detected after elapse of 432 seconds. However, it is not known at which time instant within each 1/100 second time slot each sample value of the internal clock signal is taken. Thus, a deviation of 1/100 second may not be detected. In order to make a deviation of 1/100 second reliably detectable, the minimum time period (being $\Delta T_{ref}$) between both sampling steps should at least last 864 seconds.

**[0040]** Assuming, the calibration phase starts at a time of $T_{ref,1}$ being 1 h, 0 min, 0.0 s. At this time, $T_{int,1}$ will be set to $T_{ref,1}$. Thus, the internal clock is in line with the external clock at the time $T_{ref,1}$.

**[0041]** After a lapse of one hour according to the external clock signal (more than 864 seconds) a second time sample is taken. $T_{ref,2}$ being 2 h, 0 min, 0.0 s and, as an example, $T_{int,2}$ being 2 h , 0 min, 0.720 s. Subsequently, the internal time reference will again be set to the external reference time.

**[0042]** The second sample value of the internal clock time $T_{int,2}$ having a deviation from the external clock reference of 0.720s. 0.720s being the absolute difference value $\triangle T$. The relative difference value $\Delta T_R$ may be calculated as follows:

$$\Delta T_R = 0.72s / 3600s = 200 \text{ ppm} = 2 * 10^{-4}$$

**[0043]** This value corresponds to 200ppm having been assumed to be the deviation of the internal clock

source. In general, no further calibration procedure is necessary in order to calculate a compensation value. Thus, access to an external clock is required only once in order to correct the internal clock for the life time of the electronic device.

**[0044]** The internal clock will be corrected using the stored relative difference value $\Delta T_R$ after a predetermined period of time. According to the above example, the internal clock will exceed the limit of ± 2 seconds, without any correction, after 10 000 seconds. Thus, a correction has to be carried out after lapse of that time, for instance, after 7200 seconds (corresponding to 2 hours time). After lapse of 7200 seconds the following correction value has to be subtracted or added:

$$\Delta T_R * 7200\ s = (200 / 1\ 000\ 000) * 7200\ s = 1.44\ s$$

**[0045]** The current internal clock value will be corrected using the above value. The new internal real time clock value will be written back into the real time clock memory. The internal real time clock will be further processed starting from this value. This correction procedure, using this correction value, has to be carried out all 7200 seconds.

**[0046]** In the above example, two alignment procedures are carried out. First, the speed of the internal clock is corrected. This enables the electronic device to calculate time differences which correspond to a reference time difference. Second, the absolute real time value is corrected. This enables the internal timer to provide a real time signal corresponding to an external reference. In this way, an automated operation of the electronic device with regard to an external device is possible, both using a common real time reference.

**[0047]** After long periods of time, it is desirable to set the internal timer again to the absolute time of the external clock. This may be done, for example, every time the electronic device is switched from a stand-by mode into a normal operation mode. A precision which is achieved for an internal real time accuracy according to the present invention will be sufficient for programming an automatic timer of a VCR or a TV receiver for at least more than several weeks.

**[0048]** An example for a digital TV receiver incorporating the present invention is shown in fig. 4. An external digital signal is received via an antenna 4. The received external signal is first processed in a NIM which supplies a processed signal to an MPEG TS demultiplexer 10b. The MPEG TS demultiplexer 10b provides a demultiplexed MPEG transport stream to other processing units and further provides an extracted external time signal to a CPU 9. The digital television receiver further comprises an internal clock 2. The internal clock signal is provided to a real time clock unit which is part of a processing unit 9. The CPU calculates based on the external clock signal and on the internal clock signal a compensation value and enables the real time clock unit to provide an internal clock to the CPU which is in line with the external clock.

**[0049]** The present invention does not need to receive a time reference during normal operation. The described calibration procedure may only be carried out during manufacturing. In such a situation, it will be easy to provide a precise clock reference which may be used to compare the internal clock reference to the external clock reference.

**[0050]** Further, it is not necessary to provide an absolute time reference, but reliable clock pulses having a sufficient accuracy in order to correct the internal clock reference. The calculated deviation of the internal clock reference will be stored permanently in a non-volatile memory of the device. Each electronic device may have a different correction value. During operation, the internal clock will permanently be corrected based on the value stored in the non-volatile memory of the device.

## Claims

1. A method for adjusting an internal clock reference of an electronic device, comprising the following steps:

   receiving a signal transmitted from an external source,

   retrieving an external clock reference from said received signal,

   sampling an internal clock reference and the external clock reference simultaneously in order to generate first sample values ($T_{int,1}$, $T_{ref,1}$),

   repeating the sampling step after a predetermined period of time ($\Delta T_{ref}$) in order to generate second sample values ($T_{int,2}$, $T_{ref,2}$),

   calculating an internal difference value ($\Delta T_{int}$) between both sample values ($T_{int,1}$, $T_{int,2}$) of the internal clock reference,

   calculating an external difference value ($\Delta T_{ref}$) between both sample values ($T_{ref,1}$, $T_{ref,2}$) of the external clock reference,

   calculating an absolute difference value ($\Delta T$) between the internal difference value ($\Delta T_{int}$) and the external difference value ($\Delta T_{ref}$),

   calculating a relative difference value ($\Delta T_R$) based on said absolute difference value (AT),

   storing said calculated difference value ($\Delta T_R$),

compensating said internal clock reference to be in line with said external clock reference based on said stored relative difference value ($\Delta T_R$).

**2.** A method according to claim 1 wherein said signal transmitted from the external source being a television signal or a radio signal.

**3.** A method according to claim 2 wherein said external clock reference being a Program Clock Reference (PCR) or a Time Description Table (TDT) when said received signal being a digital television signal.

**4.** A method according to claim 2 wherein said external clock reference being a videotext time information when said received signal being an analogue television signal.

**5.** A method according to claim 2 wherein said external clock reference being time information from a radio data system (RDS) when said received signal being a radio signal.

**6.** A method according to any of claims 1 to 5 wherein said method being carried out during a first setup of said electronic device.

**7.** A method according to any of claims 1 to 6 wherein said method being carried out during manufacturing of said electronic device.

**8.** A method according to any of claims 1 to 7 wherein said method being carried out at predetermined time intervals during normal operation of said electronic device.

**9.** A method according to any of claims 1 to 8 wherein said method being performed and initiated automatically.

**10.** A method according to any of claims 1 to 9 wherein said internal clock reference being compensated by adding said relative difference value ($\Delta T_R$) in predetermined intervals to a current time value.

**11.** A method according to any of claims 1 to 10 wherein a current internal time value being set to an absolute time provided by the external reference.

**12.** An electronic device comprising:

an internal clock unit (2) providing an internal clock reference,

a receiving unit (3) for receiving a signal transmitted from an external source and for retrieving an external clock reference from the received signal,

a processing unit (6) being adapted to:

generate first and second sample values ($T_{int,1}$, $T_{int,2}$, $T_{ref,1}$, $T_{ref,2}$) by sampling said internal and said external clock reference simultaneously at two different points of time having a predetermined period of time in between,

calculate an internal difference value ($\Delta T_{int}$) between both sample values of said internal clock reference ($T_{int,1}$, $T_{int,2}$) and an external difference value ($\Delta T_{ref}$) between both sample values of said external clock reference ($T_{ref,1}$, $T_{ref,2}$)

calculate an absolute difference value ($\Delta T$) between the internal difference value ($\Delta T_{int}$) and the external difference value ($\Delta T_{ref}$),

calculate a relative difference value ($\Delta T_R$),

and compensate said internal clock reference to be in line with said external clock reference based on said relative difference value ($\Delta T_R$),

a memory (7) for storing said relative difference value ($\triangle T_R$).

**13.** An electronic device according to claim 12 wherein said electronic device being a digital television receiver.

**14.** An electronic device according to claim 13 wherein said external clock reference being a Program Clock Reference (PCR) or a Time Description Table (TDT).

**15.** An electronic device according to claim 12 wherein said electronic device being an analogue television receiver and said external clock reference being a videotext time information.

**16.** An electronic device according to claim 12 wherein said electronic device being a radio and said external clock reference being time information from a radio data system (RDS).

**17.** An electronic device according to any of claims 12 to 16 further comprising an adding circuit (9) for adding said stored relative difference value ($\triangle T_R$) to said current internal time after a predetermined period of time.

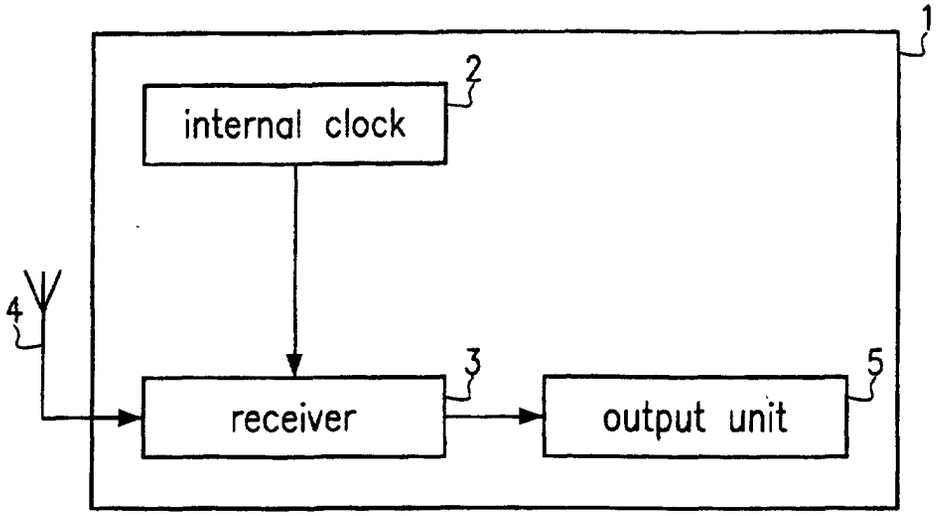
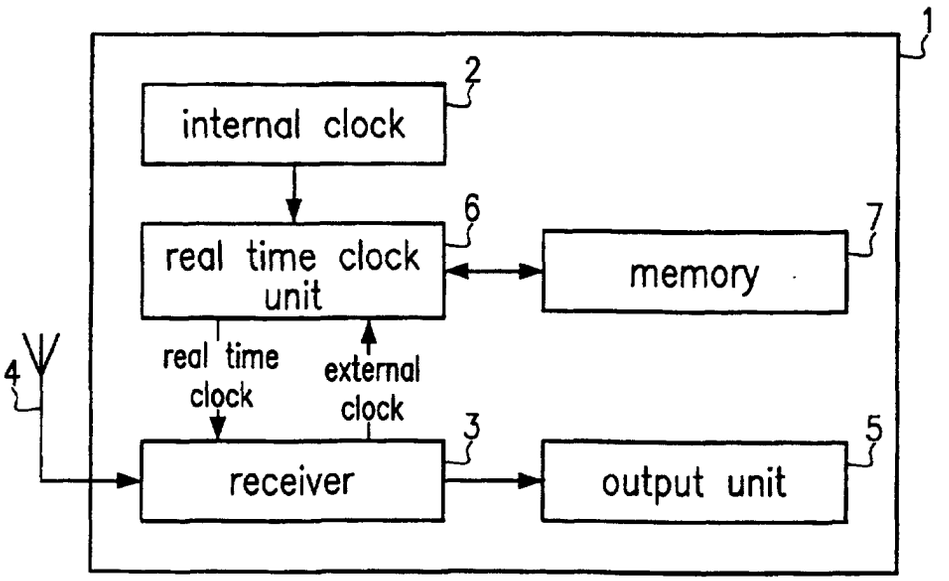

1
2
internal clock
4
3
5
receiver
output unit

FIG. 1


1
2
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6
7
real time clock unit
memory
real time clock
external clock
4
3
5
receiver
output unit

FIG. 2

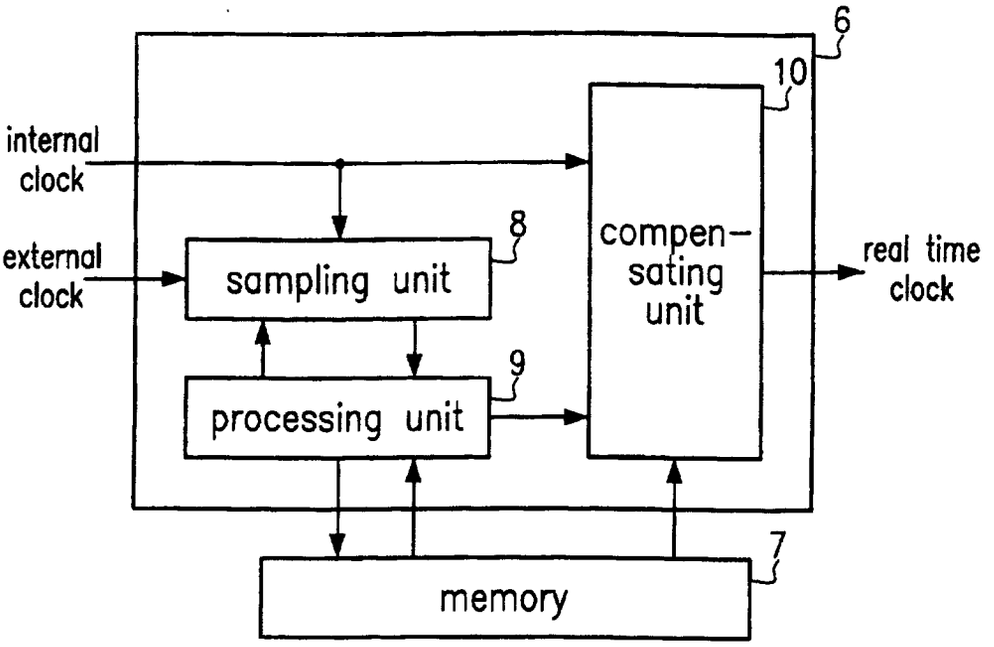
6
10
internal clock
external clock
8
sampling unit
compen-sating unit
real time clock
9
processing unit
7
memory

FIG. 3

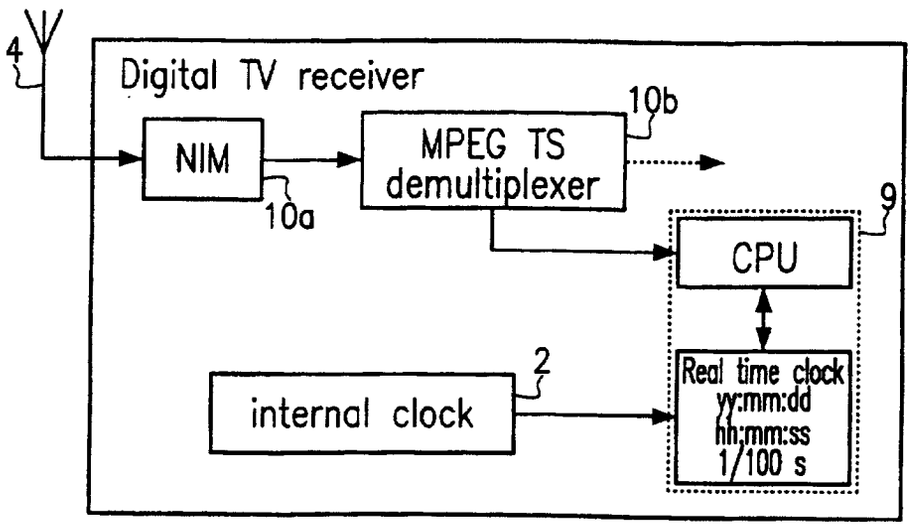
4
Digital TV receiver
10b
NIM
MPEG TS demultiplexer
10a
9
CPU
2
internal clock
Real time clock
yy:mm:dd
hh:mm:ss
1/100 s

FIG. 4

European Patent Office

# EUROPEAN SEARCH REPORT

Application Number
EP 00 10 1959

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int.Cl.7) |
|---|---|---|---|
| X | DE 44 23 366 C (GRUNDIG EMV)<br>19 October 1995 (1995-10-19)<br>* column 1, line 1 - column 3, line 66 *<br>--- | 1-17 | G04G3/02<br>G04G5/00 |
| A | EP 0 258 838 A (SIEMENS AG)<br>9 March 1988 (1988-03-09)<br>* column 1, line 50 - column 4, line 23 *<br>----- | 1-17 | |

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

G04G

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| THE HAGUE | 17 July 2000 | Exelmans, U |

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## ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 00 10 1959

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