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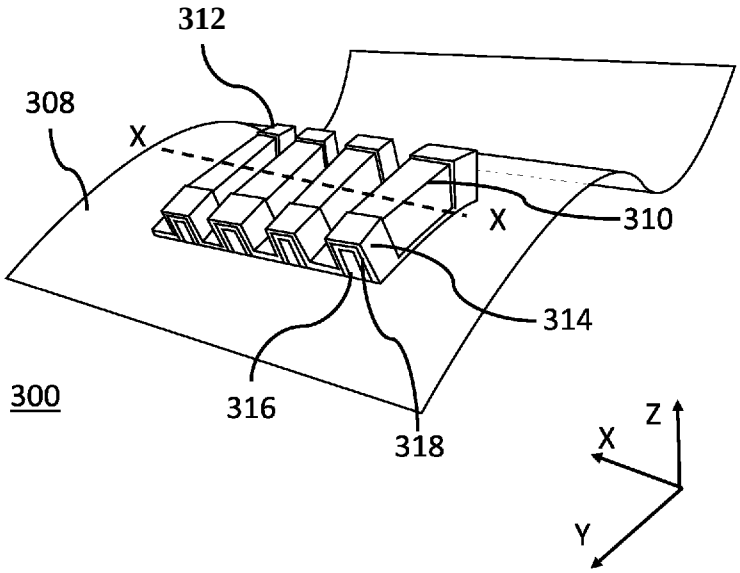
(54) Title: WAVY CHANNEL FLEXIBLE THIN-FILM-TRANSISTOR ON A FLEXIBLE SUBSTRATE AND METHOD OF PRODUCING SUCH A THIN-FILM-TRANSISTOR

FIG. 3B



(57) Abstract: A method for producing a thin-film-transistor involves forming a flexible substrate on a rigid substrate, forming a plurality of fins and trenches in a structural layer arranged on the flexible substrate, forming a wavy gate layer, channel layer, source contact layer, and drain contact layer on each of the plurality of fins and each of a plurality of trenches of the structural layer, and removing the plurality of fins and trenches having the wavy gate, channel, source contact, and drain contact layers from the rigid substrate.

WO 2018/162993 A1

[Continued on nextpage]

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Wavy Channel Flexible Thin-Film-Transistor on a Flexible Substrate and Method of Producing Such a Thin-Film-Transistor

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. Provisional Patent Application No. 62/468,608, filed on March 8, 2017, entitled "FLEXIBLE WAVY CHANNEL TRANSISTOR ARCHITECTURE FOR HIGH PERFORMANCE DISPLAYS," the disclosure of which is incorporated here by reference in its entirety.

BACKGROUND

TECHNICAL FIELD

[0002] Embodiments of the subject matter disclosed herein generally relate to a wavy channel thin-film-transistor on a flexible substrate and a method for producing such a wavy channel thin-film-transistor.

DISCUSSION OF THE BACKGROUND

[0003] There is an ever-increasing demand for improving the resolution of displays by increasing the number of displayable pixels. While displays capable of driving an 800 pixel x 600 pixel resolution were standard for a long time, display resolutions have quickly increased to so-called high definition resolutions of 1280 pixels x 720 pixels, 1280 pixels x 768 pixels, and 1280 pixels x 1024 pixels. Displays capable of achieving so-called 4K resolution, due to the use of approximately 4,000 pixels, are now becoming more and more affordable and there is an increasing demand for displays capable of 8K resolution.

[0004] Increasing display resolution requires increasing the number of displayable pixels. When the dimensions of a display are maintained, increasing the number of displayable pixels requires reducing the size of each pixel. Specifically, active-matrix displays, such as active-matrix liquid crystal display (AM-LCD) displays and active-matrix organic light emitting diode (AM-OLED) displays, contain an active-matrix backplane of thin-film-transistor (TFT) pixel circuits. Active-matrix displays thin-film-transistor pixel circuits, which control individual OLED or LCD pixels, typically include four thin-film-transistors and two capacitors. Accordingly, a smaller thin-film-transistor area is required for achieving both higher resolutions, as well as high pixel fill factors, which is defined as the ratio of the light emitting area over the total area of the pixel.

[0005] Another important motivation for scaling thin-film-transistors is that the allowed pixel size decreases as the number of Pixel Per Inch (PPI) increases, which is a critical requirement for future high resolution mobile displays, such as flexible displays for point-of-care medical diagnostic testing. For example, the pixel size for 500 PPI is only 50.8 x 16:9 μηι. Accordingly, there is a need to scale down the size of thin-film-transistors consistent with the reduced pixel size so that the thin-film-transistor pixel circuits can fit within the smaller pixel area.

[0006] Figures 1A and 1B are schematic diagrams of a top view and perspective view of a conventional coplanar thin-film-transistor on a flexible substrate. The coplanar thin-film-transistor 100 includes a channel 102 arranged between a source contact 104 and drain contact 106, all of which are arranged on a flexible substrate 108. As illustrated in Figure 1B, an insulating layer 110 is arranged between the gate layer (not visible in the Figures) and the channel 102, source

contact 104, and drain contact 106. The top of the thin-film-transistor is relatively flat.

[0007] Gate length scaling is a common technique to reduce the area occupied by the thin-film-transistors comprising a pixel circuit. There are, however, limits to gate length scaling. For example, scaling gates comprised of indium gallium zinc oxide (commonly referred to as IGZO) below 5 μηι induces short-channel effects, such as negative voltage threshold **VT** values, higher OFF current, higher subthreshold slope, lower output resistance, and lower saturation field effect mobility. The short-channel effects also result in higher static power consumption, as well as lower frame rates for scaled down pixels due to lower switching speed caused by mobility degradation.

[0008] One attempt to mitigate short-channel effects is to employ a double-gate thin-film-transistor architecture, which exhibits higher transconductance and lower subthreshold values when compared to a single gate architecture. Double-gate thin-film-transistors, however, are more complex to integrate due to the added requirement to align both gates, as well as high cost per transistor, which can be cost-prohibitive for large-area displays. Further, IGZO-based double-gate thin-film-transistors still exhibit negative voltage threshold **VT** values for gate lengths below 5 μηι.

[0009] Accordingly, there is a need for a flexible thin-film-transistor that can be scaled down in size without introducing short-channel effects.

SUMMARY

[0010] According to an embodiment, there is a method for producing a thin-film-transistor, which involves forming a flexible substrate on a rigid substrate, forming a plurality of fins and trenches in a structural layer arranged on the flexible substrate, forming a wavy gate layer, channel layer, source contact layer, and drain contact layer on each of the plurality of fins and each of a plurality of trenches of the structural layer, and removing the plurality of fins and trenches having the wavy gate, channel, source contact, and drain contact layers from the rigid substrate.

[001 1] According to another embodiment there is a thin-film-transistor, which includes a flexible substrate, a structural layer attached to the flexible substrate, wherein the structural layer includes a plurality of fins and a trench between each of the plurality of fins, and a wavy gate layer, channel layer, source contact layer, and drain contact layer formed on the plurality of fins and the trench between each of the plurality of fins.

[0012] According to a further embodiment there is a method for producing a thin-film transistor, which involves forming a flexible substrate on a rigid substrate, forming a plurality of fins and trenches in an amorphous silicon layer arranged on the flexible substrate, forming a wavy gate layer on each of the plurality of fins and each of a plurality of trenches of the amorphous silicon layer, forming a wavy channel layer on each of the plurality of fins and each of a plurality of trenches of the amorphous silicon layer, forming a wavy source contact layer and a wavy drain contact layer on lateral ends of each of the plurality of fins and each of a plurality of trenches of the amorphous silicon layer, and removing the plurality of fins and

trenches having the wavy gate, channel, source contact, and drain contact layers from the rigid substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate one or more embodiments and, together with the description, explain these embodiments. In the drawings:

[001 4] Figure 1A is a schematic diagram of a top view of a conventional coplanar thin-film-transistor on a flexible substrate;

[0015] Figure 1B is a schematic diagram of a perspective view of a conventional coplanar thin-film-transistor on a flexible substrate;

[0016] Figure 2 is a flowchart of a method for producing a wavy channel thin-film-transistor on a flexible substrate according to an embodiment;

[0017] Figure 3A is a schematic diagram of a top view of a channel support structure of a wavy channel thin-film-transistor on a flexible substrate according to an embodiment;

[001 8] Figure 3B is a schematic diagram of a perspective view of a wavy channel thin-film-transistor on a flexible substrate according to an embodiment;

[0019] Figure 3C is a schematic diagram of a cross-sectional view of a wavy channel thin-film-transistor on a flexible substrate according to an embodiment;

[0020] Figure 4 is a flowchart of a method for producing a wavy channel thin-film-transistor on a flexible substrate according to an embodiment; and

[0021] Figures 5A-5L are schematic diagrams of a method for producing a wavy channel thin-film-transistor on a flexible substrate according to an embodiment.

DETAILED DESCRIPTION

[0022] The following description of the exemplary embodiments refers to the accompanying drawings. The same reference numbers in different drawings identify the same or similar elements. The following detailed description does not limit the invention. Instead, the scope of the invention is defined by the appended claims. The following embodiments are discussed, for simplicity, with regard to the terminology and structure of thin-film-transistors used in displays. However, the embodiments to be discussed next are not limited to thin-film-transistors used in displays but instead the embodiments can be employed in connection with other applications of thin-film-transistors.

[0023] Reference throughout the specification to "one embodiment" or "an embodiment" means that a particular feature, structure or characteristic described in connection with an embodiment is included in at least one embodiment of the subject matter disclosed. Thus, the appearance of the phrases "in one embodiment" or "in an embodiment" in various places throughout the specification is not necessarily referring to the same embodiment. Further, the particular features, structures or characteristics may be combined in any suitable manner in one or more embodiments.

[0024] Referring now to Figure 2, according to an embodiment a method for producing a thin-film-transistor comprises forming a flexible substrate on a rigid substrate (step 205) and then forming a plurality of fins and trenches in a structural layer arranged on the flexible substrate (step 210). The method further comprises forming a wavy gate layer, channel layer, source contact layer, and drain contact layer on each of the plurality of fins and each of a plurality of trenches of the structural layer

(step 215). The method also comprises removing the plurality of fins and trenches having the wavy gate, channel, source contact, and drain contact layers from the rigid substrate (step 220). The transistor formed by this method can be referred to as a wavy channel thin-film-transistor due to the formation of the channel on the plurality of fins and trenches.

[0025] Figures 3A, 3B, and 3C are schematic diagrams of a top view, perspective view, and side view of a wavy channel thin-film-transistor on a flexible substrate according to an embodiment. The schematic diagram of Figure 3A illustrates the channel support structure (i.e., the structural layer) without the active areas (i.e., gate, source, drain, and channel) of the thin-film transistor. As illustrated in Figure 3A, the channel support structure of the thin-film-transistor 300 includes a plurality of fins 304A and 304B (only two of which are labeled for purposes of clarity), between which there are trenches 302. In the illustrated example the width of the individual fins, i.e., the size in the z-axis, are 2 μηι and the fin pitch is 6 μηι. Of course, other widths and pitches can be employed. The entire channel support structure is arranged on a flexible substrate 308.

[0026] Referring now to Figures 3B and 3C, which show some of the active areas of the transistor, the lateral ends of the fins and trenches support source and drain contacts 312 and 314, between which a channel 310 is formed on the fins and trenches. The channel 310 and source and drain contacts 312 and 314 are arranged on a gate dielectric layer 318, which is formed directly on the fins and trenches. All of these components are arranged on an amorphous silicon layer 316, which forms a structural layer in which the fins and trenches are formed.

[0027] As illustrated in Figure 3C, a gate metal layer 320 is arranged between the gate dielectric layer 318 and an insulating layer 322, which is directly adjacent to the amorphous silicon layer 316. Because Figure 3C is a cross-sectional view of Figure 3B along the X-X line passing through the channel 310, the source and drain contacts 312 and 314 are not illustrated in this figure. Figure 3C also illustrates the fin 304A having a non-perpendicular sidewall 324 to the trench bottom 326, which in the illustrated example is at 85° angle.

[0028] Although the fin sidewall 324 can be arranged at a variety of different angles to the trench bottom 326, including being perpendicular to the trench bottom 326, an angled side-wall improves the deposition of the various layers because there is no scalloping effect, whereas fin sidewalls 324 arranged perpendicularly to the trench bottom 326 exhibit a scalloping effect that can be detrimental to the deposition of the various layers. Those skilled in the art will recognize that scalloping occurs in the deep reactive ion etching process, also known as the Bosch process, due to consecutive steps of sidewall passivation and anisotropic etching processes, which results in a 90° sidewall angle. By avoiding the sidewall passivation step, the disclosed device has a non-perpendicular sidewall angle, such as 85°. The conformal deposition and smooth side-walls of the angled fins mitigate problems arising in typical nonplanar thin-film-transistor architectures, such as vertical thin-film-transistor architecture, which suffer from both higher gate leakage and gate-to-source/drain overlap parasitic capacitance. Further, the process flow is compatible with self-aligned source and drain deposition techniques.

[0029] A thin-film-transistor with fins and trenches is formed in the manner disclosed by increasing the width (i.e., the distance in a direction perpendicular to a

top surface of the transistor) compared to the width of conventional coplanar thin-film-transistors. The fins and trenches improve the overall electrical characteristics of the device. Specifically, the increased width allows the use of the smallest reliable gate length without changing the threshold voltage V_T or off current I_{OFF}. This allows a reduction in the other dimensions of the thin-film-transistor, which allows smaller thin-film-transistor pixel circuits and more dense pixel arrangements. A thin-film-transistor produced in the manner disclosed was arranged to drive a light emitting diode (LED), which showed 70% higher currents compared to conventional coplanar thin-film-transistors integrated on the same substrate as the disclosed flexible substrate. The 70% higher currents are due to the 70% larger width of the channel compared to coplanar devices due to the disclosed device having 2 μηι high fins and 6 μηι fin pitch.

[0030] A more detailed explanation of a method of producing a wavy channel thin-film-transistor will now be described in connection with Figures 4 and 5A-5L. Referring initially to Figures 4 and 5A, a low stress polymer 504, such as polyimide PI-621 1 from DuPont, is spun on a rigid Si substrate 502, for example at 2000 RPM, and then cured, for example at 360° C (step 405). In one embodiment, the low stress polymer layer can be 9 μηι thick. The low stress polymer layer acts as a flexible substrate for the wavy channel thin-film-transistor after it is removed from the rigid Si substrate 502. A silicon dioxide $(S1O_2)$ adhesion and etch stop layer 506 is deposited using plasma enhanced chemical vapor deposition (step 410 and Figure 5B). The silicon dioxide layer 506 acts as an adhesion layer and etch stop layer for the following layer. The silicon dioxide layer 506 can have a thickness of, for example, 200 nm.

[0031] An amorphous silicon layer 508 is then deposited, for example at 250° C, which acts as the structural layer for the subsequent formation of the fins and trenches (step 415 and Figure 5C). The amorphous silicon layer 508 is then etched to form a plurality of trenches 510i-510x and a plurality of fins 512i-512x (step 420 and Figure 5D). For example, the amorphous silicon layer 508 can be 2 μηι thick and can be etched using SF_6 based reactive ion etching. As discussed above, the sidewalls of the fins can be perpendicular to the bottom of the trenches or can be at an angle, such as an 85° angle. These figures illustrate only two fins and three trenches for purposes of clarity and a single transistor can have more fins and trenches than those illustrated.

[0032] An electrical insulation layer 514, for example an AI2O3 layer, is deposited on the fins and trenches using atomic layer deposition (ALD) in order to electrically insulate the devices from the amorphous silicon structural layer (step 425 and Figure 5E). The electrical insulation layer can be, for example, 50 nm thick. A gate pad layer 516, for example an aluminum layer, is then deposited using DC magnetron sputtering and then patterned using, for example, a lift-off technique (step 430 and Figure 5F). The gate pad layer 516 can be, for example, 200 nm thick.

[0033] The wafer is again loaded in the atomic layer deposition chamber where a gate dielectric 518 is formed (step 435 and Figure 5G). The gate dielectric layer can be comprised of, for example, AI2O3 and can be, for example, 50 nm thick. While the wafer is still in the atomic layer deposition chamber and without breaking the vacuum of the chamber, the channel is formed by applying a channel material 520 (step 440 and Figure 5H). The channel can comprise, for example, zinc oxide (ZnO), and can be, for example, 40 nm thick. The wafer is then removed from the

atomic layer deposition chamber and patterned, for example using buffered oxide etchant (BOE) for a period of time, such as 10 seconds.

[0034] Zinc oxide is a particularly advantageous channel material because it can achieve a highly uniform/conformal deposition using atomic layer deposition, which provides more uniform electrical properties across the wafer. However, the fin and trench structure is compatible with other channel deposition methods, such as DC or RF magnetron sputtering, because the angled fin side-wall allows for ample coverage of sputtered species, such as DC sputtered aluminum. Thus, the disclosed thin-film-transistor is agnostic to channel material, and other possible channel materials deposited by other deposition methods can include indium gallium zinc oxide (IGZO), indium zinc oxide (IZO), etc.

[0035] The source and drain contact layers 522 are then formed and patterned, for example using a lift-off technique (step 445 and Figure 5I). The source and drain contact layers can be formed using DC sputtering by depositing, for example, 50 nm of titanium and 200 nm of gold. It should be recognized that because Figure 5I is a side view, only one of the source and drain contact layers is visible, and also the channel is not visible because the source and drain contact layers are formed on the lateral ends of the device.

[0036] The device is then annealed in air, for example at 200° C for 1 hour, to improve the electrical characteristics (step 450). A passivation layer 524 is then applied to protect the channel from environmental degradation and the gate oxide is etched to allow access to the gate pads (step 455 and Figure 5J). The passivation layer 524 can be an organic or inorganic passivation layer. Finally, the device is removed from the rigid silicon substrate (step 460 and Figure 5K). In order to

simplify handling of the device, the device can be transferred to an additional flexible substrate 526 (Figure 5L), which is an optional step not illustrated in Figure 4.

[0037] A wavy channel thin-film transistor produced by the disclosed process was tested along with a conventional coplanar thin-film-transistor to compare the performance of the two devices. Both devices exhibited a V_0 of -2.2V, which is defined as the voltage at which the drain current increases exponentially from the noise floor, i.e., gate leakage.

[0038] The threshold voltage V_T of both devices was extracted in the saturation regime from the point of the highest first derivative of $\sqrt{I_{ds}}$ versus V_{gs} curve. The coplanar and wavy channel thin-film-transistors threshold voltage V_T values were 6.6V and 4.2V, respectively. Output characteristics demonstrated 70% higher drain current values for wavy channel device compared to the coplanar device, which is proportional to the extra device width of the wavy channel thin-film-transistor. Minimum subthreshold slope (SS) values for coplanar and wavy channel devices were 0.4 and 0.2 V/decade, respectively. The lower SS and V_T values for wavy channel thin-film-transistor can be attributed to higher electric field at trench corner, i.e., the corner effects.

[0039] Flexibility of the wavy channel thin-film-transistor was tested at a bending radius (R) of 5 mm. At this bending radius, the device "ON" current was only approximately 10% lower compared with a 1 cm bending radius. Further, at the 5mm bending radius, the device "ON" current does not degrade, gate leakage values remain below 10 nA (and did not demonstrate signs of increasing with further electric cycling), and the hysteresis in transfer characteristics remained less than 0.2V.

[0040] Saturation field effect mobility, μ_{sat} was calculated according to the MOSFET expression:

[0041] $$\mu_{sat} = \left(\frac{2L_g}{W}\right)\left(\frac{1}{C_{ox}}\right)\left(\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}\right)$$

[0042] where C_{ox} is the oxide gate capacitance per unit area, L_g is the gate length, and W is the device width. The 70% higher width was accounted for in the saturation mobility calculation, which demonstrated that the wavy channel thin-film-transistor can significantly increase output current per unit chip area without compromising static power consumption. This testing also demonstrated the output characteristics did not degrade with mechanical bending as a value of Ids = $1 * 10^{-3}$ A was achieved down to a 5 mm bending radius.

[0043] The wavy channel thin-film transistor and conventional coplanar thin-film-transistor were also tested for potential application in a flexible display application by mounting low power red light (640 nm) LEDs on a flexible substrate and driving the optical power outputs of the LED by the respective drive currents. Typical diode I-V characteristics of the off-the-shelf LED showed a turn-on voltage of ~1.6V. Testing the output power versus injection current demonstrated that the injection currents were 600 μA for a conventional coplanar thin-film-transistor and 1100 μA for the disclosed wavy channel thin-film-transistor. This demonstrates that the optical output of the LED operated by the disclosed wavy channel thin-film-transistor is ~ 2X the optical power emitted by the LED operated by a conventional coplanar thin-film-transistor, i.e. 3 mW *vs.* 1.5 mW, under similar gate and drain bias conditions for both devices.

[0044] Electro-luminescence (EL) measurements of the LED when driven by the respective currents of the coplanar and wavy channel thin-film-transistors were also performed. The LED driven by the disclosed wavy channel thin-film-transistor exhibited more than 2X intensity at the peak wavelength of 640 nm when compared to the LED driven by conventional coplanar thin-film-transistor, when both are biased under similar gate and drain bias conditions. This demonstrates that the disclosed wavy channel thin-film-transistor enables pixel area down-scaling and higher pixel fill factors when compared to the conventional coplanar thin-film-transistor when providing identical drive currents.

[0045] Accordingly, the disclosed wavy channel thin-film-transistor can achieve 70% higher device width within the same chip area when compared to a conventional coplanar thin-film-transistor. The disclosed wavy channel thin-film-transistor achieves 70% higher drive current, lower subthreshold slope, and lower V_T values when compared to conventional coplanar thin-film-transistors even when bent down to 5 mm bending radius.

[0046] Because the disclosed wavy channel thin-film-transistor exhibited 2X the output power when driving a flexible LED compared to a conventional coplanar thin-film-transistor, the disclosed wavy channel thin-film-transistor can occupy 70% lower area when compared to a conventional coplanar thin-film-transistor at an identical drive current, and thus enable higher pixel fill factor, as well as, higher number of pixels per inch (PPI). Thus, the disclosed wavy channel thin-film-transistor can be employed for, among other applications, future ultra-high-definition flexible displays of beyond 8K resolution. Drive current greater than 2X can be achieved with tighter fin pitches and higher aspect ratio trenches.

[0047] The disclosed embodiments provide a flexible, wavy channel thin-film-transistor. It should be understood that this description is not intended to limit the invention. On the contrary, the exemplary embodiments are intended to cover alternatives, modifications and equivalents, which are included in the spirit and scope of the invention as defined by the appended claims. Further, in the detailed description of the exemplary embodiments, numerous specific details are set forth in order to provide a comprehensive understanding of the claimed invention. However, one skilled in the art would understand that various embodiments may be practiced without such specific details.

[0048] Although the features and elements of the present exemplary embodiments are described in the embodiments in particular combinations, each feature or element can be used alone without the other features and elements of the embodiments or in various combinations with or without other features and elements disclosed herein.

[0049] This written description uses examples of the subject matter disclosed to enable any person skilled in the art to practice the same, including making and using any devices or systems and performing any incorporated methods. The patentable scope of the subject matter is defined by the claims, and may include other examples that occur to those skilled in the art. Such other examples are intended to be within the scope of the claims.

WHAT IS CLAIMED IS:

1. A method for producing a thin-film-transistor, comprising:

forming (205, 405) a flexible substrate (305, 504) on a rigid substrate (502);

forming (210, 420) a plurality of fins (304A, 304B, 512I-512X) and trenches (302, 510i-510x) in a structural layer (316, 508) arranged on the flexible substrate (504);

forming (215, 430, 440, 445) a wavy gate layer (320, 516), channel layer (310, 520), source contact layer (312, 522), and drain contact layer (314, 522) on each of the plurality of fins (304A, 304B, 512I-512X) and each of a plurality of trenches (302, 5101-510x) of the structural layer (316, 508); and

removing (220, 460) the plurality of fins (304A, 304B, 512I-512X) and trenches (302, 5101-510x) having the wavy gate (320, 516), channel (310, 520), source contact (312, 522), and drain contact (314, 522) layers from the rigid substrate (502).

2. The method of claim 1, further comprising:

forming an adhesion and etch stop layer on the flexible substrate prior to forming the structural layer on the flexible substrate.

3. The method of claim 1, wherein the plurality of trenches are formed in the structural layer using reactive ion etching.

4. The method of claim 1, further comprising:

forming a first electrically insulating layer on each of the plurality of fins and each of the plurality of trenches prior to forming the channel layer.

5. The method of claim 4, wherein the gate layer is formed on the first electrically insulating layer prior to forming the channel layer.

6. The method of claim 5, further comprising:

forming a second insulating layer on the gate layer prior to forming the channel layer.

7. The method of claim 6, wherein the first and second electrically insulating layers are formed using atomic layer deposition.

8. The method of claim 6, further comprising:

etching the second insulating layer to expose gate pads of the electrically conducting layer.

9. The method of claim 1, further comprising:

applying a photoresist passivation layer on the plurality of fins and plurality of trenches prior to removing the plurality of fins and trenches from the rigid substrate.

10. The method of claim 1, wherein sidewalls of each of the plurality of fins are non-perpendicular to a bottom of each of the plurality of trenches.

11. The method of claim 1, wherein the source and drain layers are formed subsequent to the channel layer.

12. The method of claim 1, wherein the structural layer is amorphous silicon.

13. A thin-film-transistor, comprising:

a flexible substrate (308, 504);

a structural layer (316, 508) attached to the flexible substrate (308, 504), wherein the structural layer (316, 508) includes a plurality of fins (304_A, 304_B, 512_I-512_X) and a trench (302, 510i-510x) between each of the plurality of fins (304_A, 304_B, 512i-512x); and

a wavy gate layer (320, 516), channel layer (310, 520), source contact layer (312, 522), and drain contact layer (314, 522) formed on the plurality of fins (304_A, 304_B, 512i-512x) and the trench (302, 510i-510x) between each of the plurality of fins.

14. The thin-film-transistor of claim 13, wherein sidewalls of each of the plurality of fins are non-perpendicular to a bottom of each of the plurality of trenches.

15. The thin-film-transistor of claim 13, wherein a thickness of the flexible substrate is such that the thin-film-transistor achieves a bending radius down of at least 5 mm.

16. The thin-film-transistor of claim 13, wherein the structural layer is amorphous silicon.

17. A method for producing a thin-film transistor, comprising:

forming (205, 405) a flexible substrate (305, 504) on a rigid substrate (502);

forming (210, 420) a plurality of fins (304_A, 304_B, 512i-512x) and trenches (302, 510i-510x) in an amorphous silicon layer (316, 508) arranged on the flexible substrate (504);

forming (215, 430) a wavy gate layer (320, 516) on each of the plurality of fins (304_A, 304_B, 512i-512x) and each of a plurality of trenches (302, 510i-510x) of the amorphous silicon layer (316, 508);

forming (215, 440) a wavy channel layer (310, 520) on each of the plurality of fins (304_A, 304_B, 512i-512x) and each of a plurality of trenches (302, 510i-510x) of the amorphous silicon layer (316, 508);

forming (215, 445) a wavy source contact layer (312, 522) and a wavy drain contact layer on lateral ends of each of the plurality of fins (304_A, 304_B, 512i-512x) and each of a plurality of trenches (302, 510i-510x) of the amorphous silicon layer (316, 508); and

removing (220, 460) the plurality of fins (304_A, 304_B, 512_I-512_X) and trenches (302, 510i-510x) having the wavy gate (320, 516), channel (310, 520), source contact (312, 522), and drain contact (314, 522) layers from the rigid substrate (502).

18. The method of claim 17, further comprising:

applying a photoresist passivation layer on the plurality of fins and plurality of trenches prior to removing the plurality of fins and trenches from the rigid substrate.

19. The method of 17, wherein sidewalls of each of the plurality of fins are non-perpendicular to a bottom of each of the plurality of trenches.

FIG. 1A

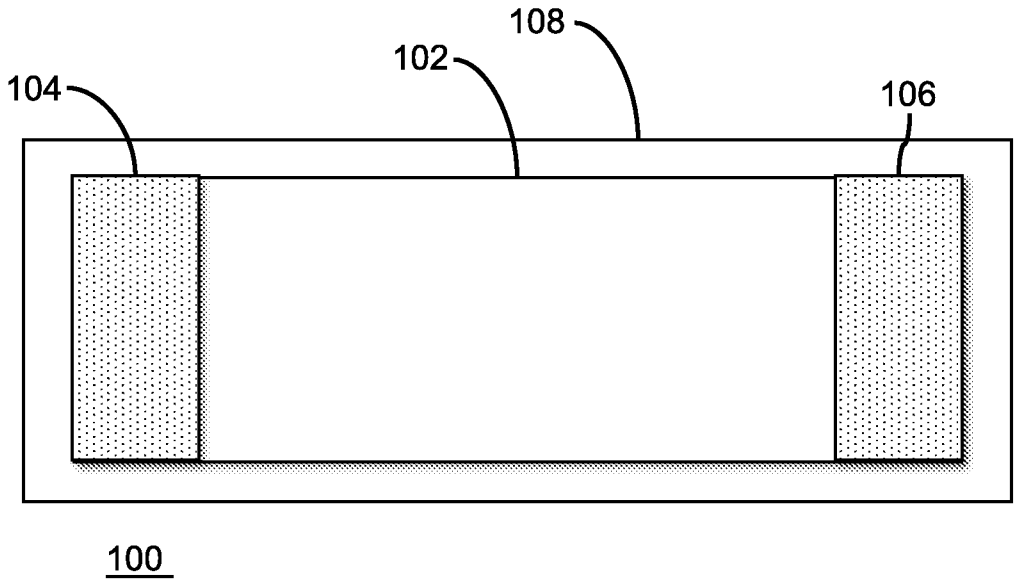


FIG. 1B

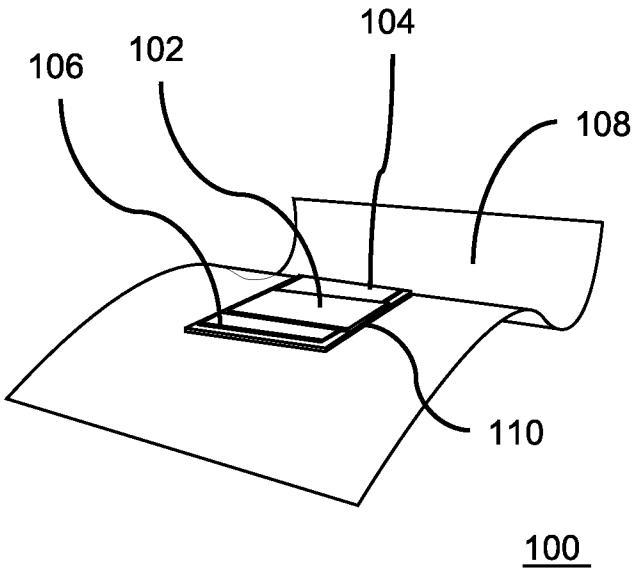


FIG. 2

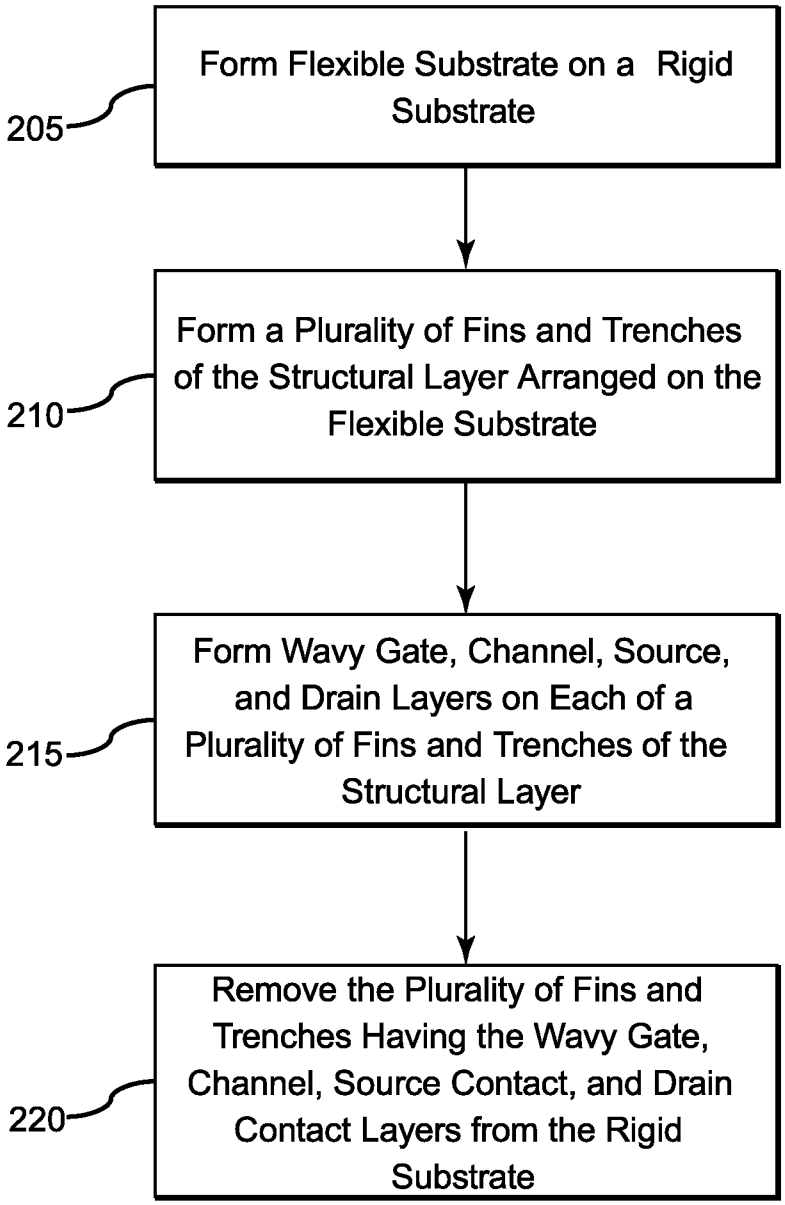

Form Flexible Substrate on a Rigid Substrate
205
Form a Plurality of Fins and Trenches of the Structural Layer Arranged on the Flexible Substrate
210
Form Wavy Gate, Channel, Source, and Drain Layers on Each of a Plurality of Fins and Trenches of the Structural Layer
215
Remove the Plurality of Fins and Trenches Having the Wavy Gate, Channel, Source Contact, and Drain Contact Layers from the Rigid Substrate
220

FIG. 3A

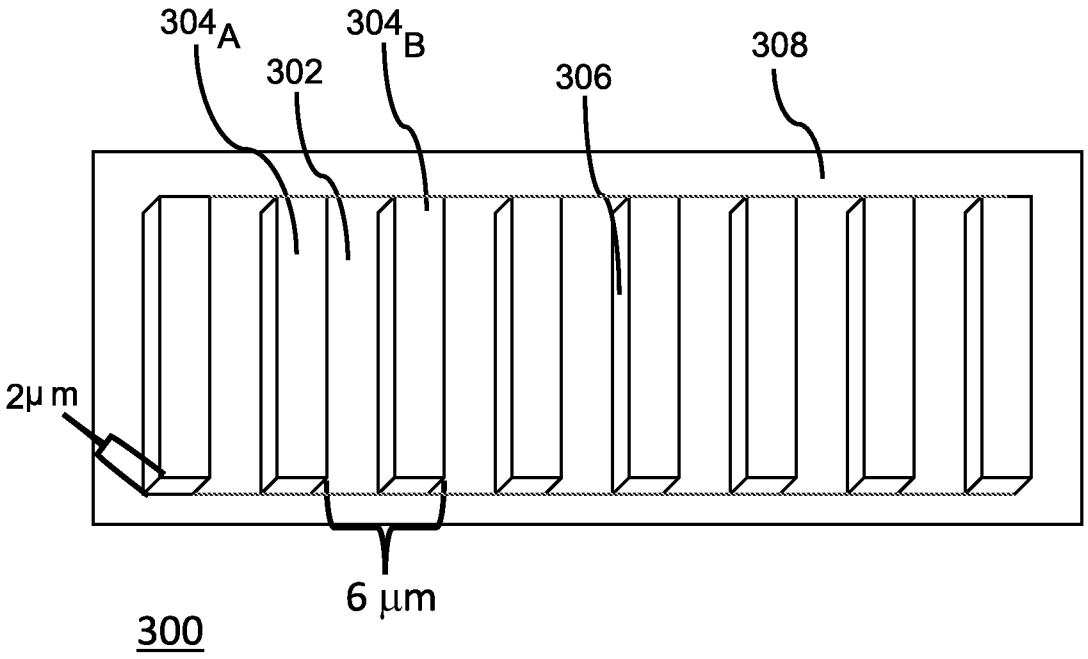

304A
304B
302
306
308
2µm
6 µm
300

FIG. 3B

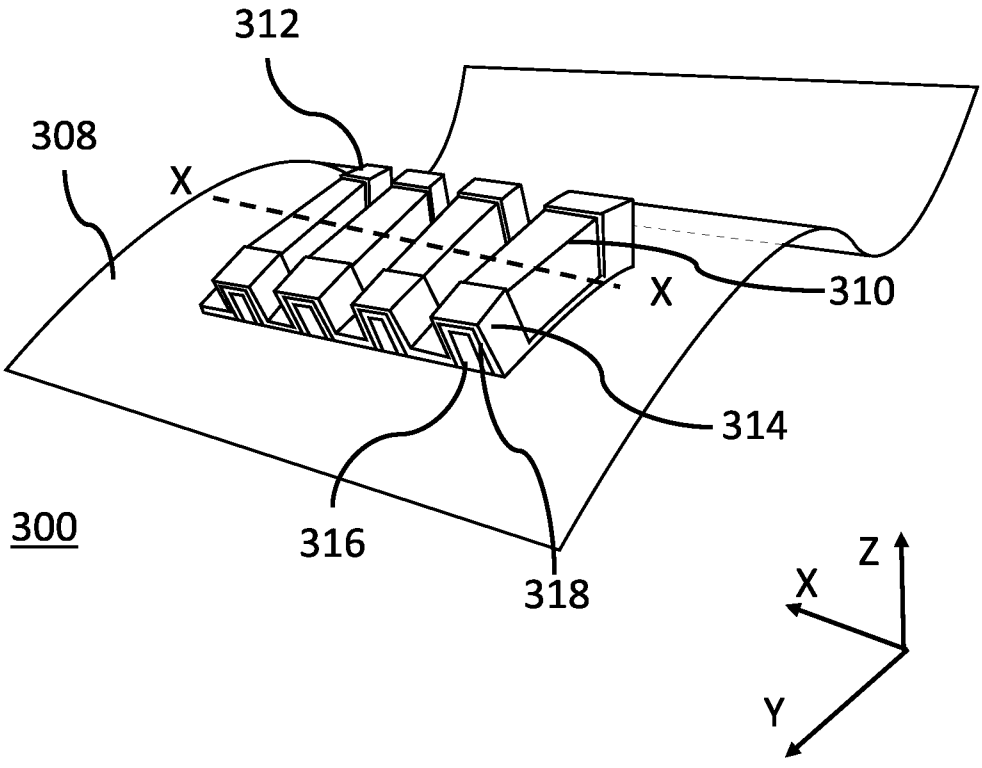

312
308
X
X
310
314
316
318
300
Z
X
Y

FIG. 3C

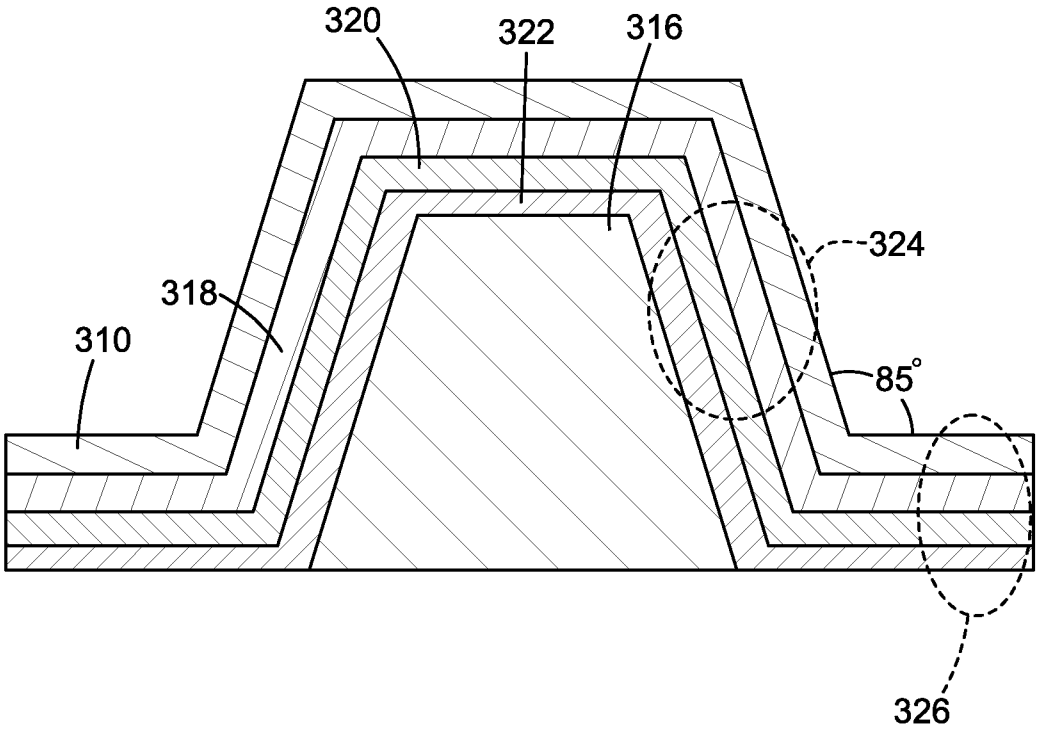


FIG. 4

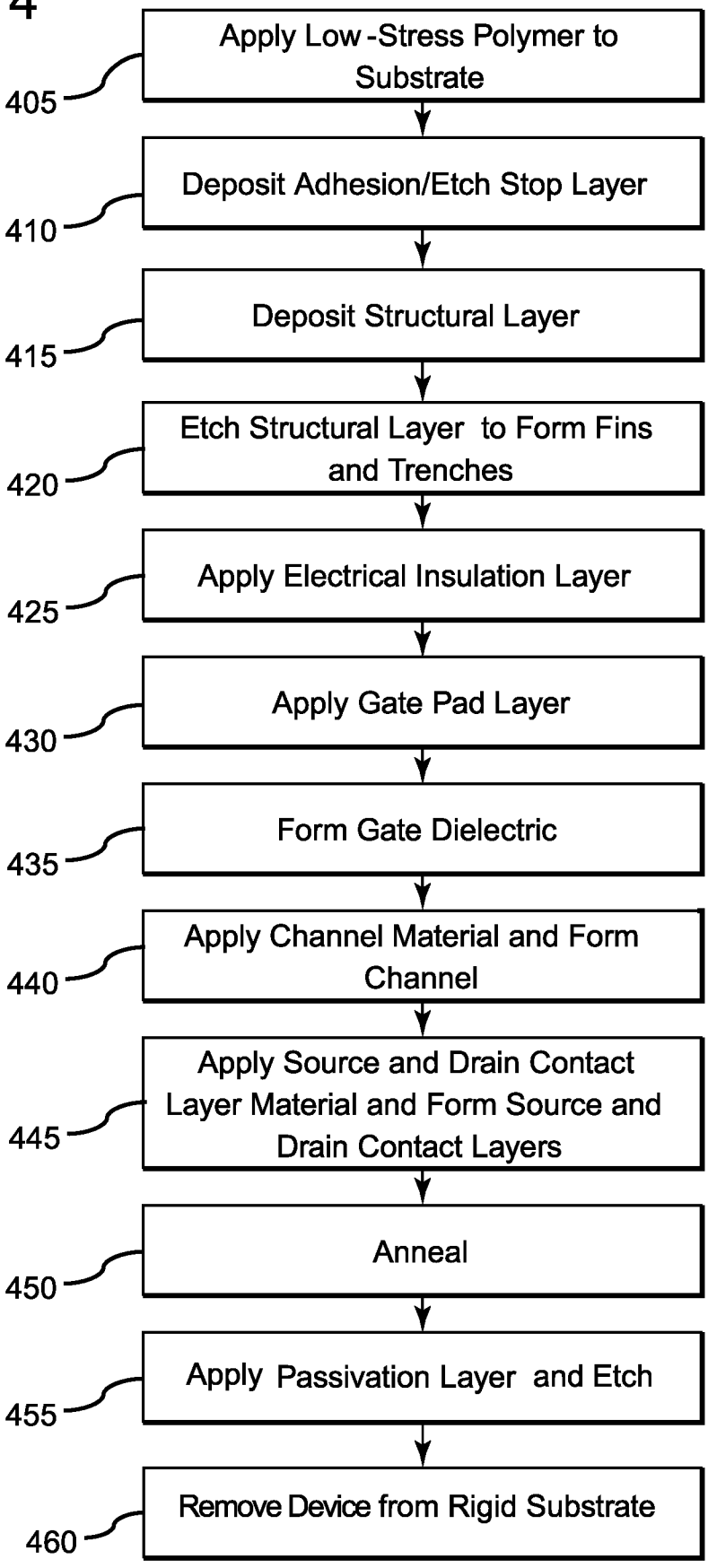

Apply Low-Stress Polymer to Substrate
405
Deposit Adhesion/Etch Stop Layer
410
Deposit Structural Layer
415
Etch Structural Layer to Form Fins and Trenches
420
Apply Electrical Insulation Layer
425
Apply Gate Pad Layer
430
Form Gate Dielectric
435
Apply Channel Material and Form Channel
440
Apply Source and Drain Contact Layer Material and Form Source and Drain Contact Layers
445
Anneal
450
Apply Passivation Layer and Etch
455
Remove Device from Rigid Substrate
460

FIG. 5A

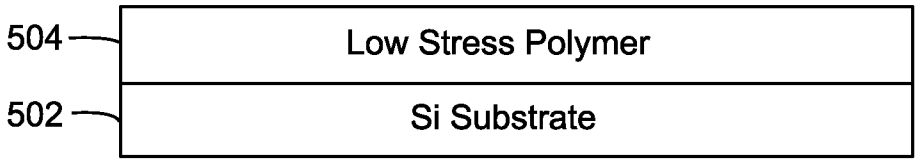

504
Low Stress Polymer
502
Si Substrate

FIG. 5B

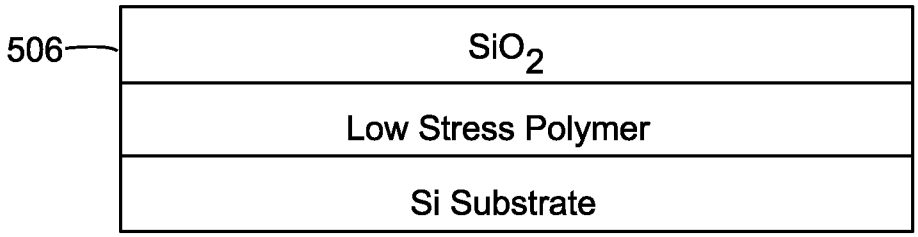

506
SiO_2
Low Stress Polymer
Si Substrate

FIG. 5C

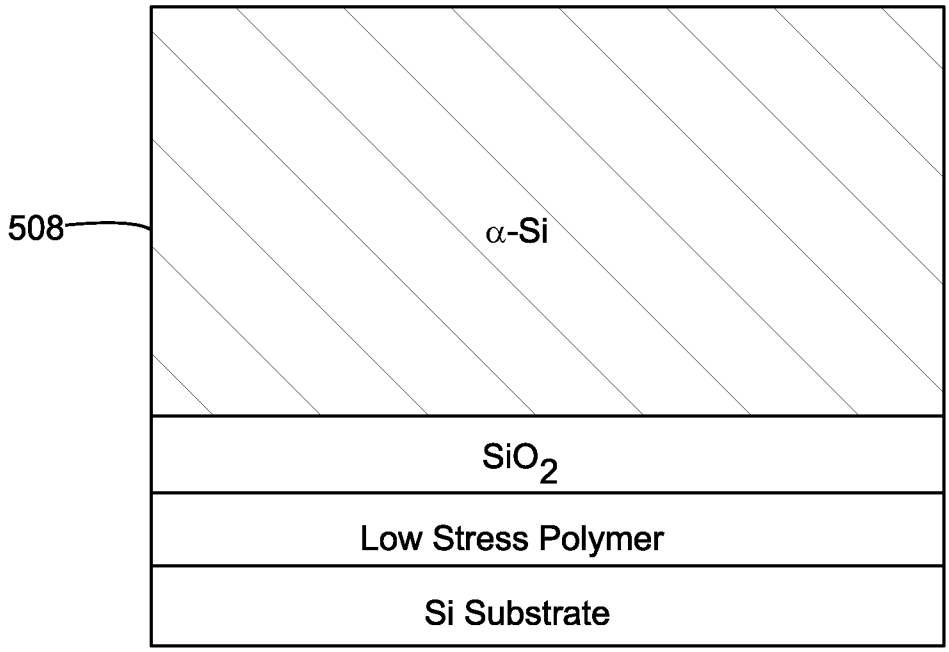

508
α-Si
SiO2
Low Stress Polymer
Si Substrate

FIG. 5D

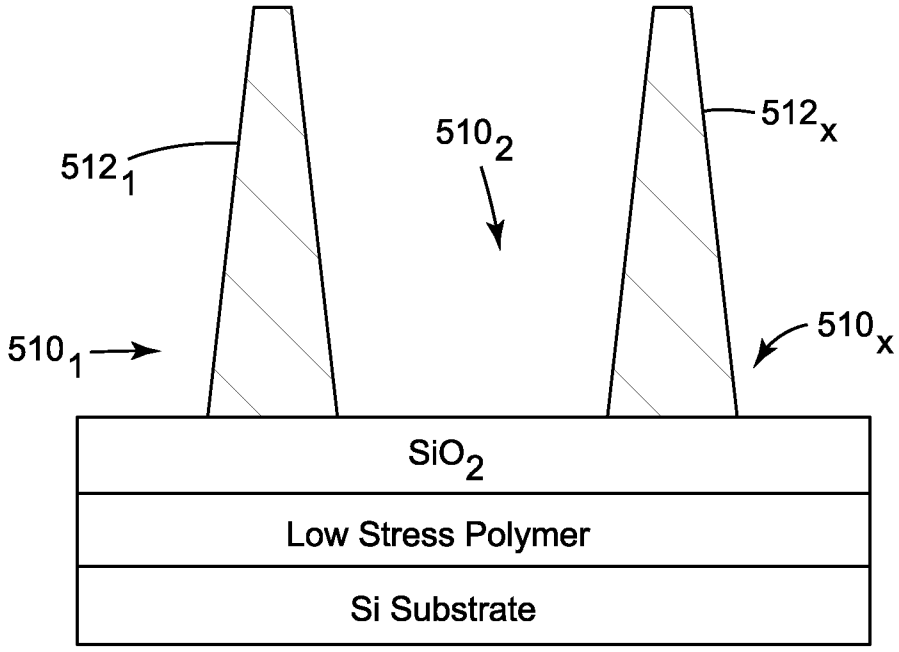

512x
510 2
512 1
510 1
510x
SiO2
Low Stress Polymer
Si Substrate

FIG. 5E

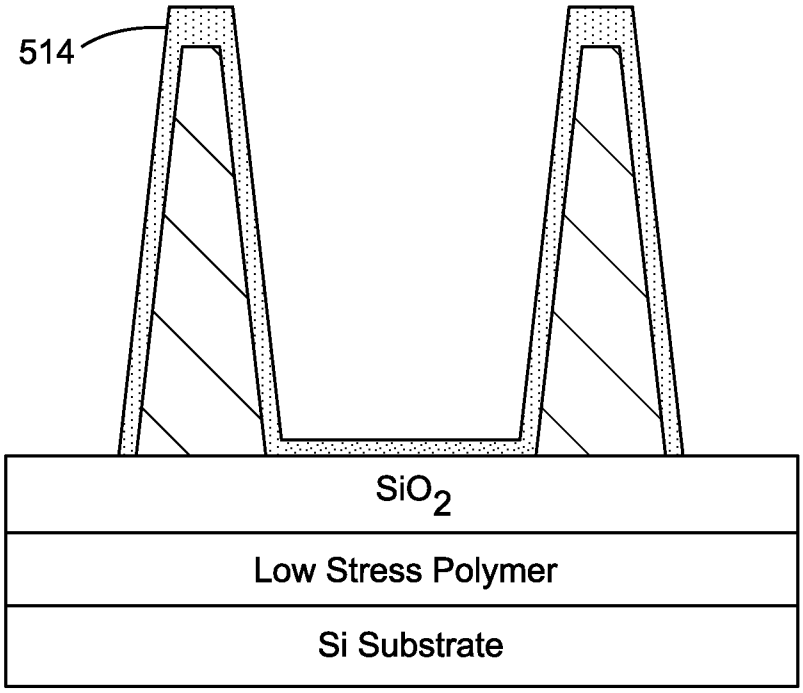

514
SiO_2
Low Stress Polymer
Si Substrate

FIG. 5F

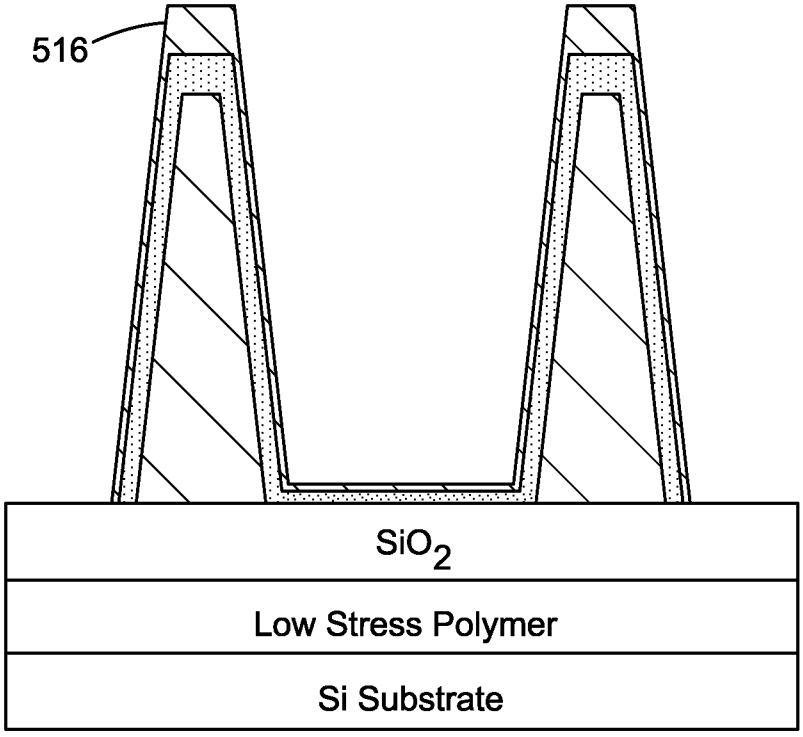

516
SiO_2
Low Stress Polymer
Si Substrate

FIG. 5G

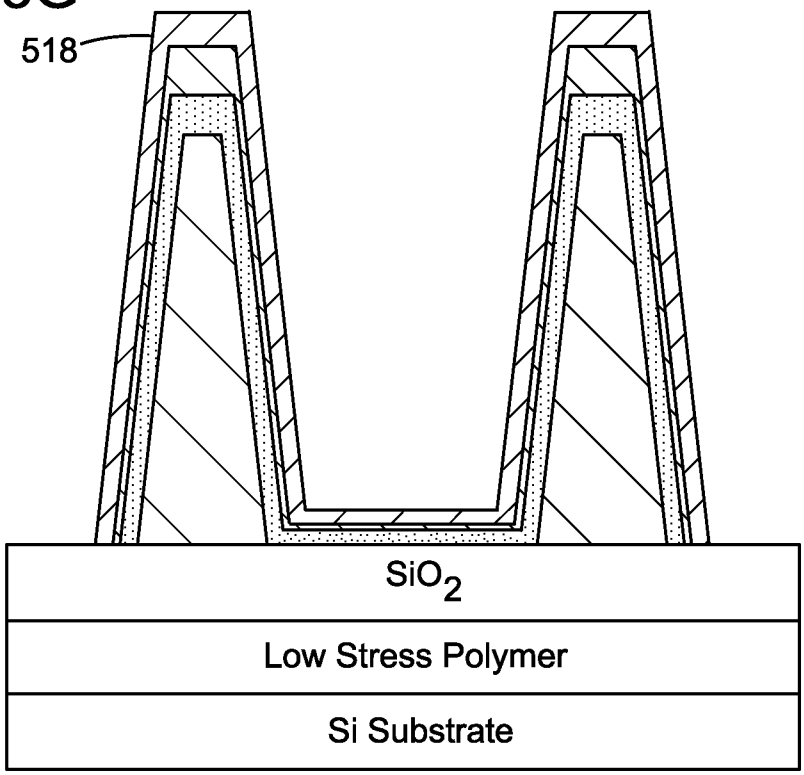

518
SiO_2
Low Stress Polymer
Si Substrate

FIG. 5H

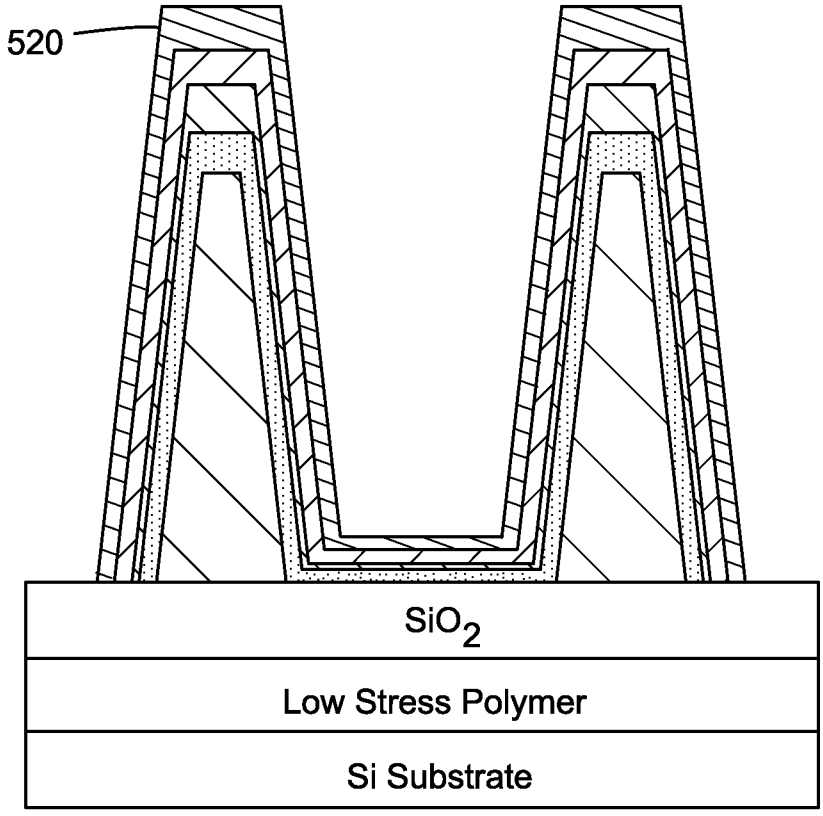

520
SiO_2
Low Stress Polymer
Si Substrate

FIG. 5I

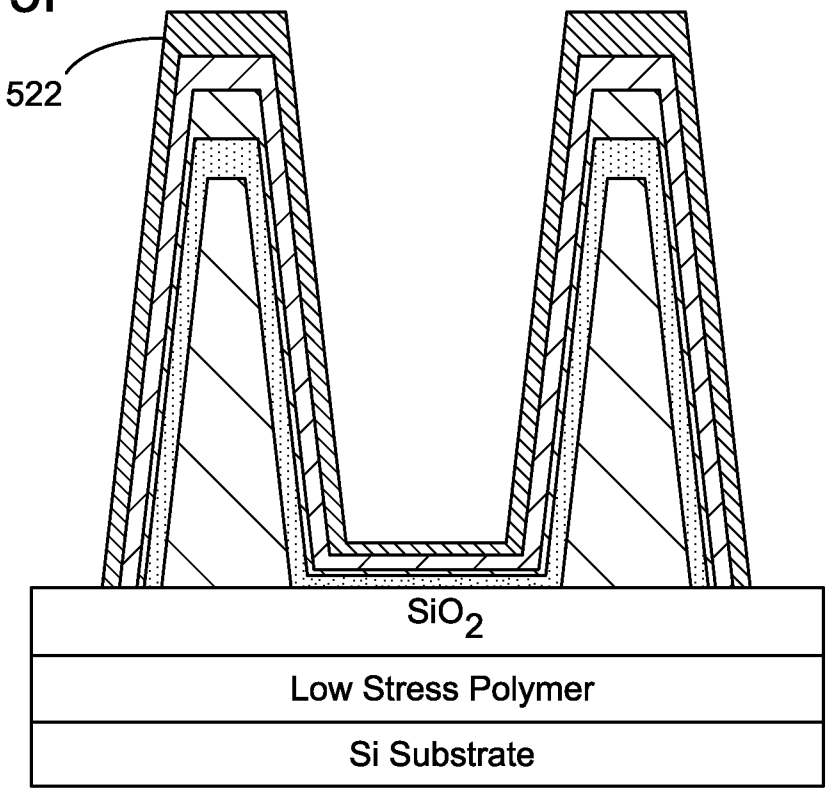

522
SiO_2
Low Stress Polymer
Si Substrate

FIG. 5J

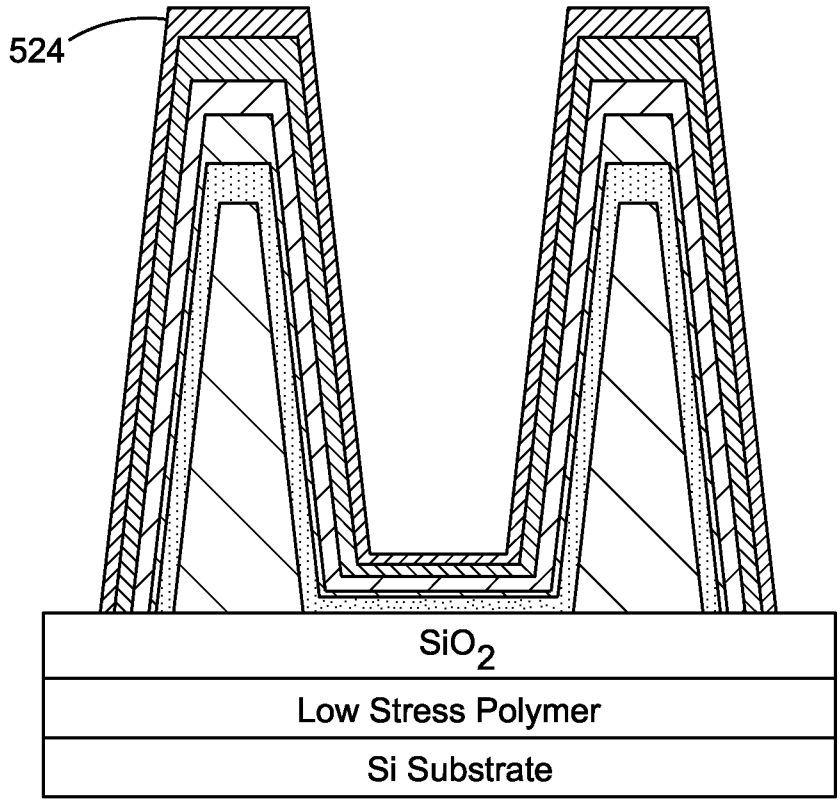

524
SiO_2
Low Stress Polymer
Si Substrate

FIG. 5K

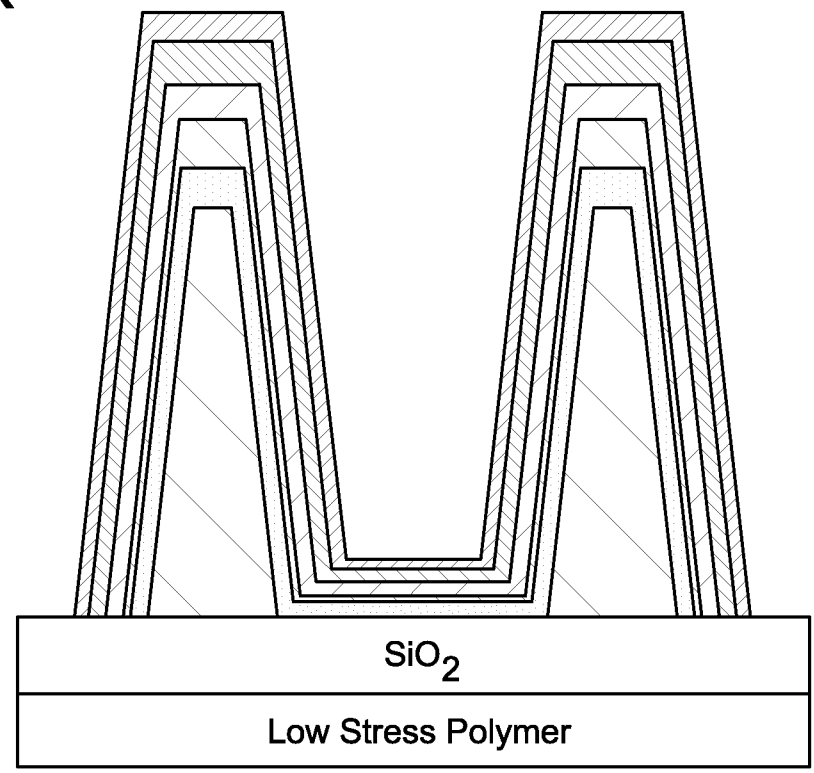
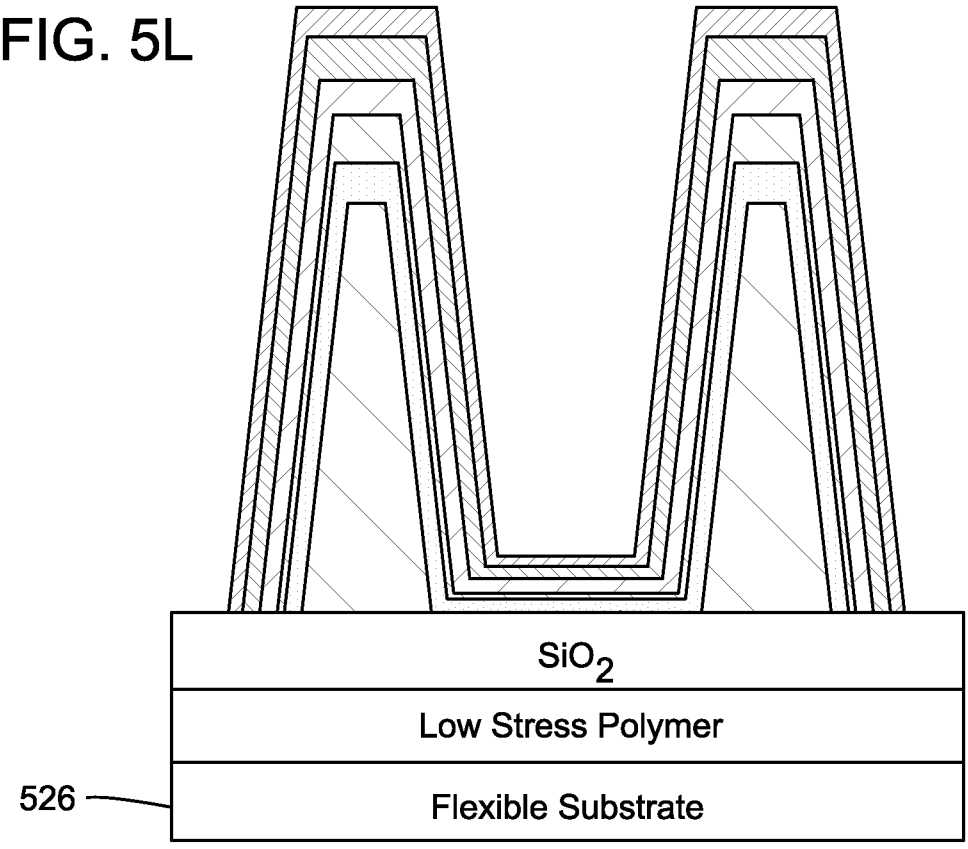

SiO2
Low Stress Polymer

FIG. 5L


SiO2
Low Stress Polymer
526
Flexible Substrate

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2018/050207

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/66 H01L29/786 H01L27/12 H01L29/423
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal , WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	HANNA AMIRNET AL: "Wavy Channel TFT-Based Digital Circuits" , IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE SERVICE CENTER, PISACATAWAY, NJ , US, vol . 63 , no. 4 , 1 April 2016 (2016-04-01) , pages 1550-1556, XP011603933 , ISSN : 0018-9383 , D0I : 10. 1109/TED. 2016. 2527795 [retrieved on 2016-03-22] page 1551 , column 1, paragraph 2 - column 2 , paragraph 1; figure 1	1-19

X	US 2016/365459 Al (HONG SUNG JIN [KR] ET AL) 15 December 2016 (2016-12-15) paragraph [0035] - paragraph [0047]	1-19

	-/- ·	

X Further documents are listed in the continuation of Box C.

X See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
11 April 2018	17/04/2018

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Hoffmann , Niels

4

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	HANNA AMIR N ET AL: "Wavy Channel architecture thin film transistor (TFT) using amorphous zinc oxide for high-performance and low-power semiconductor circuits", 2015 73RD ANNUAL DEVICE RESEARCH CONFERENCE (DRC), IEEE, 21 June 2015 (2015-06-21), pages 201-202, XP033188833, DOI: 10.1109/DRC.2015.7175633 ISBN: 978-1-4673-8134-5 [retrieved on 2015-08-03] the whole document	1-19
A	US 2013/175530 Al (NODA KOSEI [JP] ET AL) 11 July 2013 (2013-07-11) the whole document	1-19
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A	W0 2016/140975 Al (CBRITE INC [US]) 9 September 2016 (2016-09-09) the whole document	1,2,17
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2018/050207

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