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(54) **MODULATION OF STRESS IN STRESS FILM THROUGH ION IMPLANTATION AND ITS APPLICATION IN STRESS MEMORIZATION TECHNIQUE**

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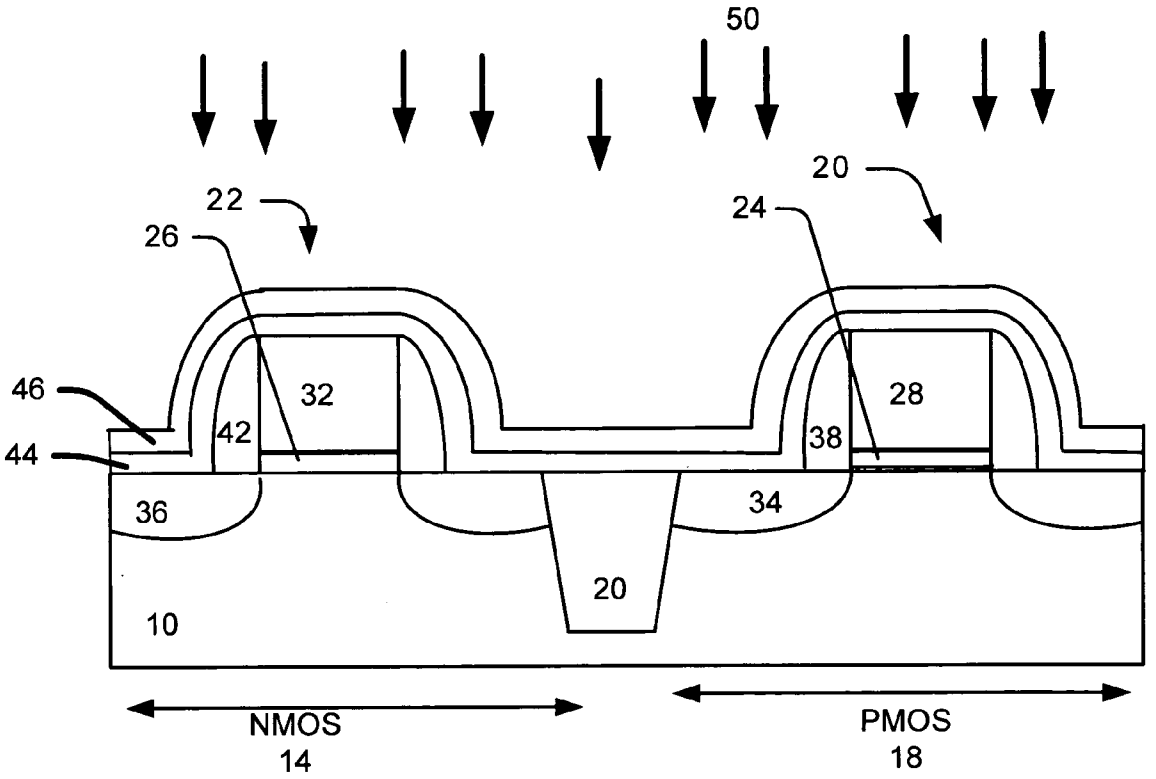
(57) **ABSTRACT**

Some example embodiments of the invention provide a method to improve the performance of MOS devices by increasing the stress in the channel region. An example embodiment for a NMOS transistor is to form a tensile stress layer over a NMOS transistor. A heavy ion implantation is performed into the stress layer and then an anneal is performed. This increases the amount of stress from the stress layer that the gate retains/memorizes thereby increasing device performance.



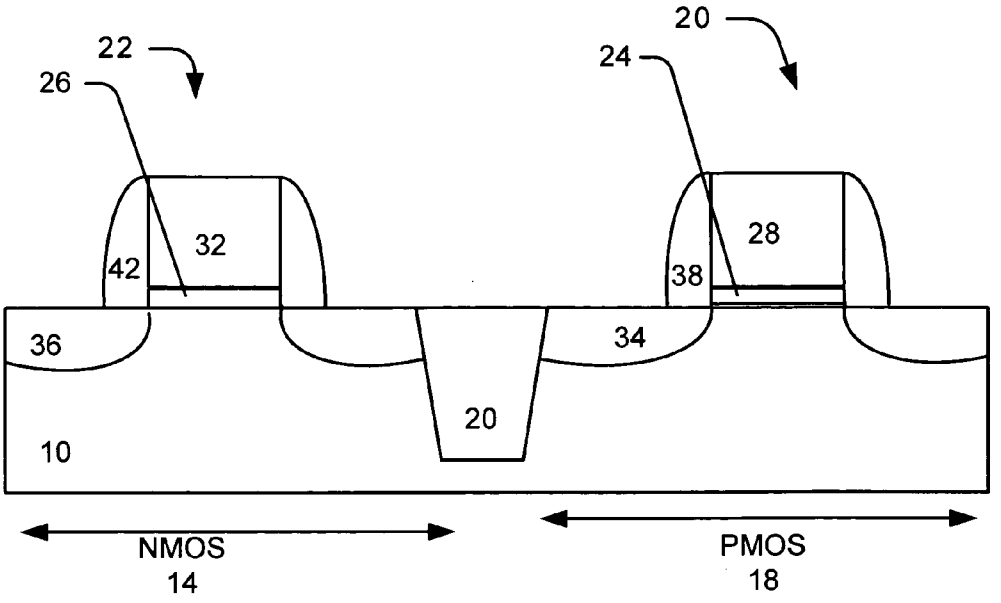


FIGURE 1

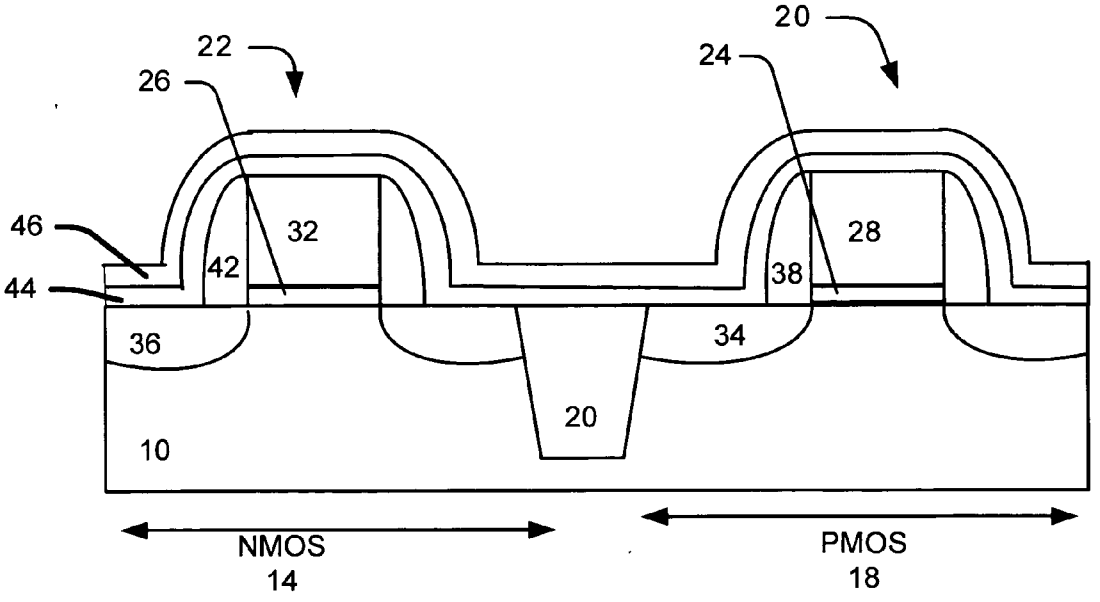


FIGURE 2

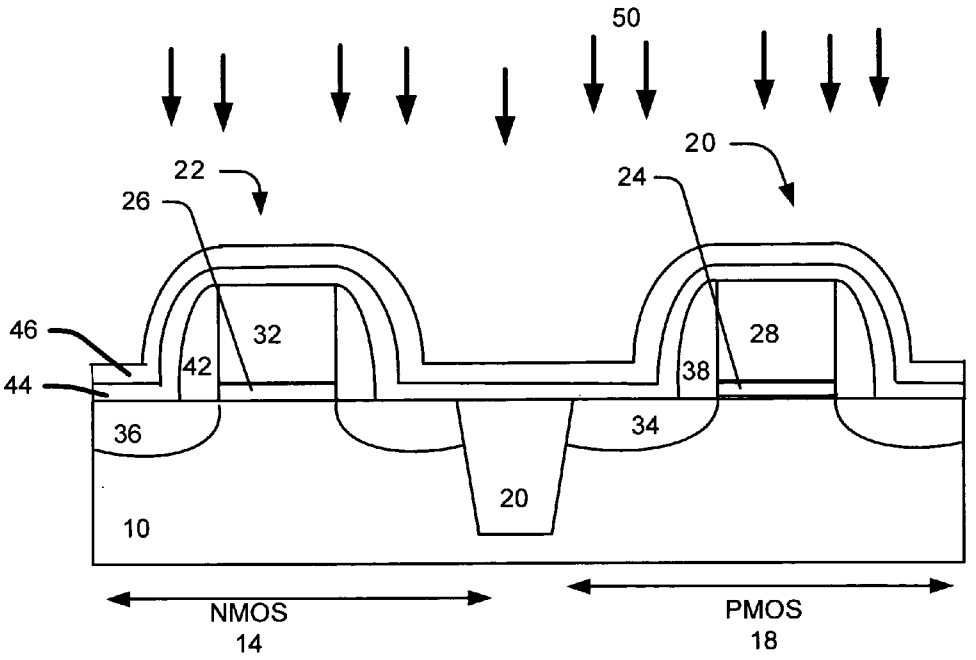


FIGURE 3

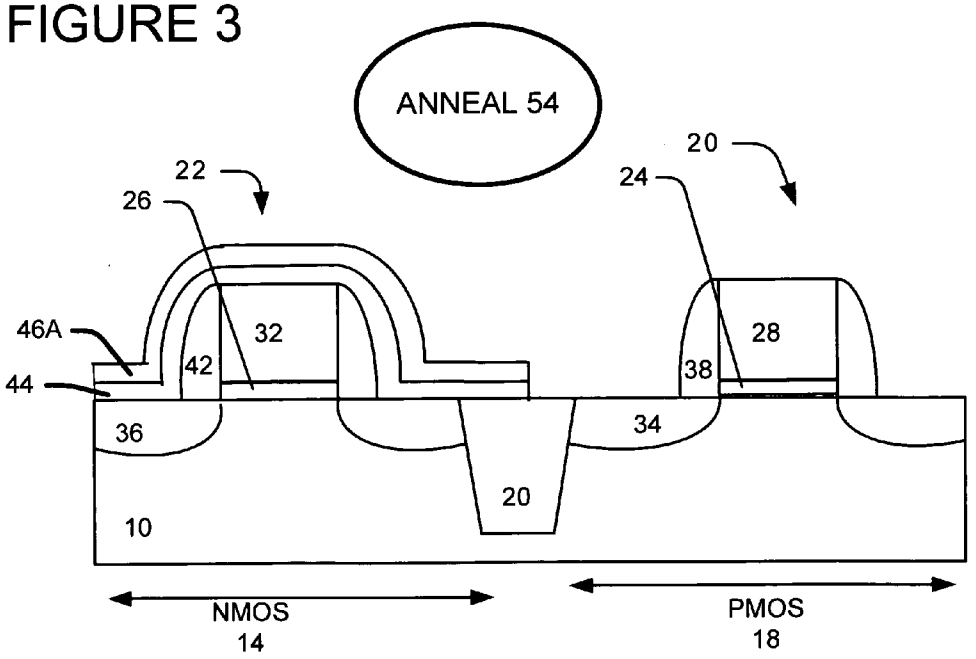


FIGURE 4

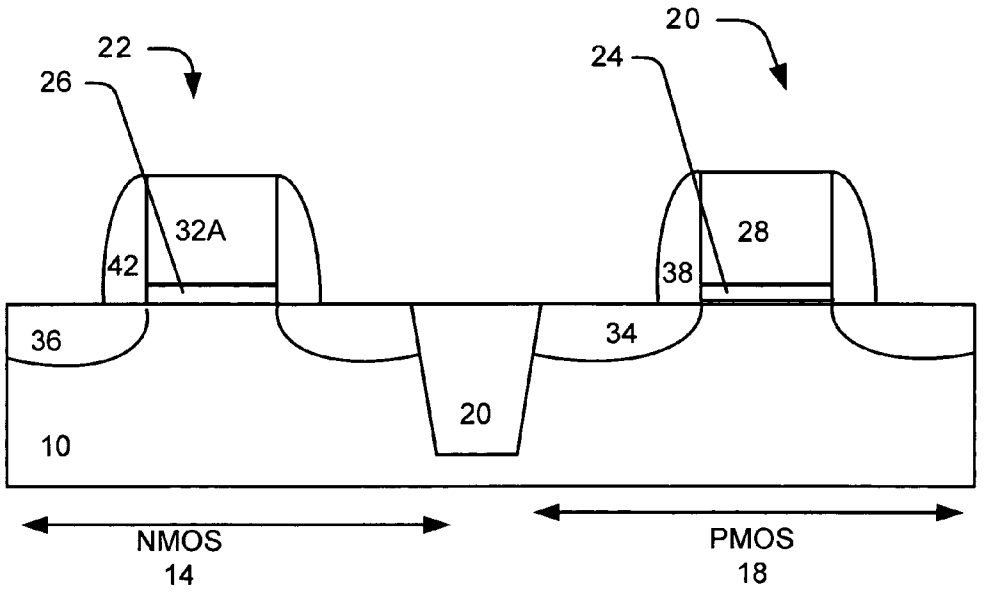


FIGURE 5A

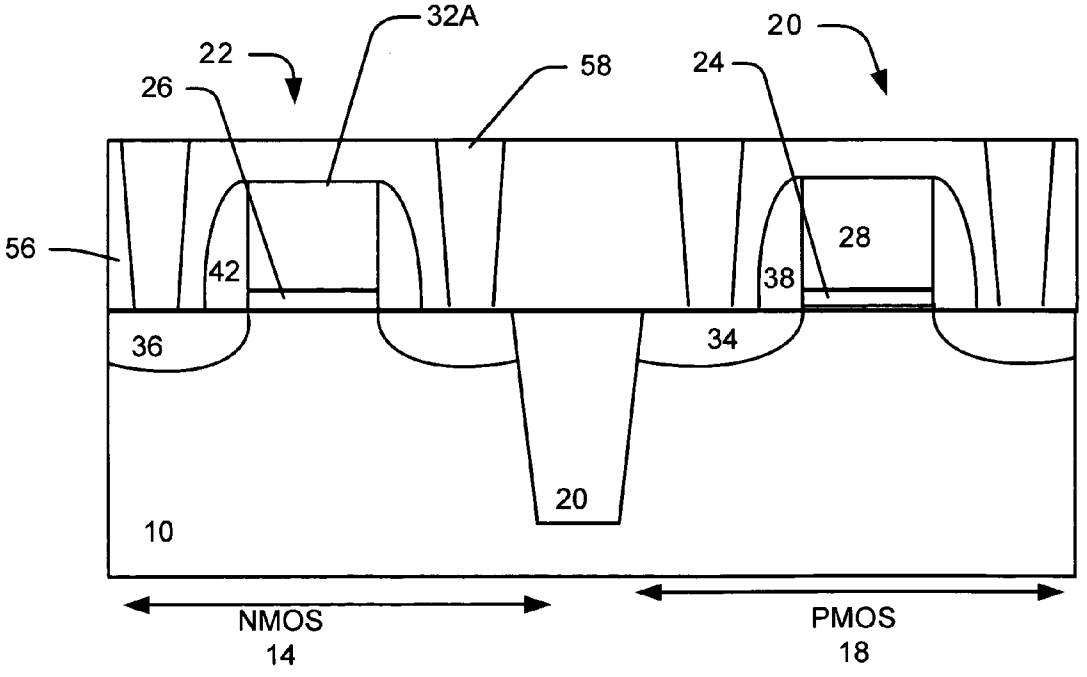


FIGURE 5B

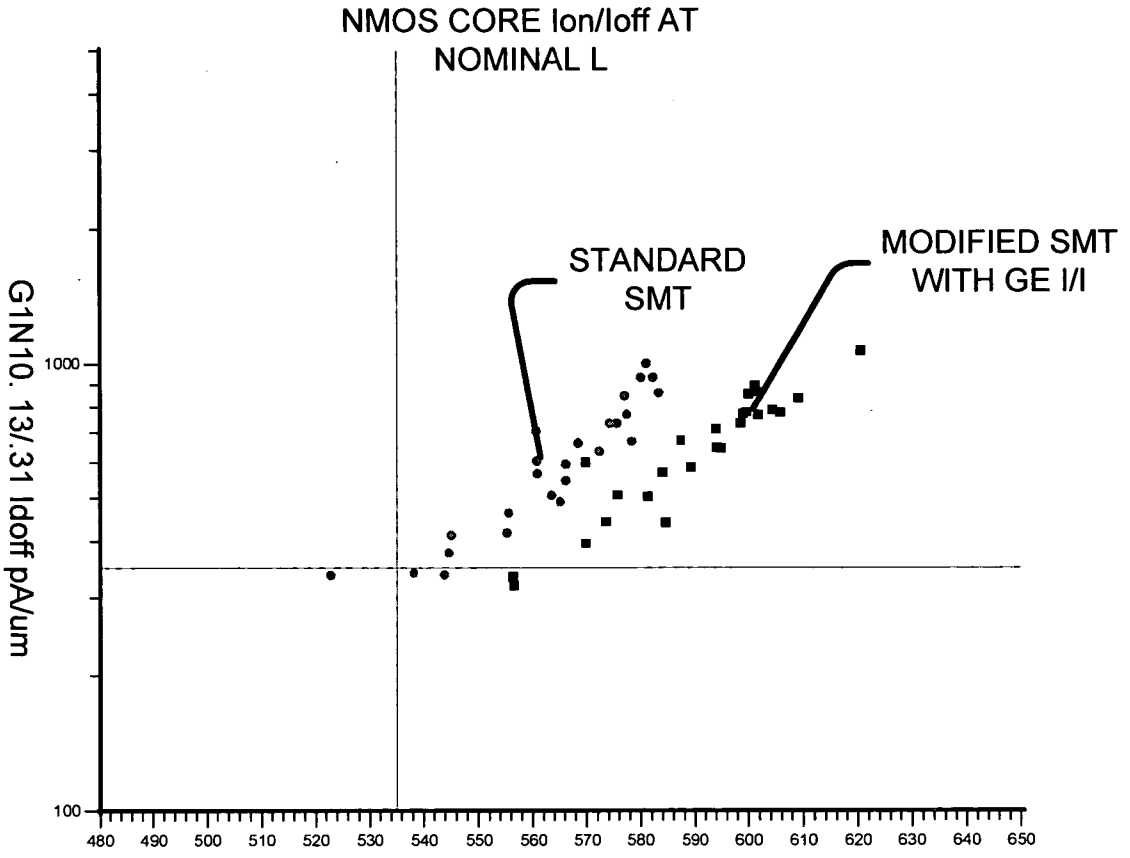

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FIGURE 6

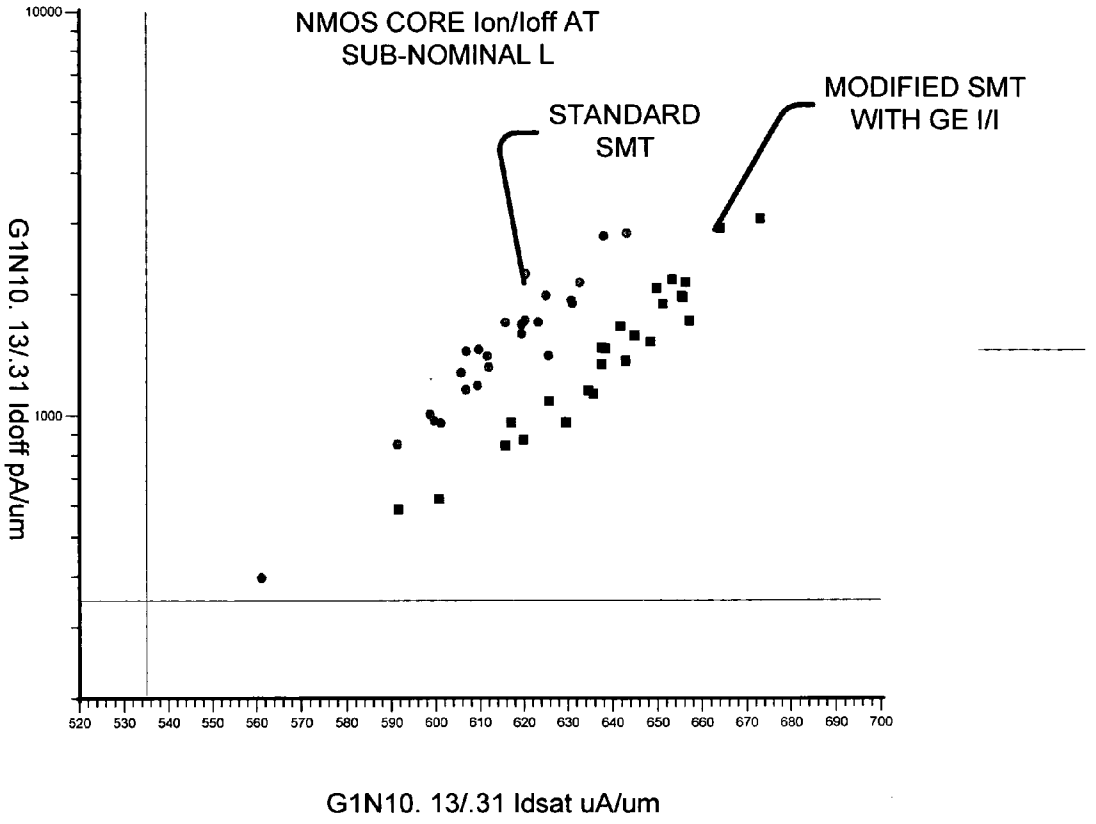
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FIGURE 7

MODULATION OF STRESS IN STRESS FILM THROUGH ION IMPLANTATION AND ITS APPLICATION IN STRESS MEMORIZATION TECHNIQUE

BACKGROUND OF INVENTION

[0001] 1) Field of the Invention

[0002] This invention relates generally to fabrication of semiconductor devices and more particularly to a method to change the stress in a stress layer over a FET device.

[0003] 2) Description of the Prior Art

[0004] Performance and economic factors of integrated circuit design and manufacture have caused the scale of elements (e.g. transistors, capacitors and the like) of integrated circuits to be drastically reduced in size and increased in proximity on a chip. That is, increased integration density and proximity of elements reduces the signal propagation path length and reduces signal propagation time and susceptibility to noise and increase of possible clock rates while the reduction in element size necessary for increased integration density increases to ratio of functionality which can be provided on a chip to the costs of production (e.g. wafer/chip area and process materials) per chip and, potentially, the cost of devices containing the chips by reducing the number of inter-chip and inter-board connections required.

[0005] It has also been shown theoretically and confirmed experimentally that mechanical stress in the channel region of an FET can increase or decrease carrier mobility significantly; depending on the sign of the stress (e.g. tensile or compressive) and the carrier type (e.g. electron or hole). Tensile stress increases electron mobility and decreases hole mobility while compressive stress increases hole mobility while decreasing electron mobility in the doped semiconductor crystal lattice forming the transistor channel. This phenomenon is well-recognized and theories concerning the physical effects by which it occurs are, in any event, unimportant to its exploitation. In this regard, numerous structures and materials have been proposed for inducing tensile or compressive force in a semiconductor material, such as shallow trench isolation (STI) structures, gate spacers, etch-stop layers and silicide which are generally included in integrated circuit designs.

[0006] The importance of overcoming the various deficiencies noted above is evidenced by the extensive technological development directed to the subject, as documented by the relevant patent and technical literature. The closest and apparently more relevant technical developments in the patent literature can be gleaned by considering the following.

[0007] C. H. Chen, T. L. Lee, T. H. Hou, C. L. Chen, C. C. Chen, J. W. Hsu, K. L. Cheng, Y. H. Chiu, H. J, Tao, Y. Jin, C. H. Diaz, S. C. Chen, and M.-S. Liang, "Stress Memorization Technique (SMT) by Selectively Strained-Nitride Capping for Sub-65 nm High-Performance Strained-Si Device Application", 2004 Symposium on VLSI Technology Digest of Technical Papers

[0008] U.S. Pat. No. 6,939,814 and US20050093078A1: Inventor: Chan, Victor;—Increasing carrier mobility in NFET and PFET transistors on a common wafer—Adjusting a carrier mobility for different semiconductor conductivities on the same chip by forming layer of material applying stress level on surface of chip, and selectively reducing the stress level of the portion of layer of material.

[0009] U.S. Pat. No. 6,573,172: Methods for improving carrier mobility of PMOS and NMOS devices—Fabrication of semiconductor device by forming P-channel and N-channel metal oxide semiconductor transistors in wafer, forming tensile film on P-channel transistor and forming compressive film on N-channel transistor—Inventor: En, William George

[0010] US20040075148A1: Semiconductor device—the transistors each comprise an insulated film wrapping a gate electrode and extending to a location adjacent to a source/drain area, and the insulated film is mainly composed of silicon nitride, and the thickness of the insulated film of the n-channel field effect transistor differs from the thickness of the insulated film of the p-channel field effect transistor. Inventor: Kumagai, Yukihiro; Tsuchiura,

[0011] US20050093081A1: OXIDATION METHOD FOR ALTERING A FILM STRUCTURE AND CMOS TRANSISTOR STRUCTURE FORMED THEREWITH—Relaxing a tensile or compressive stress present in a film contacting a base layer by oxidizing the film to reduce a magnitude of the stress by supplying atomic oxygen to surface of the film—Inventor: Belyansky, Michael P.; Bethel, C T, US20050158937A1: METHOD AND STRUCTURE FOR CONTROLLING STRESS IN A TRANSISTOR CHANNEL—Manufacture of semiconductor device including n-type and p-type transistors comprises adjusting shallow trench isolation oxide corresponding to n-type and/or p-type devices and forming strain layer over semiconductor substrate. Inventor: Yang, Haining S

SUMMARY OF THE INVENTION

[0012] The following presents a simplified summary in order to provide a basic understanding of some aspects of some of the example embodiments of the invention. This summary is not an extensive overview of the example embodiments. It is intended neither to identify key or critical elements of the example embodiments nor to delineate the scope of the invention.

[0013] Some of the example embodiments of the invention provide a method to improve the performance of MOS devices by increasing the stress in the channel region. An example embodiment for a NMOS transistor is to form a tensile stress layer over the NMOS transistor. A ion implant is performed into the stress layer and then an anneal is performed. This increases the amount of stress from the stress layer that the gate retains/memorizes.

[0014] A example embodiment method of fabricating a semiconductor device comprises the steps of:

[0015] providing a MOS transistor over substrate;

[0016] the MOS transistor comprised of a gate dielectric, a gate electrode, and source and drain regions in the substrate adjacent to the gate electrode;

[0017] forming a stress layer over the MOS transistor; the stress layer containing tensile stress;

[0018] implanting ions into the stress layer;

[0019] performing an anneal of the substrate and stress layer whereby the implant and anneal increase the stress on the channel region of the MOS transistor.

[0020] Another example embodiment is method of fabricating a semiconductor device comprises the steps of:

[0021] providing a NMOS transistor and a PMOS transistor over substrate;

[0022] the NMOS transistor comprised of a gate dielectric, a gate electrode, and source and drain regions in the substrate adjacent to the gate electrode;

[0023] forming an dielectric layer over the NMOS transistor and the substrate surface;

[0024] forming a stress layer over the MOS transistor; the stress layer containing tensile stress;

[0025] removing the dielectric layer and stress layer from over the PMOS transistor;

[0026] implanting ions into the stress layer;

[0027] performing an anneal of the stress layer and the gate electrode.

[0028] The above and below advantages and features are of representative embodiments only, and are not exhaustive and/or exclusive. They are presented only to assist in understanding the invention. It should be understood that they are not representative of all the inventions defined by the claims, to be considered limitations on the invention as defined by the claims, or limitations on equivalents to the claims. For instance, some of these advantages may be mutually contradictory, in that they cannot be simultaneously present in a single embodiment. Similarly, some advantages are applicable to one aspect of the invention, and inapplicable to others. Furthermore, certain aspects of the claimed invention have not been discussed herein. However, no inference should be drawn regarding those discussed herein relative to those not discussed herein other than for purposes of space and reducing repetition. Thus, this summary of features and advantages should not be considered dispositive in determining equivalence. Additional features and advantages of the invention will become apparent in the following description, from the drawings, and from the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029] The features and advantages of a semiconductor device according to the present invention and further details of a process of fabricating such a semiconductor device in accordance with the present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

[0030] FIGS. **1** through **5**A and **5**B are cross sectional views for illustrating a method for manufacturing a semiconductor device according to an example embodiment of the present invention.

[0031] FIGS. **6** and **7** shows Si Data for the example embodiment vs a method using only steps of: SiN stress layer and anneal (no Ge I/I).

DETAILED DESCRIPTION OF THE EXAMPLE EMBODIMENTS

I. Introduction

[0032] Some example embodiments of the invention provide a method to improve the performance of MOS devices by increasing the stress in the channel region. An example embodiment for a NMOS Transistor is to form a tensile stress layer (e.g., SiN) over a NMOS transistor.

[0033] A gate dielectric layer and poly gate are formed.

[0034] An ion implant is performed to amorphorize the gate so that the gate is comprised of amorphous Si.

[0035] A important Ion implantation (I/I) is performed on the (SiN) stress layer that will initially relax the stress film but when combined with a subsequent anneal, will increase the tensile stress in the stress film higher than the initial starting stress.

[0036] Then an anneal is performed that can serve two purposes: (i) increasing the tensile stress of the implanted stress film, (ii) crystallizes the silicon containing gate thus increasing the amount of stress from the stress layer that the gate retains/memorizes.

[0037] The Si containing gate retains/memorizes a higher tensile stress from the SiN layer and the gate transfers this stress to the NMOS Tx channel. The Si in NMOS channel is under increased tensile stress that increase the electron mobility that increase device performance.

[0038] Examples of two key steps in the modulation of the stress of the stress (e.g., nitride) film are as follows.

[0039] First, a high dose (0.5~5E15) and lower energy (15 keV) heavy ion is implanted into the stress film.

[0040] Second, a high temperature anneal (for example using the typical SD anneal) (e.g, between 850 and 1300 C) is needed to enhance/modulate the stress in the stress layer which can then be transferred to the gate.

[0041] An example of this heavy ion implantation to enhance the nitride stress film stress can be used in the modified SMT flow as show below.

[0042] The example embodiments of the present invention will be described in detail with reference to the accompanying drawings. The example embodiments provide a method of forming a FET using a stress layer and a heavy ion implant that increases stress layer stress.

[0043] A. Provide NMOS Tx and PMOS Tx

[0044] As shown in FIG. **1**, we provide a NMOS transistor **22** in a NMOS region **14** and a PMOS transistor **20** in a PMOS region **18** over substrate **10**.

[0045] The NMOS transistor **22** can be comprised of a gate dielectric **26**, a gate electrode **32**, and LDD (lightly doped source/drain or SDE) regions (not shown); source and drain region **36** in the substrate adjacent to the gate electrode; and sidewall spacers **42**.

[0046] The NMOS gate electrode **32** can be comprised of silicon, polysilicon or polySiGe or Ge; and is preferably comprised of polysilicon.

[0047] The PMOS transistor **20** can be comprised of a gate dielectric **24**, a gate electrode **28**, and LDD (lightly doped

source/drain or SDE) regions (not shown; source and drain regions **34** in the substrate adjacent to the gate electrode **28** and sidewall spacers **38**. The PMOS gate electrode **32** can be comprised of silicon, polysilicon or polySiGe or Ge.

[**0048**] B. Amorphous Gate

[**0049**] At least portions of the gate that will have the stress film and anneal process should be comprised of amorphous silicon prior to the formation of the stress film. This can be accomplished by an ion implant into the gate. For example, a separate gate amorphorizing implant can be performed to implant ions into the gate. Likewise, if a if a Source/Drain pre amorphization implant (PAI) is performed,

[**0050**] C. Form Dielectric Layer

[**0051**] Next referring to FIG. **2**, we form an optional dielectric layer **44** over the MOS transistor and the substrate surface.

[**0052**] The dielectric layer can be comprised of oxide layer **44** and is preferably comprised of oxide. The dielectric layer can have a thickness between 30 and 200 angstroms (tgt=100 angstroms). The dielectric layer can be comprised of a low temperature oxide layer (LTO).

[**0053**] The dielectric layer serves a reducing the defects when nitride layer is deposited on Si surface. It also serve as etch stop for nitride removal. It can be an optional layer if etch process is well tuned.

[**0054**] D. Form Stress Layer

[**0055**] Next, we form a (first) stress layer **46** over the dielectric layer **44**.

[**0056**] In this example, the stress layer has tensile stress. The tensile stress layer **44** puts a tensile stress on the underlying channel of the MOS Tx.

[**0057**] The stress layer **46** can be comprised of silicon oxy-nitride (SiON) or silicon nitride and can have a thickness between 300 and 1000 angstroms (tgt=400 angstroms).

[**0058**] At this time in the process, the stress layer **46** can have a tensile stress of between 0.3 GPa and 1.2 Gpa.

[**0059**] E. Ion Implant Ions Into the Stress Layer

[**0060**] As shown in FIG. **3**, in a key step, we implant ions using a high dose/low energy implant process into the stress film. The heavy ion (or large ions) ions **50** are implanted into the stress layer **46** and preferably not below the stress layer. Preferably the majority of ions stop in the stress layer **46** and more preferably substantially all the ions preferably stop in the stress layer.

[**0061**] The stress layer implant can use Ge or Xe ions or other large ions that have a molecular weight greater than or equal to 28 (e.g., Si and above Si in periodic table). For example, the ions can be comprised of: Ge, Ar, Xenon, indium, antimony, Si, N, O osr C.

[**0062**] The (e.g., Ge or Xe) ions can be implanted at a dose between 0.5E15 and 5E15 atoms/cc and preferably between 1E15 and 2 E15 atoms/cc; and at an energy between 5 and 50 KeV and preferably about 15 KeV. For example, the implant energy depends on nitride stress layer thickness, i.e., for a stress layer with a 300 Angstrom thickness, the ion implant energy will be about 15 keV.

[**0063**] Preferably, the stress film (e.g., SiN) can have a ion (e.g., Ge or Xe) concentration in the range from 1E20 to 1E22 atom/cm^{-3}.

[**0064**] This ion implant (Ge I/I) parameters are targeted so the ions are substantially contained within the SIN stress layer.

[**0065**] F. Remove the Stress Layer from the PMOS Region

[**0066**] Referring to FIG. **4**, we remove the stress layer **46** and dielectric layer **44** from the PMOS region **18**. The stress layer can be removed using a mask and pattern process. The Stress layer **46**A remains over the NMOS Tx **22**.

[**0067**] G. Perform an Anneal of the Substrate;

[**0068**] Referring to FIG. **4**, we perform an anneal **54** of the substrate.

[**0069**] The anneal can be performed at a temperature between 850 and 1300 C; for a time between 0.001 and 20 seconds. A typical anneal is performed at 950 degrees C. for about 5 seconds.

[**0070**] The purpose of the anneal is to "increase" the tensile stress of the stress layer as well as re-crystallize the poly or amorphous silicon gate.

[**0071**] The anneal can increase the tensile stress in the stress layer **46**A by between about 10 and 60%.

[**0072**] After the anneal, the SIN stress layer **46**A has a tensile stress between 1.4 and 2.0 GPa. This tensile is between about a 10 and 60% increase compared to the tensile (e.g., SiN) layer before the ion implant and anneal.

[**0073**] The anneal can be part of a S/D anneal. Also a special separate higher temperature and short duration anneal can also be inserted. For example a laser anneal can be performed.

[**0074**] An example of a S/D anneal that will adequately anneal the invention's ion implanted stress layer **46**A. The S/D anneal can be performed at a temperature between 600 and 1300 C and preferably between 850 and 1300 C and more preferably between 925 and 1300 C for a time between close to zero (spike or laser anneal) 0.1 seconds and 5 minutes. For example, a typical S/D anneal is at 950 C for 5 sec. A lower temperature than 950 C may cause large amount of transient enhance diffusion which is bad for current technologies.

[**0075**] In an other example, the anneal can be performed at a temperature between 850 and 1300 C; for a time between 0.01 seconds and 5 minutes.

[**0076**] The embodiment's steps of: (1) I/I into the SiN stress layer, and (2) anneal increases the tensile stress in the NMOS channel thereby improving NMOS performance.

[**0077**] The ion implant coupled with anneal increases the initial stress film stress. As a result the "memorized" stress transferred to the gate is more significant as compared to plainly using an initial tensile (e.g. SiN) stress film which has tensile stress to date that saturates at about 1.2 GPa.

[**0078**] There are two theories of the how the embodiment's ion implant and anneal increase the stress on the channel region. First the ions break the Si—N—H bonds in the stress layer and during the annealing process more H

escape causing the stress film to be more tensile. Second, the possibility of forming Ge—N bonds in the SiGe N system can increase the stress. (more generally X—N bonds where the implanted ion is X). For example, the Ge concentration can range from 1E20 to 1E22 cm^{-3} in a stress layer to increase the tensile stress.

[0079] H. Remove the Stress Layer

[0080] Referring to FIG. **5**A, we preferably remove the dielectric layer **44** and the stress layer **46**.

[0081] I. Subsequent Process Steps

[0082] Conventional processing is performed to complete the devices. An example sequence is salicide, ESL (any combination of tensile and compressive), IDL Deposition, contact etch, etc. . . . (i.e. standard process flow after S/D anneal). For example, FIG. **5**B shows an overlying dielectric layer **56** and contacts **58**.

[0083] It may be possible to form a tensile or compressive etch stop layer over the gate structures to further improve the channel stress.

[0084] For example, we could form a tensile CESL (contact etch stop layer) SiN over the NMOS transistor, then form ILD layer, and then form contact holes. The tensile ESL over the NMOS transistor might increase the tensile strain on the NMOS channel.

[0085] J. Review

[0086] The example embodiment aims to provide an approach to increase the overall stress of the stress film **46** and hence increasing the stress level that can be induced in the Si channel. In this example, the I/I **50** into the stress layer **46** and the subsequent anneal **54** increase the stress on the poly gate **32**A. after the stress layer **46** is removed, the poly gate **32**A retains ("Memorization") the stress from the stress layer **46** and puts a tensile stress on the channel region in the substrate.

[0087] A tensile stress layer is preferably deposited after S/D implantation. The gate and S/D regions are amorphorized either by the initial S/D implant or by additional Ge I/I during the S/D step. As such, after an annealing step, the gate and S/D region re-crystallized and memorized the stress by the tensile stress layer. The actual stress transfer mechanism is not well understood yet (i.e. it can either be from the gate or the S/D regions).

[0088] K. Examples

[0089] The following non-limiting examples represent preferred forms and best modes contemplated by the inventor for practice of his invention, as well as illustrating the results obtained through its use.

[0090] FIGS. **6** and **7** shows Si Data for the example embodiment vs a method using only steps of: SiN stress layer and anneal (no Ge I/I).

[0091] FIG. **6** shows nMOS Core Ion/Ioff at nominal L. FIG. **6**: Gate length: 110 nm, SiN stress layer thickness: 300 A, dielectric (oxide) thickness 100 A The S/D anneal was for 5 s at about 950 C.

[0092] FIG. **7** shows nMOS Ion/Ioff at sub-nominal L, FIG. **7**: Gate length: 100 nm, SiN thickness: 300 A, oxide thickness 100 A; g1n110 13/1 For FIG. **7**, the S/D anneal was for 5 s at about 950 C.

[0093] The embodiment of the invention achieved Ion/Ioff enhancement for nFET of ~4% and 5% is achieved for a gate length of 110 nm and 100 nm respectively. Since stress memorization technique (SMT) process is expected to have larger impact of smaller dimension devices, this makes the current technique more ideal for more advance technology nodes.

[0094] L. Non-Limiting Example Embodiments

[0095] Given the variety of embodiments of the present invention just described, the above description and illustrations show not be taken as limiting the scope of the present invention defined by the claims.

[0096] While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention. It is intended to cover various modifications and similar arrangements and procedures, and the scope of the appended claims therefore should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements and procedures.

What is claimed is:

1. A method of fabricating a semiconductor device comprising the steps of:

a) providing a MOS transistor over substrate;

(1) said MOS transistor comprised of a gate dielectric, a gate electrode, and source and drain regions in said substrate adjacent to said gate electrode;

b) forming a stress layer over said MOS transistor; said stress layer have a tensile stress;

c) implanting ions into the stress layer;

d) performing an anneal of said substrate and stress layer whereby the implant and anneal increase the stress on the channel region of the MOS transistor.

2. The method of claim 1 which further comprises removing the stress layer.

3. The method of claim 1 which further comprises; the MOS transistor is a NMOS transistor and the stress layer is a tensile stress layer.

4. The method of claim 1 wherein said stress layer is comprised of SiON or silicon nitride and has a thickness between 300 and 1000 angstroms;

(1) before the ion implantation and anneal steps, the stress layer has a tensile stress of between 0.3 and 1.2 Gpa.

5. The method of claim 1 wherein the ions are Ge or Xe ions and the ions implanted at an energy between 5 and 50; at a dose between 5E14 AND 5E15 ions/sq-cm; the ions are substantially implanted into the stress layer and do not significantly reach the gate electrode.

6. The method of claim 1 wherein the stress film has an ion concentration in the range from 1E20 to 1E22 $atom/cm^{-3}$.

7. The method of claim 1 wherein the ions have a molecular weight greater than or equal to 28 and the ions are implanted at an energy between 5 and 50; at a dose between 5E14 AND 5E15 ions/sq-cm.

8. The method of claim 1 wherein the anneal is performed at a temperature between 850 and 1300 C; for a time between 0.01 seconds and 5 minutes.

9. A method of fabricating a semiconductor device; comprising the steps of:

a) providing a NMOS transistor and a PMOS transistor over substrate;

(1) said NMOS transistor comprised of a gate dielectric, a gate electrode, and source and drain regions in said substrate adjacent to said gate electrode;

b) forming a stress layer over said MOS transistor; said stress layer containing tensile stress;

c) removing stress layer from over the PMOS transistor;

d) implanting ions into the stress layer;

e) performing an anneal of said stress layer and said gate electrode.

10. The method of claim 9 which further comprises removing the stress layer.

11. The method of claim 9 which further comprises forming an dielectric layer over said NMOS transistor and said substrate surface; and forming the stress layer over the dielectric layer.

12. The method of claim 9 which further comprises forming an dielectric layer over said NMOS transistor and said substrate surface; and forming the stress layer over the dielectric layer; said dielectric layer is comprised of oxide layer and has a thickness between 30 and 200 angstroms.

13. The method of claim 9 wherein said stress layer is comprised of SiON or silicon nitride and has a thickness between 300 and 1000 angstroms;

(1) before the anneal, the stress layer has a (tensile) stress of between 0.3 and 1.2 Gpa.

14. The method of claim 9 wherein the anneal is performed at a temperature between 850 and 1300 C; for a time between 0.01 seconds and 5 minutes.

15. The method of claim x wherein the stress layer has an ion concentration in the range from 1E20 to 1E22 atom/cm^{-3}.

16. The method of claim 9 wherein the ions have a molecular weight equal to or greater than 28,

17. The method of claim 9 wherein the ions are comprised of Ge or Xe and the Ge or Xe ions are implanted at an energy between 5 and 50; at a dose between 5E14 and 5E15 ions/sq-cm.

* * * * *