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[54] **DIGITAL DOWNCOUNT TIMER**

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[58] **Field of Search**..... 58/39.5, 50 R, 145 A; 235/92 PE, 92 T, 92 EA; 340/43, 309.4, 323

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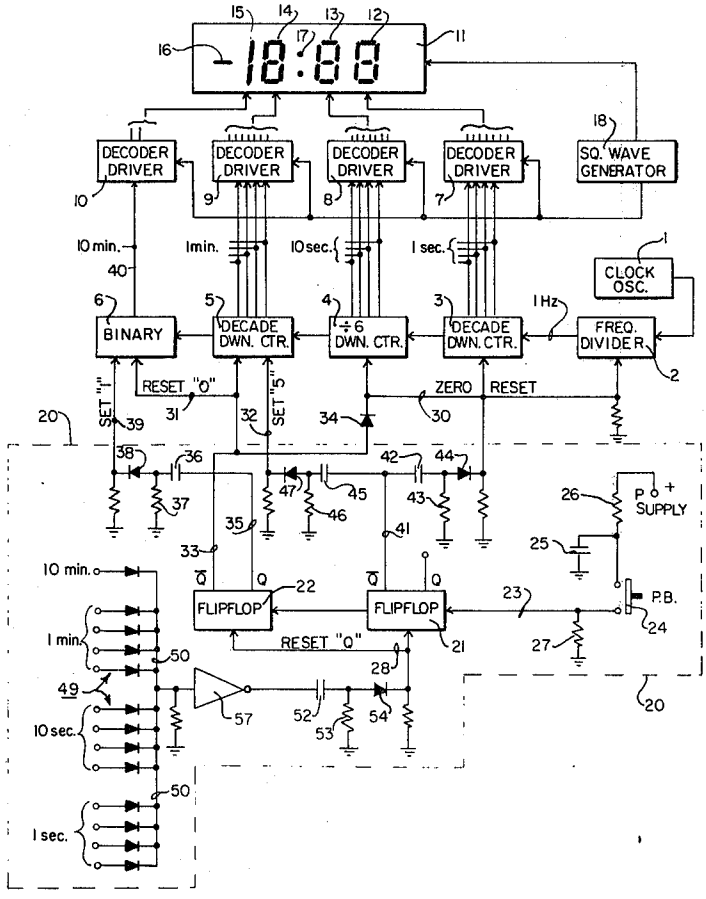
[57] **ABSTRACT**

A digital downcount timer for timing warning periods occuring before the "START" of an event, such as a sailboat race, where the warning period is commenced by a first warning signal such as a gun or flag and where there may be a second warning signal to mark a fixed intermediate instant in the warning period, the timer including a count-down clock and a programmed controller having a first step condition in which the clock shows all zeros at the display, and having a second-step condition manually initiated wherein the clock is preset to display an initial negative reading and is enabled to count down toward zero, one of these step conditions being a stable at "REST" condition, and the controller having a third step condition which can be optionally selected by manual action to correct the count to display a preset intermediate corrective negative reading from which the clock continues downcounting. When the display reads all zeros, the controller is automatically returned to the "REST" condition.

6 Claims, 2 Drawing Figures



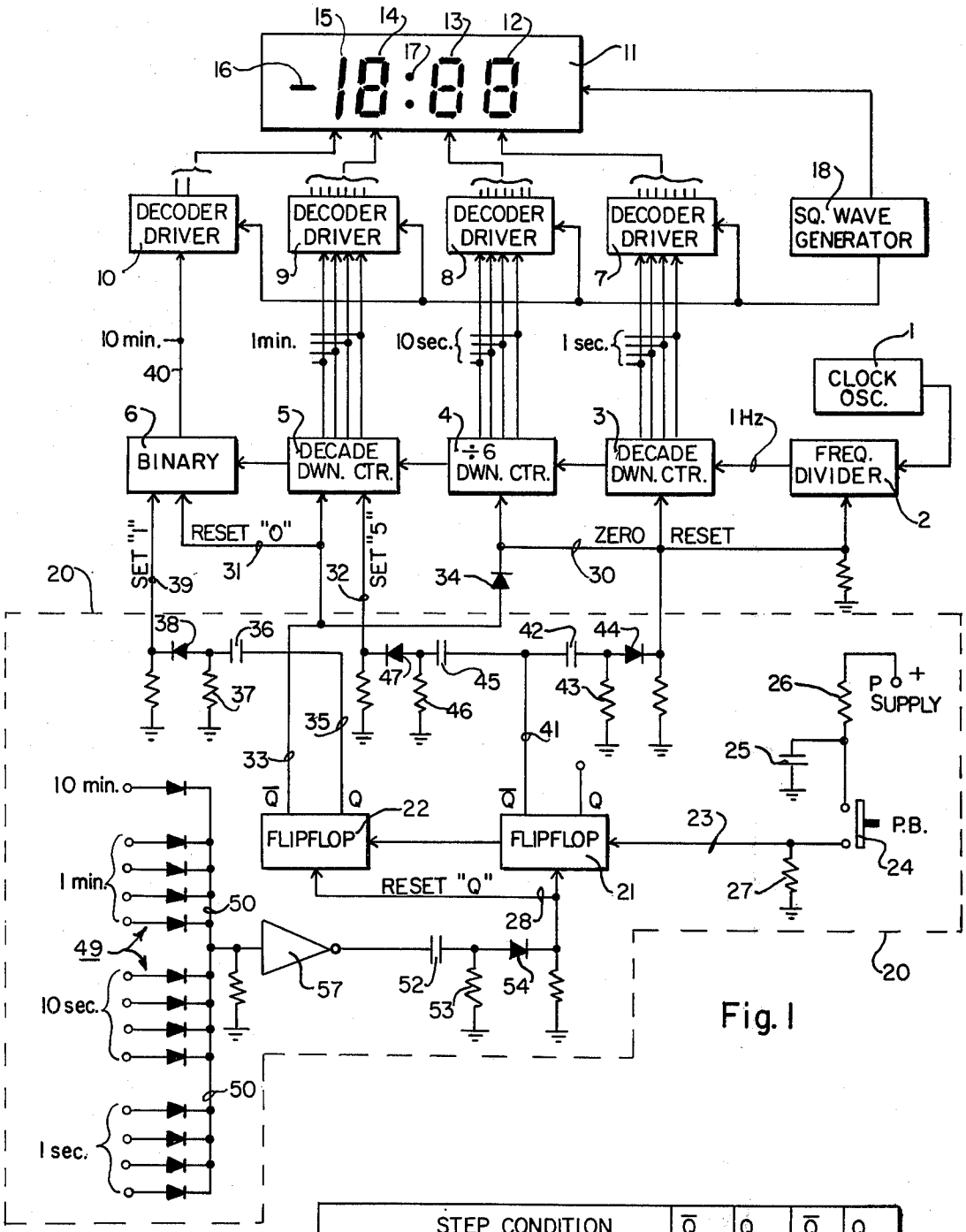


Fig. 1

STEP CONDITION	$\overline{Q}_{22}$	Q_{22}	$\overline{Q}_{21}$	Q_{21}
NUMBER 1 , REST	1	0	1	0
NUMBER 2 , RESET – 10:00	0	1	0	1
NUMBER 3 , SET – 5:00	0	1	1	0

Fig. 2

DIGITAL DOWNCOUNT TIMER

FIELD OF INVENTION

This invention relates to special purpose digital clock timers, and more particularly, relates to timers which can be actuated to commence counting down from a preset clock reading initiated at a first signalled moment, such as the first warning gun before a race, through a second signalled moment, such as the second warning gun, to eventually read "zero" at the "START" gun of the race.

BACKGROUND

There are a number of events, particularly including racing events such as sailing vessel races, in which the actual races are started after a pre-race warning period where the period is marked by signals such as warning guns and/or flags. For example, before the "START" of a sailing race, there is a 10-minute warning signal usually including a gun and a flag marking the beginning of the warning period, and this is followed by a similar 5-minute signal halfway through the period. The next signal is, of course, the START gun and/or flag starting the race. During this initial pre-race period, the skipper and crew aboard each competing boat are intensely occupied with their strategy and efforts to achieve a favorable starting position, such that their vessel will be able to cross the START line as near to the firing of the START gun as possible, but not before it. To accomplish an optimum start, it is necessary for the skipper of the vessel to have accurate and continuous knowledge of the exact interval of time remaining in the 10-minute warning period preceeding the start of the race. This is a crucial and very demanding period of time during which the skipper must keep track simultaneously of the maneuvers and positions of the other vessels, of his own strategy, and of the rate at which the pre-race period is running out.

PRIOR ART

Prior art racing timers generally comprise mechanical stop watches with specially marked dials, some of which have faces which are calibrated to show pre-race warning periods to make the timing of this period more convenient. Generally, one pushes a button on the watch to commence the timing of the warning period in a manner well known per se. There are also a number of digital clock circuits useful for general time keeping purposes, some of which also include settable timing features, such as the digital stop watch of general utility shown in U.S. Pat. No. 3,686,880, or the digital downcounter of general utility shown in U.S. Pat. No. 3,128,373. Most electronic digital clocks include some means for setting them to a particular time reading, for example, see U.S. Pat. No. 3,762,152.

THE INVENTION

This invention is a digital downcount timer clock circuit in combination with a controller circuit operative to step through a predetermined program, starting with a stable REST condition from which it is manually started counting commencing at an initially preset condition in which it contains and displays a minus reading which in the sailing race application would be "−10:00" minutes. This step condition of the controller also enables the clock to begin counting down toward "0:00". The clock continues such counting and will automatically count through a "−5:00" minute reading and eventually reach "0:00" in the absence of further manual intervention. However, another manual actuation will force the clock into an intermediate step condition to enter a reading of "−5:00" into the counters and display. Thus, at the time of the 5-minute warning signal the skipper can force an intermediate correction into the clock if its reading is erroneous at this instant. Such an error is very likely to occur under racing conditions because of error in actuation of the clock at the instant of the 10-minute warning signal. It is well known that there is a delay in the travel of the sound of the gun over the water, and therefore, if the skipper does not visually observe the puff of smoke from the gun or the raising of a flag, he must start the downcounter clock in response to his hearing the tardy sound of the gun's report. At the time of the subsequent 5-minute gun, he may be located closer to the gun, or he may concentrate his attention to see the puff of smoke or the raising of the flag, and therefore, he is able to correct the clock to a closer reading at this intermediate moment by a further manual actuation. From the point of view of the racing skipper, there is an important difference between the FIRST and the SECOND warning guns. He knows when to expect the SECOND gun and can watch for it, but he has no way of knowing when to expect the FIRST gun and therefore its firing will come at a moment which he cannot anticipate. The clock then continues counting down until it reaches 0:00, in response to which it automatically sets the controller to its REST condition and becomes dormant.

It is the principal object of the invention to provide a special purpose digital clock timer of a type which is particularly adapted to downcount the period of time between pre-race warning signals and the start of the event, where the warning signals occur at fixed time intervals before the start signal.

It is a more specific object of this invention to provide a downcounter having a digital display indicating the time remaining after one or more warning signals until the start of an event, which event is commenced by a START signal. It is especially an object of this invention to provide a programmed digital timer in which the first warning signal is used to initiate manual preset of the timer with an indication of the full period between the first warning signal and the start of the event, and to provide such a timer in which the reading of the timer can be further corrected to improve its accuracy during the downcount period at the intermediate time of occurrence of a second warning signal which comes at a known instant in the warning period and can be used to mark a second actuation of the manual device, thereby correcting the count to read the proper amount at the time of the second warning signal.

It is another important object of the invention to provide a digital display and downcounter as set forth above including a manual actuator for starting the downcount from a preset value and for correcting the count, wherein the manual actuator can be located remotely from the display and connected therewith by suitable wiring.

Still another object of the invention is to provide a digital downcount timer as set forth above having an electronic visual display of a type which is readable in high ambient light, even direct sunlight.

It is a further object of the invention to provide a digital downcount timer having the above features, and

using MOS circuitry which is extremely economical of electrical energy, so that the counter can be used for at least one season without having to change batteries, which are preferably of the type used in small transistor radios.

Other objects and advantages of the invention will become apparent during the following discussion of the drawings, wherein:

FIG. 1 is a schematic diagram showing a timer and controller circuit according to the present invention; and

FIG. 2 is a truth table showing the outputs of two controller flipflops which occur during the three programmed steps of the controller.

Referring now to the drawing, the downcount timer clock circuit selected for illustrating the present invention has been set up particularly for sailboat racing so that, when it is manually actuated from rest condition, it is preset initially to show −10:00 minutes and then to count down toward zero, optionally through an intermediate actuation at the −5:00 minute count. However, in the absence of such second actuation, it will count all the way through to 0:00 at which time the controller will stop the counting and leave the clock dormant unless and until a new first actuation of the controller starts it on a new downcount cycle commencing at −10:00 minutes. In sailboat racing, before the official start of the race the officials provide a 10 minute warning signal which is generally made by hoisting a flag and firing a 10 minute warning gun. Moreover, at 5 minutes before the start of the race, another flag is hoisted and a 5 minute warning gun is fired, and finally at the start of the race a START signal is provided comprising a third flag and a starting gun. The drawing shows an illustrative embodiment of a downcount timer specifically programmed for this type of operation.

The timer shown in FIG. 1 includes a clock circuit which is driven by a crystal oscillator **1** of any conventional design which delivers an output frequency suitable for being divided down to drive a series of clock counters. For example, in the present illustration the crystal oscillator **1** has an output frequency of 131,072 Hz and this oscillator drives a frequency divider **2** comprising 17 binary stages having an over-all division ratio of 131,072 so that the output frequency is 1 Hz. The present illustration can of course be replaced with any suitable circuit for providing a 1 Hz input to the first decade downcounter **3** which counts seconds. It is not necessary that the oscillator **1** be crystal controlled, although this is an inexpensive and easy way to provide the degree of stability required to provide accurate timing.

At the present state of the art, the C MOS series of integrated circuits available from a number of manufacturers offers the best choice from the standpoint of compatability and low power consumption. Therefore, such MOS circuitry is used throughout the present counter.

The decade downcounter **3** counts down by decreasing its digital BCD output at the rate of 1 count per second in the sequence 0,9,8,7,6,5,4,3,2,1,0, 9,... At the transition from 0 to 9, a carry pulse is fed from the downcounter **3** to a divide-by-6 downcounter **4** and this latter counter provides the 10 second count by counting 0, 5, 4, 3, 2, 1, 0, 5, 4, ... Here again, at the transition from 0 to 5 a carry pulse is fed from the divide-by-6 downcounter **4** to the count input of the decade downcounter **5** which is similar to the counter **3**, but counts minutes, this counter counting 0, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0, 9, 8, ... The downcounter **5** at the transition from 0 to 9 delivers a carry pulse to a binary flipflop **6** which is used to turn "off" and "on" the tens digit in the display, since the most significant digit of the display never exceeds 1. This is true for the present illustrative embodiment being discussed, but there is obviously no reason why the binary flipflop **6** could not be replaced, for instance, by a divide-by-6 downcounter which would then provide 60 minutes maximum in the display rather than only about 19 minutes as is possible in the present disclosure using a 3½ digit display. In the present circuit the most significant digit either displays a "1" or it displays nothing at all. A single binary flipflop **6** is accordingly adequate to provide this display, and therefore, the output of the decade downcounter **5** which consists of a carry pulse need only reset the flipflop **6** in order to remove the "1" display from the most significant digit position. Thus, the clock circuit described so far is adequate to count down from minus 10 minutes to 0 at one second intervals.

The outputs of the counters **3, 4,** and **5,** and of the flipflop **6** are respectively connected to appropriate decoder drivers **7, 8, 9,** and **10,** and the outputs of these drivers are connected in a manner well known per se to the 3½ digit display **11** which includes 7-segment displays **12** for seconds, **13** for tens of seconds, **14** for minutes, and **15** for tens of minutes, as well as a minus sign **16** and a colon **17,** the latter two of which can be painted on the display if desired since they do not require variation during operation of the timer.

While any suitable means of display can be employed, a liquid crystal display is the most desirable since it not only uses the smallest amount of power, but it can also be read at high ambient light levels, such as in direct sunlight. Present-day liquid crystal displays require a driving voltage from a generator **18** to provide an output frequency roughly between 30 and 200 Hz in order to provide optimum display. Opposite polarity output signals from the square wave generator **18** are delivered to the decoder drivers on the one hand and to the common terminal of the liquid crystal display **11** on the other hand so that there is provided a potential difference across those segments of the display which are being driven by the decoders.

Turning now to a discussion of the controller circuit, the digital clock described thus far is not simply permitted to count continuously, but is instead controlled in a manner to make it useful for the task at hand, which in the illustrative case is sailboat race starting. The program stepping of the digital timer is initiated by a manual device such as a switch **24,** which can be located either at the counter and display unit, or else remotely therefrom and attached to it by a wire. The timer is programmed in the present illustrative embodiment to stop when it reaches the count of 0:00 and remain in this condition which comprises a "rest" condition. However, it is to be understood that a rest condition at the count of −10:00 could just as well have been selected. From the above rest condition, the first closing of the manual actuator switch **24** forces an initial count of −10:00 into the counter chain including the integrated circuits **3, 4, 5,** and **6,** and this first manipulation of the actuator switch also starts the counter counting down from −10:00 toward 0:00. If no further manipulation is

made of the actuator switch **24**, the counter will count through −5:00 and keep going to zero where it will stop in the rest condition. However, if at the second warning gun the skipper observes that the timer is not at the count of −5:00, then he can manually depress the actuator switch **24** a second time, and this will force an intermediate count of −5:00 into the counters **3, 4, 5,** and **6** and this count will be displayed while at the same time the clock will continue downcounting toward the final count of 0:00 where it automatically stops counting. The second actuation of the manual switch **24** is optional, but not necessary to cause the counter to continue to zero.

The counters **3, 4, 5,** and **6** all have function inputs by which they can be reset or preset, and these inputs are connected to certain control lines coming from a Program Controller circuit which is shown enclosed within a dashed box and broadly designated by the reference character **20** in FIG. **1.** The controller **20** comprises a pair of flipflops **21** and **22** which are interconnected in such a way as to cause them to step through three conductivity conditions comprising the program steps. These steps can be seen in the truth table of FIG. **2** in which the first step comprises a rest position in which both flipflops are reset in such a way that their Q terminals are low and their $\overline{Q}$ terminals are high. Starting with this first position, an input signal on the wire **23** from the manual actuator switch **24** will deliver a high pulse from the power supply terminal P through the resistor **26** filtered by the capacitor **25,** and this input pulse will be delivered on the wire **23** across the resistor **27** to step the flipflop **21** to achieve the second step condition in which the Q terminal in flipflop **21** goes high and the $\overline{Q}$ terminal goes low. When the Q terminal in flipflop **21** goes high, the flipflop **21** also reverses the flipflop **22** so as to make the Q terminal in flipflop **22** go high and the $\overline{Q}$ terminal go low. Thus, when the switch **24** is actuated to step the controller **20** into the second step condition as shown in the truth table, both flipflops **21** and **22** reverse. Subsequently, when the same switch **24** is again actuated, the flipflop **21** is again reversed to make its $\overline{Q}$ terminal high, but the flipflop **22** is not again reversed, leaving its $\overline{Q}$ terminal low. The first step condition is again achieved to make all counter displays read zero by the application of a reset pulse on the wire **28** to reset both flipflops again to step **1** as shown in the truth table and in a manner to be presently described.

Referring again to FIG. **1,** the counter chain consisting of the downcounters **3, 4,** and **5,** and the flipflop **6** have certain functional inputs including the reset line **30** and the reset line **31.** In the case of the C MOS integrated circuits supplied with positive supply voltage, positive signals on the control lines **30** and **31** reset the counters and the flipflop **6** to read all zeros, and as long as the positive control signal remains on the lines **30** and **31** the counters **3, 4** and **5** continuously read zero. There is an additional input to the decade counter **5** which can be actuated via wire **32,** and when an input appears as a high signal on wire **32** the decade counter **5** is forced to a count of "5". The manner in which this controller operates is as follows:

The two program flipflops **21** and **22** are assumed initially to be in step condition number **1** which is the "rest" position in which the $\overline{Q}$ terminals of both flipflops are high and the Q terminals of both flipflops are low, as shown in the truth table of FIG. **2.** As mentioned above, step condition No. 1 of flipflops **21** and **22** is achieved by a high signal appearing on reset wire **28** as will be presently discussed. This reset signal appears whenever the display reads zero in all digit positions.

In step condition number **1** of the controller **20** the outputs on the $\overline{Q}$ terminals of both flipflops **21** and **22** are high. The high output appearing on the wire **33** from the $\overline{Q}$ terminal of the flipflop **22** provides a reset signal directly to the reset wire **31** of the counter **5** and the flipflop **6,** and the signal from wire **33** also passes through the diode **34** onto the reset wire **30** to reset the frequency divider chain **2** as well as the decade downcounter **3** and the divide-by-6 downcounter **4** to read zero. As long as the flipflops **21** and **22** remain in step condition number **1** according to the truth table of FIG. **2,** all of the counters **2, 3, 4, 5,** and the flipflop **6** are held in the reset position, and this is the stable rest condition of the timer to which it always returns when the reading is 0:00 at the digital display **11.** When the skipper wishes to place the clock in operation, he presses the switch **24** manually, and thereby reverses the flipflop **21** to provide a high output on its Q terminal, and this output reverses the flipflop **22,** placing a high output also on its Q terminal, both of the $\overline{Q}$ terminals having been changed to low condition. Therefore, the dividers and counters **2, 3, 4,** and **5** are no longer held reset and prevented from counting. However, the output on the Q terminal of the flipflop **22** in step position **2** places a high signal on the wire **35,** and this high signal is differentiated by the capacitor **36** and the resistor **37** to provide a brief output pulse through the diode **38** which pulse is applied to the set "1" terminal via wire **39** to set the binary flipflop **6** so that it delivers an output on the wire **40** to drive the decoder driver **10** to display the number "1" in digit position **15.** At the beginning of step condition number **2** the most significant digit **15** reads "1", and the other three digit positions **14, 13,** and **12** all read zero, whereby the clock has now been forced to contain and display an initial reading of −10:00 at the beginning of step condition number **2** as shown in the truth table.

However, the oscillator **1** immediately starts downcounting the counter chain **3, 4** and **5** through the frequency divider **2.** For instance the first one-second pulse from the counter chain **2** enters into the decade counter **3** and steps the counter downwardly to read −9:59. The next pulse of course counts it down another second so that it reads −9:58, etc. This downward counting continues in step condition No. 2 until one of two things happens. Either the skipper presses the switch **24** again to force an intermediate reading of −5:00 as will now be described, or else the counter continues until it reaches 0:00, at which time it is automatically returned to step condition number **1** in the truth table. Assuming that at the intermediate time when the second warning gun is fired the counter reads something different from −5:00, the racing skipper will then press the switch **24** to again reverse the flipflop **21** to provide a high signal on its $\overline{Q}$ terminal, while at the same time failing to reverse the flipflop **22.** This transition from step condition number **2** to step condition number **3** in the truth table makes the $\overline{Q}$ output of flipflop **21** on wire **41** go high, and the leading edge of the high output comprises a pulse which passes through the capacitor **42** and is differentiated thereby and by the resistor **43** to provide a narrow instantaneous pulse,

which pulse passes through the diode **44** and actuates the reset line **30** to reset the divider **2** and the counters **3** and **4** to zero. The high output on the wire **41** also passes through another differentiating circuit including the capacitor **45** and the resistor **46** which provides a brief narrow pulse which in turn passes through the diode **47** and actuates the terminal **32** of the decade downcounter **5** to make its count read "5". It is to be noted that the flipflop **6** has already been reset to the condition where the "1" appearing in digit position **15** is gone, and therefore, no change is necessary in order to have the entire display **11** read −5:00. The change in the controller to step condition number **3** does not stop the countdown, it merely forces the momentary reading to read −5:00 and therefore the countdown continues from that reading until it reaches all zeros in the display **11.**

The diode gating means **49** includes **13** diodes connected to all of the inputs to the decoder drivers **7, 8,** 9 and **10,** arranged such that when all of these inputs simultaneously read zero, the output level on wire **50** goes to zero, and this condition is inverted in the inverter **57** so that a high pulse appears at the output of the inverter **51** and passes through a differentiator comprising the capacitor **52** and the resistor **53.** The differentiator pulse appears briefly and passes through the diode **54** into the reset line **28,** and thereby resets both flipflops **21** and **22** in the controller to step condition number **1,** as shown in the truth table, in which step condition the output display reads 0:00 and all counters are held reset in zero condition until the next time someone closes the switch **24** and moves it to step condition number **2** as set forth above. The flipflops **21** and **22** are D-type flipflops having built-in steering pulse delays to prevent the flipflops from being reversed even in the presence of some contact bounce of the switch **24.**

In operation, the counter clock, when turned on, counts down to the 0:00 condition which then resets the flipflops **21** and **22** to the number **1** step condition at which the clock remains dormant. In operation, when the skipper hears the first warning gun 10 minutes before the start gun, he presses the switch **24** and thus changes the controller flipflops **21** and **22** to the second step condition which forces an initial −10:00 reading and allows the clock to begin counting down. When the skipper observes the 5 minute warning gun, if the counter reads −5:00 he does nothing and the counter continues to count toward zero in all digits. If the clock reads something different from −5:00 the skipper presses the switch **24** causing the controller to go into step condition number **3,** and thereby force a −5:00 reading into the counters and display, and the clock then continues automatically counting downwardly to 0:00. When the zero condition is reached in all digits, the diode gating means **49** then causes the flipflops **21** and **22** in the controller to be reset to step condition number **1,** which is a stable rest condition maintained by the system until the next time the switch **24** is manually pressed.

The optional actuation of the switch **24** to achieve the third step condition which forces the clock momentarily to −5:00 has the important advantage of providing a second opportunity to get the proper time displayed in the event that the skipper badly misjudged the 10 minute warning signal.

The present invention is not to be limited to the exact embodiment or use described in connection with the drawing, for obviously changes may be made within the scope of the following claims:

We claim:

1. A digital countdown timer for timing warning periods occurring before the START of an event where the warning period is marked by an initial warning signal commencing an interval of fixed duration preceeding said START, the timer comprising:

a. digital clock means including a chain of downcounters driving digital display means and driven by a clock pulse source;

b. a programmed controller operative to control the downcounters according to a cyclic program of multiple steps, the controller having manual actuator means for stepping it through said steps and the steps including a first step in which said downcounters all read zero count, and a second step with the downcounters all preset to read an initial count from which they are counted toward zero by said pulse source; and,

c. sensing means coupled to said downcounters and operative to sense a reading of the count in the downcounters corresponding with one of said steps, and said sensing means being responsive to the sensed count to stop said controller in a rest condition.

2. The digital timer as set forth in claim **1,** wherein said warning period is further marked by a second warning signal marking an intermediate time in the warning period occurring at a lesser interval before said START, and said controller including a third step selected by actuation of said manual means and operative to force a second preset count into said downcounters from which they continue counting toward zero.

3. The digital timer as set forth in claim **2,** wherein said controller is programmed and coupled to said downcounters to preset an initial count thereinto of minus 10 minutes during said second step, and is further programmed and coupled to said downcounters to force an intermediate preset count thereinto of minus 5 minutes during said third step.

4. The digital timer as set forth in claim **1,** wherein said controller comprises two flipflops having stable states corresponding with said steps, said second step being selectible only by actuation of said manual means, and the controller being returnable to said first step and stopped at rest in response to said sensing means detecting zero count or in response to another actuation of said manual means.

5. The digital timer as set forth in claim **1,** wherein said warning period is further marked by a second warning signal marking an intermediate time in the warning period occurring at a lesser interval before said START, and said controller including a third step selected by actuation of said manual means and operative to force a second preset count into said downcounters from which they continue counting toward zero, and said controller further comprising two flipflops having three stable states corresponding with said steps, said second and third steps being selectible only by separate actuations of said manual means, and the controller being returnable to and stopped at rest by said sensing means detecting zero count or by another actuation of said manual means.

6. The digital timer as set forth in claim 1, wherein said downcounters have multiple binary outputs connected to drive said display means, and said sensing means comprising gating means coupled to said binary outputs to detect a zero count and operative to deliver a signal to reset said controller to said first step when all of said binary outputs comprise binary zeros.

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