United States Patent

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[54] DECODER CIRCUIT EMPLOYING SWITCHES SUCH AS FIELD-EFFECT DEVICES

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[51] **Int. Cl.** **H03k 17/00**

[58] **Field of Search** 307/205, 241, 251, 269, 279, 307/304

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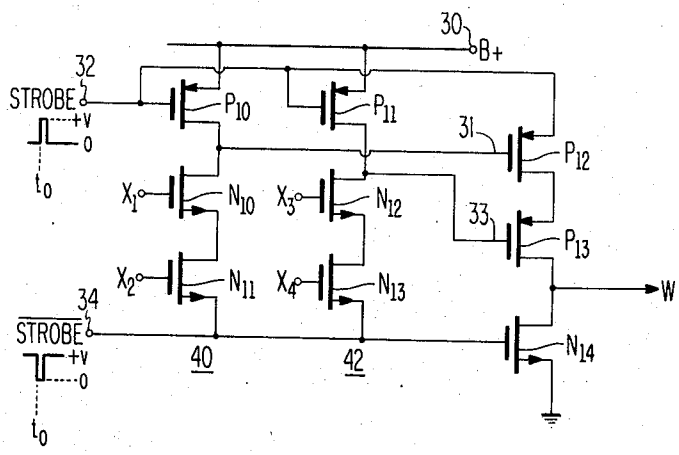
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[57] **ABSTRACT**

A decoder employing switches such as metal oxide semiconductor (MOS) field-effect devices interconnected in quasi-complementary fashion in a number of different transmission paths. In the absence of strobe and $\overline{\text{strobe}}$ signals, one device in one transmission path connects the circuit output terminal to ground. In the presence of strobe and $\overline{\text{strobe}}$ signals, the output terminal is disconnected from ground and, if the control voltages applied to certain of the devices in certain of the transmission paths all represent the desired binary value, the strobe signal is conducted via certain of the devices in said one transmission path to said output terminal.

10 Claims, 3 Drawing Figures



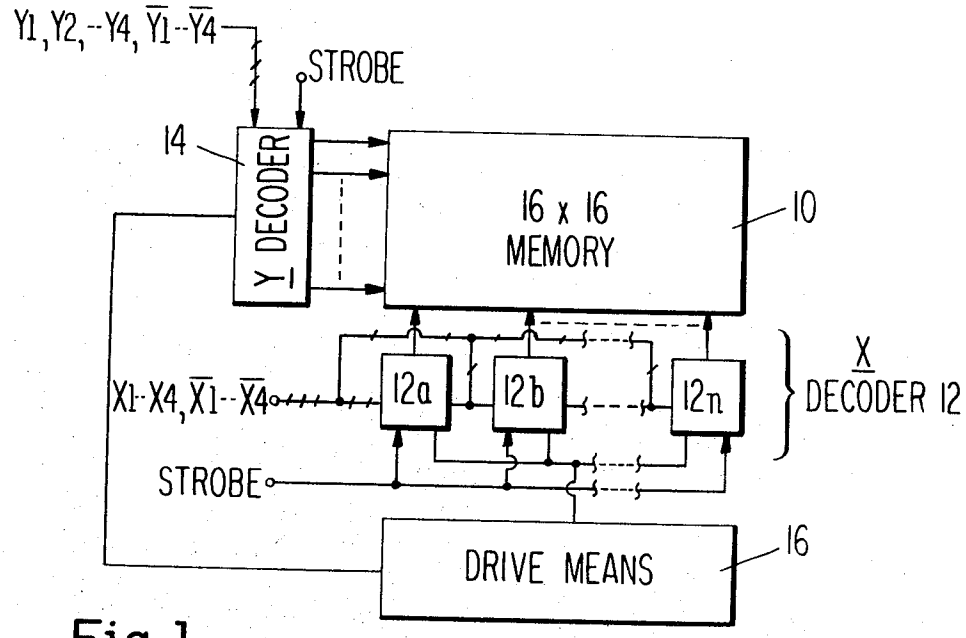
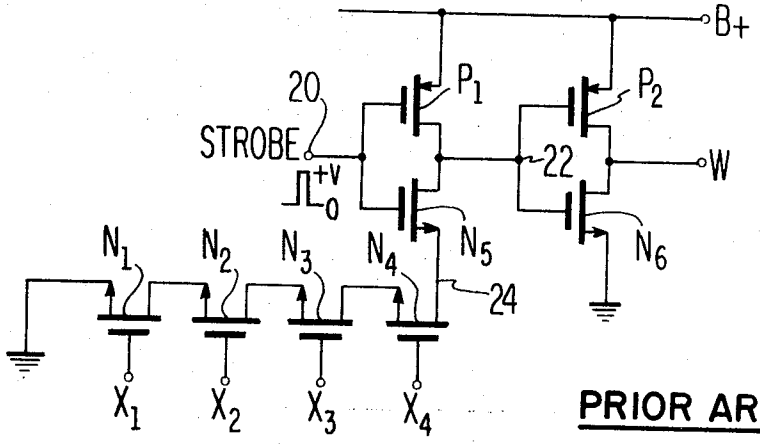


Fig. 1.



PRIOR ART

Fig. 2.

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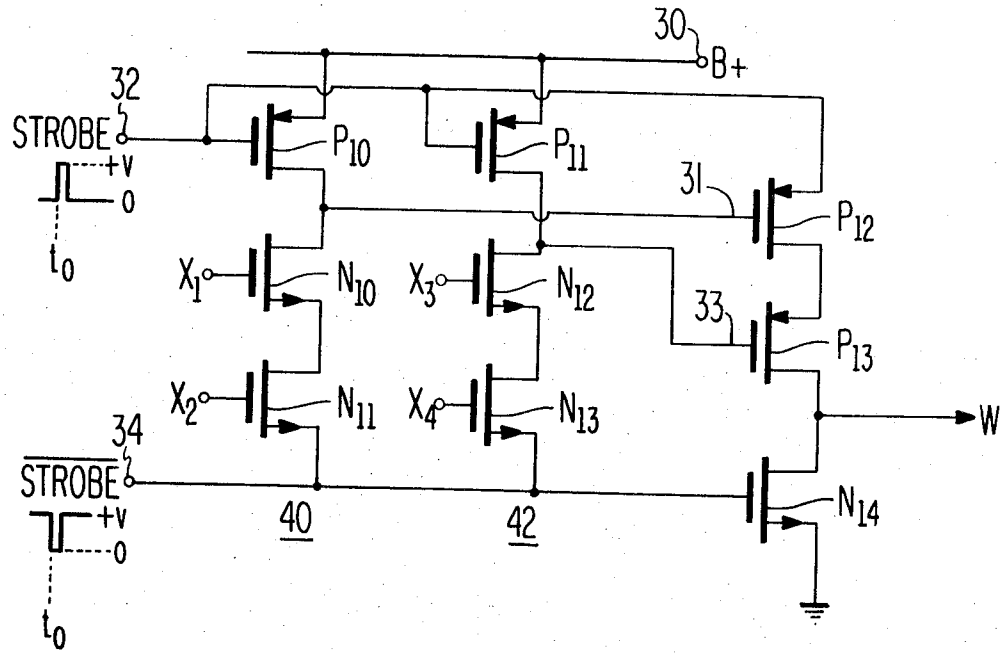


Fig. 3.

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DECODER CIRCUIT EMPLOYING SWITCHES SUCH AS FIELD-EFFECT DEVICES

STATEMENT

The invention described herein was made in the performance of work under a NASA contract and is subject to the provisions of Section 305 of the National Aeronautics and Space Act of 1958, **Public Law** 85-568 (72 Stat. 435; 42 U.S.C. 2457).

SUMMARY OF THE INVENTION

The circuit of the invention includes a first transmission path comprising *n* series connected switches connected between a strobe terminal and an output terminal and one additional, normally closed switch connected between said output terminal and ground. There are also *n* other transmission paths, each including at least two normally open switches and one normally closed switch. In response to the normally closed switches in said *n* transmission paths, the *n* series connected switches in the first transmission path are maintained open. In response to the concurrent presence of a strobe signal manifestation and the closing of all of the normally open switches in said *n* transmission paths, all of the normally closed switches in all paths are opened, the series connected switches in the first path are closed and a strobe signal is applied from the strobe terminal through the last named closed switches to the output terminal.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a block diagram of a known memory system in which the present invention may be employed;

FIG. 2 is a schematic circuit diagram of a known decoder stage; and

FIG. 3 is a block circuit diagram of one embodiment of a decoder stage according to the invention.

DETAILED DESCRIPTION

The known system of FIG. 1 includes a memory **10** which may consist of MOS semiconductor devices. For purposes of illustration, assume that the memory is 16 × 16 that is, there are 16 × 16 memory locations, each such location consisting of one or more semiconductor devices. In a memory of this type, there may be 16 X lines and 16 Y lines. To access the memory location as, for example, to write information into a memory location, it is necessary to apply a drive current to one of the X lines and to one of the Y lines. The means for routing the drive current to the desired memory location includes an X decoder **12** and a Y decoder **14**. Each such decoder consists of a plurality of stages, 16 in the present example, and three of them are shown in block form to represent decoder **12**.

In the operation of the system of FIG. 1, different combinations of, for example, X control voltages are applied to the various stages of decoder **12** and different combinations of Y control voltages are applied to decoder **14**. For example, stage **12***a* may receive the control voltages $\overline{X1}$, X2, X3, X4; stage **12***b* may receive the control voltages $\overline{X1}$, $\overline{X2}$, X3, X4, stage **12***n* may receive the control voltages $\overline{X1}$, $\overline{X2}$, $\overline{X3}$, $\overline{X4}$ and so on. When, for example, the four control voltages applied to a stage all represent the binary value 1, the current supplied by the drive means **16** is applied via that stage to the memory drive line connected to that stage.

There are a number of circuits which may be used for the decoder stages. A typical prior art circuit is shown in FIG. 2. It consists of six N-type MOS devices N1, N2...N6 and two P-type devices P1 and P2 connected as shown. In the absence of a strobe voltage applied to terminal **20**, that is, when this terminal is at ground potential, the conduction path of device P1 assumes a low value of impedance so that terminal **22** is at approximately the B+ voltage. This voltage applied to the gate electrode of device P2 causes its conduction path to assume a high impedance disconnecting the output terminal W from the B+ voltage terminal. The B+ voltage applied to the gate electrode of the device N6 causes its conduction path to assume a low impedance connecting the output terminal W to ground.

In response to a strobe signal of amplitude +V applied to terminal **20**, device P1 is cut off. If during the strobe interval the control signals X_1, X_2, X_3, and X_4 are all relatively positive representing a 1, the four devices N1 through N4 are all turned on and their conduction paths all have a low value of impedance. The strobe voltage applied to the gate electrode of the device N5 causes its conduction path also to have a low impedance. Accordingly, terminal **22** assumes a voltage level close to ground causing device P2 to turn on and device N6 to be cut off. In view of the low impedance of the conduction path of device P2, the B+ voltage appears at the output terminal W. If during the strobe interval anyone or more of devices N1–N4 remain off, output terminal W is held at or very near zero by N6 which will tend to stay on (and P2 off). This is so since the capacitance between anode **22** and ground remains charged to a value at or very near B+, not being discharged by N1–N5.

While the decoder stage of FIG. 2 is satisfactory in a number of different applications, it does have the disadvantage of relatively low speed. Because the devices N1 through N4 are connected in series, four gate delays are involved before ground voltage appears at common lead **24** and two additional gate delays, namely through devices N5 and P2 occur before the B+ voltage appears at output terminal W. In the case of N MOS devices, these gate delays are not the same device-to-device. As will be shown below, when the devices are connected in a string such as are devices N1...N4, N5 of FIG. 2, each device assumes a threshold voltage V_T which is higher than that of the device lower down on the string. For example, $V_{TN4}>V_{TN3}>V_{TN2}>V_{TN1}$. The greater the threshold voltage, the greater the amount of current overdrive required to achieve a given device speed or, put another way, for a given amount of available drive current, device N4 is slower than device N3; device N3 is slower than device N2; and so on. In other words, if the delay introduced by the first device N1 in a string is Δt_1, the delay Δt_2 introduced by the next device N2 is substantially greater than Δt_1, the delay Δt_3 introduced by the following device is substantially greater than Δt_2 and so on. In more detail, for an N MOS device in saturation,

$V_{gs}-V_t \leq V_{ds}$ and

$I_{ds}=K_n(V_{gs}-V_t)^2$, where:

V_{gs} = gate-source voltage;

V_t = threshold voltage;

V_{ds} = drain-source voltage;

I_{ds} = drain-source current, and

K_n is a gain constant.

For $V_{ds}<V_{gs}-V_t$,

$I_{ds}=K_n[2V_{ds}(V_{gs}-V_t)-V_{ds}^2]$.

In either case, the current is inversely related to the threshold V_t.

But $V_t=V_{tx}+k\sqrt{V_s-V_{sub}-2\psi_f}$, where:

V_{tx} accounts for Fermi potential, metal-semiconductor work function difference and insulator charges

k = is a constant whose terms are $\sqrt{2EsiqN'}$ *and*

ψ_f = Fermi potential of the substrate.

For the normal operation above, $V_{sub}=0$ and $V_s=0$, where: V_{sub} = substrate voltage. Therefore

$$V_t=V_{to}=V_{tx}+k\sqrt{2\psi_f}$$

However, in a logic gate, part of which is depicted at N1, N2, N3, N4, N5 in FIG. 2, this effect causes the following (assuming that all gates are conducting, that is, that all gates are at $+V > V_t$ and that $V_{sub}=0$):

$V_{t1}=V_{tx}+k\sqrt{2\psi_f=V_{to}}$

$V_{t2}=V_{tx}+k\sqrt{V_2-2\psi_f>V_{t1}}$

$V_{t3}=V_{tx}+k\sqrt{V_3-2\psi_f>V_{t2}}$

$V_{t4}=V_{tx}+k\sqrt{V_4-2\psi_f>V_{t3}}$, etc.

where V_2 = voltage at the connection between the drain of N1 and the source of N2, V_3 = voltage at the connection between the drain of N2 and the source of N3, etc.

The threshold voltages are nonlinear functions of the device source potential. Since in the above series string, only the first device's source is constant at zero, all the other devices have an effectively higher threshold during the voltage swing as V5 is discharged to zero. This effect is magnified the more devices that are put in series and the delays introduced by the successive devices are magnified accordingly.

A situation similar to that analyzed above exists when using P MOS devices, however, the delays are not as great as with N MOS devices.

The speed of each decoder stage may be substantially increased by employing the circuit of the present invention shown in FIG. 3. This speed increase is achieved by minimizing the number of devices in a string. For purposes of illustration, the four N-type transistor string of FIG. 2 is shown reduced to two strings which include two N-type transistors each. The first string includes a P-type transistor P10 and two N-type transistors N10 and N11, the conduction paths of which are all connected in series. Similarly, the second string includes a P-type transistor P11 and two N-type transistors N12 and N13 all of whose conduction paths are connected in series. The circuit includes also a third group of transistors including P-types P12, P13 and N-type transistor N14, the conduction paths of which are connected in series.

A B+ voltage terminal 30 is connected to the source electrodes of transistors P10 and P11. The source electrode of transistor N14 is connected to ground. A strobe voltage which normally has the value 0 but which, during the strobe interval, has the value $+V$ is applied to the gate electrode of transistors P10 and P11 and the source electrode of transistor P12. A $\overline{\text{strobe}}$ voltage which is complementary to the strobe voltage is applied to the source electrode of transistors N11 and N13 and to the gate electrode of transistor N14.

The common drain electrode connection of transistors P10 and N10 is connected to the gate electrode 31 of transistor P12. The common drain electrode connection of transistors N12 and P11 is connected to the gate electrode 33 of transistor P13. The circuit output terminal is at the common drain electrode connection of transistors P13 and N14.

In the operation of the circuit of FIG. 3, in the absence of strobe and $\overline{\text{strobe}}$ signals, terminal 32 is at ground and terminal 34 is at $+V$ volts. The ground voltage applied to the gate electrodes of the transistors P10 and P11 turns these transistors on and B+ is applied via the conduction paths of these transistors to the gate electrodes 31 and 33 respectively of transistors P12 and P13. This turns these transistors off isolating output terminal W from the strobe input terminal 32.

The $+V$ voltage applied to terminal 34 turns on transistor N14 causing its conduction path to assume a low impedance. This causes the output terminal W to assume a voltage close to ground voltage.

During the strobe interval, terminal 32 is placed at a voltage of $+V$ and terminal 34 is placed at ground potential. The latter disables transistor N14 and this disconnects the output terminal from ground. The $+V$ voltage applied to terminal 32 disables transistors P10 and P11 disconnecting the B+ voltage at terminal 30 from the gate electrodes 31 and 33. If during the strobe interval all of the control voltages X1, X2, X3 and X4 are positive, representing binary 1, the transistors N10, N11, N12 and N13 are turned on. The ground potential at terminal 34 in this case is applied both to gate electrode 31 and to gate electrode 33 turning transistors P12 and P13 on. During this same strobe interval, the voltage $+V$ is present at terminal 32 and it passes through the conduction paths of transistors P12 and P13, which are in their low impedance state, to the output terminal W. If, on the other hand, during the strobe interval any one or more of the voltages X1 through X4 is at ground representing binary 0, the transistor receiving that control voltage is cut off. For example, if X1 represents a 0, transistor N10 is cut off and its conduction path represents a high impedance. In this case, the gate electrode 31 is not connected to ground and the transistor P12 remains in its high impedance condition. This prevents the $+V$ voltage at terminal 32 from being applied to the output terminal W regardless of whether or not transistor P13 is on (is in the low impedance state).

The important advantage of the circuit described above, as already mentioned, is its high speed. In the example given by way of illustration, in the worst case only the delays through two N-type transistors such as N10 and N11 are involved in addition to the time required for the strobe pulse to pass through transistors P12 and P13. If there are say six or eight control voltages rather than the four, techniques similar to this may be employed to minimize delays. For example, in the case of eight control voltages rather than employing two paths such as 40 and 42, four paths could be employed, one additional path for the control voltages X5 and X6 and another for the control voltages X7 and X8. However, for each additional path an additional P-type device is needed in the final path in series with P12 and P13.

It should also be appreciated that there can be more than two N-type devices in the path such as 40. For example, in a circuit with six control voltages X1...X6 there could be three N-type devices in path 40 for the three voltages X1 through X3 respectively and three N-type devices in the path 42 for the three voltages X4 through X6. It should also be appreciated that while in the present example paths 40 and 42 have equal numbers of N-type devices, this is not essential. For example, path 40 could have three such devices in series and path 42, two such devices in series for a decoder responsive to five control voltages.

Finally, it is to be understood that while in the circuit of FIG. 3 each path 40 and 42 has two N-type and one P-type device and the output path has two P-type devices and one N-type device, the N-type devices could be substituted for the P-type and vice versa with suitable modification of the power supply voltage and strobe voltage polarities.

What is claimed is:

1. In combination:

a first transmission path comprising n series connected, normally open switches connected between a strobe terminal and an output terminal and one additional, normally closed switch connected between said output terminal and a point of reference potential, where n is an integer greater than 1;

n other transmission paths, each including, connected in series, at least two normally open switches and one normally closed switch;

means coupled between the normally closed switches in said *n* transmission paths and the normally open switches in said first transmission path, respectively, for maintaining open the *n* series connected switches in the first transmission path when said normally closed switches in said *n* other transmission paths are closed; and

means responsive to the concurrent presence of a strobe signal manifestation and to the closing of all of the normally open switches in said *n* transmission paths for opening all of the normally closed switches in all paths, closing said *n* series connected switches in said first transmission path, and applying a strobe signal from said strobe terminal through the last-named closed switches in said first transmission path to said output terminal.

2. The combination as set forth in claim 1 wherein said switches comprise field-effect transistors.

3. The combination as set forth in claim 1 wherein the *n* series connected switches in the first transmission path and the normally open switches in said other transmission paths are field-effect transistors of one conductivity type and the remaining switches are field-effect transistors of opposite conductivity type.

4. In combination:

an output terminal;

a first transmission path comprising *n* series connected switches, said path being connected at one end to said output terminal, where *n* is an integer greater than 1;

a normally conducting device connecting said output terminal to a point of reference potential;

n other transmission paths, each including at least two serially connected open switches in series with one normally conducting device;

means coupled between the normally conducting devices in said *n* other transmission paths and the *n* series connected switches in the first path, respectively for normally maintaining open said series connected switches in said first transmission path via said normally conducting devices in said *n* transmission paths respectively; and

means responsive to the concurrent presence of a strobe signal manifestation and the closing of all of the normally open switches in said *n* paths for causing said normally conducting devices in all paths to stop conducting and for applying a strobe signal through said first transmission path to said output terminal.

5. In the combination as set forth in claim **4**, said switches comprising field-effect transistors.

6. In the combination as set forth in claim **4**, said normally conducting device connected to said output terminal and said normally open switches of said other transmission paths comprising field-effect transistors of one conductivity type, and the remaining devices and switches comprising field-effect transistors of another conductivity type.

7. In the combination as set forth in claim **4**, said normally conducting device connected to said output terminal comprising a field-effect transistor of one conductivity type having a conduction path connected between said output terminal and said point of reference potential, and having a control electrode for controlling the conductivity of said path, each normally conducting device in said other paths comprising a field-effect transistor of other conductivity type having a conduction path in series with the switches in its path and having also a control electrode for controlling the conductivity of its path, and wherein said strobe signal manifestation comprises a signal of one polarity applied to the control electrode of the device connected to the output terminal for cutting off that device and a signal of opposite polarity applied to the control electrode of the other normally conducting devices for cutting off these devices.

8. In combination:

a first transmission path comprising the conduction paths of *n* field-effect transistors, said conduction paths connected in series between a strobe terminal and an output terminal, and the conduction path, normally in its low impedance condition, of one additional field-effect transistor connected between said output terminal and ground, each such transistor having also a gate electrode for controlling the conductivity of its conduction path, where *n* is an integer greater than 1;

n other transmission paths, each including, connected in series between the gate electrode of said additional transistor and a voltage supply terminal, the conduction paths normally in their high impedance condition of at least two field-effect transistors, and the conduction path normally in its low impedance condition of one field-effect transistor, each connection between a low impedance path and the high impedance paths of a transmission path comprising a circuit node, said transistors in said *n* transmission paths each having a gate electrode for controlling the conduction of its conduction path;

direct connections from said *n* circuit nodes to the respective gate electrodes of said *n* transistors in said first transmission path;

means for independently applying input signals to the gate electrodes of the field-effect transistors normally in their high impedance condition in said *n* transmission paths, each such signal when at one level placing the conduction path of the transistor to which it is applied in a low impedance condition and when of another value maintaining the conduction path of the transistor to which it is applied in a high impedance condition; and

means responsive to a strobe signal manifestation for applying to the gate electrodes of all transistors whose conduction paths normally are in the low impedance condition, a signal for placing said transistors in their high impedance condition, and for applying a signal to the strobe terminal of said first transmission path in a sense to be conducted through the conduction paths of said *n* field-effect transistors in said first transmission path to said output terminal, when said *n* field-effect transistors in said first transmission path are in their low impedance condition.

9. In the combination as set forth in claim **8**, said transistors in said *n* transmission paths whose conduction paths normally are in the high impedance condition and said transistor in said first transmission path whose conduction path is normally in its low impedance condition being of one conductivity type, and all other transistors being of opposite conductivity type.

10. In the combination as set forth in claim **9**, said strobe signal manifestation comprising a signal of one polarity applied to the gate electrode of said additional transistor in said first transmission path and a signal of opposite polarity applied both to said strobe terminal and the gate electrode of the transistors in said n transmission paths whose conduction paths normally are in the low impedance condition.

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