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(71) Applicant: EASTMAN KODAK COMPANY [US/US]; 343 State Street, Rochester, NY 14650-2201 (US).

(72) Inventors: POTUCEK, Martin ; 71 Red Cedar Drive, Rochester, NY 14616 (US). HADLEY, Mary ; 77 Webwood Circle, Rochester, NY 14626 (US). SMALL, Jeffrey, A. ; 12 Emerald Point, Chili, NY 14626 (US). MATTERN, Michael, William ; 2654 Roosevelt Highway, Hamlin, NY 14464 (US). AGAR, Keith, W. ; 74 Peakview Drive, Henrietta, NY 14467 (US). PHAM, Hieu, T. ; 610 Plank Road, Webster, NY 14580 (US). NG, Yee, Seung ; 15 Great Garland Rise, Fairport, NY 14450 (US). CHUNG, Jeremy, K. ; 116 Creighton Lane, Rochester, NY 14612 (US). KIEFFER, Kenneth, D. ; 8 Pine Ridge Drive, Rochester, NY 14624 (US).

(74) Agent: RUSHEFSKY, Norman; 343 State Street, Rochester, NY 14650-2201 (US).

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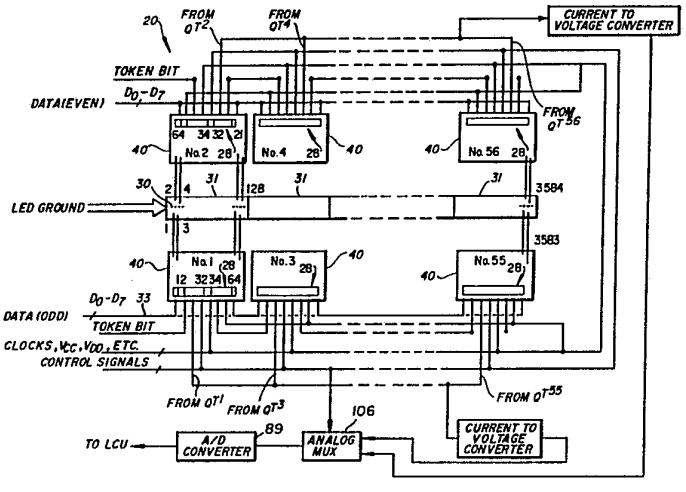
(54) Title: L.E.D. ARRAY PRINTER

(57) Abstract

A non-impact printer apparatus is described that includes a recording head having a plurality of recording elements (30) such as LED's for recording on a recording medium (12). A plurality of driver chips (40) are provided on the head and each includes a plurality of current driving channels for selectively driving a plurality of recording elements in accordance with respective image data signals. The driver chips (40) each further include an extra current driving channel not associated with a recording element (30) for generating a current related to that sent to said recording elements. Monitoring of the current in the extra channel is provided to permit for changes of current to the recording elements (30) and/or corrected image data to provide fine tuned control over uniformity of the recording elements. A digitally adjustable current mirror controls the level of current to each LED during recording. Digital current data signals for controlling this level of current are also communicated over one of the lines of the data bus. Token bit signals are used to control the latching of both current data signals and image data signals in respective registers storing the digital data used for current control and the image data used for controlling energization times. Each driver chip (40) includes two sets of digitally addressable transistors. This allows for individual chip control of current to the respective LED's to correct for nonuniformity of light output from chip to chip due to temperature gradients as well as controlling for light output due to aging of the printhead. The current mirror has a master circuit for generating a reference current and a plurality of slave circuits for providing respective driver currents to the recording elements (30) selected for energization. A transistor switch is in series with a respective recording element (30) and switchable from one state to another in response to a signal at its control electrode. Each of the slave circuits includes an additional slave circuit which provides a current path for facilitating changing of the signal at the control electrode from one voltage level to another such as by allowing a capacitive charge at the control electrode to dissipate.



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L.E.D. ARRAY PRINTER

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to non-impact printer apparatus for recording, and more specifically, to circuitry thereon for controlling current uniformity to the recording elements.

2. Description of the Prior Art

In U.S. Patent 4,831,395, an L.E.D. (light emitting diode) printhead is described wherein control of current to the LED's during recording is provided by a current mirror circuit. This circuit features an adjustable resistor and voltage supply to allow the respective currents to the LED's to be controlled so that adjustments may be provided to have the outputs of the LED's be more uniform. Where groups of LED's are driven from respective driver chips, each driver chip is separately adjustable so that LED's driven from this driver chip receive sufficient current so that their respective intensities are similar to that of LED's driven by other driver chips on this printhead. Another aspect of adjustability requires the LED's to put out sufficient light to expose the recording medium such as a photoconductor.

In U.S. Patent 4,885,597, an LED printhead is described wherein compensation for age and temperature of the LED's is accommodated to ensure that the intensity from the LED's is consistent over time. In this printhead, current to the LED's is regulated using digitally addressable current mirrors associated with each driver chip. The multi-bit digital current regulation signals used must be communicated to the driver chips and adjustments in intensities of the LED's made accordingly.

A problem therefore arises regarding the effect of temperature upon LED output and how to more accurately correct for temperature during use of the printhead.

A problem further arises regarding the increased complexity in providing current regulating signals to the printhead to correct for the effects of temperature and other factors.

A problem still further arises regarding maintaining consistency of LED light output under conditions where variations in LED driving voltage, V_{LED} or V_{cc} may occur as well as under conditions where LED's are being turned on and off at different times.

It is therefore an object of the invention to overcome these problems and to provide an improved printer apparatus with improved means for measuring localized temperature of the printhead and for providing for more consistent operation and for more prompt and fine-tuned correction of non-uniformities.

SUMMARY OF THE INVENTION

The above object and others which will become apparent in reading the specification below are realized by a non-impact printer apparatus that includes a recording head having a plurality of recording elements for recording on a recording medium; driving means including a plurality of current driving channels for selectively driving said plurality of recording elements in accordance with respective image data signals; the driving means further including an extra current driving channel not associated with a recording element for generating a current related to that sent to said recording elements; and means for monitoring a parameter related to said current in said extra

channel.

In accordance with another aspect of the invention, a non-impact printer apparatus is provided that includes a recording head having a plurality of recording elements for recording on a recording medium;

driving means for selectively driving said plurality of recording elements in accordance with respective image data signals; and

means including data bus means for carrying on said data bus means multibit image data signals determining a recording duration for a recording element and for carrying on one line of said data bus means also used for carrying image data signals, a multibit digital signal used for regulating a level of current to said recording element.

In accordance with still another aspect of the invention, there is provided a non-impact printer apparatus comprising:

a recording head having a plurality of recording elements for recording on a recording medium;

driving means for selectively driving said plurality of recording elements in accordance with respective image data signals;

said driving means including a plurality of data register means with respective data register means associated with each recording element for storing said image data signals;

data bus means for carrying image data signals;

means for commonly connecting said data bus means to said plurality of data register means;

means for generating a token bit signal;

a multistage shift register means for outputting sequentially at respective stages the token bit signal for sequentially selecting a respective data

register means for accepting image data signals;

said driving means further including current regulating means for regulating a level of electrical current to each recording element, the current regulating means being characterized by

means for adjusting a level of electrical current to each recording element in response to a multibit digital signal; and

wherein the current regulating means further includes first register means including a plurality of registers for storing digital signals related to a level of current control, second register means for storing and shifting a token bit signal, and means responsive to a token bit signal in said second register means for latching in an appropriate register of said first register means the multibit digital signal.

In yet another aspect of the invention, there is provided a non-impact printer apparatus used for recording, comprising:

a plurality of groups of recording elements,

a plurality of integrated circuit driver chips for driving respective groups of recording elements;

a) first digitally addressable current-conducting means for selectively establishing a first bias voltage in response to a first multibit digital signal;

b) second digitally addressable current-conducting means responsive to the first bias voltage and to a second multibit digital signal for generating a bias current and establishing a second bias voltage;

c) means for selectively causing current to flow through recording elements selected for energization; and

d) current mirror driver means for regulating levels of currents through said selected recording elements, the level of current being related to said second bias voltage, and characterized by

wherein elements a), b), c) and d) are all on each of said driver chips.

There is further provided in accordance with the invention a non-impact printer apparatus comprising:

a series of point-like energizable radiation sources arranged in a row;

means providing data signals representing data to be printed;

logic means responsive to the data signals for determining which of the point-like radiation sources are to be selected for energization;

current driver means responsive to the logic means for providing electrical current to the radiation sources selected for energization, the current driver means including a master circuit including a first transistor for generating a reference current through said first transistor and a plurality of slave circuits for providing respective slave driver currents to the radiation sources selected for energization, means including (a) a plurality of individually selectively addressable current-conducting devices coupled to the master circuit, (b) first control means for selectively determining which of said plurality of devices are to be current conducting, and characterized by

(c) current source means responsive to increases in temperature on the printhead for providing increased current generated by said current source means, (d) adjustable bias means coupling said current source means to said first plurality of devices to increase respective levels of currents conducted by selected

ones of said first plurality of devices and responsive thereto for generating an adjusted voltage bias signal, and (e) bias responsive means responsive to an adjustment in voltage bias for increasing the reference current in response to the increase in the temperature of the printhead.

The invention also provides a non-impact printer apparatus, comprising:

a plurality of energizable recording elements;

driving means for energizing said recording elements, said driving means including current mirror means having a master circuit means for generating a reference current and a plurality of slave circuit means for providing respective driver currents to the recording elements selected for energization;

each slave circuit means including:

(a) transistor switching means in series with a respective recording lement and switchable from one state to another in response to a signal and having a control electrode for controlling driver current to its respective recording element in response to the signal;

(b) enabling means operating upon the control electrode for switching the switching means to allow driver current to be selectively provided to a respective recording element for a predetermined period of time; and

(c) each of said slave circuit means further including its own additional slave circuit means for providing a current path for facilitating changing of the signal at the control electrode from one voltage level to another.

The above and other objects and features of the present invention will become apparent from the following description taken in conjunction with the

accompanying drawings

BRIEF DESCRIPTION OF THE DRAWINGS

The subsequent description of a preferred embodiment of the present invention refers to the attached drawings wherein:

FIG. 1 is a perspective view illustrating the general arrangement of a prior art non-impact printer;

FIG. 2 is a block diagram of a circuit for providing signals to a non-impact printhead made in accordance with the invention;

FIG. 3 is a block diagram of a printhead according to the invention, the printhead including a plurality of driver chips for driving the LED's formed on chip arrays;

FIG. 4 is a block diagram of a driver chip made according to one embodiment of the invention and used on the printhead of FIG. 3;

FIG. 5 is a circuit diagram of one circuit incorporated on the driver chip of FIG. 4 in accordance with the invention; and

FIGS. 6A, 6B, 6C, and 6D comprise a schematic of a current driving circuit incorporated on the driver chip of FIG. 4.

FIG. 7 is a block diagram of another embodiment of a printhead made according to the invention;

FIG. 8 is a block diagram of a driver chip for use on the printhead of FIG. 7;

FIG. 9 is a block diagram of an extra driver channel or current monitor channel for the driver chip of FIG. 8;

FIG. 10 is a schematic of a token bit register incorporated on the driver chip of FIG. 8;

FIG. 11 is a schematic of a token bit register incorporated on another embodiment of a driver chip that is a modification of that of FIG. 8;

FIG. 12 is a time line illustrating the occurrence of various pulses on the driver chip of FIG. 11; and

FIG. 13 is a truth table illustrating operation of the modified driver chip of FIG. 11.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Because the apparatus of the type described herein are well known, the present description will be directed in particular to elements forming part of, or cooperating more directly with, the present invention.

The apparatus for the herein disclosed invention is typified by the diagram of FIG. 1; a linear array 10 of say 3584 triggerable recording elements; e.g. LED's, is disposed to expose selectively a photosensitive image-receiver medium 12 that is movable relative to the array by suitable conventional means (not shown). While the embodiments of the invention will be described in terms of LED printheads, other recording elements may also make use of this invention. Optical means for focusing the LED's onto the medium may also be provided. In this regard, gradient index optical fiber devices such as Selfoc (trademark of Nippon Sheet Glass Co., Ltd.) arrays are highly suited. The LED's of the array are triggered into operation by means of image processing electronics 14 that are responsive to image signal information. Depending on the duration for which any given LED is turned on, the exposure effected by such LED is more or less made. Where the medium 12 is, say, photographic film the latent image formed line by line by selective exposure of said LED's may be subsequently developed by conventional means to form a visible image. Where the medium 12 is an electrophotographic receptor, the

LED's may be used to form an electrostatic image on a uniformly electrostatically charged photoconductor and this image developed using opaque toner particles and perhaps transferred to a copy sheet, see U.S. Patent 3,850,517 and 4,831,395.

With reference now to FIGS. 2, 3, and 4, a data source 15 such as a computer, word processor, image scanner or other source of digitized image data, provides image data signals to a data processor 16 which may comprise a raster image processor. The data processor under control of clock pulses from a logic and control device (LCU) 13 provides a plurality of outputs including rasterized data outputs and control signals which are fed to the printhead. Data for each pixel may be represented by a multibit signal of say 4 bits representing a grey level for exposure for recording that pixel. A programmable ROM (PROM) 16a may be provided either on or off the printhead to modify the data to provide for uniformity correction from LED to LED. In this regard, see Pham et al PCT International application US 90/0074. The PROM transforms the 4-bit signal into a 6-bit grey level signal that is adjusted or corrected for the light-emitting characteristics of the respective LED. This balance in light output from LED to LED can be corrected by modifying the data bit signals in accordance with empirical determinations. The PROM has stored therein correction factors associated with each LED for modifying that LED's respective data. As will be described below, this PROM may be modified in accordance with age and/or temperature changes to the printhead. In addition, the LCU provides exposure clock pulses to a down/up counter 18 (FIG. 4) which, when enabled by a signal from the LCU, counts such

clock pulses and provides at an output having a plurality of lines a digital signal representation of the state of the counter. Typically, such a counter has one line representing a least significant bit of such count and other lines representing other more significant bits. In accordance with a technique fully described in U.S. patent 4,750,010 in the names of Ayers et al, the output of counter 18 is provided to a first set of input terminals to a comparator 19 associated with each recording element 30, i.e., LED in this embodiment. A plurality of data lines from each of a plurality of corresponding data registers 24 is also provided to a second set of input terminals associated with each comparator 19. The comparators 19 all compare the output of the counter 18 with the value of the respective data. As will be described herein, the image data signals provided to each comparator relates to a desired ON time or period of enablement for a respective LED 30 for the recording of a particular pixel. As is well known, the LED's are alternately divided into odd and even-numbered LED's so that respective integrated circuit driver chips 40 therefor are located on opposite sides of the line of LED's. As the circuitry is identical for the corresponding driver chips, the discussion herein will be made as to one of these driver chips. The image data signals provided to each comparator 19 during the printing of a single line of dots by the row of LED's is related to the desired pixel or dot size to be exposed onto the image receiver medium by that LED for that particular line of dots. As shown in FIGS. 3 and 4, six independent lines of data DI0 through DI5 provide a six bit digital image data signal that allows for grey-scale variation of the output of each LED during

each cycle of operation. During each cycle the data to each comparator may comprise six binary bits representing an amount from decimal 0 to decimal 63. Although the data lines DI0 through DI5 are shown passing through the data registers 24 in FIG. 4, it will be appreciated that this is for the convenience of this illustration and that actually such lines comprise a plurality of data lines that are simultaneously available to all latches as will be described below.

Suppose, for example, that an LED, LED_1, is to be enabled for a time period equal to 20 clock periods plus T_{MIN}. T_{MIN} represents a pre-established minimum LED on time. In response to a start pulse on line LLATCHN, the counter 18 is enabled and commences to count exposure clock pulses from line 17 from decimal 63 to 0. Note that the clock pulses may be generated to have a variable programmable period. The six bit output of counter 18 is coupled to one set of inputs at terminal X of each of the comparators. This count is now compared with the data input at another set of inputs at terminal Y of this comparator which represents in binary form decimal ten. When there is a "match," i.e., when the count of terminal X is 10, a pulse is provided at the output terminal of comparator 19 to cause latch or toggle flip-flop 22 to enable the constant current driver 23 to commence and maintain current to LED_1. After the counter counts down to zero, the counter may be inhibited from counting additional clock pulses for a period T_{MIN} that is either programmed into the counter or provided by other suitable means. After this predetermined time period T_{MIN}, if used, the counter is set to count in its up mode and commences counting clock pulses

again. When the counter, in its count up mode, reaches decimal 10 the flip-flop 22 is reset and current to the LED ceases. The other LED's, etc. operate in similar fashion but their data may require different count values to turn on and off. What these LED's will thus have in common is that all will have their respective current pulses centered, i.e., the midpoints of the respective current pulses will occur at the same time. The pulse duration for each LED during each line of print is varied, however, in accordance with their respective image data signals. Reference is also made to aforementioned PCT International application No. US 90/00074, regarding a clocking scheme using a non-linear clock, the contents of which are incorporated by this reference. As noted in this latter reference, correction for unequal light output from LED to LED may be provided by adjustment of the data in accordance with the characteristics of each LED. Thus, a programmable read only memory device or PROM or other programmable device may store the characteristics of each LED and data for that LED can be modified to provide an input count at terminal Y that represents data modified by the exposure characteristics of the LED. For example, for an LED that is a relatively strong light emitter the PROM would modify data bits for that LED to reduce the count that otherwise would be provided at terminal Y based solely on the data.

Still other circuitry for balancing the driving current to the LED's is described below.

The description of the circuitry forming a part of the driving circuitry for distributing the image data signals to the appropriate comparator and to current driving circuits will now be described. In

the example of the circuitry for the printhead shown in FIG. 3, the driving circuitry for the LED's are provided on opposite sides of the line of LED's 20. This is a known desirable arrangement for permitting LED's to be packed closer together to provide greater image resolution capabilities for the printer. As may be noted the circuit arrangement is an alternating one such that what may be called the even-numbered LED's have their respective driving circuitry located to one side of the line of LED's and what may be called the odd-numbered LED's have their respective driving circuitry located to the other side of the line of LED's. Typically, groups of, say, 64 of the odd numbered LED's (in a chip array 31 having 128 LED's arranged in a row) will have their respective driver circuitry formed in a single integrated circuit chip 40 and thus, for a printhead having 3584 LED's on the printhead, there may be 28 driver chips located on each side of the line of LED's. In order to save on production costs for these driver chips, it is desirable that they be identical. For the driver chips to be identical, although locatable on either side of the line of LED's, it is desirable for design simplicity that signals traversing the length of the printhead be programmably movable in either direction; see in this regard U.S. Patent 4,746,941. LED chip arrays having more than 128 LED's are also known but the invention will be described with reference to those having 128 LED's.

The image data signals are output by the data processor 16 in accordance with image data signals for the odd-numbered LED's and image data signals for the even-numbered LED's. Discussion will now be made with regard to the image data signals for the

odd-numbered LED's, since operation and circuitry for driving the even-numbered LED's is identical. With reference to FIG. 4, data lines DI0 - DI5 are independent lines each carrying a signal representing a digital bit (0 or 1) so that together their respective signals define a digital six bit number from decimal 0 to decimal 63. This image data signal is passed along lines DI0 - DI5 on the printhead which comprise an image data signal bus. Associated with each LED is a data register means 24 for latching data from this bus during each cycle of operation for printing a single line of dots or pixels. As will be described, a token bit is used to enable a data register means associated with a particular LED to accept the data while other data register means associated with other LED's await their respective data. The use of a token bit in a printer apparatus for controlling latching of multibit data is described in U.S. Patent 4,746,941.

The data register means 24 for each LED comprises a pair of latches 25, 26 or bi-stable multivibrators (msff = master-slave flip flops) for each of the six data lines. The pair of latches are connected in a master-slave relationship wherein in response to a token bit signal at the enable input terminal of the master latch 25, an image data signal at the data input terminal of the master latch 25 will cause the output of the master latch to either change or remain the same depending upon the image data signal. It will be noted that the six master latches 25 in the data register means of each LED are commonly connected to a line 27 to simultaneously receive the token bit signal from the token bit shift register 28.

The token bit shift register 28 comprises a

series of flip-flops 29 which have clock pulses (SHFTCLK) applied to the clock terminals thereof and the signal representing the token bit input to the data input terminal of each. Note that the same token bit signal will be provided to both the even and odd token bit shift registers for the even and odd numbered LED's. The output of each of these flip-flops 29 is connected to the data input terminal of the next flip-flop 29 in the series. Buffers 31 with enable inputs and direction controls are coupled to the token bit shift register 28 so that programmable control may be made of the direction for shifting the token bit along the token bit shift register 28. In the example where the token bit is to be shifted from left to right in FIG. 4 for the Data Odd half of the printhead, the signal line TDIR (token direction) is made at an appropriate logic level to allow the token bit on line LTOKEN to pass from left to right. Thus, in response to clock pulses from the data processor 16 the token bit is passed from stage to stage (left to right in FIG. 4) of the token bit shift register 28 and accordingly outputted sequentially over respective lines 21 through OR gates 11 to lines 27 for enablement of all the master latches 25 of a respective data register 24. With movement of the token bit from stage to stage of the shift register 28 the data bits occurring on lines DI0-DI5 are accepted by the data registers 24 in turn from left to right until all the 1792 data registers on this side of the printhead have acquired their respective six bits of data. A latch enable signal is then pulsed low on line LLATCHN to cause the respective slave latches 26 to latch the data at their respective outputs and to reset the toggle flip-flops 22. The respective

outputs of the slave latches 26 are now communicated to the data input terminals Y of the respective comparators 19 for determining the duration of exposure for each LED in accordance with the techniques described above. The master latches 25 are now free to receive the image data signals for the next line of dots to be recorded.

The comparators 19 each have at an output an AND gate 19′ and a D type flip-flop 19″ in order to prevent the propagation of extraneous logic glitches from the comparator outputs to the toggle flip-flop inputs.

After LLATCHN returns to its inactive level, on the first rising edge of EXPCLK while a particular comparator's 19 output is at a logic high level, the respective toggle flip-flop 22 toggles from the reset state to the set state. The Q and QN outputs of this toggle flip-flop then cause the associated controlled current driver 23 to be enabled. After this same comparator's output has been returned to a low logic level, and then returns to a high logic level on some later rising edge of EXPCLK, the respective toggle flip-flop 22 toggles back to the reset state. The Q and QN outputs of this toggle flip-flop then disable the associated constant-current driver 23.

With reference now to FIGS. 6A, B, C and D, the current driving circuit 23 portion of each driver chip 40 is shown. The respective outputs of the toggle flip-flops 22 are fed over respective lines 45^1, 45^3, and the following lines not shown 45^5, --- 45^{125} and 45^{127}. As may be seen each of these lines is actually a double line one of which carries an enable signal to turn the respective LED on and the other carries a complement of this signal. The lines 45^1 are input to respective

control electrodes of transistors Q_{426}, Q_{427}. These transistors act as switches and form a part of a current mirror driving circuit that includes a master circuit formed by transistors Q_{424}, Q_{425} and a series of digitally controlled transistors. More details concerning the digitally controlled transistors will be found below with reference to the discussion of FIGS. 6A and 6B. Briefly, these digitally controlled transistors may be selectively turned on to establish a signal I (CHIP BIAS) to thereby regulate a desired current level for the LED's driven by this driver chip. As may be noted in Figure 6C, circuitry for driving two LED's, i.e., LED_1 and LED_3 are illustrated; it being understood that the driver chip would have appropriate circuits typified by those described below for driving say 64 of the odd-numbered LED's in an LED chip array having, for example, 128 LED's. Another driver chip on the other side of the LED chip array would be used to drive the 64 even-numbered LED's.

The current through the master circuit establishes a potential V_{G1} on line 117. Directly in series with LED_1 are two transistors Q_{428}, Q_{429}. Transistor Q_{428} is biased to be always conductive while transistor Q_{429} is switched on and off and thus is the transistor controlling whether or not current is driven to LED_1. The gate or control electrode of transistor Q_{429} is coupled to the drain-source connection of transistors Q_{426}, Q_{427}. When LED_1 is to be turned on, transistor Q_{427} is made conductive and when LED_1 is to be turned off, transistor Q_{426} is made conductive. The gate of transistor Q_{426} receives a logic signal that is the inverse of that to gate Q_{427} from a

data driven enabling means 22 that is the circuitry of FIG. 4 which controls whether or not an LED is to be turned on and for how long. As noted above in a grey level printhead, the LED is to be turned on for a duration determined by the grey level data signals input to the printhead.

Also associated with the circuitry for driving LED_1, is an additional current mirror that includes two slave circuits. One slave circuit comprises transistors Q_{420}, Q_{421} and Q_{430}. The other slave circuit comprises transistors Q_{422}, Q_{423} and Q_{431}. Transistors Q_{430}, Q_{431} are N-channel MOSFETS while the other transistors noted above are P-channel MOSFETS. The two additional slave circuits associated with LED_1 are on continuously and assuming a nominal driving current of say $ILED_1$=4 ma to LED_1, the current through transistor Q_{421} might be 1/80 $ILED_1$ and the current through transistor Q_{423} might be 1/800 x $ILED_1$. The currents through these slave circuits establishes a voltage level V_{G2} on line 114, which is the potential of the drain electrode of transistor Q_{427}.

In operation with transistor Q_{429} turned off, transistor Q_{426} is on and impresses approximately the voltage V_{cc} at the gate of transistor Q_{429}. When LED_1 is to be turned on to record a pixel (picture element), a signal is provided by the data enabling means 22 to the gate of transistor Q_{427} to turn same on, while an inverse signal turns transistor Q_{426} off. Before transistor Q_{429} turns on, the capacitive load or change existing between its gate and substrate must be removed. When transistor Q_{427} turns on, the charge on the gate terminal of transistor Q_{429} discharges through

transistors Q_{427} and Q_{430}. This path for discharge of the gate capacitive load at transistor Q_{429} thereby provides a turn-on time not affected by the number of LED's that are sought to be simultaneously energized. The reason for this is that each control transistor corresponding to transistor Q_{429} has its own respective path for discharge of its respective capacitive load. While the illustrated embodiment shows use of the additional current mirror circuit containing transistor Q_{430} for use in discharging the control electrode of the driving transistor, it will be understood that in some circuit arrangements, charging, rather than discharging, of the control electrode may be facilitated.

Current through transistors Q_{422}, Q_{423} and Q_{431} is proportional to, i.e. mirrors, that through the master circuit because of the identical gate to source terminal biasing (V_{GS1}) of transistors Q_{424} and Q_{422}. Thus, current is constant in this slave circuit even though V_{cc} from a conventional power supply varies since the potential difference V_{GS1} between the gate and source terminal of transistor Q_{422} remains constant. The current through the circuit comprised of transistors Q_{422}, Q_{423} and Q_{431} is mirrored by that through the slave circuit comprised of transistors Q_{420}, Q_{421} and Q_{430} due to the identical gate to source biasing of transistors Q_{430}, Q_{431}. With a constant current being generated in the slave circuit comprised of transistors Q_{420}, Q_{421} and Q_{430}, the potential difference between the gate and source terminals of transistor Q_{420} remains fixed as does that of transistor Q_{421} thereby establishing a voltage level V_{G2} on line 114 which varies with

V_{cc} although the potential difference $V_{cc}-V_{G2}$ remains constant.

With the transistor Q_{429} turned on and conducting driving current to LED_1 during an exposure period, the voltage level V_{G2} is established at the gate of transistor Q_{429} via now conducting transistor Q_{427}. The voltage level at the source terminal of transistor Q_{429} is now at a fixed threshold value above that of V_{G2}. Transistor Q_{429}, acting as a cascode transistor and having its source terminal connected to the drain terminal of transistor Q_{428}, thereby establishes the drain potential of the transistor Q_{428} as varying with changes in V_{cc}. As noted above, the potential difference V_{GS1} is constant even though V_{cc} itself varies. The voltage relationships between the various terminals of transistor Q_{428} are not affected by variations in V_{cc} and the current to LED_1 during a period for recording a pixel stays constant.

Thus, stability in driver current to LED_1 is provided since transient changes in V_{cc} do not cause corresponding changes to the current conducted through LED_1 and thus do not affect the intensity level of light output by LED_1. The tendency in some LED printheads for light output of an LED to diminish when other LED's are turned on can also be reduced with this circuit. As noted above, transistor Q_{429} conducts current to LED_1 for a time period controlled by the data bits for recording an appropriate pixel. The level of current for recording this pixel is controlled by the current mirror which is responsive to the current level I(CHIP BIAS). The circuit for generating I(CHIP BIAS) will now be described.

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used by the LCU to provide fine adjustment of current to the LED's by changing the 8-bit local current regulating signal R_{REF} stored in registers R_2 in response to an algorithm relating temperature measured with signals to be fed to a respective driver chip's registers R_2. The signal relative to temperature may also be used to adjust the data signals to regulate or correct the on-time of the LED's using pulsewidth modulation. As noted above, the LCU may calculate a new correction program based on the fall off of intensity with temperature for the LED's. This new program is then input to the PROM 16a to adjust the corrected data sent to the printhead.

Note that the 65th channels on the even driver chips are also commonly connected to the input of the A/D converter 89 (FIG. 3). A reading of the voltage generated by a respective 65th driver channel on say an even-numbered driver chip is determined by having a logic high signal on the DI5 line on the even side with a corresponding low level signal on the DI5 line on the odd side since logic AND gate 101 (FIG. 5) on each driver chip passes the token bit only when the respective (odd or even) DI5 line is logic high.

Description will now be made of the embodiment of FIGS. 7-9 wherein similar numbers to that of the prior embodiment relate to similar structures. In this alternative embodiment, image data and recording of same is handled in a similar way to that described above and is in accordance also with the description of U.S. Patent 4,746,941. In this example, eight bits of image data are used instead of six but the principle of operation is similar using an 8-bit comparator for determining exposure duration. During recording of one line of image data by the printhead

20, the next line of data is sent down the data bus D_0-D_7 and is latched in consecutive order by the respective master-slave latch registers 24 in accordance with the presence of a token bit in a respective register. As noted above, the token bit is shifted down the 64-bit bidirectional token bit shift register 28 and image data on lines D_0-D_7 is latched in a respective latch register 24. The token bit then exits the shift register and is shifted into the shift register of the next driver chip. Current monitoring is also activated during a portion of the period that the token bit is present in the driver chip's token bit shift register. A signal from the LCU is used to generate current in the 65th driver channel. The means for activation of the 65th driver channel will now be described further with reference also to FIG. 9. A latch 111 coupled with the extra, or in this example the 65th, driver channel has its output enabled or say placed logic high in response to the location of the token bit in a specific stage (N) of the token bit shift register 28. The output of token bit register stage N is coupled via the logic gates 186, 190 and 187, 191, respectively, to the preset and clear inputs of latch 111. In response to this, current flows in the 65th channel of the driver chip 40 now containing the token bit in a similar way to that described for the prior embodiment. Current to the 65th driver channel (FIG. 6D) terminates when the token bit has moved a fixed number of stages (say M stages) down the token bit shift register 28 in this same driver chip 40. In response to the token bit reaching a particular stage, N + M, the latch (111) output is disabled or cleared. The output of token bit register stage N + M is coupled via the logic gates 188, 190 and 189,

191, respectively, to the preset and clear inputs of latch 111. As may be noted in FIG. 7, the outputs of all the current monitors or 65th channels of all the odd-numbered driver chips are connected in parallel to a current to voltage converter which may be similar to that described above. These outputs are multiplexed by multiplexer 106 with the similar outputs of the current monitors to the even-numbered driver chips. An A/D converter 89 converts the analog signal which is also related to the temperature of that driver chip (and approximates the temperature of the LED's driven by that driver chip) to a digital signal that is communicated over appropriate lines to the LCU. The LCU, by keeping track of the counts of the token clock for use in shifting image data, knows which driver chip the token bit is located in and thus which driver chip's 65th channel is being activated at this time. Note that while data for recording the next line of pixels is being sent over bus lines D_0-D_7 and latched in appropriate master registers in response to the token bit, the previous line of pixels, whose data is stored in the slave registers of latches 24, is being printed by the LED's while the 65th channel driver channel is also activated. Note, too, that even though the token bit is shifted simultaneously down even and odd-numbered driver chips 40, for example, driver chips #1 and #2, or #3 and #4 ..... or #55 and #56, the LCU recognizes that for a certain part of the period for which a token bit is resident within a driver chip (and for which the 65th channel monitoring is activated) the monitored current input to the multiplexer 106 must be odd. For example, and with reference to FIG. 7, when the token bit is within registers #2 through #32 of the bi-directional

64 token bit shift register 28 of say driver chip #1, the LCU is programmed to consider the current monitored signal from the A/D converter 89 as representing the current in driver chip #1, even though the token bit is simultaneously also in the driver chip #2. However, because driver chips #1 and #2 are identical and due to the bidirectional feature of the token register 28, the token bit in register #2 moves from register #64 to register #1 so that when the token bit is in one of the registers #2 through #32 on driver chip #1, it is in one of the registers #63 through #33 on chip #2. Similarly, when the token bit is in one of the registers #32 through #2 on driver chip #2, it is also simultaneously in one of registers #33 through #63 on driver chip #1. Thus, the LCU recognizes that when the token has moved 33 clock pulses into a token shift register of a driver chip (but less than 64 clock pulses) the signals generated by the A/D converter to the LCU represent current to the LED's in a driver chip that is the even-numbered driver chip of the pair of driver chips having the token bit. Additionally, a select signal is provided by the LCU to multiplexer 106, which controls which of the current signals, odd or even, is to be sent to the LCU. The overall clock token count determines which odd and even pair of driver chips the token is in. If desired, the extra current to voltage converter and analog multiplexer may be omitted as in the printhead of FIG. 3.

With reference now to FIG. 10, further details of the token bit register 28 of the embodiment of FIG. 7 are shown. A token direction signal (Tdir) biases line 220 at one logic level and through inverter 221, biases line 222 at an opposite logic level. Assume

that the signal Tdir biases line 220 for transmission of the token bit that travels from left to right (Lbit) in FIG. 10. In such case, the tristate inverters 31 used for transmission of the right to left going token bit are disabled. The token bit is synchronized with pulses of the token clock (TCLK) and upon entering the driver chip, triggers the D input of the first token register of the token bit shift register to switch its outputs so that the Q output of the register is changed to enable the eight-bit latch 24 (FIG. 8) to latch the image data signals upon data bus lines D_0-D_7. Upon occurrence of the next clock pulse the first token register is reset and the token bit is shifted via a tristate inverter 31 from the Q output of the first token register to the D input of the second token register. The second token register now has its Q output such that image data signals on the image data bus will be latched by the appropriate latch register associated with LED_3. The change of the Q output of the second token register simultaneously sets latch 111 (FIG. 9) which triggers the 65th current channel (FIG. 6D) to enable transistor Q_{T1} to generate a current IQ^{T1} which is identical to that simultaneously being driven through the LED's that are enabled for recording the prior line of pixels. The current is monitored by the LCU via A/D converter 89 and in accordance with a program in the LCU the current is related to the temperature of the driver chip. This current is monitored until the token bit reaches the 32nd token register upon which event the Q output of this register resets latch 111. With movement of the token bit into the 33rd token register of driver chip #1, the LCU commences to monitor the current in the 65 driver channel of

driver chip #2 as described above. As noted above, monitoring of the current is done first in driver chip #1 and then driver chip #2. The token bit then passes into driver chips #3 and #4 for monitoring the current in these chips as well as for latching of image data for these chips on lines D_0-D_7.

In FIGS. 11-13, an improvement over the circuit of FIG. 10 is illustrated wherein in addition to use of the token bit for simultaneously controlling distribution of image data and use in monitoring current on driver chip temperature, there is also provided the use of the token bit for controlling the change of digital current regulation data in the driver chip just prior to recording each line of pixel data. In the embodiments described above, R_{REF} or V_{REF} digital current regulation data was provided during interframe or other non-production periods when no printing was occurring. In the embodiment now to be described, the digital current regulation data is provided during printing. This allows current not only to be monitored in real time but also to be changed more promptly as required. As the same data bus is used to carry both image data signals and current regulation signals, a logic circuit 246 is provided in each driver chip to allow the circuit to discriminate between image data signals that control the pulsewidth time duration exposures used for recording the next row of image pixels or current regulation data signals which control the level of current to each LED activated during recording of the next row of pixels.

Data for adjusting R_{REF} is provided by the LCU based upon the temperature-related current signals generated by each of the respective current drivers for the 65th current channel of each driver chip. In

response to these current signals, the LCU calculates a new 8-bit digital word for each driver chip to control the respective level of current in that driver chip. Simultaneously, a token bit is also generated on line Lbit and a control line labelled LD/Run is adjusted to a logic low level. In addition, the line T_{dir} is made a logic high level so that the logic circuit 246 has the four output lines thereof at suitable logic levels to disable the tristate inverters 31 associated with the image data token registers as well as disable the register 111 for disenabling the 65th current driver circuit. In response to the token bit input to the D input of a register 112, the Q output of this register changes to provide a load signal to the latch register 113 (FIG. 8) for loading current regulation data carried on lines D_0-D_7. The Q output of latch 112 is output to the Lbit input of the next driver chip so that with the next operation of the token clock, the output of Q changes. This provides the needed token pulse to the D input of the register 112 of the next driver chip. The LCU at this time has also changed the current regulation data upon lines D_0-D_7 to be appropriate for proper regulations of current in this next driver chip. Note that because there are separate data lines for odd and even-numbered driver chips, the token bit is simultaneously applied to odd and even-numbered driver chips so that current regulation data is provided simultaneously to an odd-numbered driver chip as well as to an even-numbered driver chip. After respective current regulation data is distributed to all the driver chips, the LCU changes the LD/Run line to a logic high level and a new token bit is sent by the LCU to the first driver chips (odd and even) on the

printhead for latching the image data signals on data bus lines D_0-D_7. With this token bit the register 111 will be set by the token bit to commence operation of the 65th channel current driver as described for the embodiment of FIGS. 7-9. Another difference in the embodiment of FIG. 11 is the use of the first token register (rather than the second token register) to commence drive to the 65th channel current driver. Other token registers may be designed for determining when the 65th channel is to be operated. It may be desirable for the LCU to have a small programmed delay as to when the LCU actually reviews the current data from the A/D converter 89 (FIG. 7). This delay will allow the driver current in the 65th current channel to stabilize.

ADVANTAGES

An improved printer apparatus has been described which provides for fine control over adjustments of current to the recording elements as well as for correction of pulsewidth durations as required for temperature compensation. There is also ensured that destructive current levels will not be generated when current to the recording elements are adjusted.

The use in the embodiment of FIGS. 7-9 and 11-13 of the token bit in the token register while the token bit is also defining which latch register is to secure image data coming over the image data bus D_0-D_7 allows current monitoring to be done during printing rather than waiting for say an interframe or other non-productive period. Thus, in response to the current (and temperature) related data obtained from each driver chip, prompt adjustment may be made by the LCU to terminate current to the LED's if an inappropriate current level is detected. In addition, if the current level is within acceptable

limits, prompt uniformity control is provided by adjusting or fine tuning image data to that driver chip. Image data from RIP 16 (FIG. 2) is a multibit digital signal indicating the level of grey of a pixel to be recorded by a particular LED. However, in response to a signal from the LCU regarding correction for uniformity, this multibit data signal may be adjusted to correct for say the decrease in light output by the LED's driven by this driver chip due to the higher temperatures of the LED array chip driven by this driver chip. As may be noted in FIG. 2, the odd and even data from RIP 16 may be first modified by a correction PROM 16a before this data is sent to the printhead. The correction PROM stores correction information so that an 8-bit word from RIP 16 is converted to a new 8-bit word that is corrected based on the temperature of the printhead to adjust pulsewidth duration. The LCU signals the PROM as to the correction factor based on the temperature related data provided in reading the 65th driver current channels. Thus, adjustability of the printhead to provide for uniformity is advantageously provided in several ways namely adjustment of current through use of current regulation data signals (V_{REF} and/or R_{REF}) by using an image data bus during say an interframe to adjust a bias current $I_{CHIP\ BIAS}$ (FIGS. 6A, B, C and D) to the constant current driver circuits and by use of the adjustment to image data during production periods. In the embodiments of FIGS. 7-10 and 11-13, the adjustments of current are provided in a manner similar to that described for the embodiment of FIGS. 1-6. Control logic on each driver chip receives a signal indicating that it is to latch current regulation data into say an 8-bit latch which is used for local

bias; i.e., this signal is particular to this driver chip. The driver chip may also receive a global bias signal V_{REF} that is received commonly by all driver chips. This signal V_{REF} may be analog or digital.

A further improvement is provided in the embodiment of FIGS. 11-13 demonstrating that data for providing further fine tune adjustment of current can be provided during each line of recording.

The described driver circuit retains the desirable feature of two-way addressability described in the prior art. That is, provision is made for digitally addressing each chip to correct for differences in light output by LED's driven by one chip versus those driven by another chip on the same printhead. These differences can arise due to processing condition differences arising during manufacture of the driver chips and for their respective driven LED's as well as nonuniformities arising from temperature differences. A second provision for digital addressability is retained to provide for global changes due to aging. By providing both addressable portions on each driver chip problems associated with noise are minimized. In addition, providing a non-digitally controlled transistor on each addressability portion simplifies calibration and allows for more accuracy in control of uniformity.

The provision of a temperature compensated current source 172 advantageously and promptly increases current on a real-time basis by altering current to a series of digitally addressable transistors. This provides for instantaneous changes in current levels to the LED's for providing at least some correction for temperature excursions and thus provides an additional device for complementing the

main temperature control which is provided through selection of transistors in one series of digitally addressable transistors.

A printhead has also been described which provides efficient use of the electrical lines provided thereon. Multibit image data is effectively latched into appropriate registers in accordance with a token bit. Current regulation is effectively controlled using digitally addressed current regulation. Data for the image signals and current regulations are carried over the same lines, thereby reducing the need for additional lines. This reduces the number of bonding pads and connections required to be made in fabricating the printhead.

While an embodiment of the invention has been described employing a single data line D15 (for say the odd-numbered driver chips) for carrying current regulating signals, it will be appreciated that multiple lines of the image data bus may be used for carrying current regulation data in parallel.

Thus, there has also been described an LED printhead having an improved driving circuit for generating driving current to the recording elements that provides for turn-on times that are relatively independent of the number of recording elements turned on and further provides for constancy in light output by making the driving current insulated from changes in the driver voltage. Modifications to the circuit may, of course, be made. For example, transistors Q425 and Q423 are used effectively as resistors and may be also eliminated.

While the preferred embodiment has been described in terms of MOSFET transistors that have their respective gates controlled, other devices providing an equivalent function such as bipolar or other gate

controlled devices are also contemplated. Where bipolar transistors are used, transistor geometry or doping levels to respective transistors may be modified to provide the current scaling characteristics described herein.

Although the invention has been described with respect to embodiment wherein an extra current driver channel is provided in each driver chip, the invention in its broader aspect contemplates that the current may be sensed in the driver channels of the recording elements.

The invention has been described in detail with particular reference to preferred embodiments thereof, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention.

Claims:

1. A non-impact printer apparatus comprising:

a recording head having a plurality of recording elements for recording on a recording medium;

driving means including a plurality of current driving channels for selectively driving said plurality of recording elements in accordance with respective image data signals; said driving means being characterized by an extra current driving channel not associated with a recording element for generating a current related to that sent to said recording elements; and

means for monitoring a parameter related to said current in said extra channel.

2. The printer apparatus of Claim 1 and including means for shutting down current to the recording elements in response to sensing of a current level that is inappropriate for recording.

3. The printer apparatus of Claim 1 and including means for adjusting respective currents in a plurality of current driving channels in response to the parameter related to current sensed in the extra channel.

4. The printer apparatus of Claims 1, 2 or 3 and wherein the driving means comprises a current mirror having a master circuit and the current driving channels are slaves of said master circuit.

5. The printer apparatus of Claim 4 and including a plurality of digitally addressable transistors for changing a level of current in said master circuit.

6. The printer apparatus of Claims 1, 2 or 3 and including image data bus means for carrying image data signals;

said driving means including respective data register means associated with each recording element for storing said image data signals;

means for commonly connecting said data bus means to plural data register means associated with respective plural recording elements;

means for generating a token bit signal;

means including a multistage token bit shift register means having a plurality of respective stages for outputting sequentially at respective stages the token bit signal and for sequentially selecting a respective data register means for accepting image data signals.

7. The printer apparatus of Claim 6 and including a plurality of driver chips, each driver chip includes one of said driving means, and said apparatus further including means responsive to the token bit signal to select which driver chip's extra current driving channel current is being monitored.

8. The printer apparatus of Claim 7 and wherein

the recording elements are arranged in a row;

a respective multistage token bit shift register means is associated with each driver chip;

the driver chips are arranged in a series of two rows of driver chips with the row of recording elements located between said two rows;

means for shifting respective token bit signals simultaneously down the token bit shift register means of respective rows of driver chips; and

means responsive to lodging a token bit signal in a particular stage of a multistage register associated with a respective driver chip for controlling monitoring of current in an extra current driving channel of said driver chip.

9. The printer apparatus of Claim 8 and wherein the recording elements are light-emitting diodes.

10. The printer apparatus of Claim 8 and including means for adjusting image data signals in

response to current sensed in an extra current driving channel.

11. The printer apparatus of Claim 1 and including means for adjusting image data signals to the recording elements in response to the parameter related to said current sensed in the extra channel.

12. The printer apparatus of Claim 1 or 11 and including means for adjusting current for driving said plurality of recording elements in response to a level of a parameter related to current sensed in the extra channel.

13. The printer apparatus of Claim 12 and wherein the driving means comprises a current mirror having a master circuit and the current driving channels are slaves of said master circuit.

14. The printer apparatus of Claim 13 and including a plurality of digitally addressable transistors for changing a level of current in said master circuit.

15. The printer apparatus of Claims 12, 13 or 14 and including image data bus means for carrying image data signals;

a plurality of image data register means for storing said image data signals, a respective image data register means being associated respectively with each recording element for storing respective image data signals for enabling a respective recording element for recording;

means commonly connecting said data bus means to said plurality of image data register means;

means for generating a token bit signal;

a multistage token bit shift register means for outputting sequentially at respective stages the token bit signal for sequentially selecting a respective image data register means for accepting image data signals.

16. The printer apparatus of Claim 15 and including a plurality of driver chips, each driver chip includes one of said driving means and said apparatus further includes means responsive to the token bit signal to select which driver chip's extra current driving channel parameter related to current is being sensed.

17. The printer apparatus of Claim 16 and wherein the recording elements are arranged in a row;

a respective multistage token bit shift register means is associated with each driver chip;

the driver chips are arranged in a series of two rows of driver chips with the row of recording elements located between said two rows;

means for shifting respective token bit signals simultaneously down the token bit shift register means of respective rows of driver chips; and

means responsive to the lodging of a token bit signal in a particular stage of a multistage register associated with a respective driver chip for controlling monitoring of a parameter related to current in an extra current driving channel of said driver chip.

18. The printer apparatus of Claim 17 and wherein the recording elements are light-emitting diodes.

19. The printer apparatus of Claim 1 and including a plurality of driver chips, each driver chip includes one of said driving means , said apparatus further includes a plurality of token bit registers wherein at least one of said registers is associated with each driver chip; means for generating a token bit signal; and means responsive to the token bit signal to select which driver chip's extra current driving channel parameter related to current is being monitored.

20. The printer apparatus of Claim 19 and wherein a token bit shift register means is associated with each driver chip;

the driver chips are located at opposite sides of an array of recording elements;

means for shifting the token bit simultaneously down the token bit shift register means of opposing driver chips and means responsive to the position of the token bit in a particular stage controls the monitoring of the parameter related to current from one of the opposing driver chips containing a token bit.

21. The printer apparatus of Claim 7 and including means for generating current regulation data on at least one line of said image data bus means for regulating a level of current for driving recording elements and means for generating a token bit signal for selecting which driver chip is to receive the current regulation data.

22. The printer apparatus of Claim 21 and including means for generating current regulating signals during recording by said recording elements and means for disabling said data register means from accepting current regulating signals as image data signals.

23. The printer apparatus of Claim 1, the apparatus including a plurality of driver chips, each driver chip including said driving means, token bit shift register means, means for shifting a token bit down the token bit shift register means, and said monitoring means is responsive to the position of the token bit for controlling the monitoring of the parameter related to current in a particular one of the driver chips.

24. The printer apparatus of Claim 23 and wherein the recording elements are light-emitting diodes.

25. The printer apparatus of Claim 23 and including means for adjusting image data signals in response to the parameter related to current sensed in an extra current driving channel.

26. The printer apparatus of Claims 1, 3-6, 11-24 or 25 and wherein the parameter related to current is current.

27. A non-impact printer apparatus comprising:

a recording head having a plurality of recording elements for recording on a recording medium;

driving means for selectively driving said plurality of recording elements in accordance with respective image data signals; and characterized by

means including data bus means for carrying on said data bus means multibit image data signals determining a recording duration for a recording element and for carrying on one line of said data bus means also used for carrying image data signals, a multibit digital signal used for regulating a level of current to said recording element;

28. The printer apparatus of Claim 27 and said driving means including a plurality of data register means with respective data register means being associated with each recording element for storing said image data signals;

means for commonly connecting said data bus means to said plurality of data register means;

means for generating a token bit signal;

a multistage shift register means for outputting sequentially at respective stages the token bit signal for sequentially selecting a respective data register means for accepting image data signals;

said driving means further including current regulating means for regulating a level of electrical current to each recording element, the current

regulating means including means for adjusting a level of electrical current to each recording element in response to the multibit digital signal used for regulating current.

29. The printer apparatus of Claim 28 and wherein the current regulating means includes first register means including a plurality of registers for storing a multibit digital signal related to a level of current control, second register means for storing and shifting a token bit signal and means responsive to a token bit signal in said second register means for latching in an appropriate register of said first register means a digital signal found on said data bus means.

30. A non-impact printer apparatus comprising:

a recording head having a plurality of recording elements for recording on a recording medium;

driving means for selectively driving said plurality of recording elements in accordance with respective image data signals;

said driving means including a plurality of data register means with respective data register means associated with each recording element for storing said image data signals;

data bus means for carrying image data signals;

means for commonly connecting said data bus means to said plurality of data register means;

means for generating a token bit signal;

a multistage shift register means for outputting sequentially at respective stages the token bit signal for sequentially selecting a respective data register means for accepting image data signals;

said driving means further including current regulating means for regulating a level of electrical current to each recording element, the current regulating means being characterized by

means for adjusting a level of electrical current to each recording element in response to a multibit digital signal; and

wherein the current regulating means further includes first register means including a plurality of registers for storing digital signals related to a level of current control, second register means for storing and shifting a token bit signal, and means responsive to a token bit signal in said second register means for latching in an appropriate register of said first register means the multibit digital signal.

31. A non-impact printer apparatus used for recording, comprising:

a plurality of groups of recording elements,

a plurality of integrated circuit driver chips for driving respective groups of recording elements;

a) first digitally addressable current-conducting means for selectively establishing a first bias voltage in response to a first multibit digital signal;

b) second digitally addressable current-conducting means responsive to the first bias voltage and to a second multibit digital signal for generating a bias current and establishing a second bias voltage;

c) means for selectively causing current to flow through recording elements selected for energization; and

d) current mirror driver means for regulating levels of currents through said selected recording elements, the level of current being related to said second bias voltage, and characterized by

wherein elements a), b), c) and d) are all on each of said driver chips.

32. The printer apparatus of Claim 31 and wherein each driver chip further includes a non-digitally addressable continuously operating current-conducting means cooperating with said first digitally addressable current-conducting means to establish an offset bias voltage level for said first bias voltage.

33. The printer apparatus of Claims 31 or 32 and wherein each driver chip further includes a non-digitally addressable continuously operating current-conducting means cooperating with said second digitally addressable current-conducting means to establish an offset bias current level for said bias current.

34. A non-impact printer apparatus comprising:

a series of point-like energizable radiation sources arranged in a row;

means providing data signals representing data to be printed;

logic means responsive to the data signals for determining which of the point-like radiation sources are to be selected for energization;

current driver means responsive to the logic means for providing electrical current to the radiation sources selected for energization, the current driver means including a master circuit including a first transistor for generating a reference current through said first transistor and a plurality of slave circuits for providing respective slave driver currents to the radiation sources selected for energization, means including (a) a plurality of individually selectively addressable current-conducting devices coupled to the master circuit, (b) first control means for selectively determining which of said plurality of devices are to

be current conducting, and characterized by (c) current source means responsive to increases in temperature on the printhead for providing increased current generated by said current source means, (d) adjustable bias means coupling said current source means to said first plurality of devices to increase respective levels of currents conducted by selected ones of said first plurality of devices and responsive thereto for generating an adjusted voltage bias signal, and (e) bias responsive means responsive to an adjustment in voltage bias for increasing the reference current in response to the increase in the temperature of the printhead.

35. The printer apparatus of Claim 33 and wherein the bias responsive means includes a second plurality of individually selectively addressable current-conducting devices including terminals connected to said adjustable bias means and responsive to said adjusted voltage bias signal for generating plural currents by selected ones of said second plurality of devices, the second plurality of devices being in series with said first transistor, and second control means for selectively determining which of said second plurality of devices are to be current conducting.

36. The printer apparatus of Claim 35 and including a transistor coupled in series to said current source means that is not selectively addressable for establishing a minimum offset level for the adjusted voltage bias signal and another transistor that is not selectively addressable and is in parallel with said second plurality of devices for establishing a minimum offset reference current in response to a minimum offset level for the adjusted voltage bias signal.

37. A non-impact printer apparatus, comprising:

a plurality of energizable recording elements;

driving means for energizing said recording elements, said driving means including current mirror means having a master circuit means for generating a reference current and a plurality of slave circuit means for providing respective driver currents to the recording elements selected for energization;

each slave circuit means including:

(a) transistor switching means in series with a respective recording lement and switchable from one state to another in response to a signal and having a control electrode for controlling driver current to its respective recording element in response to the signal;

(b) enabling means operating upon the control electrode for switching the switching means to allow driver current to be selectively provided to a respective recording element for a predetermined period of time; and characterized by

(c) each of said slave circuit means further including its own additional slave circuit means for providing a current path for facilitating changing of the signal at the control electrode from one voltage level to another.

38. The printer apparatus of Claim 37 and including second transistor means in series with said transistor switching means for generating a first voltage signal that is input to one electrode of said transistor switching means, said first voltage signal varying with variations in said reference voltage; and

said additional slave circuit means generating a second voltage signal at a control electrode of the transistor switching means that varies with the reference voltage.

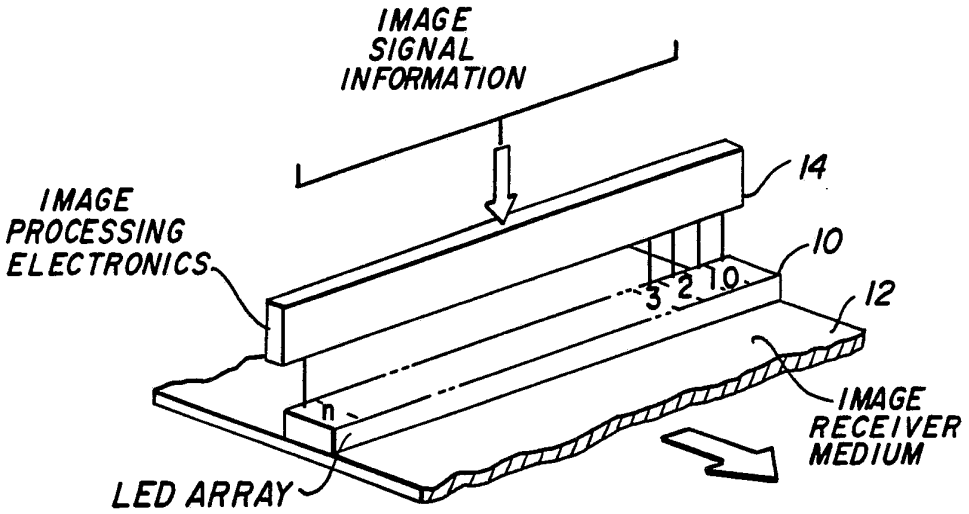


FIG. 1
(PRIOR ART)

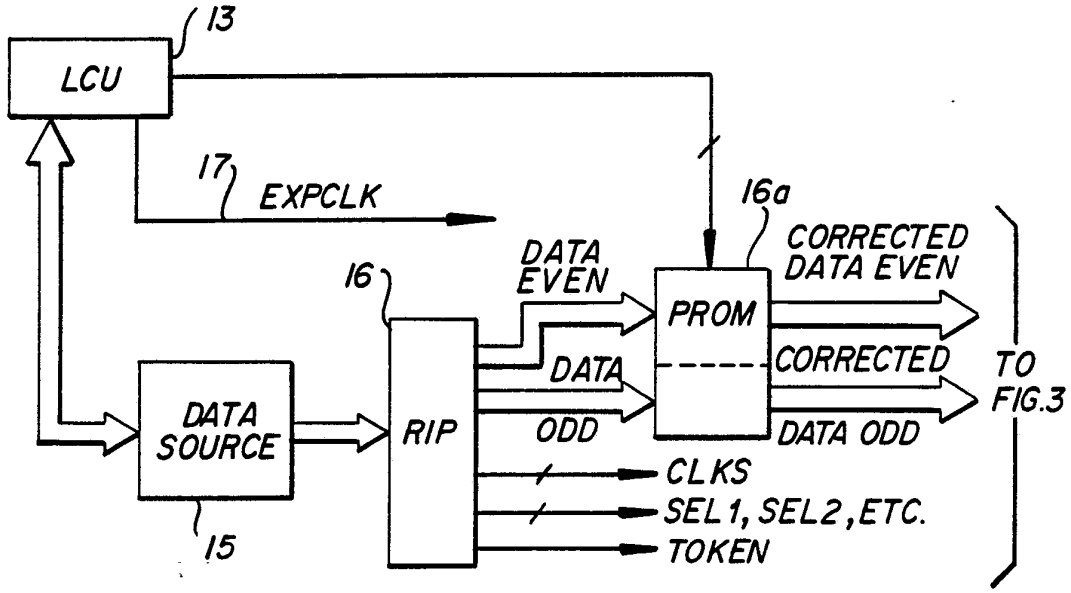


FIG. 2

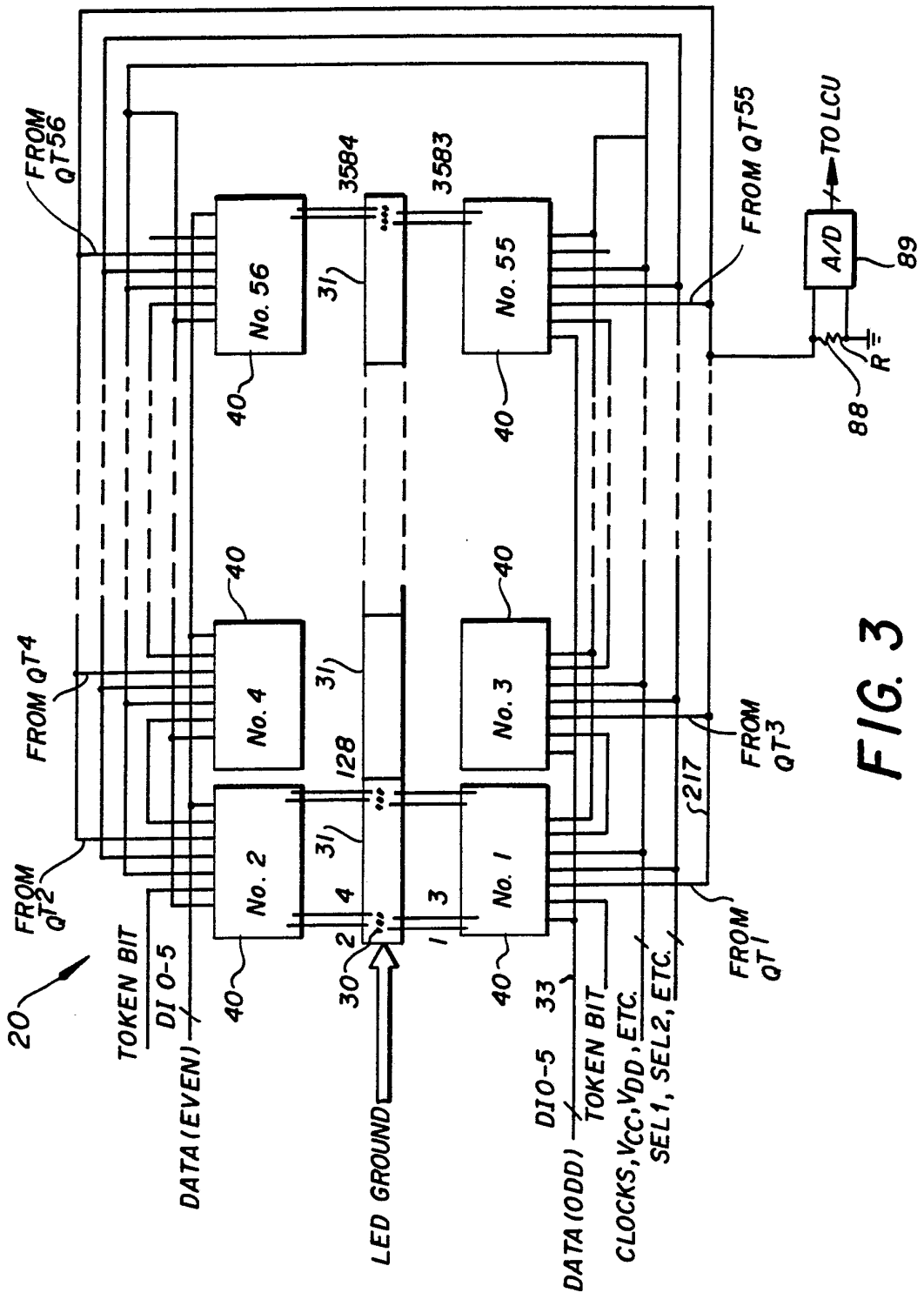
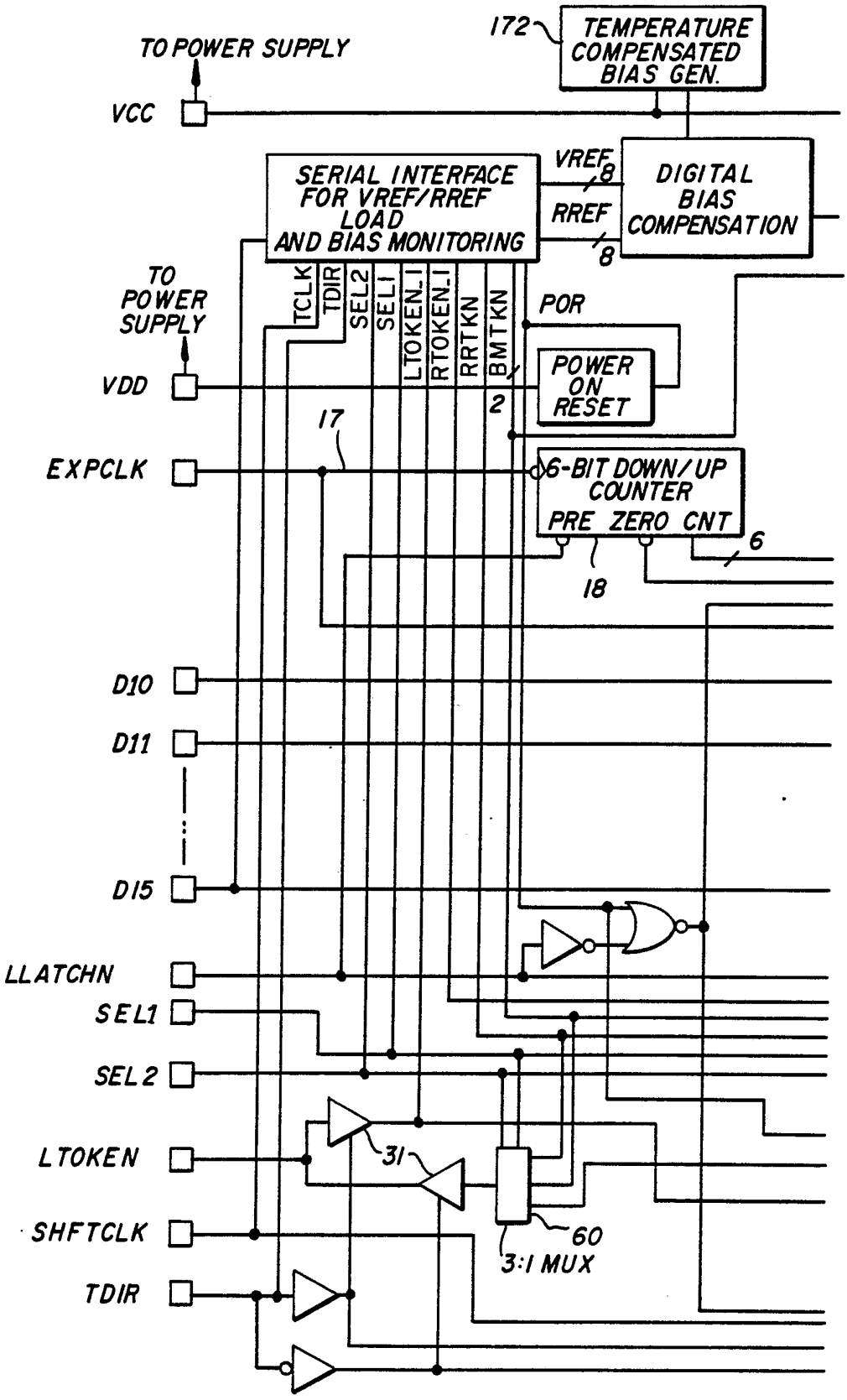

FROM QT56
3584
3583
No. 56
No. 55
31
40
FROM QT55
A/D
TO LCU
89
88
R
FROM QT4
No. 4
No. 3
128
FROM QT3
217
FROM QT2
No. 2
No. 1
4
3
2
1
30
33
20
TOKEN BIT
DI 0-5
DATA (EVEN)
LED GROUND
DATA (ODD)
DI0-5
TOKEN BIT
CLOCKS, V_{CC}, V_{DD}, ETC.
SEL1, SEL2, ETC.
FROM QT1

FIG. 3

FIG. 4a


TO POWER SUPPLY
VCC
172
TEMPERATURE COMPENSATED BIAS GEN.
SERIAL INTERFACE FOR VREF/RREF LOAD AND BIAS MONITORING
VREF
8
RREF
8
DIGITAL BIAS COMPENSATION
TO POWER SUPPLY
VDD
TCLK
TDIR
SEL2
SEL1
LTOKEN_I
RTOKEN_I
RRTKN
BMTKN
2
POR
POWER ON RESET
17
EXPCLK
6-BIT DOWN/UP COUNTER
PRE ZERO CNT
6
18
D10
D11
D15
LLATCHN
SEL1
SEL2
LTOKEN
31
SHFTCLK
60
3:1 MUX
TDIR

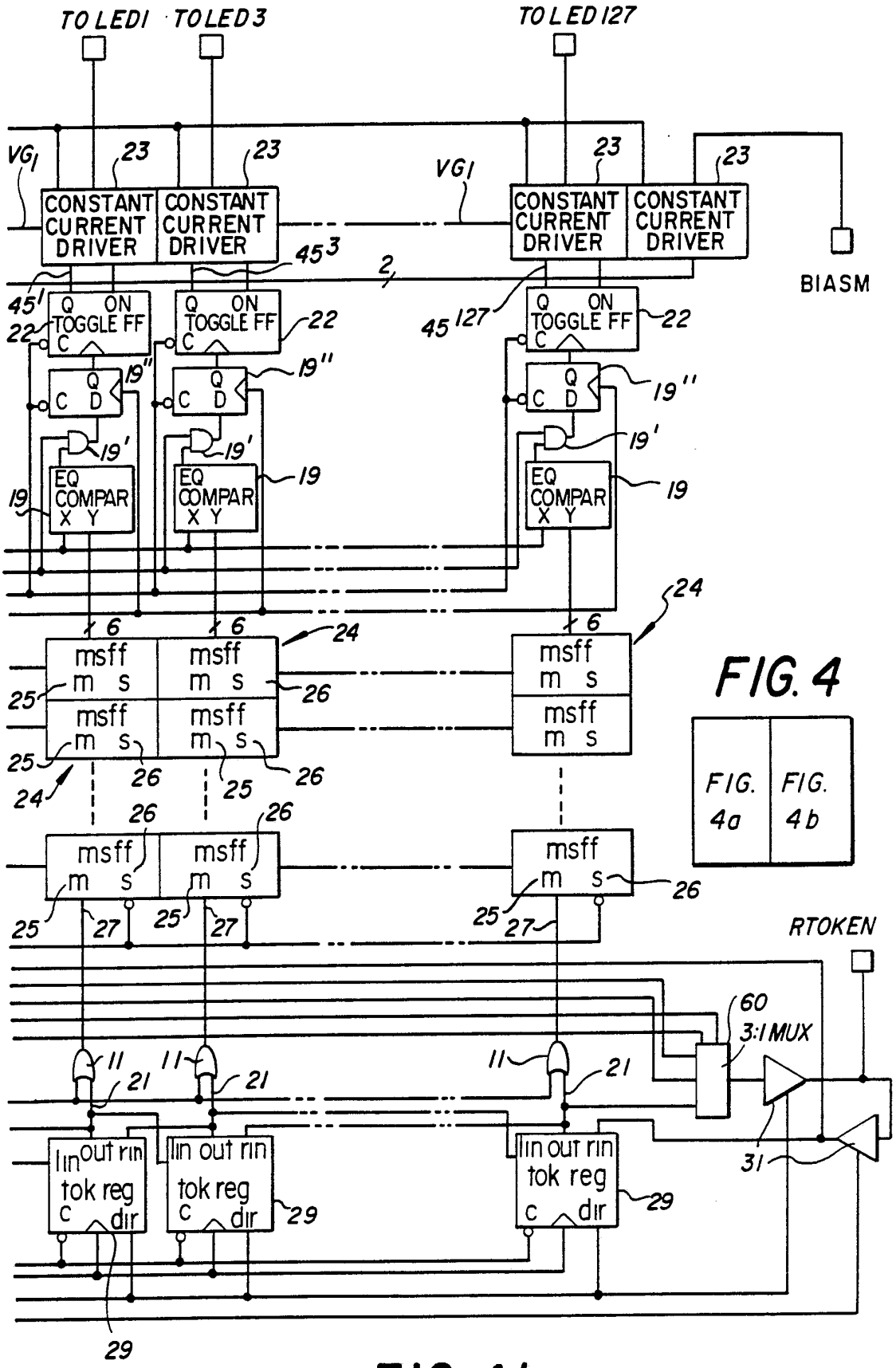


FIG. 4

FIG. 4a | FIG. 4b

FIG. 4b

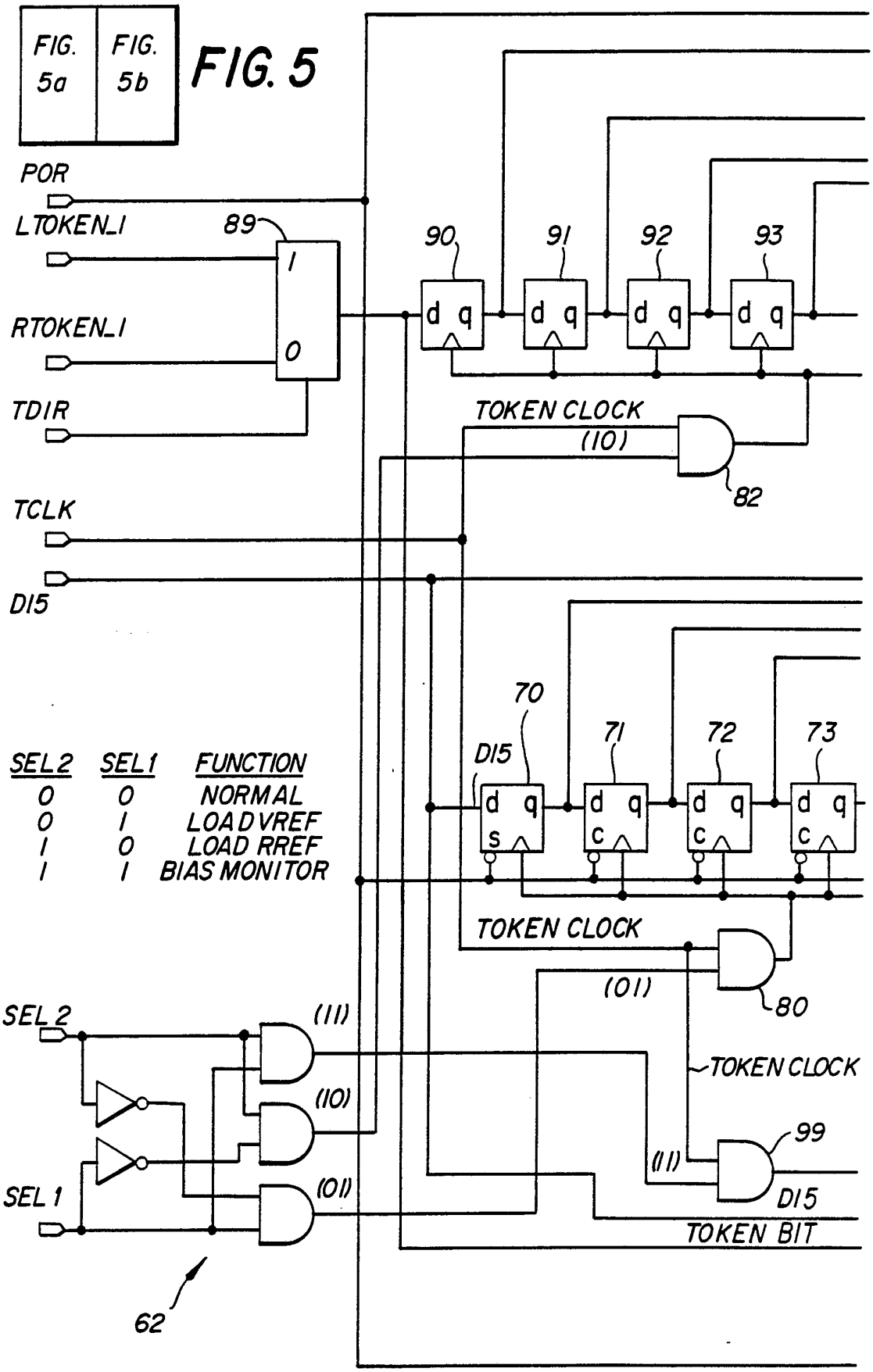
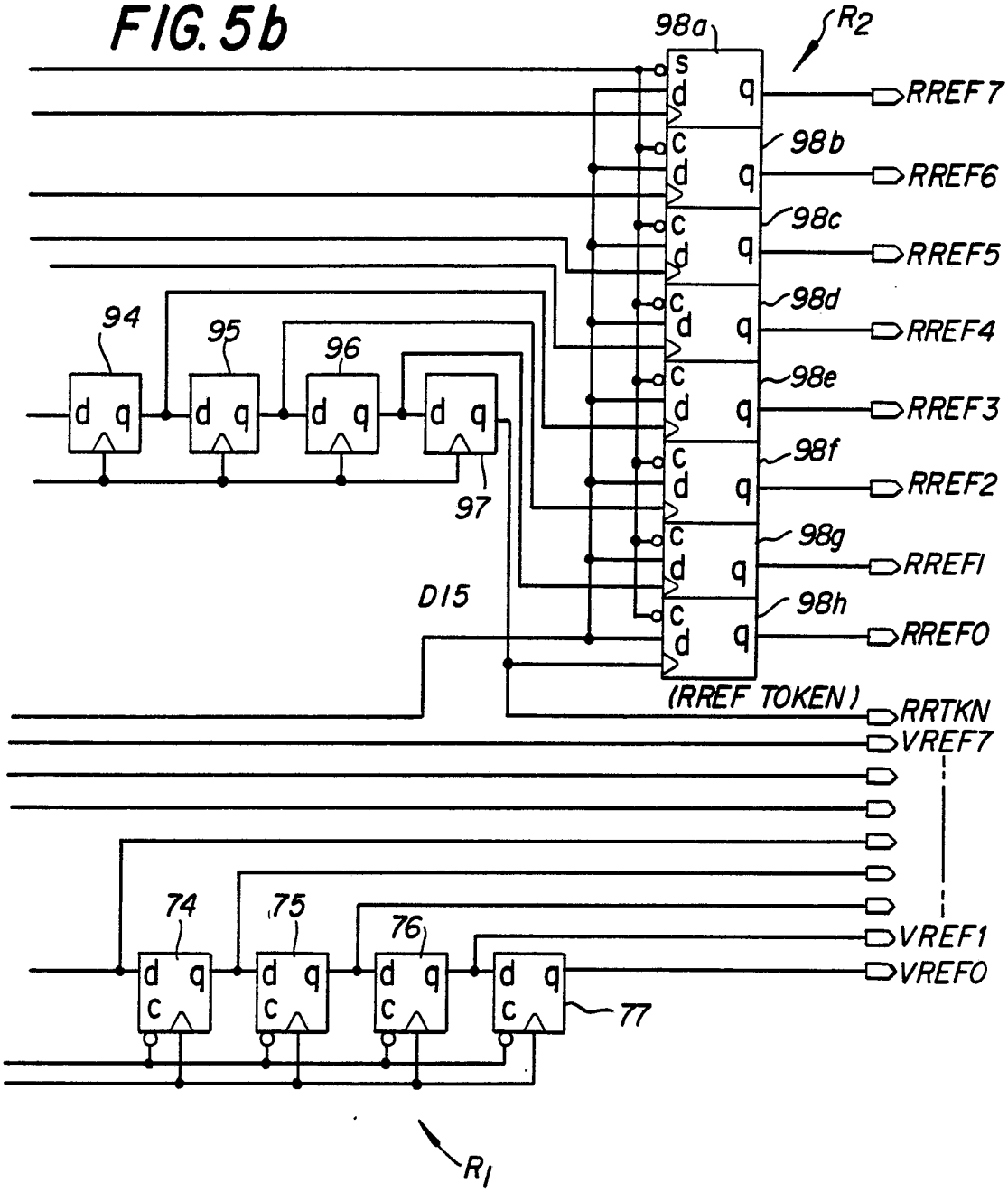
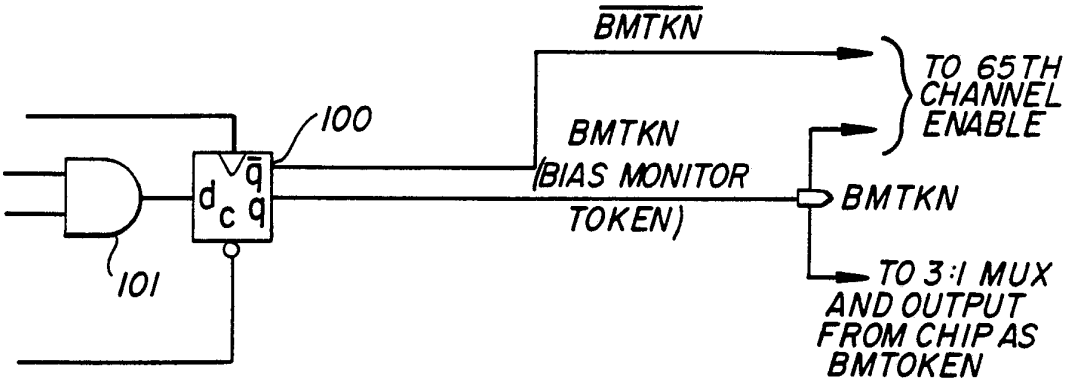


FIG. 5a
FIG. 5b
POR
LTOKEN_I
RTOKEN_I
TDIR
TCLK
DI5
89
1
0
90
91
92
93
d q
TOKEN CLOCK
(10)
82
70
71
72
73
DI5
d q s
d q c
SEL2 SEL1 FUNCTION
0 0 NORMAL
0 1 LOAD VREF
1 0 LOAD RREF
1 1 BIAS MONITOR
TOKEN CLOCK
(01)
80
SEL 2
SEL 1
(11)
(10)
(01)
TOKEN CLOCK
99
(11)
DI5
TOKEN BIT
62

FIG. 5a

FIG. 5b


98a
R2
RREF7
98b
RREF6
98c
RREF5
98d
RREF4
98e
RREF3
98f
RREF2
98g
RREFI
98h
RREFO
94
95
96
97
D15
(RREF TOKEN)
RRTKN
VREF7
VREF1
VREFO
74
75
76
77
R1


BMTKN
TO 65TH CHANNEL ENABLE
100
BMTKN (BIAS MONITOR TOKEN)
BMTKN
101
TO 3:1 MUX AND OUTPUT FROM CHIP AS BMTOKEN

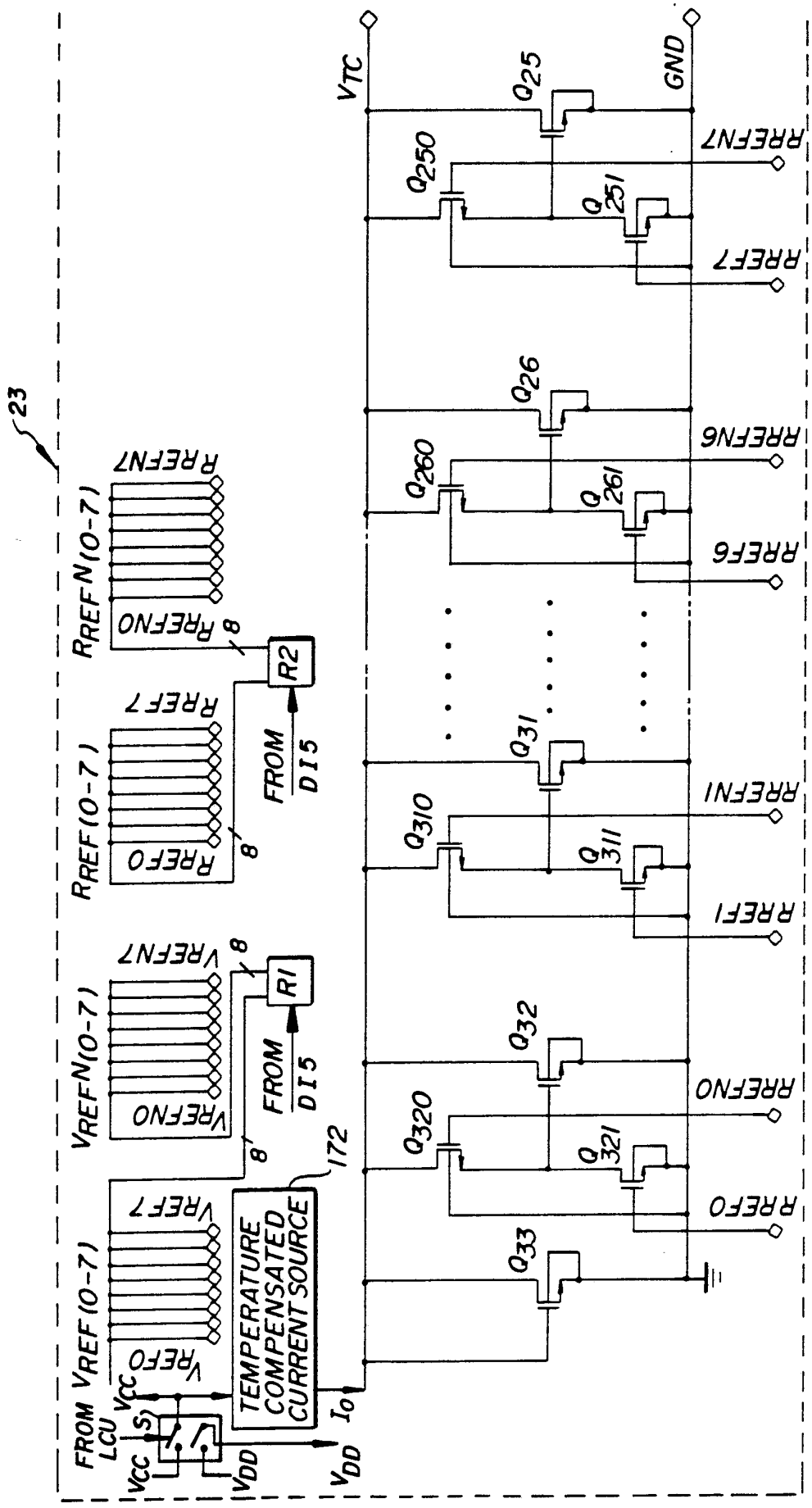

23
VTC
GND
Q25
Q250
Q251
RREFN7
RREF7
Q26
Q260
Q261
RREFN6
RREF6
Q31
Q310
Q311
RREFN1
RREF1
Q32
Q320
Q321
RREFN0
RREF0
Q33
RREFN7
RREFN(0-7)
RREFN0
8
R2
RREF7
RREF(0-7)
RREF0
FROM DI5
VREFN7
VREFN(0-7)
VREFN0
R1
VREF7
VREF(0-7)
VREF0
172
TEMPERATURE COMPENSATED CURRENT SOURCE
FROM LCU
VCC
S
VDD
Io

FIG. 6A

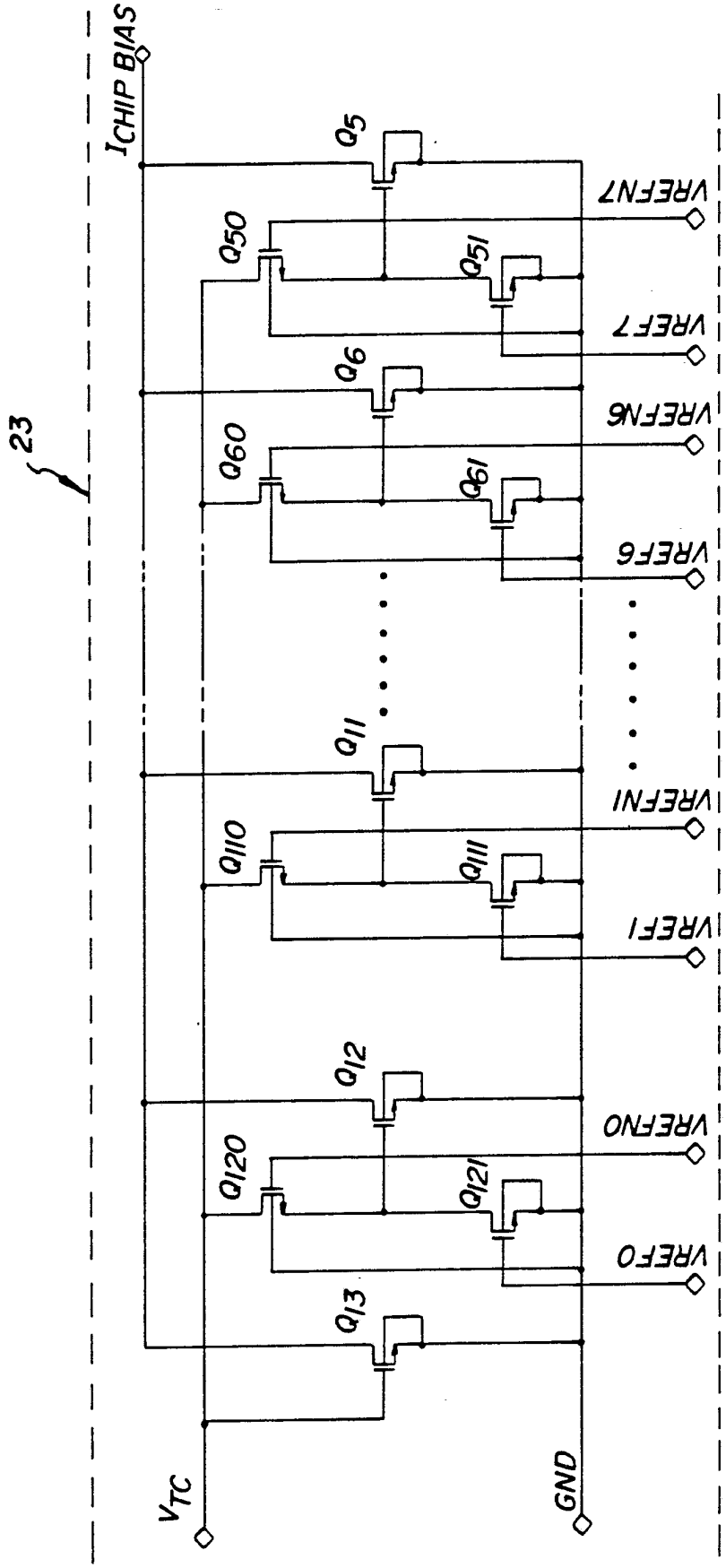

23
$I_{CHIP\ BIAS}$
Q_5
Q_{50}
Q_{51}
Q_6
Q_{60}
Q_{61}
Q_{11}
Q_{110}
Q_{111}
Q_{12}
Q_{120}
Q_{121}
Q_{13}
V_{TC}
GND
VREFN7
VREF7
VREFN6
VREF6
VREFN1
VREF1
VREFN0
VREF0

FIG. 6B

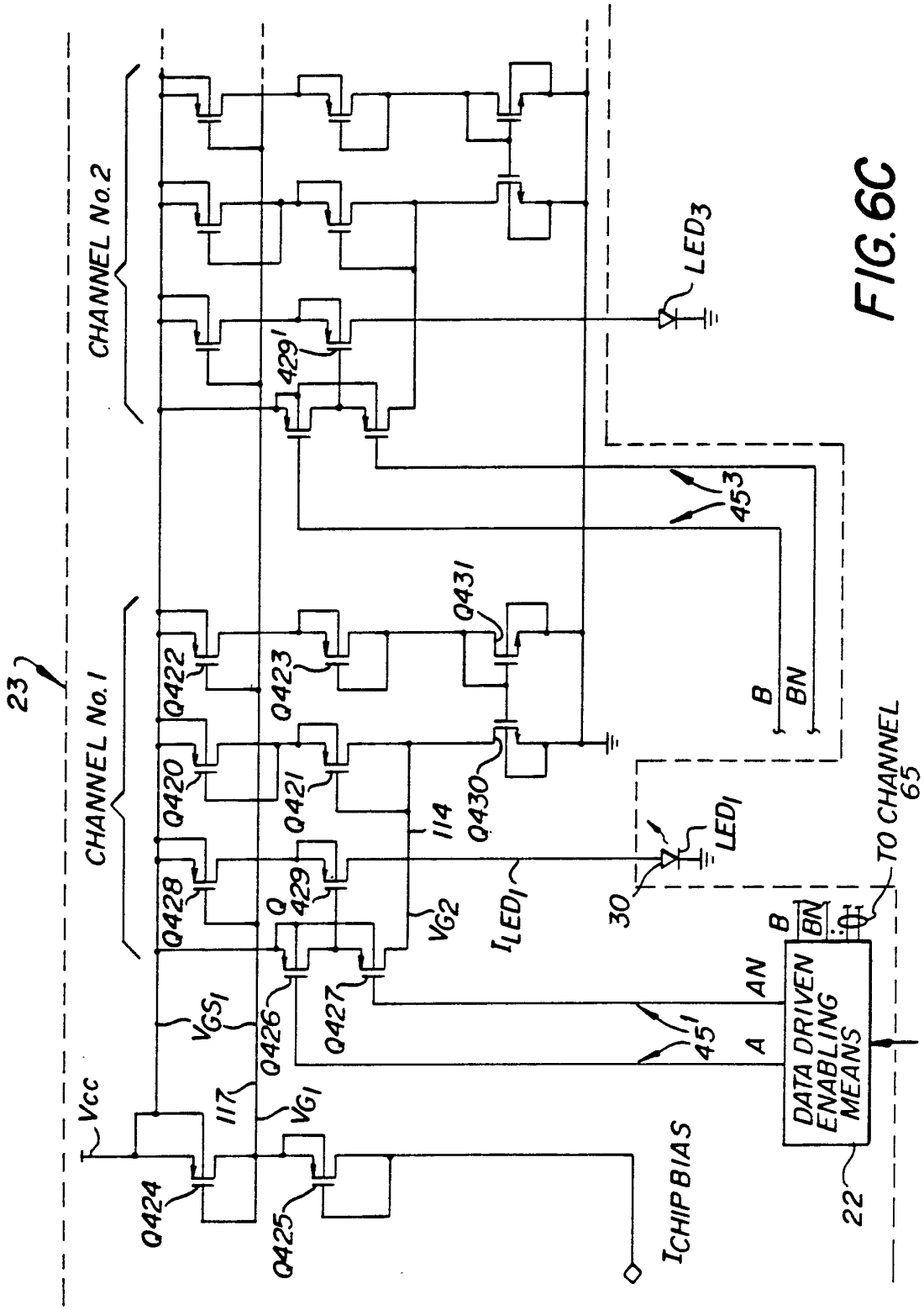

23
CHANNEL No.1
CHANNEL No.2
Vcc
Q424
Q425
Q426
Q427
Q428
Q429
Q420
Q421
Q422
Q423
Q430
Q431
429'
117
VG1
VGS1
VG2
114
ILED1
ICHIP BIAS
LED1
LED3
30
45'
453
B
BN
AN
A
DATA DRIVEN ENABLING MEANS
22
TO CHANNEL 65

FIG. 6C

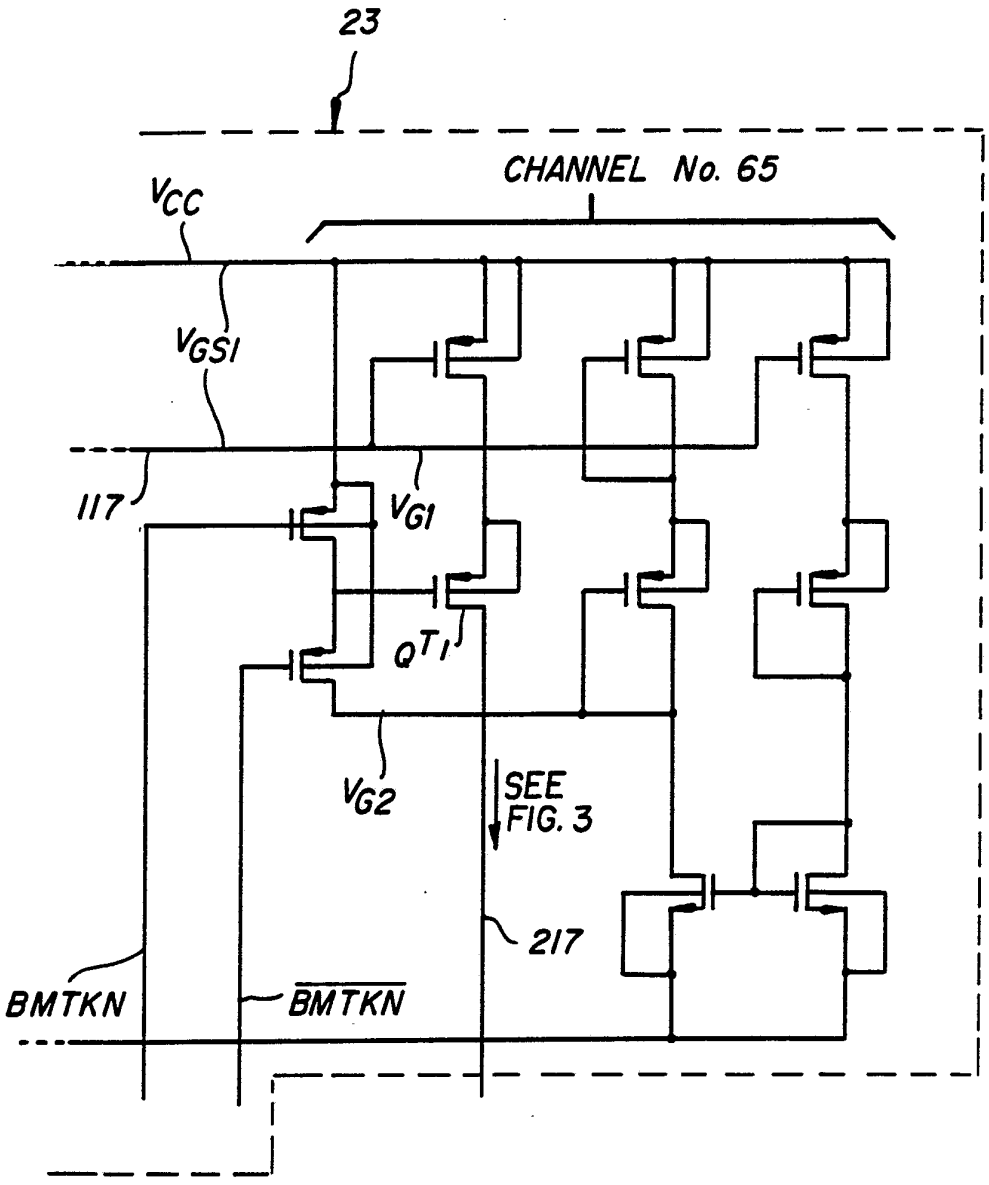

23
CHANNEL No. 65
V_{CC}
V_{GS1}
117
V_{G1}
Q^{T1}
V_{G2}
SEE FIG. 3
217
BMTKN
$\overline{BMTKN}$

FIG. 6D

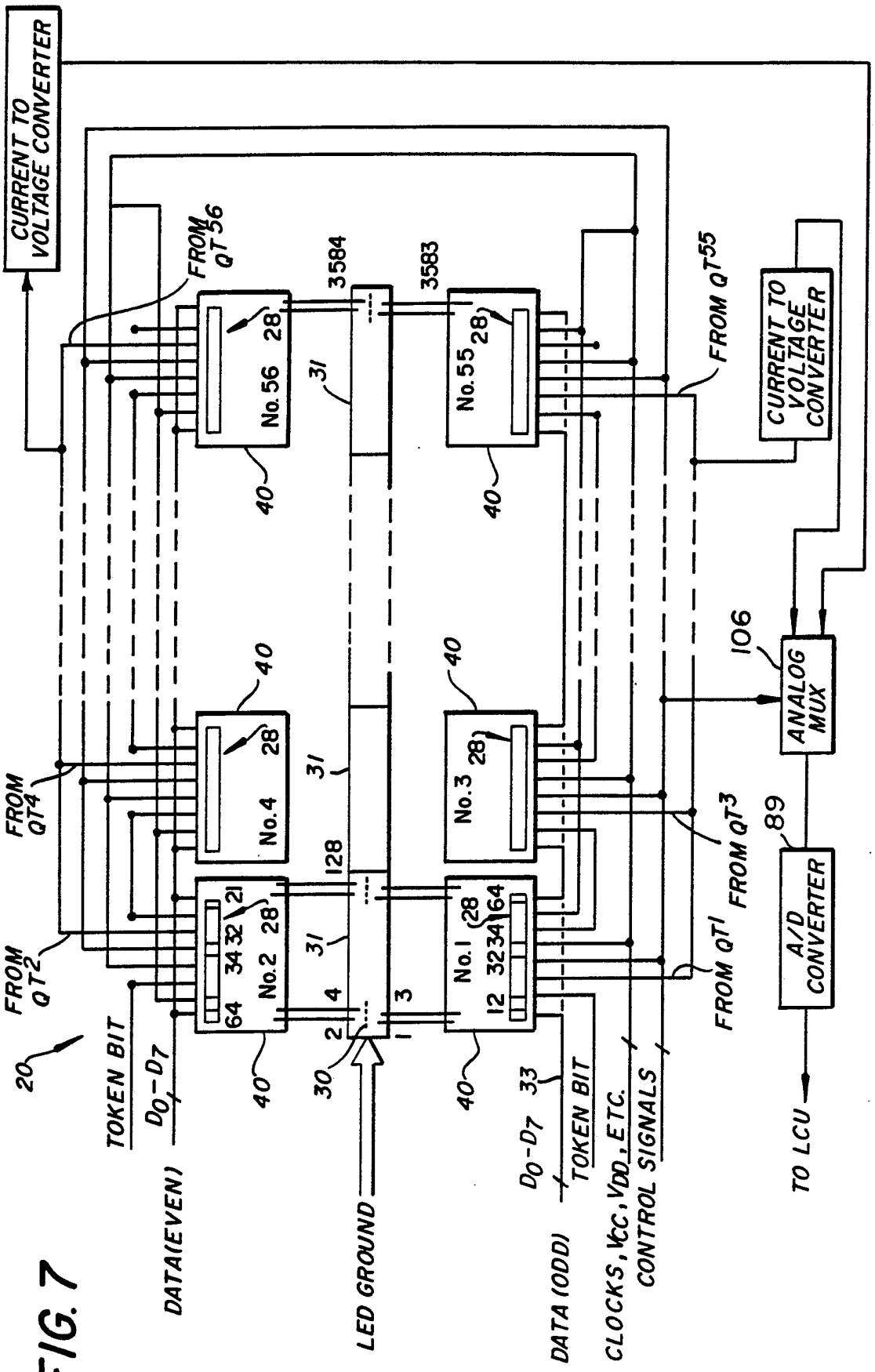
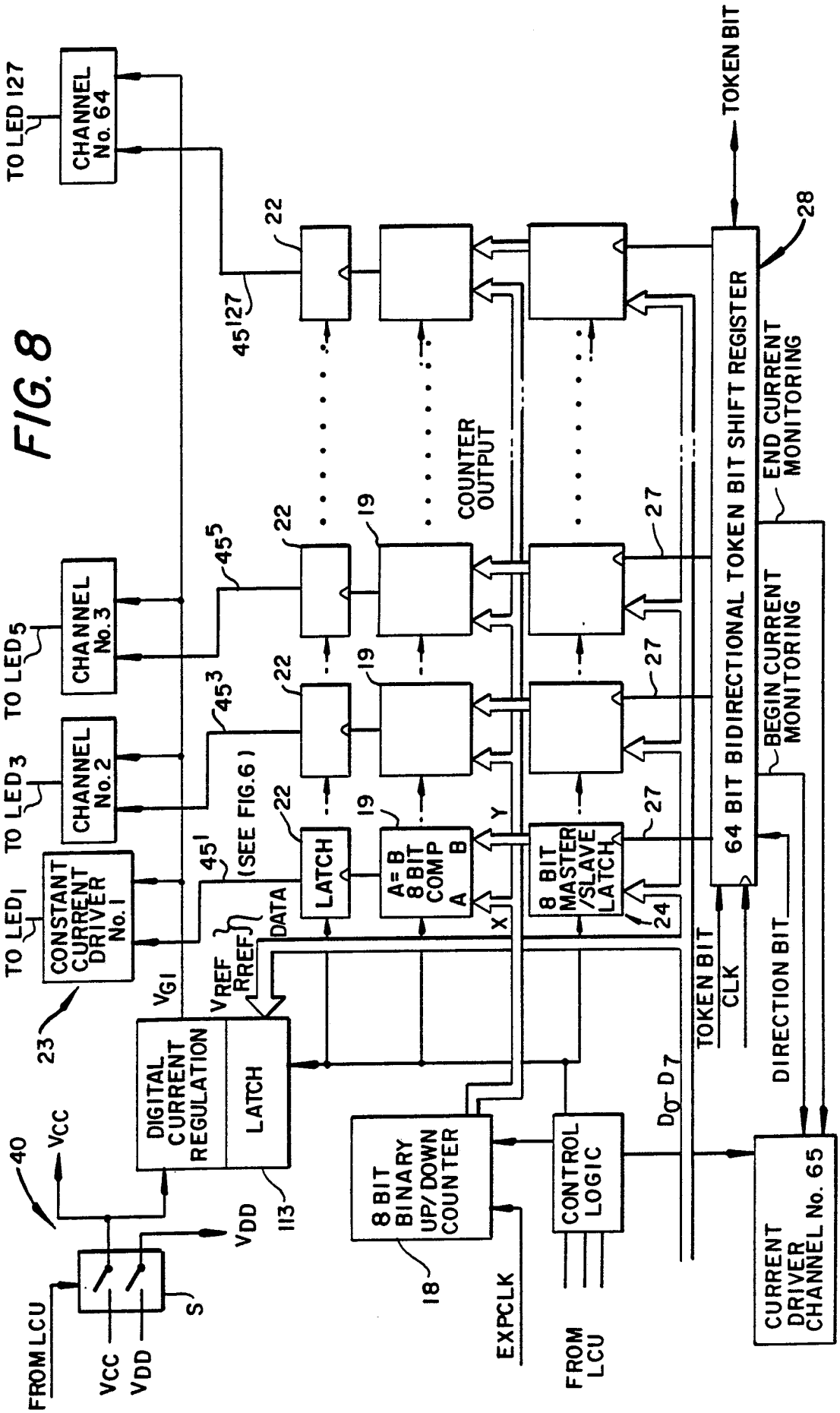

CURRENT TO VOLTAGE CONVERTER
FROM QT56
3584
3583
No.56
No.55
28
31
40
FROM QT55
CURRENT TO VOLTAGE CONVERTER
106
ANALOG MUX
FROM QT4
No.4
No.3
128
FROM QT3
89
A/D CONVERTER
FROM QT2
No.2
No.1
64
34
32
21
12
3234
4
3
2
1
30
20
FROM QT1
TO LCU
TOKEN BIT
D0-D7
DATA(EVEN)
LED GROUND
33
DATA (ODD)
CLOCKS, VCC, VDD, ETC.
CONTROL SIGNALS

FIG. 7

FIG. 8


TO LED 127
CHANNEL No. 64
TOKEN BIT
28
45 127
22
COUNTER OUTPUT
END CURRENT MONITORING
TO LED 5
CHANNEL No. 3
45 5
19
27
BEGIN CURRENT MONITORING
TO LED 3
CHANNEL No. 2
45 3
(SEE FIG. 6)
64 BIT BIDIRECTIONAL TOKEN BIT SHIFT REGISTER
TO LED 1
CONSTANT CURRENT DRIVER No. 1
45 1
LATCH
A=B 8 BIT COMP
8 BIT MASTER /SLAVE LATCH
24
DATA
X
Y
VREF
RREF
VGI
23
DIGITAL CURRENT REGULATION
LATCH
113
TOKEN BIT
CLK
DIRECTION BIT
40
VCC
VDD
D0-D7
8 BIT BINARY UP/DOWN COUNTER
18
CONTROL LOGIC
EXPCLK
FROM LCU
S
CURRENT DRIVER CHANNEL No. 65

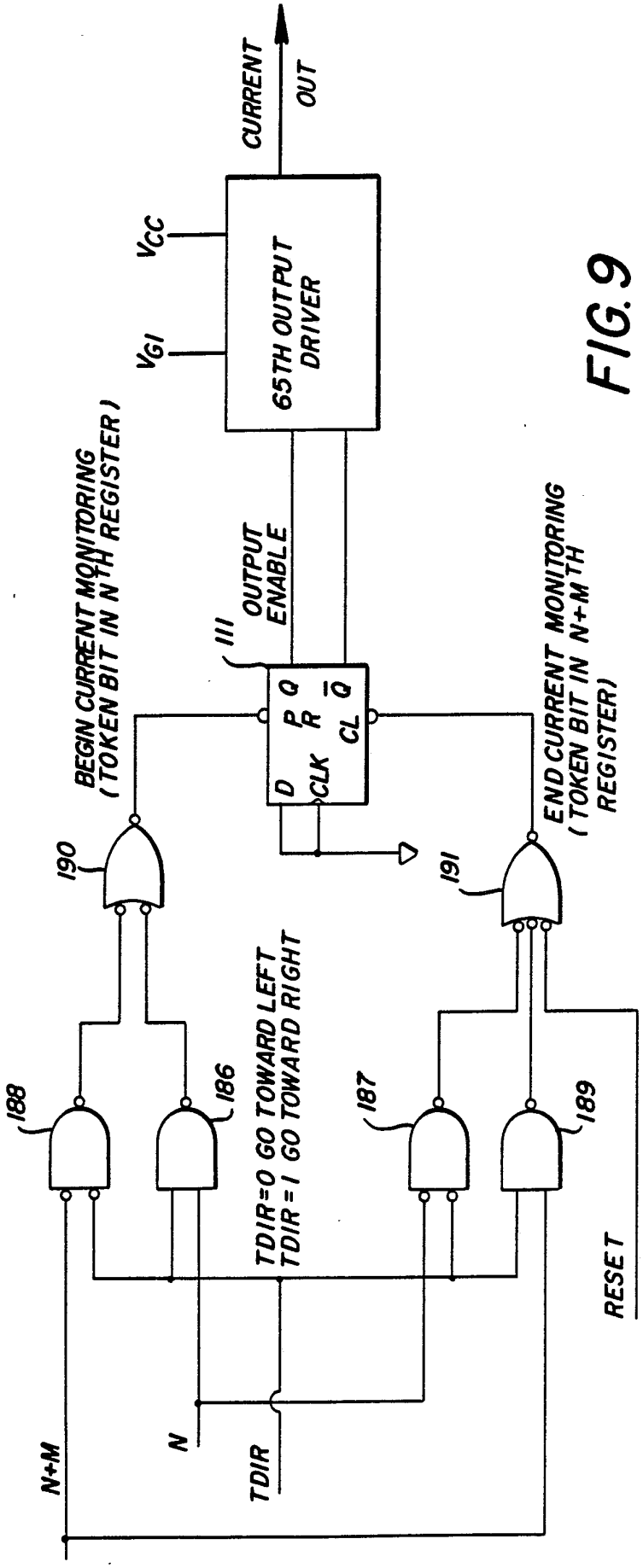

CURRENT OUT
65TH OUTPUT DRIVER
V_{CC}
V_{GI}
OUTPUT ENABLE
111
D
CLK
R
CL
Q
$\bar{Q}$
BEGIN CURRENT MONITORING (TOKEN BIT IN NTH REGISTER)
END CURRENT MONITORING (TOKEN BIT IN N+MTH REGISTER)
190
191
188
186
187
189
TDIR=0 GO TOWARD LEFT
TDIR=1 GO TOWARD RIGHT
N+M
N
TDIR
RESET

FIG. 9

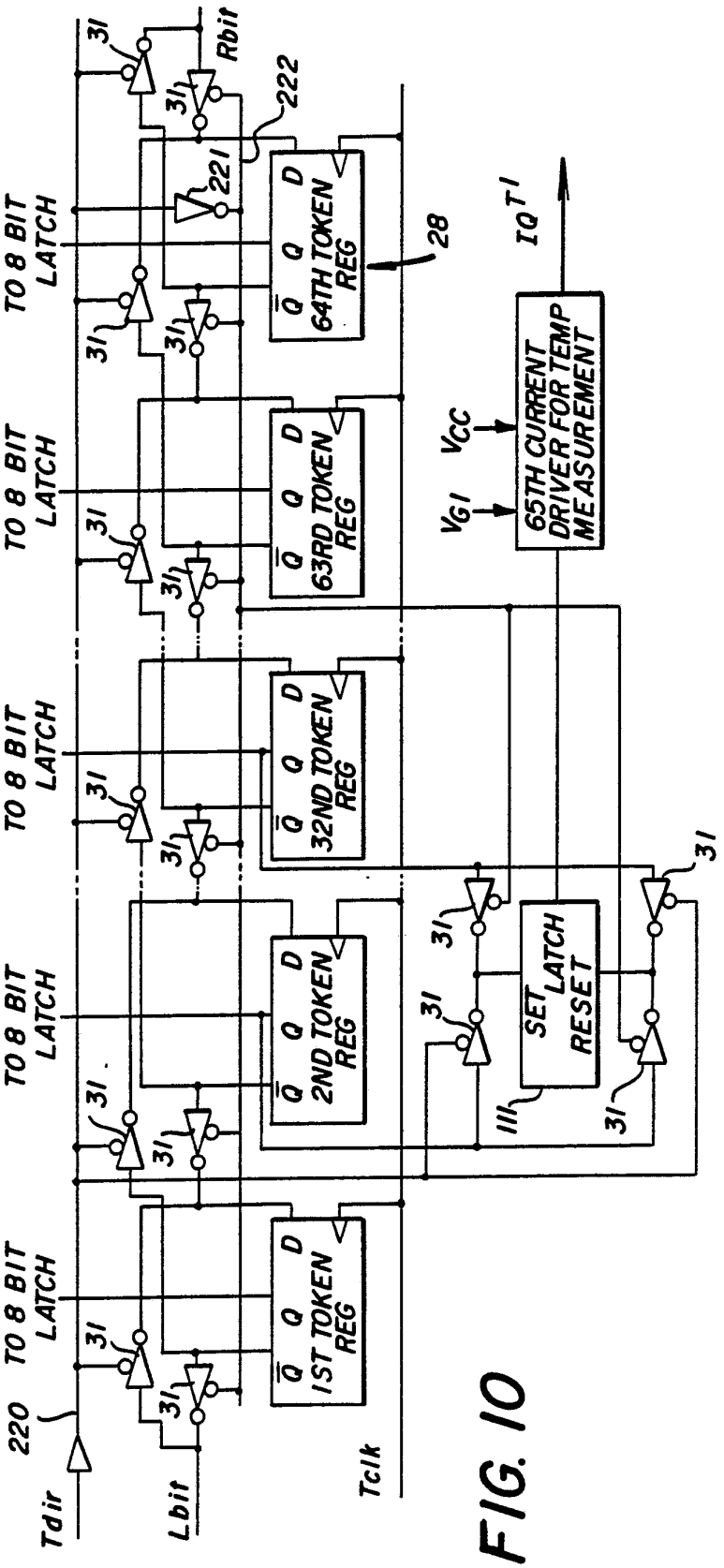


FIG. 10

TDir	LD/RUN	
L	L	LOADING Rref DATA FROM RIGHT TO LEFT
L	H	LOADING IMAGE DATA FROM RIGHT TO LEFT
H	L	LOADING Rref DATA FROM LEFT TO RIGHT
H	H	LOADING IMAGE DATA FROM LEFT TO RIGHT

FIG. 13

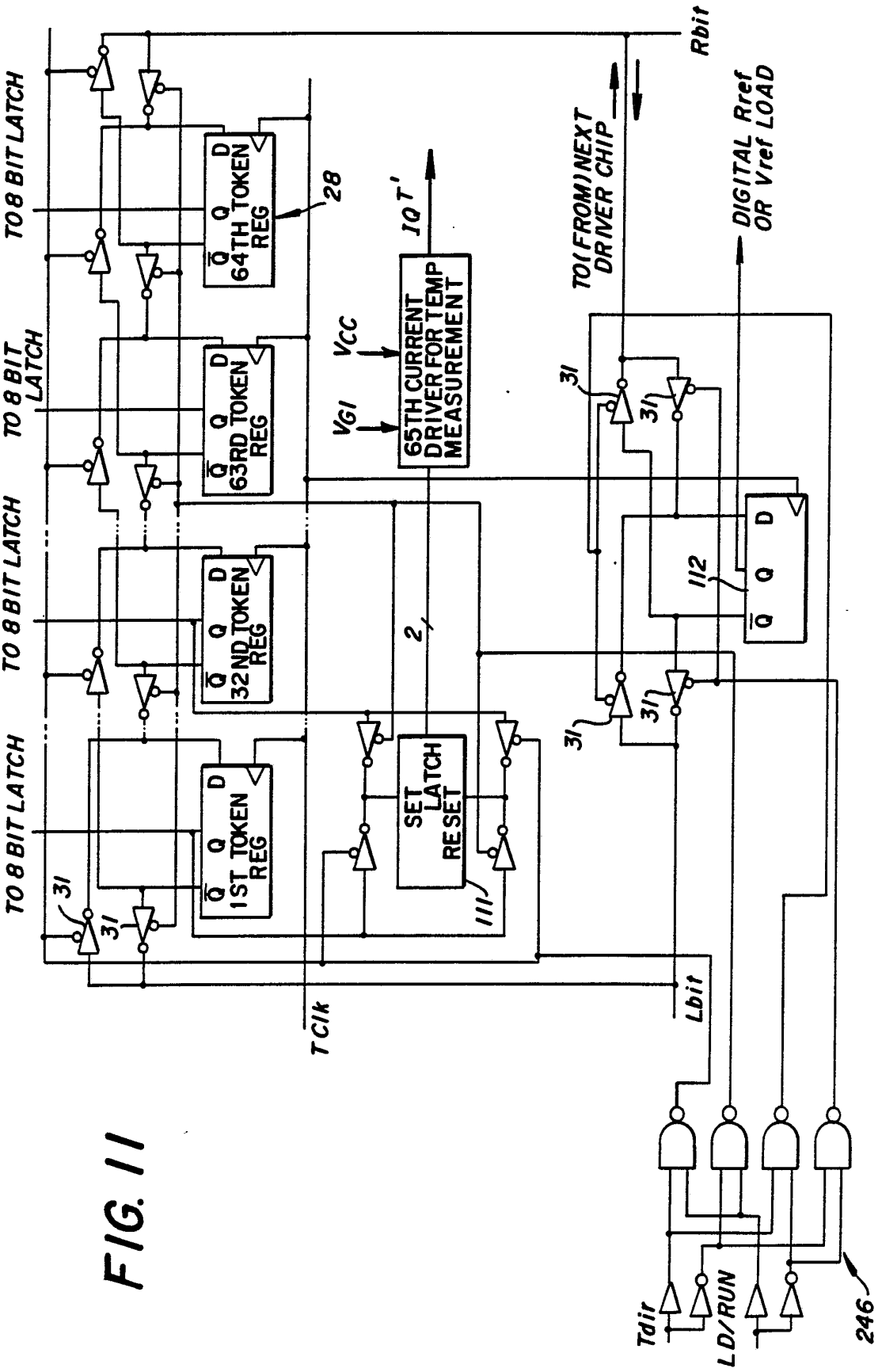

TO 8 BIT LATCH
TO 8 BIT LATCH
TO 8 BIT LATCH
TO 8 BIT LATCH
64TH TOKEN REG
63RD TOKEN REG
32ND TOKEN REG
1ST TOKEN REG
28
65TH CURRENT DRIVER FOR TEMP MEASUREMENT
IQT'
VCC
VGI
SET LATCH RESET
111
2
112
31
TCIk
Lbit
Rbit
TO(FROM) NEXT DRIVER CHIP
DIGITAL Rref OR Vref LOAD
Tdir
LD/RUN
246

FIG. 11

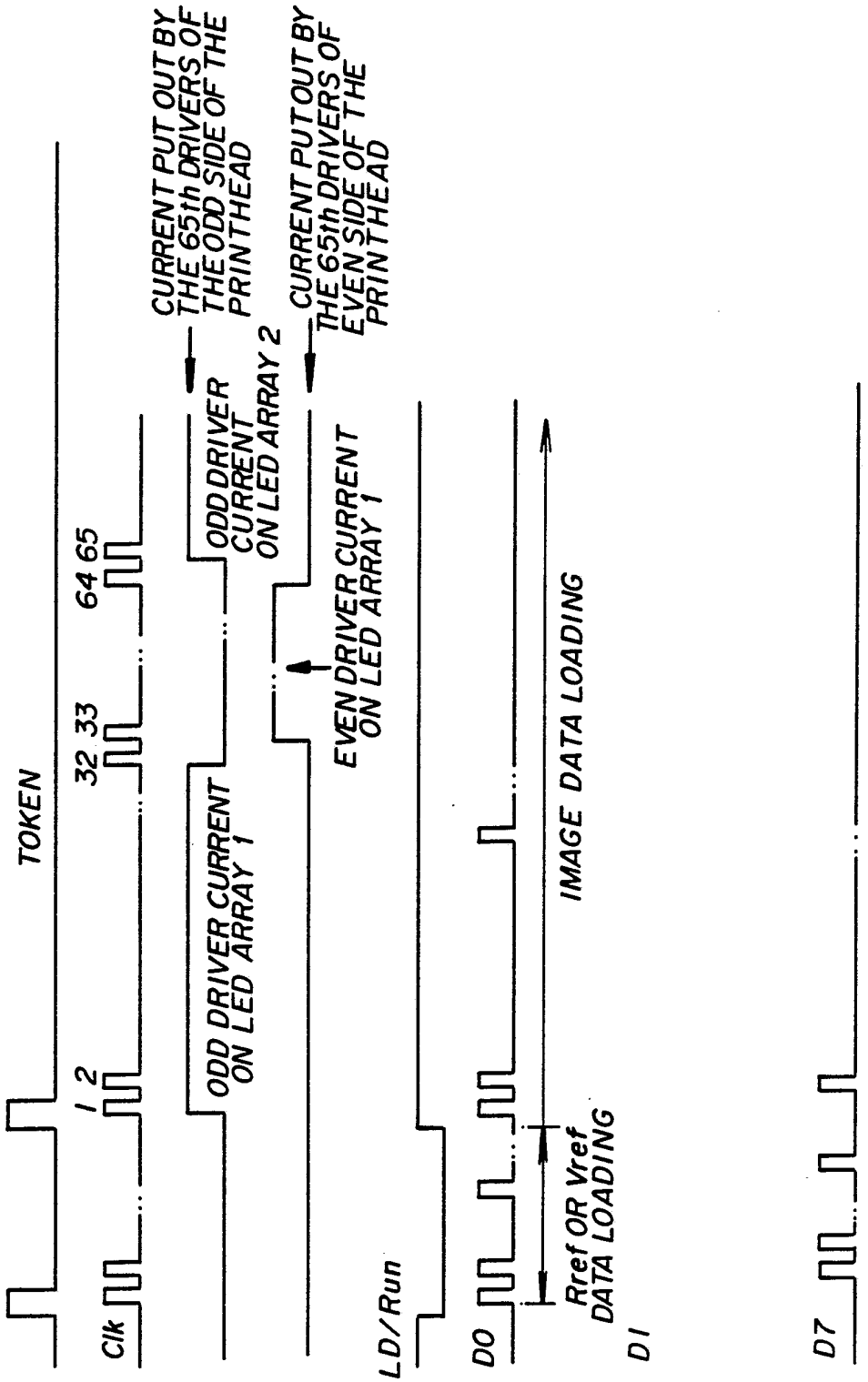

TOKEN
Clk
1 2
32 33
64 65
ODD DRIVER CURRENT ON LED ARRAY 1
ODD DRIVER CURRENT ON LED ARRAY 2
EVEN DRIVER CURRENT ON LED ARRAY 1
CURRENT PUT OUT BY THE 65th DRIVERS OF THE ODD SIDE OF THE PRINTHEAD
CURRENT PUT OUT BY THE 65th DRIVERS OF EVEN SIDE OF THE PRINTHEAD
LD/Run
DO
D1
D7
IMAGE DATA LOADING
Rref OR Vref DATA LOADING

FIG.12

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 91/04488

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 B41J2/45

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	B41J ; G06K

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No.[13]
P,X	US,A,4 952 949 (UEBBING) 28 August 1990	1,3,11, 12
P,Y		13,14, 19,20,34
P,A		2,5-10, 15-18, 21-33, 35-38
	see column 2, line 33 - column 6, line 21; figures	

X	PATENT ABSTRACTS OF JAPAN vol. 13, no. 299 (M-847)(3647) 11 July 1989 & JP,A,1 090 774 (HIRANE) 7 April 1989	1,3,11, 12
A		2,5-10, 15-18, 21-38
	see abstract	

	-/--	

° Special categories of cited documents :[10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
23 OCTOBER 1991	25. 11. 91
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	ADAM E.M.P.

Form PCT/ISA/210 (second sheet) (January 1985)

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category °	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
Y	US,A,4 746 941 (PHAM) 24 May 1988 cited in the application	19,20
A	see abstract	1-3, 5-12,15, 17,18, 21-38
Y	US,A,4 831 395 16 May 1989 cited in the application	13,14,34
A	see abstract	1,4-12, 15-18, 21-33, 35-38
A	US,A,4 370 666 (NODA) 25 January 1983	
A	PATENT ABSTRACTS OF JAPAN vol. 4, no. 139 (M-34)(621) 30 September 1980 & JP,A,55 095 584 (MINOWA) 19 July 1980 see abstract	

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. US 9104488 SA 49398

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information. 23/10/91

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US-A-4952949	28-08-90	None		
US-A-4746941	24-05-88	EP-A-	0393073	24-10-90
		JP-T-	2501646	07-06-90
		WO-A-	8903628	20-04-89
US-A-4831395	16-05-89	EP-A-	0308492	29-03-89
		JP-T-	1502734	21-09-89
		WO-A-	8807729	06-10-88
		US-A-	4941004	10-07-90
US-A-4370666	25-01-83	JP-B-	1002075	13-01-89
		JP-A-	56027370	17-03-81
		DE-A,C	3030129	02-04-81