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WO-A-85/04774

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269 524 (HITACHI LTD) 28-11-1986

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Description

Field of the Invention

This invention relates in general to emitter coupled logic (ECL) circuits and, more particularly, to a circuit that discharges the capacitive load at the output of an emitter follower with a pulse whose amplitude and duration is determined by the charge on the load.

Background of the Invention

Historically, one of the most important advantages of bipolar transistor technology has been its ability to drive large resistive and capacitive loads with relatively small device geometries. For instance, a typical emitter coupled logic gate comprises an emitter coupled logic stage coupled to a transistor emitter-follower output stage which restores DC levels. The emitter-follower output stage sources output current at the output of the ECL gate that is an exponential function of the emitter-base voltage of the output transistor. High fanout operation is possible because of the high input impedance of the emitter coupled logic gate and the low output impedance of the emitter-follower output stage. Early conventional emitter-follower output stages typically included a resistor coupled as a "pull-down" device between the output of the ECL gate and the negative power supply rail which sets the quiescent current in the emitter-follower output stage. A problem occurs when such prior art ECL gates are operated into large capacitive loads which must be discharged as the output of the gate switches from a first logic level to a second logic level. In prior art ECL gates, the discharge current must flow through the resistor to the negative supply rail of the gate. Since the resistor is much larger in value than the "on" resistance of the emitter-follower transistor, discharge of the capacitor is much slower than the charge thereof since discharge is at a near constant rate determined by the resistor. Hence, the input logic signal applied to the subsequent gate is skewed. This is highly undesirable because of the added difficulty in designing the remaining circuitry due to the skewed edges.

To decrease the discharge time, the value of the resistor coupled to the emitter follower stage of the ECL gate can be made smaller. However, this results in a undesirable increase in quiescent power dissipation since the quiescent current flowing through the emitter-follower output stage is increased.

Another previously known driver circuit includes a "pull-down" PNP transistor having an emitter coupled to the output terminal, a collector

coupled to the negative power supply rail, and a base coupled to a current path driven by the same signal driving the emitter follower. However, present technology is unable to provide a process for creating a PNP transistor of sufficient quality for competitive performance.

Yet another previously known driver circuit includes a "pull-down" NPN transistor having a collector connected to the output terminal, an emitter connected to the negative power supply rail, and a base coupled by a capacitor to an inverse signal to that driving the emitter follower. This circuit produces a high discharge current and a low standby current, however the discharge current is not proportional to the load capacitance.

Another previously known driver circuit is disclosed in U.S. Patent Number 4,675,554 that is similar to the previously mentioned circuit.

Still another previously known driver circuit is disclosed in U.S. Patent Number 4,687,953, wherein a dynamic ECL transient driver circuit is disclosed having a current enhancement portion for increasing the current to the base of the "pull-down" transistor. The current enhancement portion comprises differentially connected first and second transistors having their collectors coupled to the output terminal and their emitters coupled to the negative supply voltage rail by a current source. The base of the first transistor is connected to a current source voltage and the base of the second transistor is connected to its own collector and the base of the "pull-down" transistor by a resistor. Additionally, a capacitor is coupled between the base of the second transistor and the base of a transistor sourcing current to the output terminal. The discharge current of this circuit is not proportional to the load capacitance.

In order to utilize bipolar ECL gates in complex logic circuits, the static power requirement of the ECL gate needs to be reduced without sacrificing speed. Additionally, the bipolar ECL gates must be able to provide transient source and sink currents such that large capacitive loads can be driven at high speed while at the same time minimizing the quiescent power dissipation of the ECL gates.

Yet another previously known driver circuit is disclosed in European Patent Application EP-A-0 294 163 including pull-up and pull-down circuits.

This application represents prior art according to Article 54(3) EPC. and substantially corresponds to figure 7 of the present application, except for a further resistor inserted in the pull-down branch, the connection of a further current source to the output node and the connection of the collector of one transistor of the comparator circuit to the output node.

What is needed is an ECL transient driver circuit that discharges capacitive load at the output

of an emitter follower with a pulse whose amplitude and duration is determined by the charge on the load.

Summary of the Invention

Accordingly, the invention provides a circuit for driving a load at an output, including logic means for providing first and second output signals at first and second nodes respectively in response to an input signal. The circuit includes a first transistor having a base coupled to the first node, an emitter coupled to the output of the circuit, and a collector coupled to a first power supply conductor. A second transistor has a base receiving a reference voltage and a collector coupled to the second node. A third transistor includes a base coupled to the output of the circuit and a collector coupled to the first power supply conductor. A first current supply means has an output coupled to the emitters of the second and third transistors for providing a current. A fourth transistor includes a base coupled to the second node and a collector coupled to the first power supply conductor, while a fifth transistor has a base and collector coupled together to the emitter of the fourth transistor. A first resistor is coupled between the emitter of the fifth transistor and a second power supply conductor, and a sixth transistor has a base coupled to the emitter of the fifth transistor and a collector coupled to the output of the circuit. A second resistor is coupled between the emitter of the sixth transistor and the second power supply conductor.

Brief Description of the Drawing

FIG. 1 is a block diagram of the preferred embodiment of the present invention.

FIG. 2 is a schematical implementation of the preferred embodiment as a second embodiment.

FIG. 3 is a schematical implementation of the preferred embodiment as a third embodiment.

FIG. 4 is a schematical implementation of the preferred embodiment as a fourth embodiment.

FIG. 5 is a schematical implementation of the preferred embodiment as a fifth embodiment.

FIG. 6 is a block diagram of another driver circuit.

FIG. 7 is a schematical implementation of an embodiment of the driver of figure 6.

Detailed Description of the Invention

Referring to FIG. 1, a block diagram of the driver circuit in accordance with the present invention comprises a logic circuit 11 that may comprise any type of logic such as a gate, a register, or a

memory cell. The invention is shown in subsequent figures as emitter coupled logic, however may also be implemented in other logic families. A pull-up circuit 12 is connected to an output terminal 13 for supplying current thereto in response to a digital signal 14 from the driver circuit 11, and a pull-down circuit 15 is connected to the output terminal 13 for sinking current therefrom in response to a signal from an AND gate 16. A comparator circuit 17 is connected to the output terminal 13 for receiving an output voltage thereon and to the AND gate 16 for enabling the pull-down circuit 15. AND gate 16 is further connected to logic circuit 11 for enabling pull-down circuit 15 in response to the signals from logic circuit 11 and comparator circuit 17.

The signal 14 comprising a first digital state from the logic circuit 11 enables the pull-up circuit 12 for providing current to the output terminal 13 that charges a capacitive load 19 connected thereto. When the signal 14 from the logic circuit 11 changes to a second digital state, the pull-up circuit 12 will no longer supply current to the output terminal 13, and the pull-down circuit 15 will sink current therefrom. Signals 14 and 18 comprise inverse digital signals. When the signal 18 changes to the second state, and the output voltage on the output terminal 13 exceeds a reference voltage, the comparator circuit 17 enables the pull-down circuit 15. This enabling pulse has an amplitude and duration (time integral) that is determined by the charge on the load. The operation will be explained further with the more detailed embodiments described hereinafter.

Referring to FIG. 2, a detailed schematic of the block diagram of FIG. 1 in ECL technology comprises a pair of differentially connected transistors 21 and 22 having their collectors coupled to the supply voltage terminal V_{CC} by resistors 23 and 24, respectively, their bases connected to an input terminal 25 and the voltage reference V_{BB} , respectively, and their emitters connected to the collector of a current source transistor 26. The transistor 26 has its base connected to the current source voltage V_{CS} and its emitter coupled to the supply voltage terminal V_{EE} by a resistor 27. An emitter follower transistor, or pull-up transistor, 28 has a collector connected to the supply voltage terminal V_{CC} , a base connected to the collector of the transistor 22, and an emitter connected to an output terminal 29. A pull-down transistor 31 has a collector connected to the output terminal 29 and an emitter coupled to the supply voltage terminal V_{EE} by a resistor 32.

Differentially connected transistors 33 and 34 have collectors connected to the collector of the transistor 21 and the supply voltage terminal V_{CC} , respectively, bases connected to the voltage reference V_{BB} and the output terminal 29, respectively,

and emitters connected to the collector of a current source transistor 35. The transistor 35 has a base connected to the current source voltage V_{CSB} and an emitter coupled to the supply voltage terminal V_{EED} by a resistor 36. A transistor 37 has a collector connected to the supply voltage terminal V_{CC} and a base coupled to the collector of the transistor 21. A diode connected transistor 38 has a collector and base connected to the emitter of transistor 37, and an emitter connected to the base of the transistor 31 and coupled to the supply voltage terminal V_{EED} by a resistor 39.

In operation, assuming the output is initially in the high state, the transistor 34 will draw current from the current source transistor 35. When the input switches high to low, the differential pair transistors 21 and 22 switch states causing current to be routed from resistor 23 to resistor 24, causing the collector of transistor 21 to move up toward supply voltage V_{CC} . That rising collector voltage 18 for transistor 21 is transferred through the base-emitter junctions of transistors 37 and 38 to create a rising voltage on the base of the pull-down transistor 31. Transistor 31 will become more conductive, providing discharge current to pull the output voltage V_{OUT} low. When the output voltage V_{OUT} falls past V_{BB} , the differential transistors 33 and 34 switch states, with transistor 33 drawing the transistor 35 current. The transistor 33 current then pulls down through resistor 23 to create a falling voltage on the base of the transistor 37 which reduces the current flow through transistor 31 back to standby current level, completing the high to low transition. The low to high transition is accomplished in the conventional emitter follower fashion, with transistor 28 providing the charging current for the output voltage V_{OUT} rising edge.

Referring to FIG. 3, another embodiment teaches how to provide a bias voltage to the base of transistor 33. The components of FIG. 3 similar to those of FIG. 2 have been designated by the same reference numerals. A transistor 41 has a collector connected to the supply voltage terminal V_{CC} , a base connected to the collector of the transistor 34 and coupled to the supply voltage terminal V_{CC} by a resistor 42, and an emitter connected to both the base of the transistor 33 and to the collector of a current source transistor 43. The transistor 43 has a base coupled to the current source voltage V_{CSB} and an emitter coupled to the supply voltage terminal V_{EED} by a resistor 44. This circuit embodiment provides a method to more closely control the switching characteristics of the differential transistors 33 and 34. The base voltage of transistor 33 is the base-emitter voltage of transistor 41 plus the voltage across resistor 42. The base voltage of transistor 33 can be tailored through the sizing of resistor 42 to control the shutoff timing of pull-down

transistor 31, thus helping to control overshoots and undershoots of output voltage V_{OUT} . An offset voltage 40 can be applied to center the hysteresis.

Referring to FIG. 4, another embodiment teaches how to implement voltage supply compensation. The components of FIG. 4 similar to those of FIG. 2 have been designated by the same reference numerals. A transistor 45 has a collector coupled to the supply voltage terminal V_{CC} by a resistor 49 and connected to the base of transistor 50, a base coupled to voltage V_{CSB} , and an emitter coupled to supply voltage terminal V_{EED} by resistor 51. Transistor 50 has a collector connected to the supply voltage terminal V_{CC} and an emitter connected to the collector and base of the diode connected transistor 57. The emitter of transistor 57 is coupled to the supply voltage terminal V_{EED} by resistor 58 and connected to the base of transistor 46. The transistor 46 has a collector connected to the base of the transistor 38 and coupled to the collector of the transistor 38 by a resistor 47, and an emitter coupled to the supply voltage terminal V_{EED} by a resistor 48. This embodiment provides a method of compensation for V_{EED} voltage supply variations. The current source comprising transistor 46 and resistor 48 sets up a voltage across resistor 47. A bias voltage V_{CSB} is applied to the base of transistor 46 to compensate for changes in V_{EED} in such a way as to mirror, one to one, a V_{EED} voltage change to a voltage change across resistor 47. The transistors 45, 50 and 57 and resistors 49, 51 and 58 provide the voltage V_{CSB} to a plurality of pull-down circuits 15. Proper voltage V_{EED} regulation is attained if resistor pairs 23 and 49, and 36 and 51 are matched. This unity gain amplifier configuration results in a constant voltage difference from the base of transistor 38 to V_{EED} , thus keeping standby currents in resistor 39 and transistor 31 insensitive to V_{EED} variations.

Referring to FIG. 5, yet another embodiment teaches how to implement the invention in a dual differential mode. The components of FIG. 5 similar to those of FIG. 2 have been designated by the same reference numerals. Since the components on the left side of the figure are mirrored from the right side of the figure, like components are identified with a prime ('). Components for this embodiment include a transistor 51 having a collector connected to the supply voltage terminal V_{CC} , a base connected to the collector of the transistor 21, and an emitter coupled to a node 52 by a resistor 53. A current source transistor 54 has a collector connected to the node 52, a base connected to the current source voltage V_{CSB} , and an emitter coupled to the supply voltage terminal V_{EED} by a resistor 55. The transistor 33 has its collector connected to the node 52. A transistor 56 has a collector connected to the supply voltage terminal V_{CC} , a

base connected to the node 52, and an emitter connected to the base of the transistor 31 and coupled to the supply voltage terminal V_{EE} by a resistor 57. This embodiment provides a way to operate differentially by recapturing correct logic levels on the complimentary output side (the collector of transistors 21 and 22). For the circuit of FIG. 2, when shutting off the pulldown transistor 31, transistor 33 pulls currents down through resistor 23, losing the logic high that would normally result from the switching of a differential pair, thus making the complement output unavailable. The embodiment of FIG. 5 solves that problem by adding a "stage" between the logic gate 11 and the pull-up circuit 12. Now instead of transistor 33 drawing current directly from resistor 23, it pulls current through the emitter follower stage of transistor 51 and resistor 53. Only base current of transistor 51 is pulled through resistor 23, maintaining its correct logic level. The current source comprised of transistor 54 and resistor 55 sets up a bias in the emitter follower stage. To prevent saturation in the differential transistors 33 and 34, they are referenced down to V_{BB} , the second level of ECL series gating. Transistors 51 and 56 provide the same level shifting function as did transistors 37 and 38 of FIG. 2. This explanation also applies to the complimentary output side identified by the prime (') marks.

Referring to FIG. 6, another driver in block diagram form teaches how to implement the active pull-down with only single ended input from the logic gate. The components of FIG. 6 similar to those of FIG. 1 have been designated by the same reference numerals. In accordance with this embodiment, a comparator circuit 59 is connected for enabling pull-down circuit 15 in response to an output signal on output terminal 13 and a digital signal 14 from logic circuit 11. The operation thereof will be better understood by referencing the discussion of the following schematical implementation.

Referring to FIG. 7, an embodiment of the circuit shown in FIG. 6 is shown schematically and includes a transistor 61 having a collector connected to the supply voltage terminal V_{CC} , a base connected to the collector of the transistor 22, and an emitter connected to both the base of transistor 33 and the collector of current source transistor 62. The transistor 62 has a base connected to current source voltage V_{CSD} and an emitter coupled to supply voltage terminal V_{EE} by resistor 63. The collector of the transistor 33 is coupled to the supply voltage terminal V_{CC} by resistor 64 and is connected to the base of the transistor 37. This embodiment uses only the collector of transistor 22 as an input to the driver. The voltage on the collector of transistor 22 is provided to two emitter

followers 61 and 28. Transistor 61, which is biased by the current source comprised of transistors 62 and resistor 63, is used to supply base current to transistor 33. The comparator 59, then, instead of comparing the output voltage to a reference voltage as in the previous embodiment, compares the loaded output voltage V_{OUT} to the unloaded output voltage on the emitter of transistor 61. Thus, the pull-down pulse is not terminated until the end of the fall transition.

By now it should be appreciated that there has been provided a circuit that discharges the capacitive load at the output of an emitter follower with a pulse whose amplitude and duration is determined by the charge on the load.

Claims

1. A circuit for driving a load (19) at an output (29), including logic means (11) for providing first and second output signals at first (14) and second (18) nodes respectively in response to an input signal;
 - a first transistor (28) having a base, a collector and an emitter, said base being coupled to said first node, said emitter being coupled to the output (29) of the circuit, said collector being coupled to a first power supply conductor;
 - a second transistor (33) having a base, a collector and an emitter, said base receiving a reference voltage, said collector being coupled to said second node;
 - a third transistor (34) having a base, a collector and an emitter, said base being coupled to the output (29) of the circuit, said collector being coupled to said first power supply conductor;
 - first current supply means (35, 36) having an output coupled to said emitters of said second and third transistors for providing a current;
 - a fourth transistor (37) having a base, a collector and an emitter, said base being coupled to said second node, said collector being coupled to said first power supply conductor;
 - a fifth transistor (38) having a base, a collector and an emitter, said base and collector being coupled together to said emitter of said fourth transistor;
 - a first resistor (39) coupled between said emitter of said fifth transistor and a second power supply conductor;
 - a sixth transistor (31) having a base, a collector and an emitter, said base being coupled to said emitter of said fifth transistor, said collector being coupled to the output (29) of the circuit; and

a second resistor (32) coupled between said emitter of said sixth transistor and said second power supply conductor.

The circuit of claim 1 wherein said first current supply means includes:

a seventh transistor (35) having a base, a collector and an emitter, said base receiving a first current source voltage, said collector being coupled to said emitters of said second and third transistors; and

a third resistor (36) coupled between said emitter of said seventh transistor and said second power supply conductor.

3. The circuit of claim 2 wherein said logic means includes:

an eighth transistor (21) having a base, a collector and an emitter, said base receiving the input signal, said collector being coupled to said second node;

a ninth transistor (22) having a base, a collector and an emitter, said base receiving said reference voltage, said collector being coupled to said first node;

a fourth resistor (23) coupled between said second node and said first power supply conductor;

a fifth resistor (24) coupled between said first node and said first power supply conductor;

a tenth transistor (26) having a base, a collector and an emitter, said base receiving a second current source voltage, said collector being coupled to said emitters of said eighth and ninth transistors; and

a sixth resistor (27) coupled between said emitter of said tenth transistor and said second power supply conductor.

Patentansprüche

1. Schaltung zum Treiben einer Last (19) an einem Ausgang (29), mit einer Logikeinrichtung (11), um erste und zweite Ausgangssignale an ersten (14) und zweiten (18) Knoten als Reaktion auf ein Eingangssignal bereitzustellen;

einen ersten Transistor (28) mit einer Basis, einem Kollektor und einem Emitter, wobei die Basis mit dem ersten Knoten, der Emitter mit dem Ausgang (29) der Schaltung und der Kollektor mit einem ersten Stromversorgungsleiter verbunden ist;

einen zweiten Transistor (33) mit einer Basis, einem Kollektor und einem Emitter, wobei die Basis eine Referenzspannung empfängt und wobei der Kollektor mit dem zweiten Knoten verbunden ist;

einen dritten Transistor (34) mit einer Basis, einem Kollektor und einem Emitter, wobei die Basis mit dem Ausgang (29) der Schaltung und der Kollektor mit dem ersten Stromversorgungsleiter verbunden ist;

eine erste Stromversorgungseinrichtung (35,36) mit einem Ausgang, der mit den Emittern der zweiten und dritten Transistoren verbunden ist, um einen Strom zu liefern;

einen vierten Transistor (37) mit einer Basis, einem Kollektor und einem Emitter, wobei die Basis mit dem zweiten Knoten und der Kollektor mit dem ersten Stromversorgungsleiter verbunden ist;

einen fünften Transistor (38) mit einer Basis, einem Kollektor und einem Emitter, wobei die Basis und der Kollektor gemeinsam mit dem Emitter des vierten Transistors verbunden sind;

einen ersten Widerstand (39), der zwischen den Emitter des fünften Transistors und einen zweiten Stromversorgungsleiter geschaltet ist;

einen sechsten Transistor (31) mit einer Basis, einem Kollektor und einem Emitter, wobei die Basis mit dem Emitter des fünften Transistors und der Kollektor mit dem Ausgang (29) der Schaltung verbunden ist; und

einen zweiten Widerstand (32), der zwischen den Emitter des sechsten Transistors und den zweiten Stromversorgungsleiter geschaltet ist.

2. Schaltung nach Anspruch 1, worin die erste Stromversorgungseinrichtung enthält:

einen siebten Transistor (35) mit einer Basis, einem Kollektor und einem Emitter, wobei die Basis eine erste Stromquellenspannung empfängt und wobei der Kollektor mit den Emittern der zweiten und dritten Transistoren verbunden ist; und

einen dritten Widerstand (36), der zwischen den Emitter des siebten Transistors und den zweiten Stromversorgungsleiter geschaltet ist.

3. Schaltung nach Anspruch 2, worin die Logikeinrichtung enthält:

einen achten Transistor (21) mit einer Basis, einem Kollektor und einem Emitter, wobei die Basis das Eingangssignal empfängt und wobei der Kollektor mit dem zweiten Knoten verbunden ist;

einen neunten Transistor (22) mit einer Basis, einem Kollektor und einem Emitter, wobei die Basis die Referenzspannung empfängt und wobei der Kollektor mit dem ersten Knoten verbunden ist;

einen vierten Widerstand (23), der zwischen den zweiten Knoten und den ersten Stromversorgungsleiter geschaltet ist;

einen fünften Widerstand (24), der zwischen den ersten Knoten und den ersten Stromversorgungsleiter geschaltet ist;

einen zehnten Transistor (26) mit einer Basis, einem Kollektor und einem Emitter, wobei die Basis eine zweite Stromquellenspannung empfängt und wobei der Kollektor mit den Emittern der achten und neunten Transistoren verbunden ist; und

einen sechsten Widerstand (27), der zwischen den Emitter des zehnten Transistors und den zweiten Stromversorgungsleiter geschaltet ist.

Revendications

1. Circuit permettant d'exciter une charge (19) se trouvant en une sortie (29), qui comporte un moyen logique (11) servant à fournir des premier et deuxième signaux de sortie, respectivement en un premier noeud (14) et un deuxième noeud (18), en réponse à un signal d'entrée;

un premier transistor (28) possédant une base, un collecteur et un émetteur, ladite base étant connectée audit premier noeud, ledit émetteur étant connecté à la sortie (29) du circuit, ledit collecteur étant connecté à un premier conducteur d'alimentation électrique;

un deuxième transistor (33) possédant une base, un collecteur et un émetteur, ladite base recevant une tension de référence, ledit collecteur étant connecté audit deuxième noeud;

un troisième transistor (34) possédant une base, un collecteur et un émetteur, ladite base étant connectée à la sortie (29) du circuit, ledit collecteur étant connecté audit premier conducteur d'alimentation électrique;

un premier moyen d'alimentation en courant (35,36) dont la sortie est connectée auxdits émetteurs desdits deuxième et troisième transistors, afin de produire un courant;

un quatrième transistor (37) possédant une base, un collecteur et un émetteur, ladite base étant connectée audit deuxième noeud, ledit collecteur étant connecté audit premier conducteur d'alimentation électrique;

un cinquième transistor (38) possédant une base, un collecteur et un émetteur, ladite base et ledit collecteur étant connectés, ensemble, audit émetteur dudit quatrième transistor;

une première résistance (39) connectée entre ledit émetteur dudit cinquième transistor et un deuxième conducteur d'alimentation

électrique;

un sixième transistor (31) possédant une base, un collecteur et un émetteur, ladite base étant connectée audit émetteur dudit cinquième transistor, ledit collecteur étant connecté à la sortie (29) du circuit ; et

une deuxième résistance (32) connectée entre ledit émetteur dudit sixième transistor et ledit deuxième conducteur d'alimentation électrique.

2. Circuit selon la revendication 1, où ledit premier moyen d'alimentation en courant comporte :

un septième transistor (35) possédant une base, un collecteur et un émetteur, ladite base recevant une première tension de source de courant, ledit collecteur étant connecté auxdits émetteurs desdits deuxième et troisième transistors ; et

une troisième résistance (36) connectée entre ledit émetteur dudit septième transistor et ledit deuxième conducteur d'alimentation électrique.

3. Circuit selon la revendication 2, où ledit moyen logique comporte :

un huitième transistor (21) possédant une base, un collecteur et un émetteur, ladite base recevant le signal d'entrée, ledit collecteur étant connecté audit deuxième noeud;

un neuvième transistor (22) possédant une base, un collecteur et un émetteur, ladite base recevant ladite tension de référence, ledit collecteur étant connecté audit premier noeud;

une quatrième résistance (23) connectée entre ledit deuxième noeud et ledit premier conducteur d'alimentation électrique;

une cinquième résistance (24) connectée entre ledit premier noeud et ledit premier conducteur d'alimentation électrique;

un dixième transistor (26) possédant une base, un collecteur et un émetteur, ladite base recevant une deuxième tension de source de courant, ledit collecteur étant connecté auxdits émetteurs desdits huitième et neuvième transistors; et

une sixième résistance (27) connectée entre ledit émetteur dudit dixième transistor et ledit deuxième conducteur d'alimentation électrique.

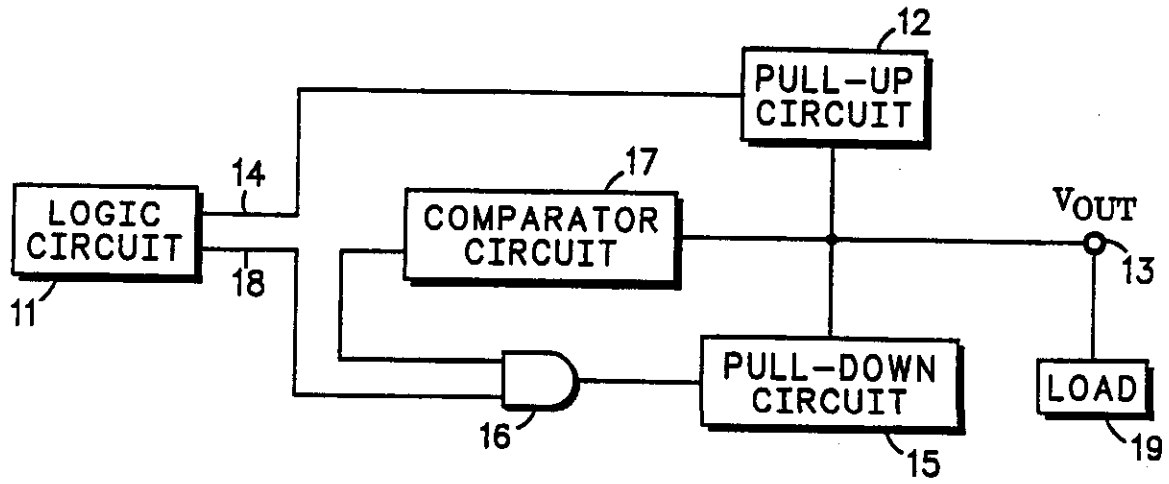
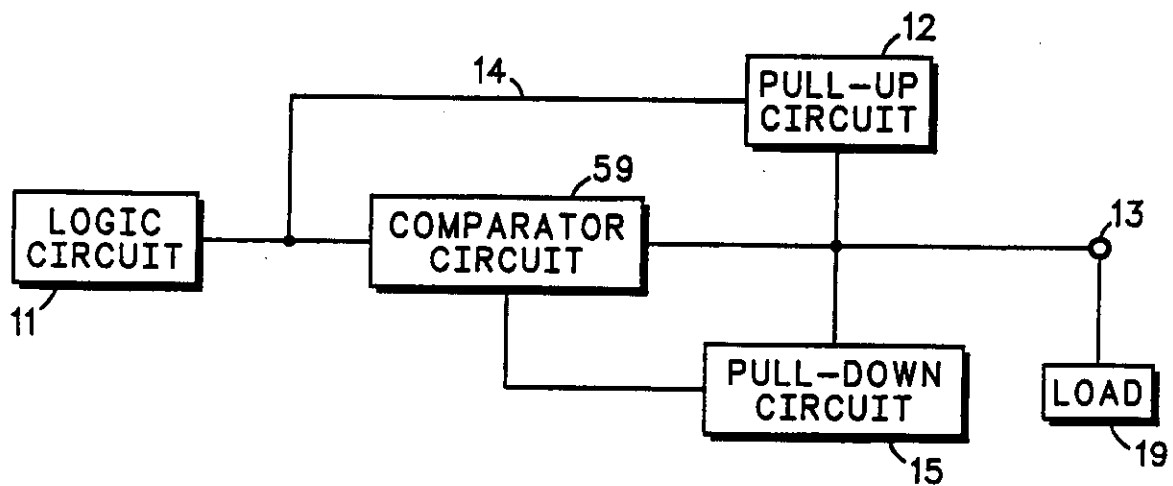


FIG. 1

FIG. 6



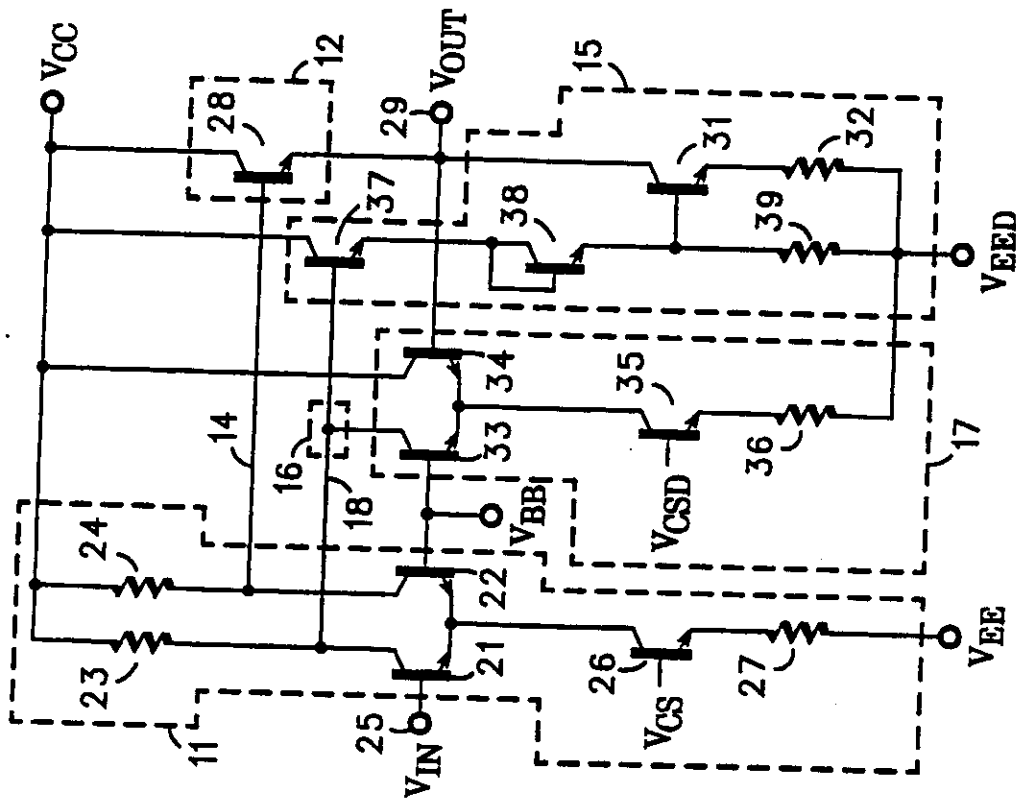


FIG. 2

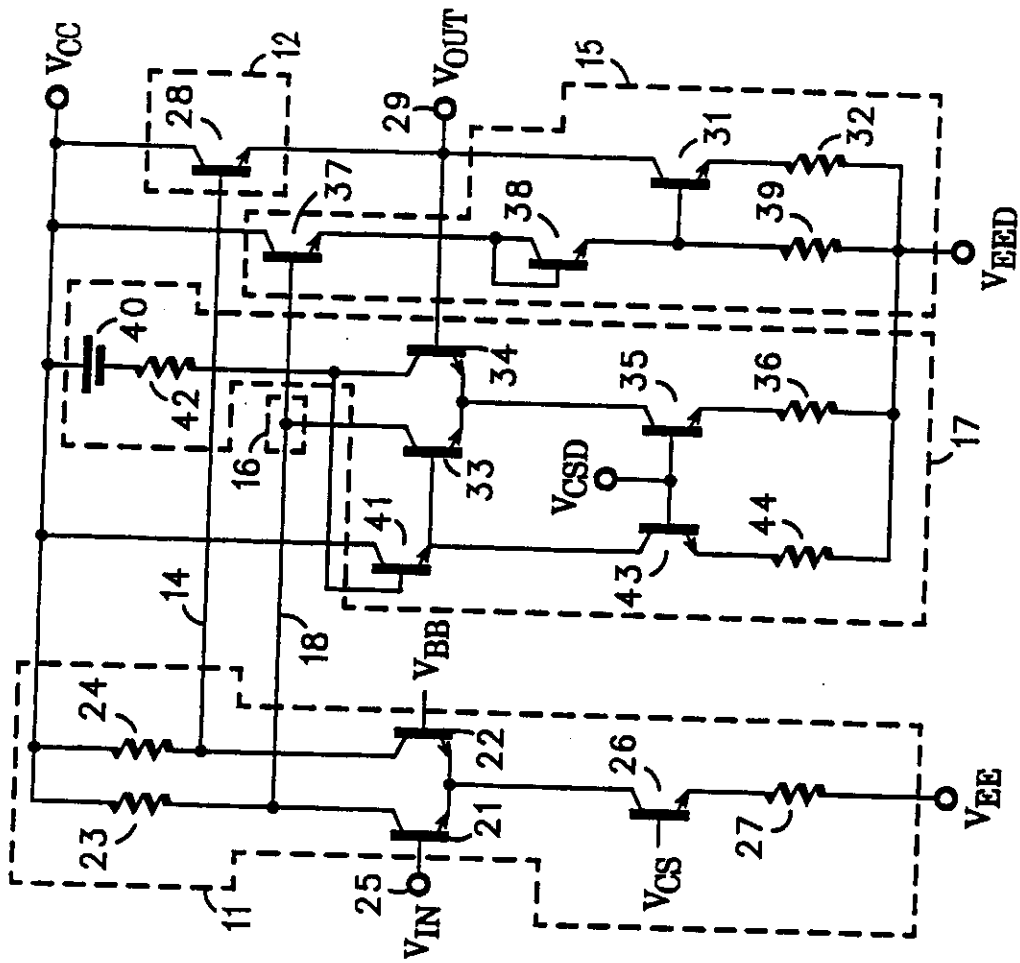


FIG. 3

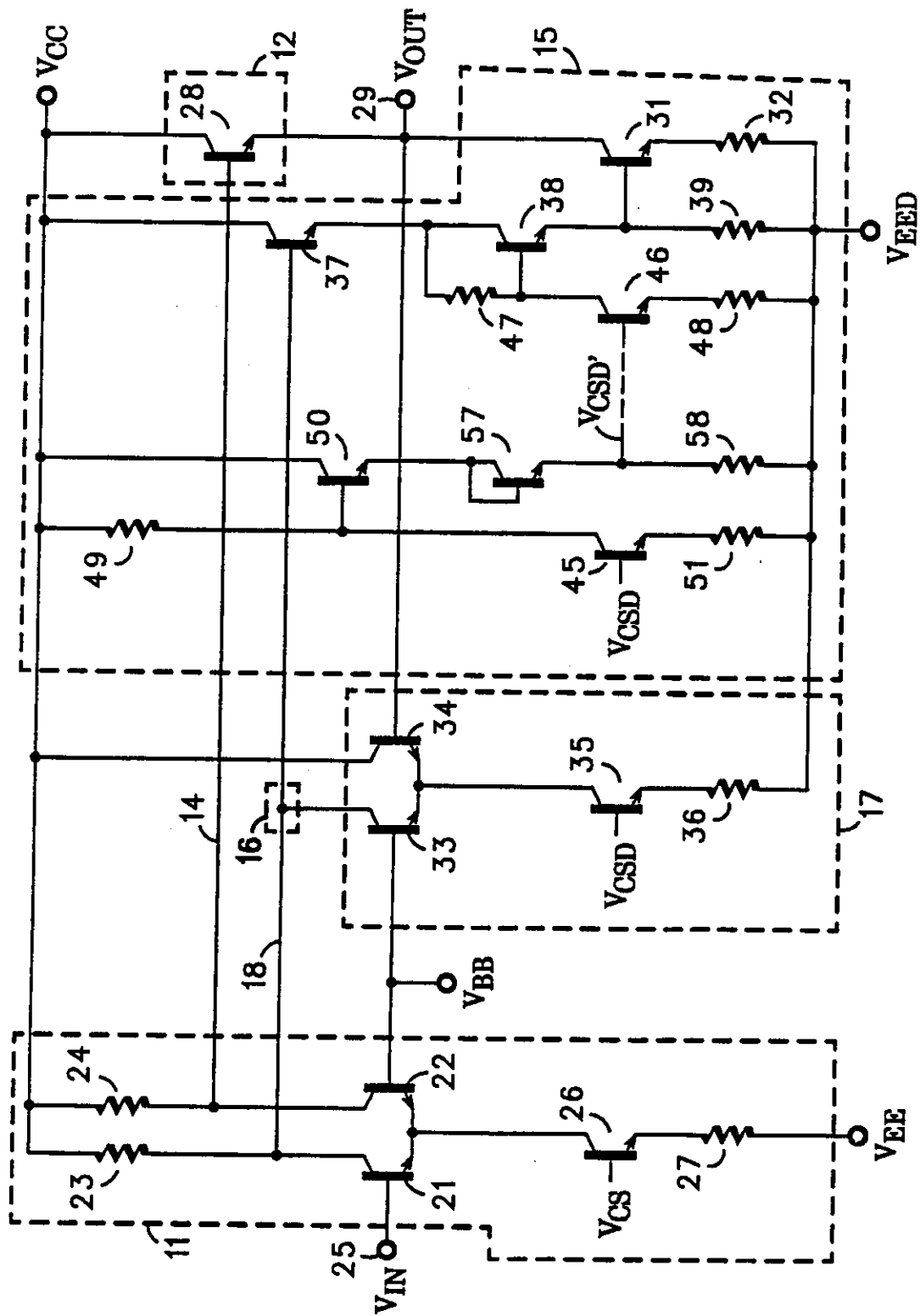


FIG. 4

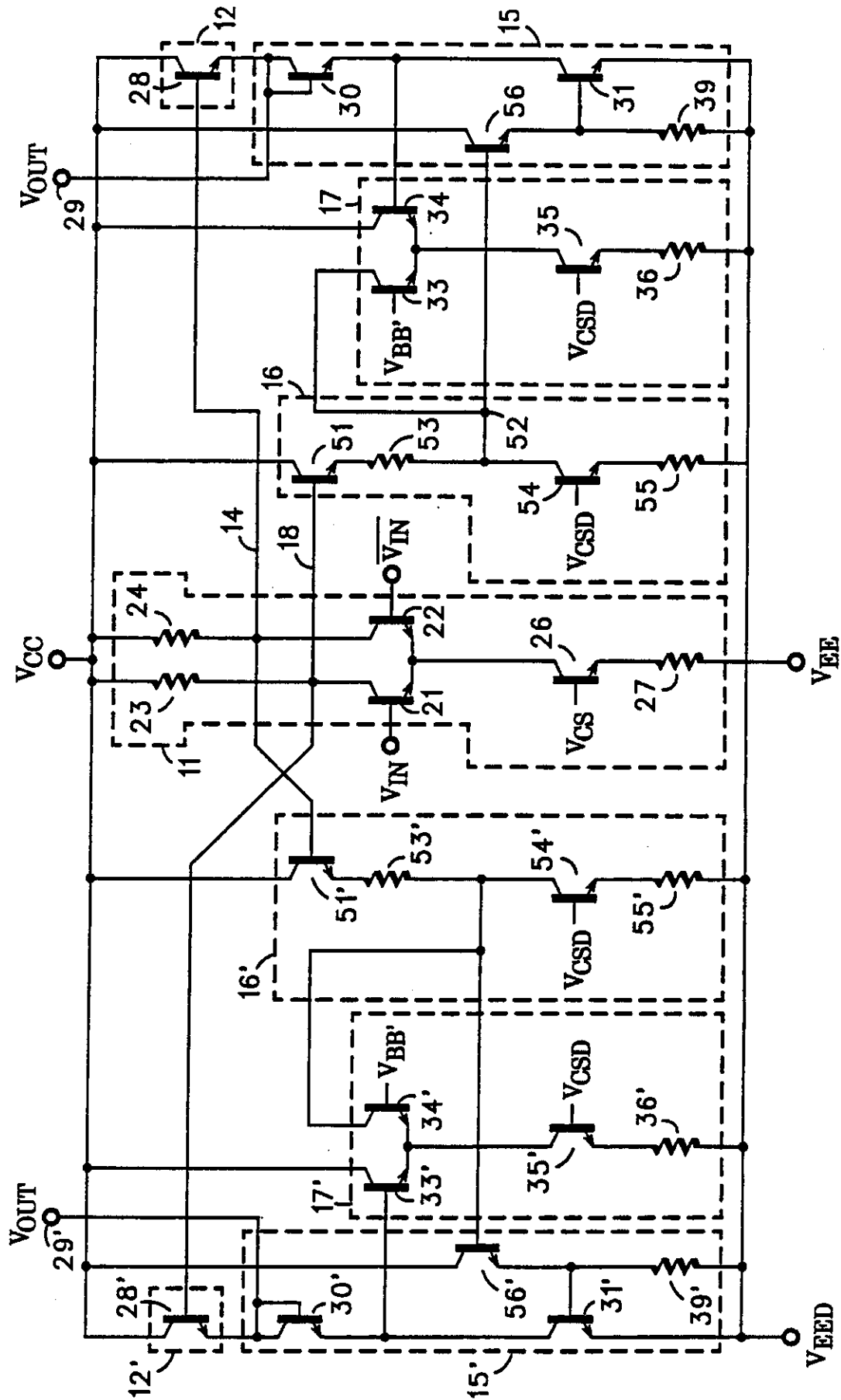


FIG. 5

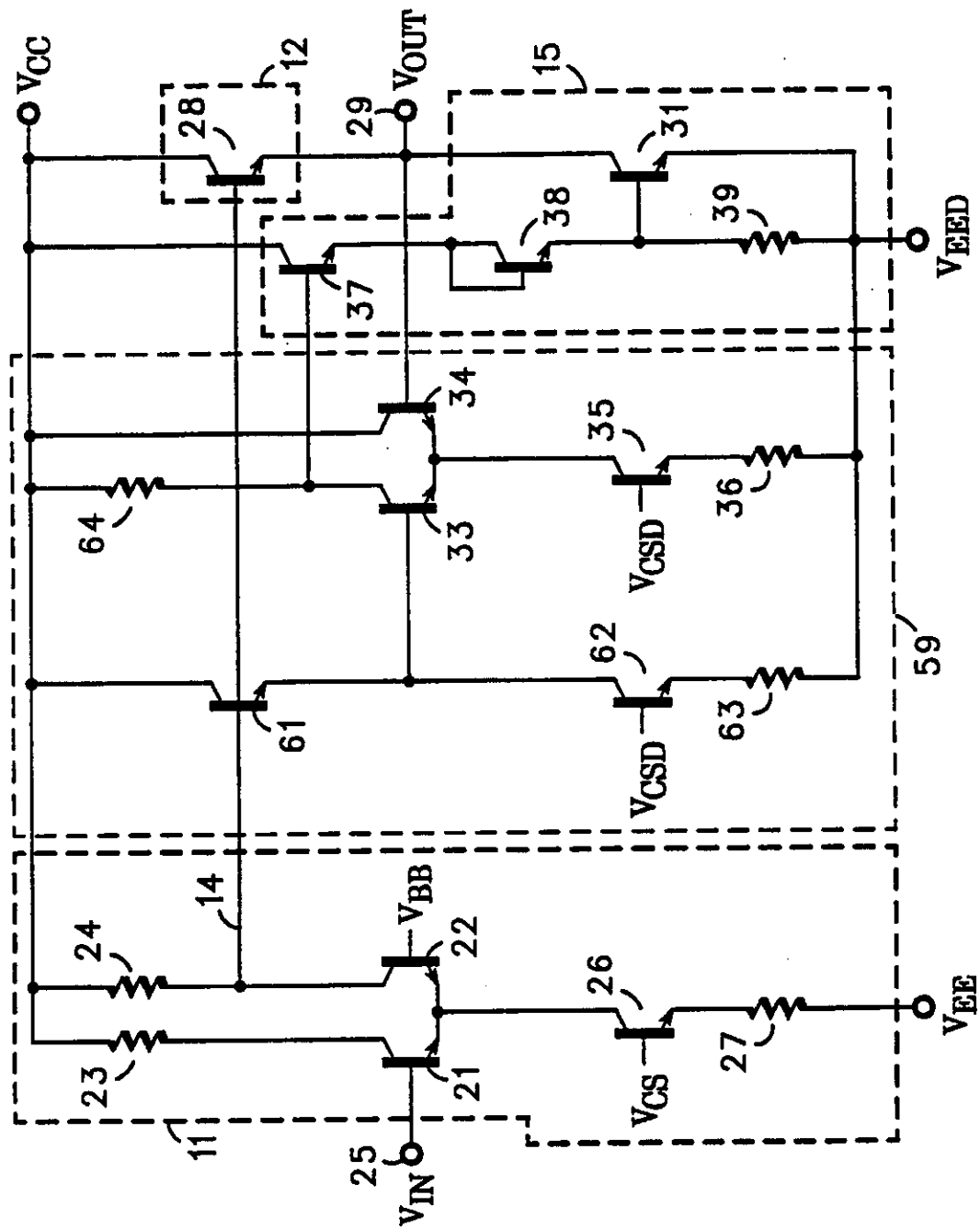


FIG. 7

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Priority claimed:

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Title LOAD CONTROLLED ECL TRANSIENT DRIVER.

Applicant/Proprietor

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Classified to

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from

MOTOROLA, INC., 1303 East Algonquin Road, Schaumburg IL 60196,

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[ADP No. 50019769003]

to

→ MOTOROLA, INC./ 1303 East Algonquin Road, Schaumburg, IL 60196,

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