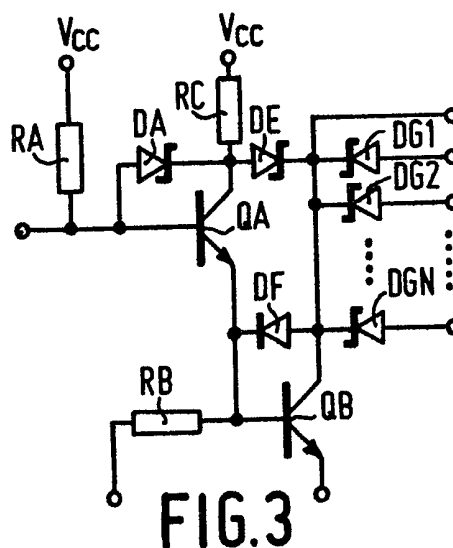


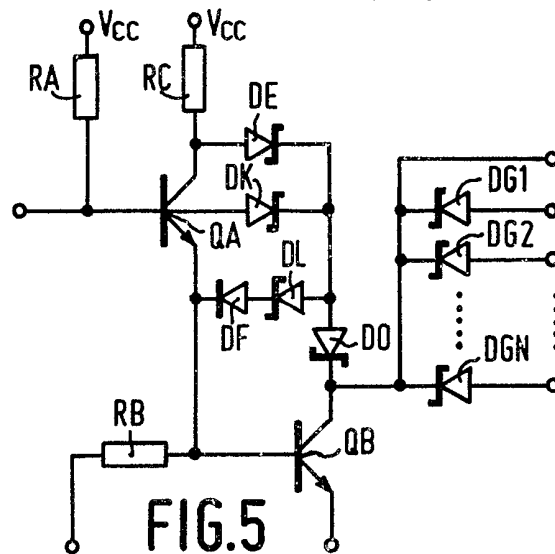
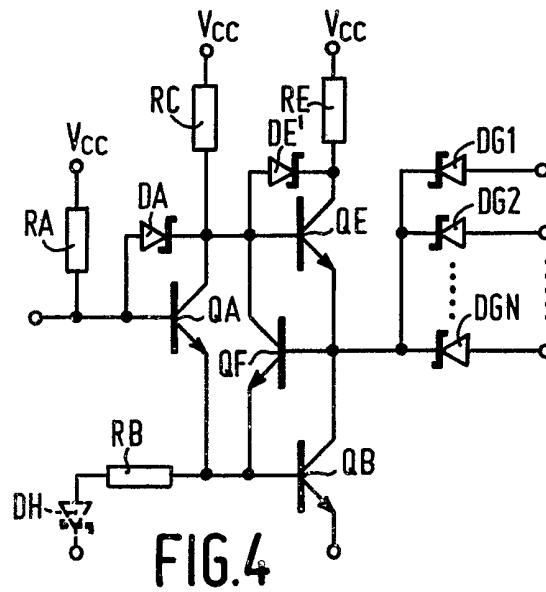
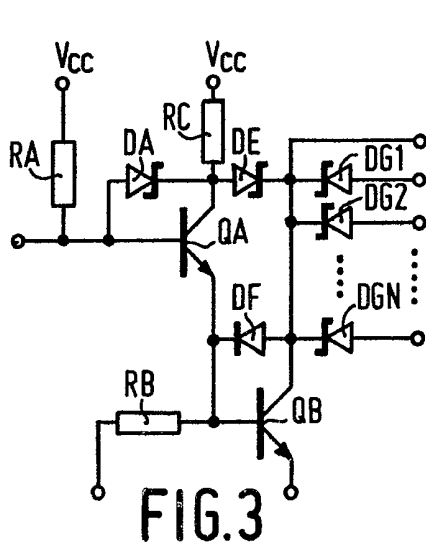
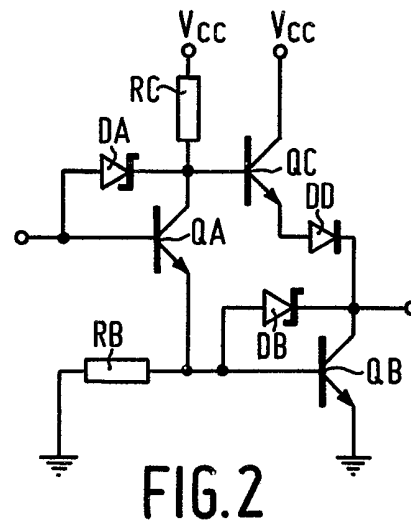
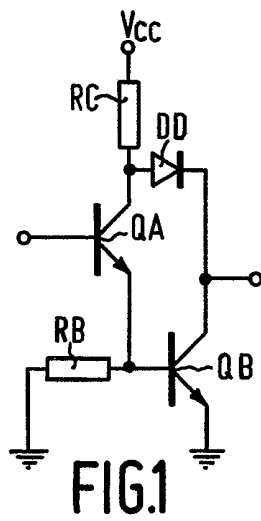
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 11C1A 11C4 11D 1AA9
 1BC 1BD 1FJ 4C11
 4C1R 9B1 9B1A 9D1 9E
 9N2 9N3 9R2 GAX
(56) Documents cited
 GB 1349445
 GB 1203626
 GB 1118640
 GB 1130192
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(54) **Bipolar logic inverter**

(57) A logic inverter comprises a first transistor (QA) having its collector coupled to a voltage source (V_{CC}) via a load (RC) and its emitter connected to the base of a second transistor (QB). The collector of the second transistor is also fed from the load (RC). In order to reduce the switching time of the circuit means are provided for preventing the second transistor from either turning off or normally going into deep saturation. These means comprise a first diode (DF) feeding the base of the second transistor and a second diode (DE) which feeds the collector of the second transistor, the second diode acting, when the input voltage (V_{IN}) is high, in conjunction with a Schottky clamp (DA) provided for the first transistor to hold up the voltage on the collector

of the second transistor relative to that on its base. The Schottky clamp may be replaced by a diode connected between the base of the first transistor and the collector of the second transistor.
(Fig. 3).





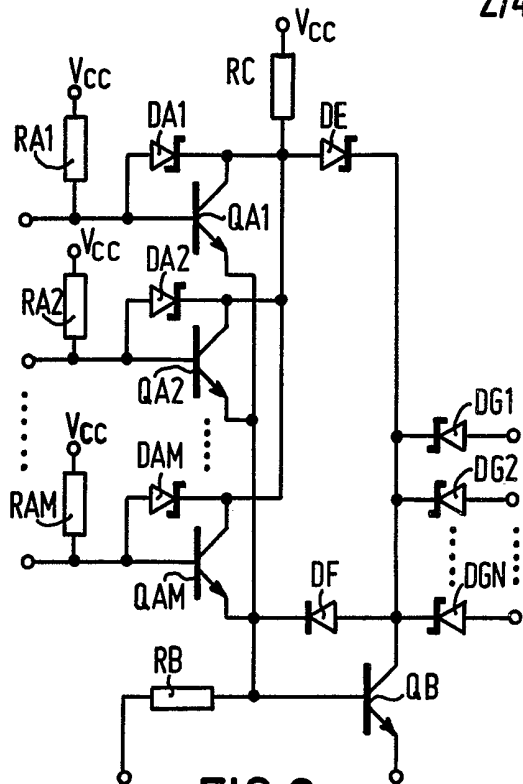


FIG.6

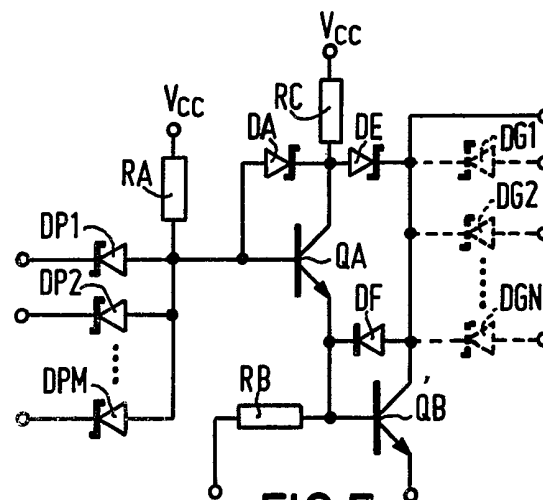


FIG.7

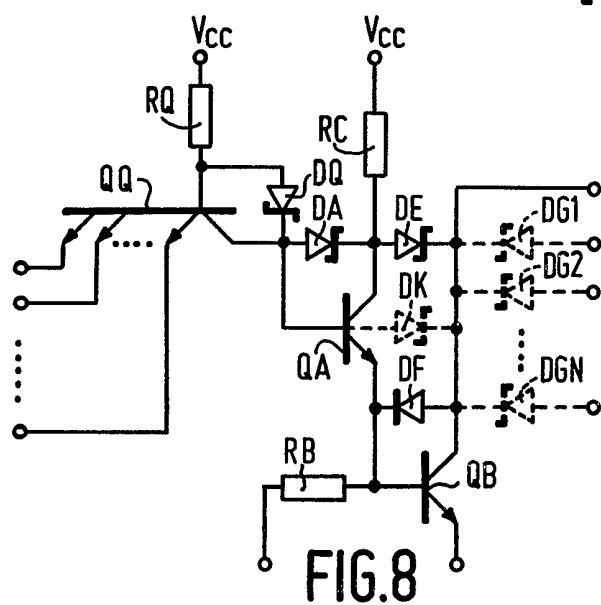
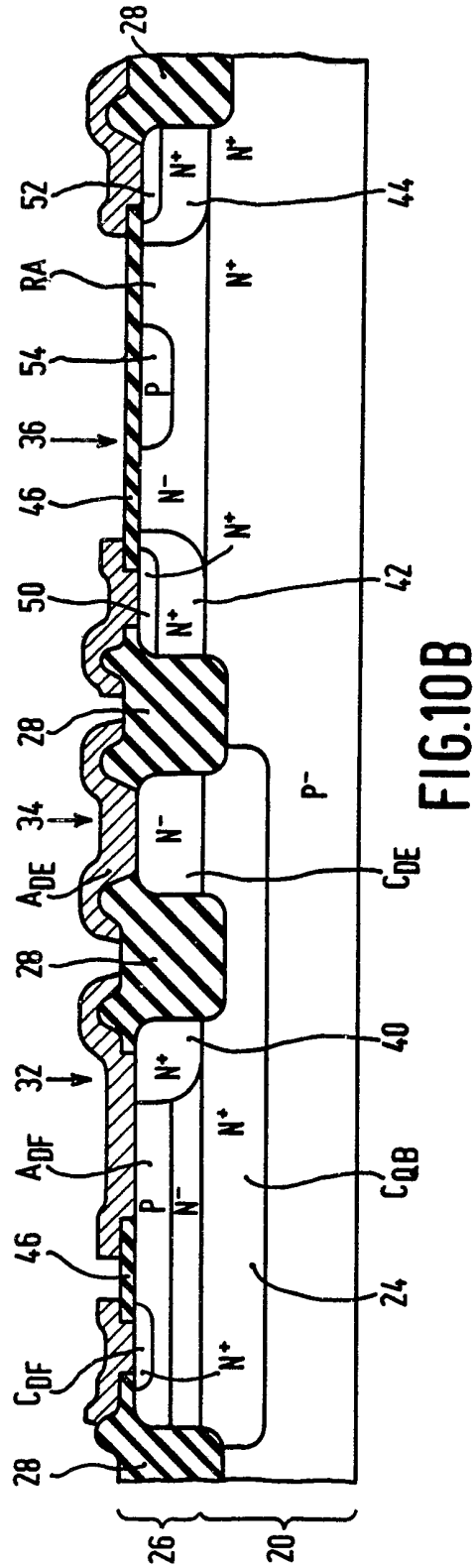


FIG.8





SPECIFICATION

Logic circuit

5 This invention relates to logic circuits including bipolar transistors. 5

In designing a digital logic gate in a semiconductor integrated circuit, an important objective is to reduce the gate propagation delay. This is the average time needed for an output signal of the gate to switch from a desired logical or "0" value to a desired logical high or "1" value and vice versa in response to a change in the logical value of an input signal to the gate. Such a gate typically consists of a switching transistor in combination with a mechanism to pull the output signal rapidly down to logical "0" and/or a mechanism to pull the output signal rapidly up to logical "1". 10

Referring to the drawings, Fig. 1 illustrates a conventional inverting logic gate of the type briefly mentioned by H. Ishino in U.S. Patent 4,107,547. This transistor-transistor logic (TTL) inverter receives an input voltage V_{IN} at the base of a bipolar NPN transistor QA and provides an output voltage V_{OUT} at the collector of another bipolar NPN transistor QB having its emitter grounded and its base connected to the emitter of transistor QA. The collector of transistor QA is resistively coupled to a voltage/current source V_{CC} and is coupled through a conventional PN diode DD to the collector of transistor QB. 15

Transistor QA or QB is in the on or conductive state when its base-to-emitter junction voltage V_{BEQA} or V_{BEQB} equals a PN diode-drop voltage termed a " V_{BE} " and is in the off or substantially non-conductive state when voltage V_{BEQA} or V_{BEQB} is less than $1V_{BE}$. Accordingly, transistors QA and QB both turn on as input voltage V_{IN} is raised from a logical "0" of less than $1V_{BE}$ to a logical "1" of $2V_{BE}$. Both transistors QA and QB go into "deep" saturation. This means that the base-collector junction of transistor QA or QB is sufficiently forward biased so as to be fully conductive. As transistor QB saturates, it draws progressively more current from source V_{CC} to actively pull output voltage V_{OUT} down to a logical "0" near 0 volt. When voltage V_{IN} is brought back down to its logical "0", transistors QA and QB both turn off. Depending on the load which voltage V_{OUT} is applied to, diode DD may be conductive. If so, a PN diode-drop voltage of $1V_{BE}$ occurs across diode DD, and voltage V_{OUT} rises up to a logical "1" of at least $1V_{BE}$ below V_{CC} . 20 25 30

A significant drawback of this inverter is that there is a rather large output voltage swing since transistor QB turns off when voltage V_{OUT} rises to logical "1". This voltage swing limits the output switching speed. Another disadvantage is that transistors QA and QB are initially both in deep saturation as voltage V_{IN} is switched from logical "1" to logical "0", and their bases therefore contain large amounts of stored charge. In transistors not made by gold-doped processes, these charges take a rather long time to flow to ground compared to the input switching time. As a result, the low-to-high output switching speed is limited by the time needed to discharge transistors QA and QB from deep saturation. Even with gold-doped transistors, the average propagation delay is usually about 3 nanoseconds. 35

Another conventional inverter, this time as disclosed by J. Kane et al. in U.S. Patent 3,962,590, is shown in Fig. 2. This TTL inverter contains all of the elements of Fig. 1 plus an NPN bipolar transistor QC having its collector connected to source V_{CC} and its base and emitter coupled, respectively, to the collector of transistor QA and the anode of diode DD. A Schottky diode DA connected between the base and collector of transistor QA Schottky clamps it. Transistor QB is similarly Schottky clamped with a Schottky diode DB. 40 45

Although Kane et al. do not describe the switching operation of this inverter in detail, it appears to operate as follows: As voltage V_{IN} is raised to a logical "1" of $2V_{BE}$, transistors QA and QB both turn on and saturate. Because they are Schottky clamped, neither normally goes into deep saturation. Instead, both go into "low" saturation where their base-collector junctions are forward biased, but below the normal fully conductive level. This occurs because diodes DA and DB become conductive and clamp the voltages across the base-collector junctions of transistors QA and QB at a Schottky diode-drop voltage which may be termed a " V_{SH} " and is normally slightly less than $1V_{BE}$. This clamped value of $1V_{SH}$ is usually not high enough to allow either of these base-collector junctions to become full conductive in the forward direction. As transistor QB turns on, it actively pulls voltage V_{OUT} down. Meanwhile, transistor QC turns off. When voltage V_{IN} is brought back down to a logical "0" of $1V_{BE}$ or lower, transistors QA and QB turn off. Transistor QC turns on to actively pull voltage V_{OUT} up to a logical "1" of at least $2V_{BE}$ below V_{CC} if diode DD is conductive. 50 55

By having transistors QA and QB Schottky clamped, less charge must be dissipated from their bases as voltage V_{IN} switches from logical "1" to logical "0". This reduces the low-to-high output switching time compared to that of Fig. 1. However, diode DA or DB may not always keep its transistor QA or QB from going into deep saturation. Because of processing variations from transistor to transistor and different doping levels in the collector and base compared to the emitter and base, the base-collector junction may become conductively forward biased at a voltage less than $1V_{BE}$. Sometimes the base-collector junction becomes conductively forward 60 65

biased at a voltage of $1V_{SH}$ or less. A Schottky-clamped transistor may also go into deep saturation if its Schottky diode is improperly designed or is operated at a high current level. Moreover, there is a rather sharp bend in the curve of collector-to-emitter voltage as a function of collector current that defines the low and deep saturation regions. In short, a Schottky-clamped transistor may still accumulate a moderately large amount of charge. In addition, the output swing is again rather large since transistor QB turns off during a corresponding switching operation. The average propagation delay for a gate such as that of Fig. 2 is usually about 2 nanoseconds.

In accordance with the invention, a logic circuit comprising a first bipolar transistor having a base, an emitter, and a collector coupled to a voltage/current source, and a second bipolar transistor having a base coupled to the emitter of the first transistor, an emitter coupled to a constant voltage source, and a collector coupled to the voltage/current source for supplying an output signal is characterized by means for preventing the second transistor from either turning substantially off or normally going into deep saturation.

Because the second transistor always remains on the output voltage swing occurring during a switching operation can be less than that which occurs when pull-down/pull-up transistors that switch on and off are employed, as is the case in comparable prior art logic gates, giving a corresponding reduction in the average propagation delay of the circuit.

Each transistor may be an NPN transistor. The said means then preferably comprises first means for providing positive current from the voltage/current source in a single current-flow direction to the collector of the second transistor and second means for providing positive current from the first means in a single current-flow direction to the base of the second transistor.

The first means may comprise a first diode, for example a Schottky diode, having its anode and cathode coupled respectively to the collectors of the first and second transistors, and clamping means for preventing the first transistor from going into deep saturation. The clamping means may comprise a Schottky diode having its anode and cathode connected respectively to the base and collector of the first transistor. As an alternative to the clamping means the first means may include a Schottky diode having its anode and cathode coupled respectively to the base of the first transistor and the collector of the second transistor.

The second means may comprise a further diode, for example a PN diode, having its anode and cathode coupled respectively to the cathode of the first diode and the base of second transistor. (This is the opposite direction to which a Schottky diode would be connected for Schottky clamping the second transistor).

An advantage of the present logic circuit is that its average propagation delay can be about 1 nanosecond. This is less than that of otherwise comparable prior art devices. Moreover, the noise margin for both high-to-low and low-to-high switching is an adequate value of about 0.5 volt in a given embodiment. If Schottky diodes are included, the present logic circuit can be such as to perform very well over the temperature range of -55°C to 150°C . An inverter constituted by the present logic circuit may occupy as little as 4800 microns^2 which is smaller than prior art TTL and emitter-coupled logic (ECL) inverters. Such an inverter may also require less power than conventional ECL inverters.

The logic circuit can be used as a building block in the logic portions of numerous types of integrated circuits. It can have a high fan-out capability and can be generally compatible with TTL systems.

Embodiments of the invention will be described, by way of example, with reference to the accompanying diagrammatic drawings in which:-

Figures 1 and 2 are circuit diagrams of prior art inverting logic gates,

Figure 3 is a circuit diagram of a first embodiment in the form of an inverting logic gate,

Figure 4 is a circuit diagram of a variation of the inverter of Fig. 3

Figure 5 is a circuit diagram of another embodiment of the invention in the form of an inverting logic gate,

Figure 6 is a circuit diagram of a NOR logic gate employing the inverter of Fig. 3,

Figures 7 and 8 are circuit diagrams of NAND logic gates employing the inverter of Fig. 3,

Figure 9 is a topographical view of a possible layout for the inverter of Fig. 3, and

Figures 10A and 10B are cross-sectional views of portions of the inverter shown in Fig. 9.

Likewise reference symbols are employed in the drawings and in the description of the embodiments to denote corresponding items.

Referring to the drawings, Fig. 3 illustrates an inverting logic gate having a very high switching speed. Input voltage V_{IN} is applied to the base of silicon NPN bipolar transistor QA whose base and collector are tied to voltage/current source V_{CC} through a resistor RA and a resistor RC, respectively. Aluminium-silicon Schottky diode DA is connected between the base and collector of transistor QA to prevent its base-collector junction from becoming forward biased more than $1V_{SH}$ which is 0.4-0.7 volts depending on the diode current and typically is 0.5 volt. The base-collector junction of transistor QA normally does not become fully conductive

until its base-to-collector voltage V_{BCOA} exceeds $1V_{SH}$. Accordingly, diode DA normally prevents transistor QA from going into deep saturation.

The anode and cathode of an aluminium-silicon Schottky diode DE are connected to the collectors of transistors QA and QB, respectively. The collector of transistor QB is also connected to the anode of a silicon PN diode DF whose cathode is connected to the base of transistor QB. This base is further connected to the emitter of transistor QA and through a resistor RB to a source V_{REF} of a constant reference voltage. The emitter of transistor QB is connected to constant voltage source V_{REF} which preferably is ground potential.

Output voltage V_{OUT} can be taken directly from the collector of transistor QB. Preferably, a series of N output voltages $V_{OUT1}, V_{OUT2}, \dots, V_{OUTN}$ are taken from the anodes of N corresponding aluminium-silicon output Schottky diodes DG1, DG2, \dots DGN, respectively, whose cathodes are connected to the collector of transistor QB. This arrangement provides both a high fanout and suitable input voltage levels for additional logic gates connected to the inverter of Fig. 3 for receiving voltages $V_{OUT1}-V_{OUTN}$.

The inverter of Fig. 3 operates as follows: In the situation where voltage V_{REF} is ground potential, the desired logical "1" input value for voltage V_{IN} is a threshold value of $2V_{BE}$. For silicon bipolar transistors and silicon PN diodes, $1V_{BE}$ is 0.6–1.0 volt depending on the current and typically equals 0.8 volt. The desired logical "1" input value exceeds the desired logical "0" input value for voltage V_{IN} by a suitable amount which may be termed the logical "0" input noise margin. To facilitate connection of the present inverter to another logic circuit having the same input/output characteristics as the present inverter, the logical "0" input noise margin preferably equals the corresponding logical "0" output noise margin which is $1V_{SH}$ as discussed below. Accordingly, the desired logical "0" input value is $2V_{BE}-V_{SH}$. The desired output logic levels are the same for each voltage V_{OUTJ} where J varies from 1 to N. That is, the desired logical "1" output value is $2V_{BE}$ (with a suitable logical "1" output noise margin); the desired logical "0" output value is $2V_{BE}-V_{SH}$.

When voltage V_{IN} is raised from logical "0" to logical "1", transistor QA turns on. This establishes a current path from source V_{CC} through resistor RC and transistor QA to the base of transistor QB that acts to pull its base voltage up. Transistor QB which was previously on turns on harder. Transistor QA draws current from source V_{CC} to cause a greater voltage drop across resistor RC. The voltage at the anode of diode DE which was previously conductive drops accordingly. Nonetheless, diode DE remains conductive. Diode DA becomes conductive to Schottky clamp transistor QA.

The voltage at the base of transistor QB is V_{BEQB} and equals $1V_{BE}$. If V_{DDA} and V_{DDE} are the conductive voltages across diodes DA and DE, respectively, the voltage at the collector of transistor QB is $V_{BEQB} + V_{BEQA} - V_{VDDA} - V_{VDE}$ and equals $2V_{BE} - 2V_{SH}$ here. The base-to-collector voltage V_{BCQB} for transistor QB is therefore $1V_{BE} - (2V_{BE} - 2V_{SH})$ which is $2V_{SH} - V_{BE}$ or about 2 volt. This is significantly below the forward voltage needed to make the base-collector junction of transistor QB fully conductive. Transistor QB cannot deeply saturate. Its operation is limited to its low saturation range. In effect diode DE in combination with transistor QA and its Schottky clamp DA act to clamp transistor QB well out of deep saturation. This substantially reduces the low-to-high output switching time when voltage V_{IN} is later brought back down to its logical "0" since the charge that must be dissipated from the base of transistor QB is substantially reduced because it does not approach deep saturation.

During low-to-high input switching, the collector-to-emitter resistance of transistor QB decreases when it turns on harder. This actively pulls each output voltage V_{OUTJ} down to its logical "0" to decrease the high-to-low output switching time. The voltage V_{DDGJ} across each diode DDJ is $1V_{SH}$ while voltage V_{OUTJ} equals V_{DDGJ} plus the collector voltage of transistor QB. As a result, voltage V_{OUTJ} reaches the desired logical "0" output value of $2V_{BE} - V_{SH}$. Since the desired output logical "1" is $2V_{BE}$, the logical "0" output noise margin is $1V_{SH}$.

The voltage across diode DF goes to $-V_{BCQB}$ which is $1V_{BE} - 2V_{SH}$ or about -0.2 volt when voltage V_{IN} reaches its logical "1". Diode DF is reverse biased and therefore inactive at this point.

As voltage V_{IN} is returned to logical "0", transistor QA turns off. Likewise, diode DA becomes non-conductive. The voltage at the base of transistor QA decreases as it moves toward the non-conductive state. However, transistor QB cannot turn off. As the base voltage for transistor QB drops, diode DF becomes forward biased and finally conductive until another current path from source V_{CC} to the base of transistor QB is established through resistor RC by way of diode DE which remains conductive and diode DF. The current through diode DF to the base of transistor QB keeps it on.

The base voltage for transistor QB is V_{BEQB} which again equals $1V_{BE}$. If V_{DDF} is the voltage across diode DF when it is conductive, the collector voltage for transistor QB is $V_{BEQB} + V_{DDF}$ and equals $2V_{BE}$ here. Voltage V_{BCQB} is therefore $-1V_{BE}$ so that the base collector junction of transistor QB is reversed biased and it operates in the linear range.

Were diode DF non-existent, there would be no alternative current path to the base of

transistor QB to keep it on when voltage V_{IN} drops to its logical "0". Thus diode DF prevents transistor QB from turning off. This decreases the voltage swing across transistor QB and in turn, reduces the average gate propagation delay.

During high-to-low input switching, each voltage V_{OUTJ} moves upward as the collector-to-emitter resistance of transistor QB increases, causing the current through resistor RC to decrease. Voltage V_{OUTJ} can rise as high as V_{DDGJ} plus the collector voltage of transistor QB, i.e. to $2V_{BE} + 1V_{SH}$. However, the desired logical "1" output level is $2V_{BE}$. Accordingly the inverter of Fig. 3 provides a logical "1" output signal of $2V_{BE}$ with a logical "1" output noise margin of $1V_{SH}$ (which is the same as the logical "0" output noise margin). The output voltage swing is the difference between the maximum and minimum values of voltage V_{OUTJ} and here equals $2V_{BE} + V_{SH} - (2V_{BE} - V_{SH})$ which is $2V_{SH}$ or about 1.0 volt.

Diode DF may be configured in any one of several ways. Preferably, diode DF consists of an NPN bipolar transistor in which its emitter serves as the cathode and its base is tied to its collector to serve as the anode. Alternatively, diode DF may be a conventional two-element diode having a P-type region as the anode and an N-type region as the cathode.

Still further, diode DF may consist of the base-emitter junction of an NPN bipolar transistor QF. Fig. 4 shows a circuit diagram of an inverter in which this is the case; transistor QF has its collector tied, in common with the collector of transistor QA, through resistor RC to source V_{CC} . Insofar as transistor QF is concerned, the operation of the inverter of Fig. 4 is substantially the same as that described above for Fig. 3.

Diode DF may be replaced by a Schottky diode connected in the same manner as diode DF. Operation is basically the same as when diode DF is a PN diode except that the logical "1" output noise margin decreases slightly to $2V_{SH} - V_{BE}$ or about 2.0 volt. This makes the output switching speed slightly greater due to the resulting slightly smaller output voltage swing.

Even further, PN diode DF may have one or more additional diodes in series with it. In this case, operation is substantially the same as that described above for Fig. 3, except that the logical "1" output noise margin is greater. If, for example, a single Schottky diode is connected in series with PN diode DF, the logical "1" output noise margin becomes $2V_{SH}$ or about 1.0 volt. This tends to make the output switching speed decrease slightly because of greater output voltage swing, but the provision of the Schottky diode might also tend to make the switching speed increase due to less parasitic capacitance at the collector of transistor QB.

As long as diode DE is a Schottky diode, transistor QB never goes into deep saturation irrespective of whether diode DF is a PN diode, is replaced by a Schottky diode, or includes one or more other diodes in series with it. Voltage V_{BCQB} goes no higher than $2V_{SH} - V_{BE}$ or about 0.2 volt so that the base-collector junction never becomes fully conductively forward biased.

In some applications, it may be desirable to substitute a PN diode for Schottky diode DE. In such case, voltage V_{BCQB} at input logical "1" becomes $1V_{SH}$. This is the condition that exists when a transistor is Schottky clamped. Accordingly, transistor QB will be effectively Schottky clamped and normally will not go into deep saturation. The logical "1" output noise margin will be a slightly higher value of $1V_{BE}$, resulting in a slightly higher propagation delay. Transistor QB otherwise will operate in precisely the same manner as described above for Fig. 3. Where diode DF is also replaced by a Schottky diode or is in series with one or more other diodes, the logical "0" output noise margin will be the same as that described above.

When diode DE is replaced with a PN diode it may be configured in any one of several ways. It may be a conventional two-element PN diode or an NPN bipolar transistor in which its emitter is the cathode and its base is connected to its collector to serve as the anode. Alternatively, the PN diode may consist of the base-emitter junction of an NPN bipolar transistor QE having its collector connected through a resistor RE to source V_{CC} as shown in Fig. 4. Preferably, a Schottky diode DE' Schottky clamps transistor QE. Aside from the use of diode DE', the operation of the inverter of Fig. 4 with respect to transistor QE is otherwise the same as that described above for the case in which diode DE is replaced with a PN diode.

Table I below summarizes the operating characteristics of the embodiment and the principal variations to it. The entries "SH" and "PN" for the category "DE" indicate the cases where diode DE is a Schottky diode or is replaced by a PN diode, respectively. Likewise, the entries "PN", "SH", and "PN + SH" for the category "DF" indicate the cases where diode DF is a PN diode, is replaced by a Schottky diode, or is in series with a Schottky diode, respectively.

TABLE I

	DE	DF	V_{IN}	V_{OUT}	V_{BCQB}	Noise Margin	
5	SH	PN	1 0	0 1	$2V_{SH}-V_{BE}$ $-V_{BE}$	V_{SH} V_{SH}	5
10	SH	SH	1 0	0 1	$2V_{SH}-V_{BE}$ $-V_{SH}$	V_{SH} $2V_{SH}-V_{BE}$	10
	SH	PN + SH	1 0	0 1	$2V_{SH}-V_{BE}$ $-V_{BE}-V_{SH}$	V_{SH} $2V_{SH}$	
15	PN	PN	1 0	0 1	V_{SH} $-V_{BE}$	V_{BE} V_{SH}	15
	PN	SH	1 0	0 1	V_{SH} $-V_{SH}$	V_{BE} $2V_{SH}-V_{BE}$	
20	PN	PN + SH	1 0	0 1	V_{SH} $-V_{BE}-V_{SH}$	V_{BE} $2V_{SH}$	20

25 Referring again to Fig. 4, an aluminium-silicon Schottky diode DH is optionally included 25
between resistor RB and source V_{REF} . Diode DH in combination with resistor RB acts to turn off
transistor QB in certain high-speed switching operations.

Figure 5 shows another inverting logic gate of very high switching speed. This inverter
contains all the elements of Fig. 3 except that transistor QA is not Schottky clamped by means
30 of diode DA. Instead, the base of transistor QA is connected to the anode of an aluminium- 30
silicon Schottky diode DK whose cathode is connected to the cathode of diode DE. An
aluminium-silicon Schottky diode DL is connected in series with diode DF. Another aluminium-
silicon Schottky diode DO has its anode connected to the anode of diode DL and its cathode
connected to the collector of transistor QB.

35 The inverter of Fig. 5 operates similarly to the inverter of Fig. 3. The input and output logical 35
levels are the same. Transistor QB is continuously on and does not go into deep saturation.
Diode DE is always conductive as long as power is supplied to the inverter.

When voltage V_{IN} is brought to logical "1", transistor QA turns on. Current from source V_{CC}
flows through transistor QA to the base of transistor QB to turn it on harder. Diode DK becomes
40 conductive while diode DO which was conductive remains conductive. 40

The collector voltage of transistor QB is $V_{BEQB} + V_{BEQA} - V_{DDK} - V_{DDO}$ which again equals $2V_{BE} - 2V_{SH}$
(V_{DDK} and V_{DDO} are the conductive voltages across diodes DK and DO respectively). Accordingly,
voltage V_{BCQB} is $2V_{SH} - V_{BE}$ just as in the inverter of Fig. 3. Again, transistor QB cannot go into
deep saturation. Its operation is limited to its low saturation range. In effect, diodes DK and DO
45 in combination with transistor QA clamp transistor QB well out of deep saturation. Diodes DF 45
and DL are non-conductive. As transistor QB turns on harder, it actively pulls each voltage V_{OUTJ}
down to its logical "0". The logical "0" output noise margin is again $1V_{SH}$.

When voltage V_{IN} is returned to logical "0", transistor QA turns off and diode DK becomes
non-conductive. As the base voltage for transistor QA drops, diodes DF and DL become
50 conductive to establish an alternative current path from source V_{CC} through them to the base of 50
transistor QB. The current flowing through this path keeps transistor QB on. The collector
voltage for transistor QB is $V_{BEQB} + V_{DDF} + V_{DDL} - V_{DDO}$ which again is $2V_{BE}$. (V_{DDI} is the conductive
voltage for diode DDL.) As with Fig. 3, each voltage V_{OUTJ} rises to its logical "1" of $2V_{BE}$ with a
logical "1" output noise margin of $1V_{SH}$.

55 The inverter of Fig. 5 can provide a slightly greater switching speed than that of Fig. 3 at the 55
cost of adding diodes DL and DO and using diode DK instead of diode DA.

The inverter circuits described can be used as basic building blocks for more advanced logic
gates. Fig. 6 illustrates a multi-input NOR gate employing the basic inverter of Fig. 3. Instead of
transistor QA, this NOR gate has M transistors QA1, QA2 . . . QAM having their simple
60 emitters connected in common to the base of transistor QB and having their single collectors 60
connected in common through resistor RC to source V_{CC} . Each transistor QA1, where I varies
from 1 to M, receives a corresponding input signal V_{INI} at its base which is coupled through a
corresponding resistor RAI to source V_{CC} . Likewise, each transistor QA1 is Schottky clamped with
a corresponding Schottky diode DAI.

65 The NOR gate operates basically in the same manner and at the same logical levels as the 65

inverter of Fig. 3. When all voltages $V_{IN1}-V_{INM}$ go to logical "0", transistors QA1-QAM all turn off. Diode DF becomes conductive to provide a current path from source V_{CC} to the base of transistor QB to prevent it from turning off. Each voltage V_{OUTJ} rises to logical "1". When any voltage V_{INI} is raised to logical "1", corresponding transistor QAI turns on to cause diode DF to become non-conductive. Current from source V_{CC} is supplied through this transistor QAI to the base of transistor QB which turns on harder but does not go into deep saturation. Voltage V_{OUT} drops to logical "0".

Figure 7 shows a multi-input NAND logic gate in which the inverter of Fig. 3 is the basic building block. In this NAND gate, the anodes of M aluminium-silicon input Schottky diodes DP1, DP2, . . . DPM are connected to the base of transistor QA. Each input voltage V_{INI} applied to the cathode of corresponding diode DPI is $1V_{SH}$ lower than the voltage (V_{IN} of Fig. 3) at the base of transistor QA when diode DPI is conductive. The output signal, which should also be $1V_{SH}$ lower so as to be compatible with other logic gates connected to this NAND gate, is voltage V_{OUT} taken directly from the collector of transistor QB. In some applications—e.g. where this NAND gate is the last of a series of logic gates—it may be desirable or necessary to take the output signal(s) from one or more Schottky diodes connected to the collector of transistor QB. For this reason, Fig. 7 shows diodes DG1-DGN in dotted line form for providing output voltages $V_{OUT1}-V_{OUTN}$. Except in unusual situations, the NAND gate normally contains either input diodes DP1-DPM or output diodes DG1-DGN but not both sets of diodes because the set not included forms either the output diodes to a preceding logic gate or the input diodes to a following gate.

The NAND gate of Fig. 7 operates basically in the same manner as the inverter of Fig. 3. The desired logical "0" and logical "1" levels are $2V_{BE}-2V_{SH}$ and $2V_{BE}+V_{SH}$, respectively. The resistance of resistor RA is chosen appropriately to match the logical "1" input level. When any voltage V_{INI} is at logical "0", corresponding diode DPI conducts so as to cause a sufficiently large voltage drop across resistor RA to turn transistor QA off. Transistor QB then operates as described above for Fig. 3. When all diodes DP1-DPM are at logical "1", the current through resistor RA decreases to reduce its voltage drop sufficiently to turn transistor QA on. Transistor QB again operates as described for Fig. 3.

Figure 8 illustrates another multi-input NAND logic gate in which the inverter of Fig. 3 is the basic building block. In addition to the basic elements of Fig. 3, this NAND gate contains a multiple-emitter transistor QQ having its collector connected to the base of transistor QA. The base of transistor QQ is tied to source V_{CC} through a resistor RQ which replaces resistor RA of Fig. 3. A Schottky diode DQ Schottky clamps transistor QQ which has M emitters, each of which receives one of M input signals $V_{IN1}, V_{IN2}, \dots V_{INM}$. The output signal is normally voltage V_{OUT} from the collector of transistor QB. Diodes DG1-DGN are illustrated in dotted line form for the situations in which the output signal(s) must be higher. Diode DK is also optionally included in the NAND gate to replace diode DA in the manner generally described above for Fig. 5.

Each emitter-base junction of transistor QQ functions basically in the same manner as one of input diodes DP1-DPM of the NAND gate of Fig. 7 except that each input voltage $1V_{INI}$ is $1V_{BE}-1V_{SH}$ lower than the base voltage (V_{IN} of Fig. 3) of transistor QA because transistor QQ is Schottky clamped. Accordingly, the desired logical "1" level is $1V_{BE}+1V_{SH}$ at the input and output. The desired logical "0" level is the minimum value of voltage V_{OUT} . When diode DK is absent, the desired logical "0" value is $2V_{BE}-2V_{SH}$, which is $1V_{SH}$ lower than that of Fig. 3. Transistors QA and QB are controlled in the same manner as described above for Fig. 3. The output noise margins are, however, slightly different because of the different logical levels.

When diode DK is present (and diode DA is preferably absent), the desired logical "0" level is $2V_{BE}-2V_{SH}$. Transistor QA is controlled in substantially the same manner as described above for Fig. 5. Transistor QB, however, operates somewhat differently. When voltage V_{OUT} goes to logical "1", voltage V_{BCQB} is again $-1V_{BE}$ so that transistor QB operates in the linear range, but, when voltage V_{OUT} goes to logical "0", voltage V_{BCQB} is clamped at $1V_{SH}$ higher than described above for Fig. 3 or 5. In particular, voltage V_{BCQB} is $1V_{SH}-1V_{BE}$ which is negative so that the base-collector junction of transistor QB is reverse-biased and it does not saturate at all. In short transistor QB always operates in the linear range when diode DK is employed in the NAND gate of Fig. 8. The output voltage swing is $1V_{SH}$ which is one half of that in Fig. 3. The output noise margins are likewise about one half of those of Fig. 3.

Table II summarizes the operating characteristics for the NAND gate of Fig. 8.

TABLE II

DA	DK	V_{OUT}	V_{BCQA}	V_{BCQB}	Noise Margin	
5		0	V_{SH}	$2V_{SH}-V_{BE}$	$3V_{SH}-V_{BE}$	5
Present	Absent	1	—	$-V_{BE}$	$V_{BE}-V_{SH}$	
10		0	0	$V_{SH}-V_{BE}$	$2V_{SH}-V_{BE}$	10
Absent	Present	1	—	$-V_{BE}$	$V_{BE}-V_{SH}$	
15	If transistor QQ has only one emitter (or, equivalently, if all of voltages $V_{IN1}-V_{INM}$ but one are held at logical "1"), the circuit of Fig. 8 functions as an inverter.					15
	Methods for manufacturing the various elements of the circuits described are well known in the semiconductor art. Preferably, each logic gate is fabricated according to conventional planar processing techniques using oxide isolation to separate active semiconductor regions.					
20	Figure 9 shows a plan view of a possible layout for the inverter of Fig. 3 when it is manufactured according to planar techniques using oxide isolation. In particular, Fig. 9 shows the P-type and N-type regions along the top surface of the inverter below overlaying insulating material and metallic electrical connections. The overlying insulating material is not shown at all. The area shaded in diagonal lines indicates insulating material separating the various active semiconductor regions from one another. The overlying metallic connections are indicated as thick lines extending from the various contact windows schematically depicted as rectangles or squares. "A" and "C" followed by a subscript which is the symbol for a diode indicate its anode and cathode, respectively. "B", "E", and "C" followed by a subscript which is a symbol for a transistor indicate its base, emitter, and collector, respectively. Three output diodes DG1, DG2, and DG3 are shown in Fig. 9. The size of this inverter is approximately 48 microns by 100 microns.					20
25	To further illustrate the construction of the logic gate of Fig. 3, Figs. 10A and 10B depict cross-sectional views of portions of the layout of Fig. 9. The cross-sections are taken through the planes indicated by arrows 10A and arrows 10B in Fig. 9. All of the elements of the inverter of Fig. 3 not shown in Figs. 10A and 10B as well as all of the other transistors, resistors, diodes electrical connections, and other elements of the logic circuit in which it is included are preferably fabricated in the manner described below.					25
30	Conventional masking, etching and cleaning techniques, which are well known in the art, are employed in creating the various P-type and N-type regions shown in Figs. 10A and 10B. To simplify the discussion, references to the masking, etching, cleaning and other well-known steps in the semiconductor art are omitted from the following fabrication discussion.					30
35	Boron is utilized as the P-type impurity for creating the various regions of P-type conductivity on a semiconductor wafer. Phosphorous, arsenic, and antimony are used selectively as the complementary N-type dopants. Other appropriate impurities may be used in place of these dopants. In many of the diffusion steps, an impurity may alternatively be introduced to the wafer by ion implantation or vice versa.					35
40	The starting material is a P-type monocrystalline silicon substrate having a thickness indicated by reference numeral 20 and a resistivity of 7-15 ohm-centimetres. An N-type impurity (antimony) is selectively diffused into the upper surface of the substrate to form N+ regions 22 and 24 having a depth of 2.5-3.0 microns and a sheet resistance of approximately 25 ohms/square. The N-type portions C_{QA} and C_{QB} of regions 22 and 24, respectively, remaining after subsequent processing steps serve as the collectors for transistors QA and QB, respectively. An N-epitaxial layer having an original thickness of about 1.2 microns indicated by reference numeral 26 is then grown over the upper surface of the substrate, including over N+ regions 22 and 24. This epitaxial layer has an original resistivity of approximately 0.5 ohm-centimetre. Oxide-isolation regions 28 having a depth of about 1.3-1.4 microns are then formed according to conventional techniques through the epitaxial layer and partially into the substrate to define active semiconductor regions 30, 32, 34, and 36 and electrically isolate them from one another and from other such active semiconductor regions on the wafer.					40
45	An N-type impurity (phosphorous) is selectively ion implanted at an energy of 50 kiloelectron volts and a dosage of 1.4×10^{15} ions/centimetre ² to define deep N+ regions 38, 40, 42, and 44. A thin electrically insulating layer 46 consisting of silicon dioxide and silicon nitride is then formed at the top of the wafer. The silicon dioxide is 500 angstroms in thickness while the overlying silicon nitride is 700 angstroms in thickness. After selectively etching oxynitride layer 46 to form windows through it, an N-type impurity (arsenic) is diffused into the epitaxial layer					45
50						50
55						55
60						60
65						65

through these windows to define shallow N + regions E_{QA} , 48, C_{DF} , 50, and 52 having a sheet resistance of about 30 ohms/square. A p-type impurity (boron) is then selectively ion implanted at an energy of 50 kiloelectron volts and a dosage of 1.5×10^{14} ions/centimetre² through layer 46 to form P regions B_{QA} , A_{DF} , and 54. The structure is then annealed for 25–30 minutes at 1000°C to cause the various impurities to diffuse to the locations generally shown in Figs. 10A and 10B.

Regions B_{QA} and E_{QA} are the base and emitter, respectively, for transistor QA. The remaining N-portion C_{DA} of the epitaxial layer between regions B_{QA} and 38 in island 30 serves as the cathode for diode DA. Deep N + region 38 in combination with shallow contact N + region 48 connect the collector C_{QA} of transistor QA to the anode A_{DE} of diode DE. Diode DF is a transistor in which the cathode is emitter region C_{DF} while the anode is base region A_{DF} connected by way of N + collector region 40 to the collector C_{QB} of transistor QB. The remaining N-portion C_{DE} of the epitaxial layer in island 34 is the cathode for diode DE. The remaining N-portion of the epitaxial layer in island 36 forms resistor RA. Deep N + regions 42 and 44 in combination with shallow N + contact regions 50 and 52, respectively, serve as connections for resistor RA while P region 54 "pinches off" resistor RA to control its resistance.

A pattern of leads indicated by diagonal-line shading is formed according to conventional techniques over the contact windows down to the underlying semiconductor regions, over the remaining portions of insulation layer 46 and over oxide-isolation regions 28 to connect the conductive regions in the desired manner. Each lead consists of a thin lower layer of platinum silicide over the underlying silicon, a thin intermediate layer of titanium-tungsten, and an upper layer of aluminium. Lead A_{DE} forms the anode for diode DE. Lead A_{DA} forms the anode for diode DA and also serves as the electrical connection to base B_{QA} of transistor QA. The structure in Figs. 10A and 10B is then finished in a conventional manner. In the final structure, resistor RA is 20 kilohms, resistor RB is 3 kilohms, and resistor RC is 10 kilohms. Source V_{CC} is 5.0 volts.

While the invention has been described with reference to particular embodiments, the description is solely for the purpose of illustration and various modifications, changes and applications may be made by those skilled in the art. For example, semiconductor materials of opposite conductivity type to those described above might be employed to accomplish the same results.

CLAIMS

1. A logic circuits comprising a first bipolar transistor having a base for receiving an input signal, an emitter, and a collector coupled to a voltage/current source; and a second bipolar transistor having a base coupled to the emitter of the first transistor, an emitter coupled to a constant voltage source, and a collector coupled to the voltage/current source for supplying an output signal; characterized by means for preventing the second transistor from either turning substantially off or going into deep saturation.

2. A logic circuit as claimed in Claim 1 characterized in that earth transistor is an NPN transistor.

3. A logic circuit as claimed in Claim 2 characterized in that the means comprises first means for providing positive current from the voltage/current source in a single current flow direction to the collector of the second transistor; and second means for providing positive current from the first means in a single current-flow direction to the base of the second transistor.

4. A logic circuit as claimed in Claim 3 characterized in that the first means comprises a first diode having its anode and cathode coupled respectively to the collectors of the first and second transistors.

5. A logic circuit as claimed in Claim 4 characterized in that the first diode is a Schottky diode.

6. A logic circuit as claimed in Claim 4 or Claim 5 characterized in that the first means includes clamping means for preventing the first transistor from going into deep saturation.

7. A logic circuit as claimed in Claim 6 characterized in that the clamping means comprises a Schottky diode having its anode and cathode connected respectively to the base and collector of the first transistor.

8. A logic circuit as claimed in Claim 4 or Claim 5 characterized in that the first means includes a Schottky diode having its anode and cathode coupled respectively to the base of the first transistor and the collector of the second transistor.

9. A logic circuit as claimed in Claim 8, characterized in that a diode having its cathode connected to the collector of the second transistor is included between said collector and both said first diode and the Schottky diode specified in Claim 8.

10. A logic circuit as claimed in any of Claims 4 to 9 characterized in that the second means comprises a further diode having its anode and cathode coupled respectively to the cathode of the first diode and the base of the second transistor.

the first diode and the base of the second transistor.

11. A logic circuit as claimed in Claim 10 characterized in that the further diode is a PN diode.

12. A logic circuit as claimed in Claim 11 characterized in that the second means includes a Schottky diode in series with the further diode.

13. A logic circuit as claimed in any preceding Claim, constructed to function as an inverter.

14. A logic circuit as claimed in Claim 7, or in Claim 10 or Claim 11 when appended to Claim 7, including $(M - 1)$ additional NPN transistors and $(M - 1)$ additional Schottky diodes, where M is a positive integer greater than one, each said additional transistor having a base for receiving an input signal, an emitter connected to the emitter of the first transistor, a collector connected to the collector of the first transistor, and one of said additional Schottky diodes connected between its base and collector in such manner that the diode anode is connected to the transistor base, so that the logic circuit constitutes a NOR gate.

15. A logic circuit as claimed in Claim 6 or Claim 7, or in Claim 10 or Claim 11 when appended to Claim 6 or Claim 7, including a plurality of input diodes having their anodes coupled to a voltage/current source and to the base of the first transistor, so that the logic circuit constitutes a NAND gate.

16. A logic circuit as claimed in any of Claims 7 to 11, including a third NPN transistor having a base coupled to a voltage/current source, an emitter for receiving an input signal, and a collector connected to the base of the first transistor.

17. A logic circuit substantially as described herein with reference to any of Figs. 3 to 8 of the drawings, or to Figs. 3, 9 and 10 of the drawings.