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(71) Applicant *(for all designated States except US)*: **EASTMAN KODAK COMPANY** [US/US]; 343 State Street, Rochester, New York 14650-2201 (US).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **XU, Weize** [CN/US]; 155 Crandon Way, Rochester, New York 14618 (US).

(74) Common Representative: **EASTMAN KODAK COMPANY**; 343 State Street, Rochester, New York 14650-2201 (US).

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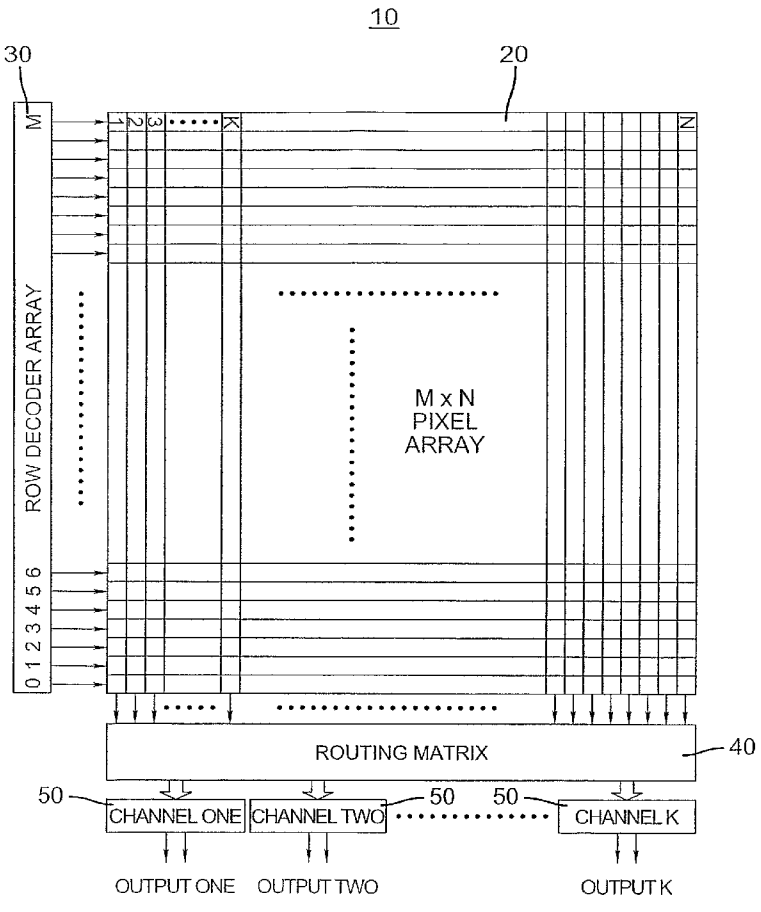
(54) **Title:** OUTPUT ROUTING STRUCTURE FOR CMOS IMAGE SENSORS



(57) **Abstract:** A CMOS image sensor includes a plurality of pixels arranged in an array; a plurality of sample and hold arrays; and a routing matrix which routes a signal from each pixel to one of the sample and hold arrays in a predetermined order.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

OUTPUT ROUTING STRUCTURE FOR CMOS IMAGE SENSORS

FIELD OF THE INVENTION

The invention relates generally to the field of CMOS image sensors having multiple sample and hold processing channels and, more particularly, to such CMOS image sensors having a routing matrix that routes signals from the pixel array to each sample and hold processing channel in which each channel includes only one color.

BACKGROUND OF THE INVENTION

As the image size and speed of CMOS image sensors continue to increase, a multi-channel output architecture is being used. However, with the multi-channel output, the video signals must be put back into their proper order. This task is becoming more and more difficult and is causing a noise problem in the final video signal string.

Although the prior art is satisfactory, they include the above-described drawbacks. Consequently, a need exists for a CMOS image sensor having multi-channel output in which re-organizing the signals is eliminated.

SUMMARY OF THE INVENTION

The present invention is directed to overcoming one or more of the problems set forth above. Briefly summarized, according to one aspect of the present invention, the invention resides in a CMOS image sensor having a plurality of pixels arranged in an array; a plurality of sample and hold arrays; and a routing matrix which routes a signal from each pixel to one of the sample and hold arrays in a predetermined order.

These and other aspects, objects, features and advantages of the present invention will be more clearly understood and appreciated from a review of the following detailed description of the preferred embodiments and appended claims, and by reference to the accompanying drawings.

Advantageous Effect Of The Invention

The present invention has the following advantage of eliminating signal reorganization at readout, increasing operational speed by reducing the load at the sample and hold circuit output, and increasing effective usability of pixel arrays having a large physical surface area.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a top view of the CMOS image sensor of the present invention;

Fig. 2 is a schematic diagram of a typical CMOS active pixel of the present invention;

Fig. 3 is a diagram illustrating routing from the pixels to four sample and hold arrays; and

Fig. 4 is a perspective view of a digital camera containing the image sensor of the present invention for illustrating a typical commercial embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring to Fig. 1, there is shown a top view of a CMOS image sensor 10 of the present invention. The sensor 10 includes a two-dimensional array of pixels 20 arranged in rows and columns, a color filter array (CFA) (not shown) is positioned spanning over the pixels so that each pixel receives a particular color. In the preferred embodiment, the CFA is a Bayer color filter, which is well known in the art. A row decoder 30 is electrically connected to the array of pixels 20 and functions to selectively read out predetermined rows of pixels to a routing matrix 40. Preferably, the rows are routed to the routing matrix one row at a time. The routing matrix 40 will then route the signals from the pixel array 20 to one of a plurality of sample and hold arrays 50. It is further noted that pixels are routed to the sample and hold array 50 so that only one color is routed to any one particular sample and hold array 50. The number of sample and hold arrays 50 can vary to four or more depending on the desired speed. In the low

speed arrangement shown in Fig. 3, there are four sample and hold arrays 50 and each array receives only one color. To double the speed, there would be 8 sample and hold arrays 50, and to triple the speed, there will be 12 arrays 50. For clarity, it is noted that in each arrangement, each channel will receive only one color as will be described in detail hereinbelow. From the sample and hold array 50, the signals are routed to further processing circuits (not shown) as is well know in the art for producing an electronic representation of an image.

Referring to Fig. 2, there is shown a schematic diagram of a typical pixel 60 of the CMOS image sensor 10. The pixel 60 includes a photodiode 70 that receives incident light that is converted into a charge. A transfer gate (TG) 80 transfers the charge to a floating diffusion 90 which will convert the charge into a voltage. The voltage is sent to an amplifier transistor 100 for buffering the signal amplitude. In the preferred embodiment, the gain of the amplifier 100 is unity, or one, although other gain factors may be used depending on the desired design. The row select transistor 110 receives a signal from the row decoder array 30 (see Fig. 1) for enabling the particular row of pixels to pass to the routing matrix 40. A reset gate transistor 120 functions to reset and clear the floating diffusion 90 of any residual charge before passing another image signal to the floating diffusion 90.

Referring to Fig. 3, there is shown a schematic diagram of the connections between the array of pixels 20 to the routing matrix 40 and then to a sample and hold array 50. Fig. 3 depicts only four sample and hold arrays, although as stated hereinabove, to increase the speed the number of sample and hold arrays may be increased. In a general overview, each of the four colors is routed to a particular sample and hold array sequentially in time in a predetermined order. For example, color one is readout out first by enabling one of four sets of switches. The number of switches in each set is determined by N/4 where N is the number of pixels in each row. In transferring color one, the first set of switches including switches S1, S5, S9 and S13 and etc. are closed (all of the switches are not shown for drawing clarity). In this embodiment, three switches are skipped so that very 4^{th} switch is closed. A corresponding second set of

switches are connected to the first set of switches, and in transferring color one, this set of switches are also substantially simultaneously closed (S'1, S'5, S'9 and S'13 and etc) for transferring color one that particular sample and hold circuit 50. The number of switches in the set second set is also N/4 where N is the total number of pixels in a row. After completion of the transfer to the sample and hold circuit 50, these two sets of switches are opened (S1, S5, S9, S13, S'1, S'5, S'9, S'13 and etc.).

The second color is then transferred to a sample and hold array 50 by repeating the above sequence with its corresponding first and second set of switches (S2, S6, S10 and S14 and S'2, S'6, S'10, S'14). The process is synchronized so that the first color is transferred before the second color is transferred. Likewise, color three (using switches S3, S7, S11, S15 and etc. S'3, S'7, S'11, S'15) and color four (using switches S4, S8, S12, S16 and etc. S'4, S'8, S'12, S'16 and etc.) are also repeated in this synchronized manner for transferring their particular colors. It is noted that for a Bayer pattern the color in sample and hold channel 1 (50) is green 1; sample and hold channel 2 (50) contains green 2; sample and hold channel 3 (50) contains red; and sample and hold channel 4 (50) contains blue. It is noted that, for four channels, the color information from the sample and hold channels 50 are output substantially simultaneously so that all the color information (four color channels) for each pixel is received by the subsequent attached off-chip signal processing circuitry at substantially the same time. It is noted that, if there are 8 channels, two sequential color information signals are sent out on each clock cycle to the off-chip processing circuitry. Those skilled in the art will recognize that, as the number of channels is increased, the number of color information signals is accordingly increased as described hereinabove.

Referring to Fig. 4, there is shown a digital camera 130 containing the image sensor 10 of the present invention for illustrating a typical commercial embodiment of the present invention with which the ordinary consumer is acquainted.

PARTS LIST

10	CMOS image sensor
20	pixel arrays
30	row decoder
40	routing matrix
50	sample and hold arrays
60	typical pixel
70	photodiode
80	transfer gate
90	floating diffusion
100	pixel amplifier transistor
110	row select transistor
120	reset gate transistor
130	digital camera

CLAIMS:

1. A CMOS image sensor comprising:

(a) a plurality of pixels arranged in an array;

(b) a plurality of sample and hold arrays; and

(c) a routing matrix which routes a signal from each pixel to one of the sample and hold arrays in a predetermined order.

2. The CMOS sensor as in claim 1, wherein the pixels are electronically divided into groups by the routing matrix and a first signal from each group is routed to the same sample and hold array.

3. The CMOS sensor as in claim 2, wherein a second signal from each group is routed to the same sample and hold array.

4. The CMOS sensor as in claim 1, wherein the pixels are electronically connected into groups by the routing matrix and the routing matrix sends signals to the plurality of sample and hold circuits in a repeating pattern or substantially repeating pattern.

5. The CMOS sensor as in claim 4, wherein the repeating pattern is determined so that the signals to each sample hold circuit from the routing matrix contain the same color signal.

6. The CMOS sensor as in claim 3, wherein the first and second signals are routed respectively through a set of switches in the routing matrix which are substantially synchronized in time.

7. The CMOS sensor as in claim 6, wherein the synchronization occurs so that the first signals are sent first out of the routing matrix and the second signals are sent second out of the routing matrix.

8. The CMOS sensor as in claim 4, wherein the repeating pattern is synchronized in time so that the particular signals are sent out from the routing matrix at substantially the same time.

9. An digital camera comprising:

a CMOS image sensor comprising:

(a) a plurality of pixels arranged in an array;

(b) a plurality of sample and hold arrays; and

(c) a routing matrix which routes a signal from each pixel to one of the sample and hold arrays in a predetermined order.

10. The digital camera as in claim 9, wherein the pixels are electronically divided into groups by the routing matrix and a first signal from each group is routed to the same sample and hold array.

11. The digital camera as in claim 10, wherein a second signal from each group is routed to the same sample and hold array.

12. The digital camera as in claim 9, wherein the pixels are electronically connected into groups by the routing matrix and the routing matrix sends signals to the plurality of sample and hold circuits in a repeating pattern or substantially repeating pattern.

13. The digital camera as in claim 12, wherein the repeating pattern is determined so that the signals to each sample hold circuit from the routing matrix contain the same color signal.

14. The digital camera as in claim 11, wherein the first and second signals are routed respectively through a set of switches in the routing matrix which are substantially synchronized in time.

15. The digital camera as in claim 14, wherein the synchronization occurs so that the first signals are sent first out of the routing matrix and the second signals are sent second out of the routing matrix.

16. The digital camera as in claim 12, wherein the repeating pattern is synchronized in time so that the particular signals are sent out from the routing matrix at substantially the same time.

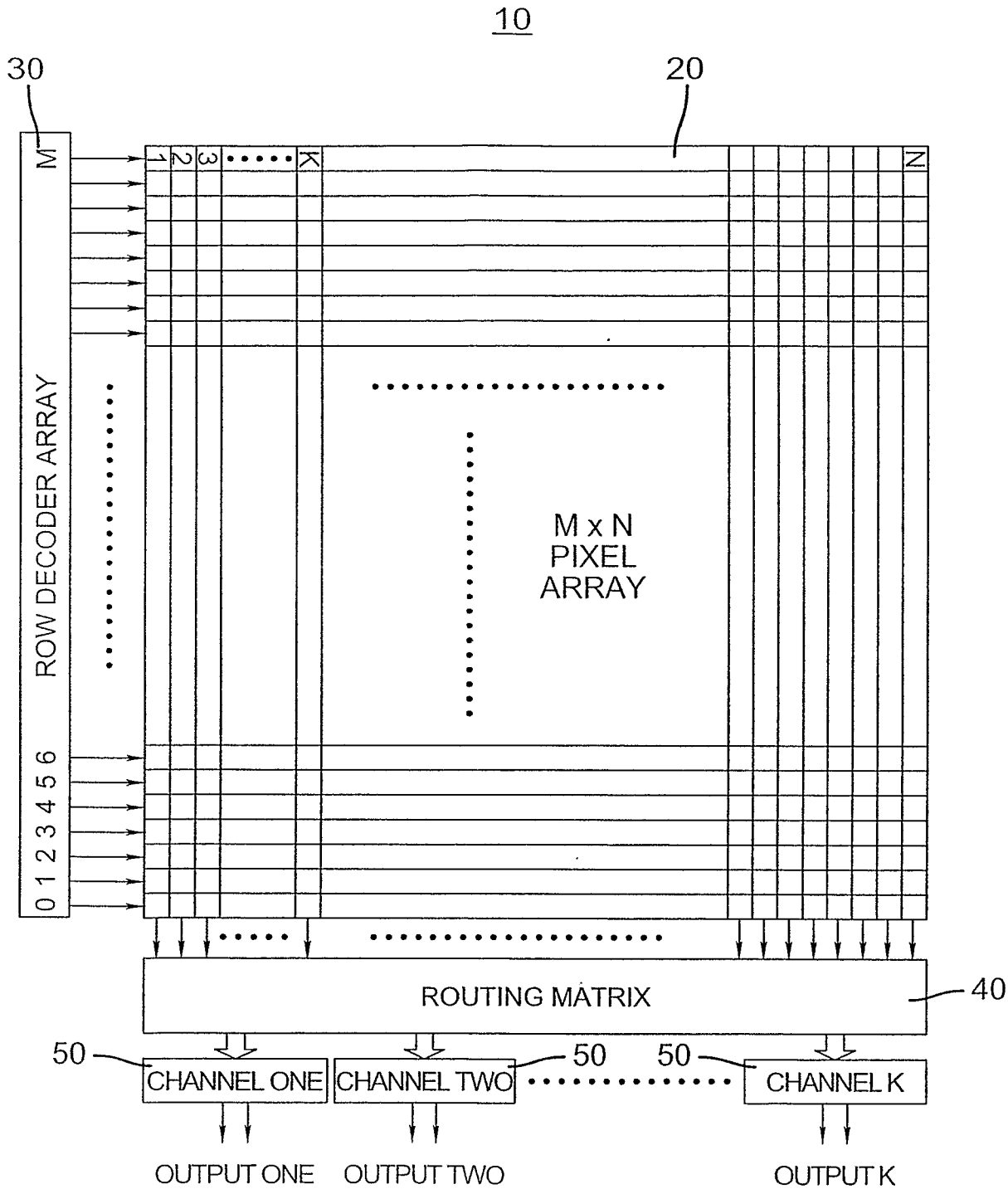
10
30
20
M
ROW DECODER ARRAY
0 1 2 3 4 5 6
1
2
3
K
N
M x N
PIXEL
ARRAY
ROUTING MATRIX
40
50
50
50
CHANNEL ONE
CHANNEL TWO
CHANNEL K
OUTPUT ONE
OUTPUT TWO
OUTPUT K

FIG. 1

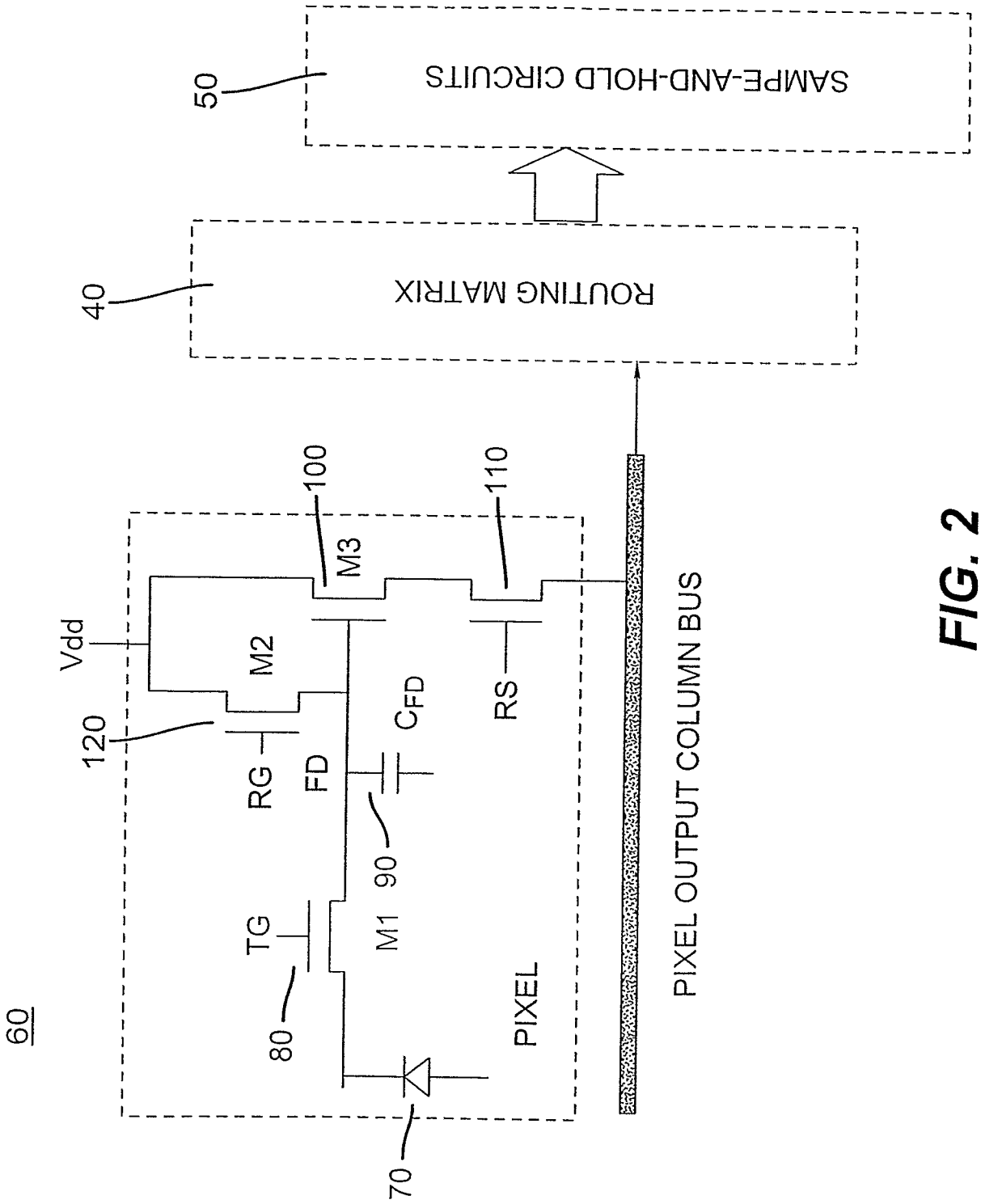
50
SAMPLE-AND-HOLD CIRCUITS
40
ROUTING MATRIX
PIXEL OUTPUT COLUMN BUS
60
100
M3
110
Vdd
M2
RS
120
RG
FD
C_{FD}
90
M1
TG
80
PIXEL
70

FIG. 2

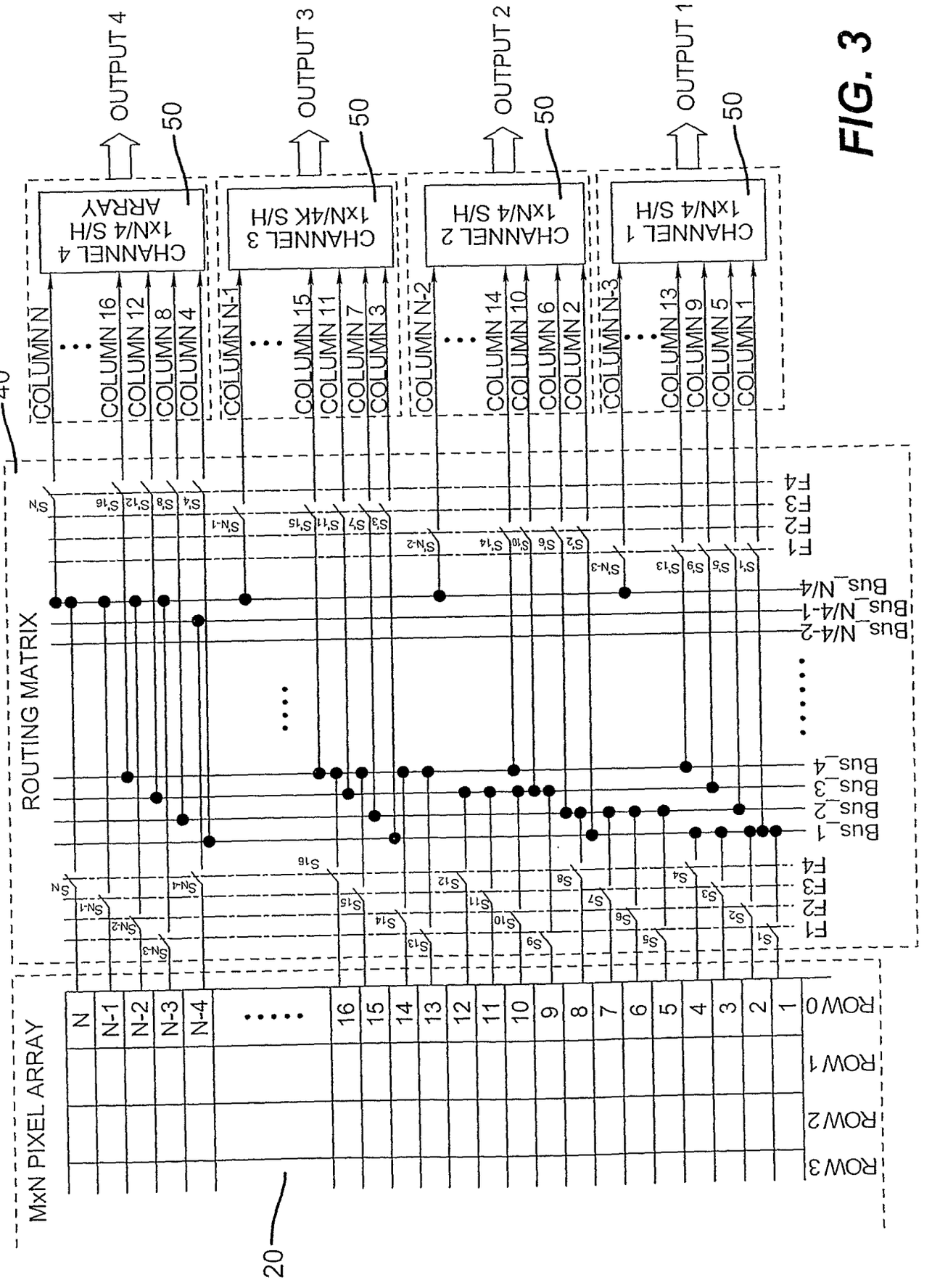
OUTPUT 4
OUTPUT 3
OUTPUT 2
OUTPUT 1
50
CHANNEL 4 1xN/4 S/H ARRAY
CHANNEL 3 1xN/4K S/H
CHANNEL 2 1xN/4 S/H
CHANNEL 1 1xN/4 S/H
COLUMN N
COLUMN 16
COLUMN 12
COLUMN 8
COLUMN 4
COLUMN N-1
COLUMN 15
COLUMN 11
COLUMN 7
COLUMN 3
COLUMN N-2
COLUMN 14
COLUMN 10
COLUMN 6
COLUMN 2
COLUMN N-3
COLUMN 13
COLUMN 9
COLUMN 5
COLUMN 1
40
ROUTING MATRIX
F1
F2
F3
F4
Bus_1
Bus_2
Bus_3
Bus_4
Bus_N/4
Bus_N/4-1
Bus_N/4-2
MxN PIXEL ARRAY
ROW 0
ROW 1
ROW 2
ROW 3
20

FIG. 3

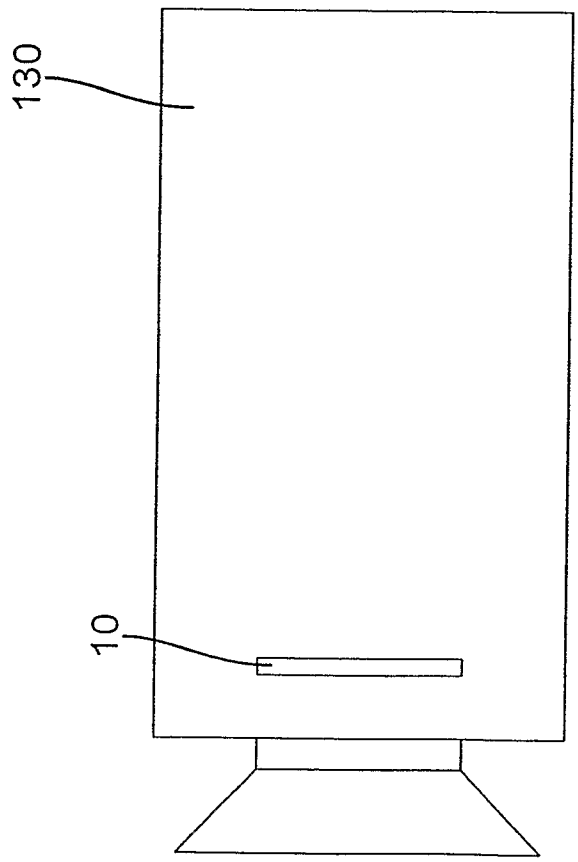

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/036252

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04N9/04 H04N3/15

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 757 497 A2 (CANON KK [JP]) 5 February 1997 (1997-02-05) page 2, line 52 - line 53; figure 1 page 4, line 7 - line 19	1-16
X	US 2005/145777 A1 (BARNA SANDOR L [US] ET AL) 7 July 2005 (2005-07-07) paragraphs [0009], [0011]; figure 3	1-16
X	EP 0 967 795 A2 (EASTMAN KODAK CO [US]) 29 December 1999 (1999-12-29) column 7, line 3 - line 10	1-16
X	EP 1 349 399 A2 (MATSUSHITA ELECTRIC IND CO LTD [JP]) 1 October 2003 (2003-10-01) column 5, line 6 - line 15; figure 1 paragraphs [0053] - [0058]	1-16

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 January 2007	26/01/2007

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Bequet, Thierry

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2006/036252

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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