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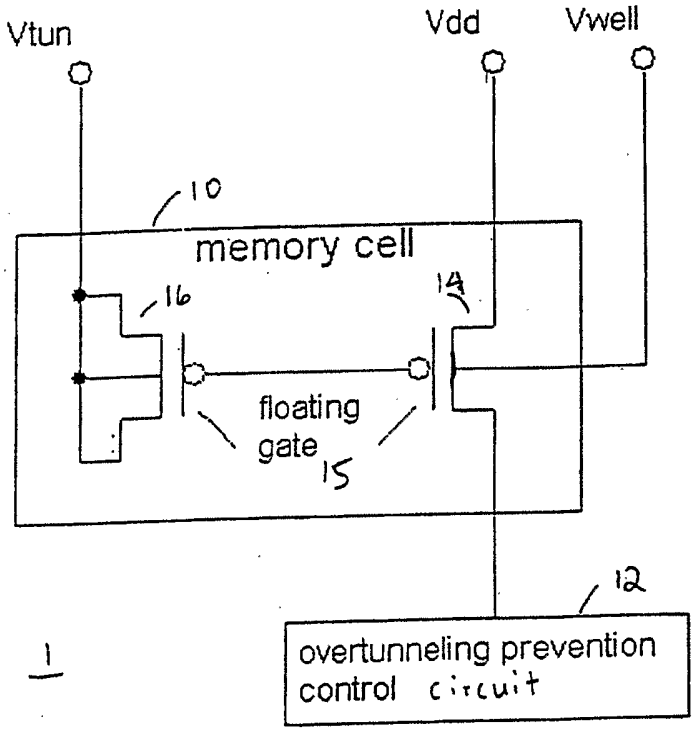
(54) Title: COUNTERACTING OVERTUNNELING IN NONVOLATILE MEMORY CELLS



(57) Abstract: Methods and apparatuses prevent overtunneling in nonvolatile floating gate memory (NVM) cells. An individual cell includes a circuit with a transistor that has a floating gate that stores charge, and a capacitor structure for extracting charge from the gate, such as by tunneling. A counteracting circuit prevents extracting charge from the floating gate beyond a threshold, therefore preventing overtunneling or correcting for it. In one embodiment, the counteracting circuit supplies electrons to the floating gate, to compensate for tunneling beyond a point. In another embodiment, the counteracting circuit includes a switch, and a sensor to trigger the switch when the appropriate threshold is reached. The switch may be arranged in any number of suitable ways, such as to prevent a high voltage from being applied to the capacitor structure, or to prevent a power supply from being applied to a terminal of the transistor or to a well of the transistor.

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Counteracting Overtunneling in Nonvolatile Memory Cells

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is based on United States Patent Application Serial no. 10/830,280, filed on April 21, 2004, which is a continuation-in-part of United States Patent Application Serial no. 10/245,183, entitled "Method and Apparatus for Preventing Overtunneling in p*FET*-Based Nonvolatile Memory Cells", filed on September 16, 2002, now United States Patent No. 6,853,583, in the name of the same inventors and commonly owned herewith.

FIELD OF THE INVENTION

[0002] The present invention relates generally to nonvolatile memory (NVM). More particularly, the present invention relates to methods of and apparatuses for preventing overtunneling in NVM memory cells.

BACKGROUND OF THE INVENTION

[0003] The demand for embedded nonvolatile memory (NVM) in integrated circuits has grown steadily over the past decade. Desirable characteristics of embedded NVM include low cost, low power, high speed, and high reliability (data retention and program/erase cycling endurance). NVM may be embedded in various integrated circuit (IC) technologies such as, for example, the widely used Complementary Metal Oxide Semiconductor (CMOS) technology. Some embedded CMOS applications include, for example, storing: (1) chip serial numbers, (2) configuration information in ASICs (Application Specific Integrated Circuits), (3) product data in radio frequency

identification integrated circuits, (4) code or data in embedded microcontrollers, and (5) analog trim information.

[0004] A major barrier for using embedded NVM is cost. An IC fabricator typically requires additional processing steps to manufacture NVM storage transistors. For example, IC fabricators sometimes use two layers of polysilicon for the gate of an NVM storage transistor, rather than one layer as in standard CMOS technology. The additional fabrication step increases the total cost of the IC. Typical embedded EEPROM (electrically erasable programmable read only memory) or Flash NVM uses *n*FET (n-channel field effect transistor) storage transistors. To ensure charge retention in *n*FETs, the IC fabricator typically uses a thicker gate oxide than is found in logic transistors, again increasing cost.

[0005] To reduce the costs and added complexities of embedding NVM in integrated circuits, efforts have been made to design an NVM that can be integrated with CMOS process technology without introducing additional processing steps. These integration efforts have also involved endeavoring to use *p*FET-based NVM, rather than the more traditional *n*FETs-based NVM. The reason for this is that *p*FET-based memory cells exhibit various performance advantages compared to *n*FET-based memory cells. *p*FETs have the following advantages over their *n*FET-based NVM counterparts: 1) increased program/erase cycle endurance (due to reduced oxide wearout); 2) availability in logic CMOS processes (due to reduced memory leakage arising from more favorable oxide physics); 3) ability to easily store analog as well as digital values (due to precise memory

writes); and 4) smaller on-chip charge pumps (due to decreased charge-pump current requirements).

[0006] Whether using *p*FETs or *n*FETs as NVM transistors, the possibility of "overtunneling" in either type of such cells poses a significant problem. The referred to "overtunneling" problem, in *p*FET-based memory cells for example, manifests itself as follows. Such cells use electron tunneling to raise the floating-gate voltage, and impact-ionized hot-electron injection (IHEI) to lower the floating-gate voltage. One characteristic of the IHEI programming method is that the MOSFET channel must be conducting current to allow electrons to inject onto the floating gate. If during a prior tunneling cycle the floating-gate voltage was raised so high that the *p*FET was turned off, there will be no channel current when a write to the cell is attempted. Effectively, by overtunneling the memory cell, the memory cell becomes "stuck" in an off state, and in the absence of channel current no electron injection can be performed during a programming (i.e. injection) cycle to lower the floating-gate voltage.

[0007] The overtunneling problem, at least as observed in *p*FET-based NVM cells, detracts from their use as reliable memory devices. Accordingly, there is a need for methods and apparatuses for preventing overtunneling in NVM cells.

BRIEF DESCRIPTION OF THE INVENTION

[0008] The invention overcomes the problems of the prior art. The invention provides memory devices having individual cells that can store data. An individual cell includes a circuit with a transistor that has a floating gate that stores charge, and a capacitor structure for extracting charge from the gate, such as by tunneling. A counteracting circuit prevents extracting charge from the floating gate beyond a threshold, therefore preventing overtunneling or correcting for it. In one embodiment, the counteracting circuit supplies electrons to the floating gate, to compensate for tunneling beyond a point. In another embodiment, the counteracting circuit includes a cutoff switch, and a sensor to trigger the cutoff switch when the appropriate threshold is reached. The cutoff switch may be arranged in any number of suitable ways, such as to prevent a high voltage from being applied to the capacitor structure, or to prevent a power supply from being applied to a terminal of the transistor or to a well of the transistor.

[0009] These and other aspects and advantages of the invention are described in more detail with reference to the remaining portions of the specification and the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 shows a memory circuit for preventing overtunneling in a *p*FET-based memory cell, according to an embodiment of the present invention.

FIG. 2 shows another memory circuit for preventing overtunneling in a *p*FET-based memory cell, according to an embodiment of the present invention.

FIG. 3A is shows yet another memory circuit for preventing overtunneling in a *p*FET-based memory cell, according to an embodiment of the present invention.

FIG. 3B shows a timing diagram illustrating the operation of the memory circuit in FIG. 3A, according to an embodiment of the present invention.

FIG. 4 shows the memory circuit of FIG. 3A, modified to take advantage of an available negative voltage source, according to an embodiment of the present invention.

FIG. 5 shows the memory circuit of FIG. 1, modified so that it includes a select/bias transistor, according to an embodiment of the present invention.

FIG. 6 shows the memory circuit of FIG. 1, modified so that it includes a capacitor coupled between the floating gate of the memory cell and a voltage source Vdd, according to an embodiment of the present invention.

FIG. 7 shows how the capacitor in the memory circuit shown in FIG. 6 may be formed from a *p*FET configured as a MOS capacitor (MOSCAP), according to an embodiment of the present invention.

FIG. 8 shows how the capacitor in the memory circuit shown in FIG. 6 may be formed from half of a *p*FET configured as a MOSCAP, according to an embodiment of the present invention.

FIG. 9 shows the memory circuit of FIG. 6, modified so that the added capacitor is coupled to a control source Vcontrol, rather than Vdd, according to an embodiment of the present invention.

FIG. 10 shows a memory circuit similar to the memory circuit of FIG. 9, where the added capacitor is formed from an *n*FET, according to an embodiment of the present invention.

FIG. 11 shows a memory circuit that includes both a select/bias transistor similar to that shown in the memory circuit in FIG. 5 and a capacitor similar to that shown in the memory circuit in FIG. 6, according to an embodiment of the present invention.

FIG. 12A shows a memory circuit similar to the memory circuit in FIG. 3A, including a high-voltage switch, according to an embodiment of the present invention.

FIG. 12B shows a timing diagram illustrating the operation of the memory circuit in FIG. 12A, according to an embodiment of the present invention.

FIG. 13 shows a memory circuit similar to the memory circuit in FIG. 12A, including a Vdd switch and a Vwell switch, according to an embodiment of the present invention.

FIG. 14 shows a memory circuit, including capacitor similar to the added capacitor in the memory circuit in FIG. 6, according to an embodiment of the present invention.

FIG. 15A shows a memory circuit employing a source-follower-connected *p*FET and an additional pulse driver, according to an embodiment of the present invention.

FIG. 15B shows a timing diagram of the operation of the memory circuit in FIG. 15A, according to an embodiment of the present invention.

FIG. 16 shows the memory circuit of FIG. 3A, modified so that it includes a tristate logic gate, according to an embodiment of the present invention.

FIG. 17 shows the memory circuit of FIG. 3A, modified so that it incorporates an *n*FET in series with a diode, according to an embodiment of the present invention.

FIG. 18 shows the memory circuit of FIG. 3A, modified so that it incorporates a *p*FET between the current sense amplifier and the drain of the injection transistor, according to an embodiment of the present invention.

FIG. 19 shows an overtunneling prevention memory circuit including a 2 x 2 array of memory cells and associated overtunneling prevention control circuits, according to an embodiment of the present invention.

FIG. 20 shows an overtunneling prevention memory circuit including a 2 x 2 array of memory cells and associated overtunneling prevention control circuits, according to an embodiment of the present invention.

FIG. 21 shows an overtunneling prevention memory circuit including a 2 x 2 array of memory cells with a single shared overtunneling prevention control circuit, according to an embodiment of the present invention.

DETAILED DESCRIPTION

[0011] Embodiments of the present invention are described herein in the context of methods and apparatuses for preventing overtunneling in *p*FET-based nonvolatile memory cells. Those of ordinary skill in the art will realize that the following detailed description of the present invention is illustrative only and is not intended to be in any way limiting. Other embodiments of the present invention will readily suggest themselves to such skilled persons having the benefit of this disclosure.

[0012] Reference will now be made in detail to implementations of the present invention as illustrated in the accompanying drawings. The same reference indicators will be used throughout the drawings and the following detailed description to refer to the same or similar parts.

[0013] In general, the invention provides memory devices having individual cells that can store data. An individual cell includes a circuit with a transistor that has a floating gate that stores charge, and a capacitor structure for extracting charge from the gate, such as by tunneling. The transistor may be a pFET injection transistor, or an nFET transistor. There is a large variety of cells covered under the invention, for example where a coupling capacitor is coupled between the floating gate and a source of the injection transistor, or an additional transistor is provided, and so on. The capacitor structure may advantageously be made from a MOSFET structure, in association with making the transistor.

[0014] Importantly, the invention also includes a counteracting circuit, to prevent extracting charge from the floating gate beyond a threshold. As will be seen below, the threshold may be a preset amount of charge, a preset electrical potential, or a preset amount of electrical current. The preset amount of electrical current may be associated with a minimum channel current required to maintain a conducting channel in the transistor. The invention will now be described in more detail.

[0015] Referring first to FIG. 1, there is shown a memory circuit 1 for preventing overtunneling in a *p*FET-based memory cell, according to an embodiment of the present invention. Memory circuit 1 comprises a memory cell 10 and a counteracting circuit implemented as an overtunneling prevention control circuit 12. Memory cell 10 comprises an injection transistor 14 and a tunneling capacitor 16. Injection transistor 14 has a floating gate 15, a source coupled to a voltage source Vdd, a body coupled to a well voltage source Vwell, and a drain coupled to overtunneling prevention control circuit 12. As shown, tunneling capacitor 16 is formed from a *p*FET, with the source, drain and body of the *p*FET shorted together and coupled to a tunneling voltage source Vtun. However, a tunneling capacitor constructed from other structures such as, for example, an *n*FET can also be used. The gate of tunneling capacitor 16 is coupled to the floating gate 15 of injection transistor 14.

[0016] In one embodiment of the invention, the counteracting circuit is adapted to add charge to the gate. This way, while tunneling may continue, electrons being

added prevent the state of overtunneling from taking place. The counteracting circuit may be coupled to a drain of the transistor, and includes a source of electrons, as will be described in more detail below.

[0017] FIG. 2 shows a memory circuit 2 for preventing overtunneling in a *p*FET-based memory cell, according to an embodiment of the present invention. Similar to the embodiment in FIG. 1, the memory circuit 2 comprises a memory cell 10 having an injection transistor 14 and a tunneling capacitor 16. Memory circuit 2 also includes an *n*FET (i.e. an n-channel MOSFET) overtunneling prevention transistor 24 having a drain coupled to the drain of injection transistor 14, a source coupled to a negative supply voltage Vss, and a gate coupled to a reference voltage Vref.

[0018] Memory circuit 2 in FIG. 2 operates as follows. Assume the voltage on the floating gate 15 is low, and it is desired to tunnel it up. To tunnel up floating gate 15 a tunnel voltage Vtun of about (Vfg + 10V), where Vfg is the floating gate voltage and 10V is typical for a 0.35μm CMOS process with 75Å oxides, is applied to the tunneling capacitor 16. Vtun causes electrons to tunnel from floating gate 15, through the tunneling capacitor's dielectric (i.e., the gate oxide, if tunneling capacitor is formed from a *p*FET or an *n*FET), to Vtun, thereby raising Vfg. To prevent overtunneling, a reference voltage Vref is applied to the gate of overtunneling prevention transistor 24. Overtunneling prevention transistor 24 operates by sinking a small current Imin (e.g. ~250nA) from injection transistor 14.

As long as injection transistor 14 is able to source more current than overtunneling prevention transistor 24 sinks, Vdrain remains high, and injection transistor 14 will not inject electrons onto floating gate 15. When, however, Vfg rises so high that injection transistor 14 can no longer source Imin, Vdrain will fall, causing injection transistor 14 to begin injecting electrons onto floating gate 15. Eventually, Vdrain will stabilize at a voltage where the IHEI gate current is equal and opposite to the tunneling gate current. Hence, overtunneling prevention transistor 24 prevents injection transistor 14 from turning off by injecting electrons back onto floating gate 15, thereby forcing the channel current of injection transistor 14 to maintain a value equal to Imin.

[0019] In 0.35μm and smaller CMOS logic processes, a voltage of not more than about 12V can be applied to the body of tunneling capacitor 16, without risking body-to-substrate breakdown. Because a voltage of ~10V is needed across the gate oxide of tunneling capacitors 16 to cause appreciable electron tunneling, Vfg must be roughly (12V–10V) = 2V. To obtain channel currents in the range of 10nA to 10μA, Vdd should then be ~3.3V. To obtain reasonable IHEI in injection transistor 14, Vdrain should be ~ –2V, meaning Vss should be ~ –2.5V. Unfortunately, most modern n-well CMOS processes do not offer *n*FETs that operate with a Vss of more than a few hundred millivolts below ground, because the *n*FET's substrate-to-source and substrate-to-drain p-n junctions become forward biased. If such limitations are encountered, other embodiments of the present invention may be used. One alternative embodiment is to use a deep n-well or a dual-well process

and fabricate an overtunneling prevention transistor, like transistor 24 shown in FIG. 2, in a p-well that can be biased ~2.5V below ground. A second alternative embodiment is to provide an overtunneling prevention control circuit to emulate the functions of the overtunneling prevention transistor 24 without having to resort to additional processing steps necessary to create a p-well operating below ground. FIG. 3A shows an example of the latter alternative, in accordance with an embodiment of the present invention.

[0020] In another embodiment of the invention, a counteracting circuit includes a current sensor to monitor a drain current of the memory cell and to generate a trigger event when the threshold is reached, and a pulse driver to add charge to the gate responsive to the trigger event. In this case, the threshold may be a preset amount of electrical current, which may be associated with a minimum channel current required to maintain a conducting channel in the transistor.

[0021] Referring to FIG. 3A, there is shown a memory circuit 3 for preventing overtunneling in a *p*FET-based memory cell, according to an embodiment of the present invention. Memory circuit 3 comprises a memory cell 10 having an injection transistor 14 and a tunneling capacitor 16, which may be formed from a *p*FET transistor as shown. The drain of injection transistor 14 is coupled to an overtunneling prevention control circuit 12, which comprises a current sensor. The current sensor includes a current sense amplifier 26, and a controller 28 coupled to current sense amplifier 26 that outputs a control signal. Circuit 12 also includes a pulse driver 30 coupled to controller 28, a capacitor 32 coupled between pulse

driver 30 and the drain of injection transistor 14 and a diode 34 coupled between the drain of injection transistor 14 and ground.

[0022] Memory circuit 3 in FIG. 3A operates as follows. During tunneling, current sense amplifier 26 monitors the drain current Idrain of injection transistor 14. Tunneling causes Idrain to initially gradually decrease, as shown in the timing diagram provided in FIG. 3B. Current sense amplifier 26 is configured to trigger when Idrain decreases to a value of Imin. When current sense amplifier 26 triggers, controller 28 instructs pulse driver 30 to pull Vp from Vdd (nominally 3.3V) down to ground. This is indicated in FIG. 3B as occurring at time t1. Capacitor 32 then pulls the drain voltage Vdrain of injection transistor 14 from 0.7V (the "on" voltage of diode 34) to –2.6V, causing electron injection to commence in injection transistor 14, and thereby causing Idrain to increase. After a short period of time, at time t2 controller 28 instructs pulse driver 30 to pull Vp from ground back up to Vdd, and waits for current sense amplifier 26 to trigger again. In this fashion overtunneling prevention control circuit 12 pulses Vdrain as needed to ensure that injection transistor 104 is not overtunneled into an "off" state. Note that, although a "current sense" amplifier is employed to determine when Vdrain must be pulsed low to avoid overtunneling, other sensing or monitoring devices and circuits may be used. For example, the cell current may be supplied to any one of many possible current-to-voltage circuit elements (e.g. resistor, diode, current source, etc) so that a voltage is measured and/or monitored, rather than transistor 14's drain current itself.

[0023] FIG. 4 shows the memory circuit of FIG. 3A, modified to take advantage of an available negative voltage source Vminus, which would nominally be about –3.3V in a 0.35μm CMOS process, according to an embodiment of the present invention. Memory circuit 4 in FIG. 4 comprises essentially the same elements as in memory circuit 3 of FIG. 3A, but also includes a source-follower-connected *p*FET 36 configured to operate as a negative-voltage switch. In one embodiment, Vminus may be provided by an off-chip voltage source. In an alternative embodiment, Vminus may be generated on the same semiconductor chip shared by memory cell 10 by using, for example, a negative-voltage charge pump. Source-follower-connected transistor 36 forms a negative-voltage switch as follows. When pulse driver 30 pulls Vp from Vdd (e.g. 3.3V) to ground and the gate of source-follower-connected transistor 36 is pulled to about –2.6V, the source of source-follower-connected transistor 36, and with it Vdrain, gets pulled down to about –2V.

[0024] FIG. 5 shows the memory circuit of FIG. 1, modified so that it includes a select/bias transistor 38 comprising a *p*FET, according to an embodiment of the present invention. Select/bias transistor 38 has a gate selectively coupled to a Vbias/select voltage source, a source coupled to Vdd, a drain coupled to the source of injection transistor 14, and a well coupled to voltage source Vwell. Select/bias transistor 38 in memory circuit 5 may be used to select memory cell 10 for injection (e.g. from among an array of memory cells) by controlling the current in injection

transistor 14, and/or to limit the current in injection transistor 14 during other operations such as reading, for example.

[0025] FIG. 6 shows the memory circuit of FIG. 1, modified so that it includes a capacitor 40 coupled between floating gate 15 of memory cell 10 and voltage source Vdd, according to an embodiment of the present invention. Capacitor 40 of memory circuit 6 may be used to ensure that, when Vdd is pulled low, the floating gate follows.

[0026] FIG. 7 shows how capacitor 40 in memory circuit 6 in FIG. 6 may be formed from a *p*FET 42 configured as a MOS capacitor (MOSCAP), according to an embodiment of the present invention. *p*FET 42 of memory circuit 7 has a gate coupled to floating gate 15, a source, a drain shorted to the source and coupled to voltage source Vdd, and a body coupled to the body of injection transistor 14 and to a well voltage source Vwell.

[0027] FIG. 8 shows how capacitor 40 in memory circuit 6 in FIG. 6 may be formed from half of a *p*FET 44 configured as a MOSCAP, according to an embodiment of the present invention. Half *p*FET 44 may be constructed from, for example, a *p*FET with either the drain or source terminal left floating, or a *p*FET having either a drain or source terminal but not both. The latter embodiment saves layout area of the integrated circuit on which memory circuit 8 is formed.

[0028] FIG. 9 shows the memory circuit 6 of FIG. 6, modified so that capacitor 40 is coupled to a control source Vcontrol, rather than Vdd, according to an embodiment of the present invention. This alternative connection allows the independent control of Vdd and the floating-gate voltage Vfg. Capacitor 40 can be constructed from a *p*FET or from half of a *p*FET, as described in FIGS. 7 and 8. Additionally, capacitor 40 may be formed in the same n-well as injection transistor 104, or in a separate n-well.

[0029] FIG. 10 shows a memory circuit 100 similar to the memory circuit 9 of FIG. 9, where capacitor 40 in FIG 9 is formed from an *n*FET 42, according to an embodiment of the present invention. As shown in FIG. 10, *n*FET 42 is configured as a MOSCAP, having a gate coupled to floating gate 15 and shorted source, drain and body terminals coupled to the control source Vcontrol. In various alternative embodiments, *n*FET 42 may be formed with no drain or source terminal, with either a drain terminal or a source terminal but not both, or with both a drain terminal and a source terminal.

[0030] FIG. 11 shows a memory circuit 111 that includes the select/bias transistor 38 of memory circuit 5 in FIG. 5 and the capacitor 40 of memory circuit 6 in FIG. 6, according to an embodiment of the present invention. Capacitor 40 may comprise any of the forms described above and may connect to either Vdd or a separate control input.

[0031] In another embodiment, the counteracting circuit includes a cutoff switch, and a sensor to trigger the cutoff switch when the appropriate threshold is reached. The cutoff switch may be arranged in any number of suitable ways, such as to prevent a high voltage from being applied to the capacitor structure, or to prevent a power supply from being applied to a terminal of the transistor or to a well of the transistor. The sensor may be the same as was described in connection with FIG. 3A. In addition, if in the particular implementation overtunneling is permitted to take place initially, additional structure may be provided to supply electrons back to the floating gate.

[0032] FIG. 12A shows a memory circuit 112 similar to the memory circuit in FIG. 3A, including a cutoff switch implemented as high-voltage switch 44, according to an embodiment of the present invention. High-voltage switch 44, as controlled by controller 28, is opened to prevent tunneling during times when memory cell 10 is being sensed or when charge carriers are being injected onto floating gate 15. High-voltage switch 44 prevents tunneling during sense and inject operations to avoid capacitive coupling between tunneling capacitor 16 and floating gate 15. Capacitive coupling undesirably causes floating gate 15 to be pulled high during tunneling, artificially decreasing the drain current Idrain of injection transistor 14 as shown in the timing diagram provided in FIG. 12B. To read the drain current Idrain accurately, tunneling must first be terminated. Memory circuit 112, including overtunneling prevention control circuit 12 and high-voltage switch 44 performs the following sequence of operations as illustrated in the timing

diagram shown in FIG. 12B. During phase 1 a positive-going tunneling pulse is applied to tunneling capacitor 16. Next, during phase 2 controller 28 causes high-voltage switch 44 to open to turn off tunneling. During phase 2, Idrain is measured by sense amplifier 26. Finally, during phase 3, if Idrain is smaller than a predetermined minimum drain current Imin, controller 28 causes pulse driver 30 to pulse, thereby lowering the drain voltage Vdrain of inject transistor 14. The lowering of Vdrain causes inject transistor 14 to begin injecting charge carriers onto floating gate 15.

[0033] FIG. 13 shows a memory circuit 113 similar to the memory circuit in FIG. 12A, including cutoff switches implemented as a Vdd switch 46 and a Vwell switch 48, according to an embodiment of the present invention. This alternative embodiment may be used to decouple Vdd and Vwell from memory cell 10 or to set them to a low voltage such as ground during tunneling, to capacitively couple floating gate 15 down by a volt or more and thereby reduce the required tunneling voltage Vtun by this same volt or more.

[0034] FIG. 14 shows a memory circuit 114, including the capacitor 40 in memory circuit 6 of FIG. 6, according to an embodiment of the present invention. Because capacitor 40 provides significant capacitive coupling between Vdd and floating gate 15, there is less need to switch Vwell down to ground during tunneling. (Capacitor 40 effectively replaces the parasitic well-to-floating-gate capacitance of injection transistor 14.) Consequently, the Vwell switch in the

embodiment shown in FIG. 13 is not required. Those skilled in the art will readily understand that many other combinations of switches and memory cells are possible.

[0035] FIG. 15A shows a memory circuit 115 employing a source-follower-connected *p*FET 50 and an additional pulse driver 52, according to an embodiment of the present invention. Pulse drivers 52 and 54 are controlled by a controller 56, which is coupled to a current sense amplifier 58. A first capacitor 60 is coupled between pulse driver 54 and the drain of injection transistor 14. A second capacitor 62 is coupled between pulse driver 52 and the gate of *p*FET 50. The source of *p*FET 50 is coupled to the drain of injection transistor 14 and the source and body of *p*FET 50 are shorted together and coupled to ground. A diode 64 is coupled between the gate of *p*FET 50 and ground. The use of source-follower-connected transistor 50 allows a lower drop in the drain voltage Vdrain to be realized, compared to some of the previous embodiments described above. The reason for this is that the saturated drain voltage of source-follower-connected transistor 50 can be 100 millivolts or less, whereas the "on-voltage" of diode 34 in the previous embodiments is closer to 700 millivolts. With this difference, Vdrain transitions from 0.1V to –3.2V during an injection cycle rather than from 0.7V to –2.6V. Because IHEI increases exponentially with drain-to-gate voltage, memory circuit 115 has more efficient injection compared with, for example, memory circuit 3 in FIG. 3A.

[0036] FIG. 15B shows a timing diagram of the operation of memory circuit 115 in FIG. 15A. During phase 1 Vpp transitions from 3.3V to ground, pulling the gate of source-follower-connected transistor 50 to ~ 2.6V below ground, thereby turning source-follower-connected transistor 50 on and pulling Vdrain close to ground (limited only by the saturation voltage of source-follower-connected transistor 50). During phase 2 Vpp transition from ground to 3.3V, returning the gate of transistor 50 back to ~0.7V and discharging any accumulated charge on capacitor 62 through diode 64; also, Vp transitions from 3.3V to ground, pulling Vdrain from ~0.1V to ~–3.2V and causing injection transistor 14 to inject. During phase 3 Vp transitions from ground to 3.3V, thereby turning off injection.

[0037] FIG. 16 shows the memory circuit of FIG. 3A, modified so that it includes a tristate logic gate 66, according to an embodiment of the present invention. Tristate logic gate 66 of memory circuit 116 is driven by pulse driver logic 68, which is controlled by a controller 70. Similar to the previous embodiments, drain current of injection transistor 14 is monitored by a current sense amplifier 72. A capacitor 74 is coupled between tristate logic gate 66 and the drain of injection transistor 14 and a diode 76 is coupled between the drain of injection transistor 14 and ground. As shown, tristate logic gate 66 is an inverter. However, alternative logic gates with tristate outputs may also be used (e.g., such as NANDs or NORs). A benefit of a tristated output is that it reduces the capacitive load presented by capacitor 74 on the Vdrain line during reading and/or sensing, thereby reducing the read/sense times compared to embodiments using non-tristated pulse drivers.

[0038] FIG. 17 shows the memory circuit of FIG. 3A, modified so that it incorporates an *n*FET 76 in series with diode 34, according to an embodiment of the present invention. *n*FET 76 of memory circuit 117 has a gate, which is controlled by controller 28, a drain coupled to the cathode of diode 34 and a source coupled to ground. Controller 28 is configured to turn off *n*FET 76 during reading/sensing. A benefit of using *n*FET 76 is that, when *n*FET 76 is turned off, Vdrain can have values greater than 700mV above ground. Note that diode 34 may comprise a source-follower or diode-connected *p*FET, rather than a p-n junction as shown, and that *n*FET 76 may be used in all the other circuit implementations in this disclosure (such as, for example, being used in series with transistor 50 in FIG. 15A).

[0039] FIG. 18 shows the memory circuit of FIG. 3A, modified so that it incorporates a *p*FET 78 between current sense amplifier 26 and the drain of injection transistor 14, according to an embodiment of the present invention. *p*FET 78 of memory circuit 118 has a gate and body, both coupled to ground, a drain coupled to current sense amplifier 26 and a source coupled to the drain of injection transistor 14. The reason for adding *p*FET 78 is that, if current sense amplifier 26 has an n-type (i.e. *n*MOS or NPN) input stage, this stage's substrate-to-drain p-n junction cannot assume values more than about 700mV below ground without turning on (assuming the chip substrate is grounded). Diode-connected *p*FET 78, or an alternative structure such as a p-n diode, allows Vdrain to pulse more than 700mV below ground during injection.

[0040] Although embodiments have been shown using a single cell, the invention also covers memory devices with multiple cells. These are advantageously arranged along individually addressable lines, such as rows and columns. Moreover, it will be appreciated that a single counteracting circuit may be used for a group of memory cells, such as those along an individual one of the addressable lines.

[0041] Referring now to FIG. 19, there is shown an overtunneling prevention memory circuit 119 including a 2 x 2 array of memory cells and associated overtunneling prevention control circuits, according to an embodiment of the present invention. In this embodiment the memory cells 10 in a first row of the array have injection transistors 14 with interconnected sources and interconnected bodies. The interconnected sources are coupled to a voltage source Vdd0 and the bodies are coupled to a well voltage source Vwell0. Tunneling capacitors 16 in the first row of the array are coupled to a tunneling voltage source Vtun0. Memory cells 10 in a second row of the array have injection transistors 14 and tunneling capacitors 16, which are configured similar to the injection transistors 14 and tunneling capacitors 16 in the cells in the first row, except that the various transistor and capacitor terminals are coupled to voltage sources Vdd1, Vwell1 and Vtun1, as shown in the figure. In this embodiment, each column of the array has an associated overtunneling prevention control circuit 12, which may comprise any of the previously described overtunneling prevention control circuits. An

overtunneling prevention control circuit 12 of an associated column of the array is coupled to the drains of the injection transistors 14 of the memory cells 10 within the associated column. Additionally, the memory cells 10 may comprise any of the various memory cell embodiments shown in FIGS. 5-11 above (or others extrapolated from them) as appropriate. Those skilled in the art will also readily understand that, although only a 2 x 2 memory array is shown, the array size could be extended to any m-row by n-column, where m and n are integers both greater than or equal to two.

[0042] FIG. 20 shows an overtunneling prevention memory circuit 120 including a 2 x 2 array of memory cells and associated overtunneling prevention control circuits, according to an embodiment of the present invention. This alternative embodiment modifies the embodiment shown in FIG. 19, by adding a master controller 80 that controls the overtunneling prevention control circuits 12 of the two columns so that one row of the array is tunneled at a time. Master controller 80 may be also configured to control high-voltage switch 44, Vdd switch 46 and Vwell switch 48 in an associated row of the array, in the manner and for the purposes described above. Master controller 80 may also provide a "tunneling done" output for the following reason. As master controller 80 monitors the various controllers 28 of the corresponding overtunneling prevention control circuits 12, it knows which cells have tunneled to the point where they need injection pulses to prevent overtunneling. When every cell in a given row has undergone at least one injection pulse, then the cells have been tunneled to the desired value, so master controller 80

halts further tunneling pulses and issues the "tunneling done" signal. As with the embodiment in FIG. 19, overtunneling prevention control circuits 12 may comprise any of the previously described overtunneling prevention control circuits. Additionally, memory cells 10 may comprise any of the various memory cell embodiments shown in FIGS. 5-11 above (or others extrapolated from them) as appropriate.

[0043] Overtunneling prevention memory circuit 120 in FIG. 20 may further include a high-voltage charge pump 82, under the control of master controller 80. Use of charge pump 82 is as follows. Every nonvolatile memory system is faced with the dilemma of how to regulate the high-voltage charge pump's output voltage. If the voltage is too low, then the tunneling rate will be too slow. On the other hand, if the voltage is too high, then the memory cells may tunnel so fast that the overtunneling prevention control circuits, as controlled by master controller 80, cannot correct any overtunneling problems. In an embodiment including charge pump 82, charge pump 82 is unregulated (i.e. not set to a fixed voltage) and is designed to gradually ramp up its output voltage and use the "tunneling done" signal to turn off pumping, as soon as cells are fully tunneled. By this means the tunneling voltage is never too low because it continually ramps upward; the tunneling voltage is also never too high, because the master controller 80 turns off pumping when all cells are done (prior to the tunneling voltage becoming too high).

[0044] FIG. 21 shows an overtunneling prevention memory circuit 121 including a 2 x 2 array of memory cells with a single shared overtunneling prevention control circuit, according to an embodiment of the present invention. In contrast to the memory array embodiments shown in FIGS. 19 and 20, a 2:1 multiplexer 84 is employed to route selected column Vdrain lines into a single overtunneling prevention control circuit 12. This implementation saves circuit area compared to the embodiments shown in FIGS. 19 and 20. Memory circuit 121 functions as follows. A tunneling pulse is applied to one row of the array. Then, sequentially, using multiplexer 84 to select individual columns, each cell's drain current Idrain is measured. If necessary, one or more injection pulses are applied to correct overtunneled cells. As with the embodiments in FIGS. 19 and 20, overtunneling prevention control circuits 12 may comprise any of the previously described overtunneling prevention control circuits. Additionally, memory cells 10 may comprise any of the various memory cell embodiments shown in FIGS. 5-11 above (or others extrapolated from them) as appropriate. Those skilled in the art will also readily understand that, although a 2:1 multiplexer is shown, the multiplexer could be extended to any n:p multiplexer, where n is an integer that is greater than or equal to one and represents the number of columns in the memory array, and p is an integer that is greater than or equal to one and represents the number of overtunneling prevention control circuits coupled to the multiplexer.

[0045] Methods of the invention are now described in more detail. In a general method of the invention, charge is extracted from a floating gate of a transistor,

such as a transistor of a memory cell. If an extraction threshold is sensed, the extraction of charge is counteracted. The extraction threshold may be sensed that it has been approached, reached or exceeded, by sensing a preset current or a potential.

[0046] In one embodiment, the preset current may be associated with a minimum channel current required to maintain a conducting channel in the transistor. In that case, counteracting is performed by adding charge to the gate.

[0047] In one embodiment, the charge is extracted by applying a high voltage to a capacitor structure that is associated with the gate. In that case, counteracting may be performed by switching off the high voltage. In other embodiments, counteracting is performed by switching off power to a terminal of the transistor, or to a well of the transistor. In some of those embodiments, the high voltage or power is switched off after overtunneling, in which case charge may be injected back into the floating gate.

[0048] While particular embodiments of the present invention have been shown and described, it will be obvious to those skilled in the art that, based upon the teachings herein, changes and modifications may be made without departing from this invention and its broader aspects. Therefore, the appended claims are intended to encompass within their scope all such changes and modifications as are within the true spirit and scope of this invention.

CLAIMS

The claimed invention is:

1. A circuit comprising:

a transistor with a floating gate;

a capacitor structure for extracting charge from the gate; and

a counteracting circuit to prevent extracting charge beyond a threshold.

2. The circuit of claim 1, wherein the transistor is a pFET injection transistor.

3. The circuit of claim 2, further comprising:

a coupling capacitor coupled between the floating gate and a source of the injection transistor.

4. The circuit of claim 1, wherein extracting is performed by tunneling.

5. The circuit of claim 1, wherein the transistor is an nFET transistor.

6. The circuit of claim 1, wherein the threshold is a preset amount of electrical current.

7. The circuit of claim 6, wherein the preset amount of electrical current is associated with a minimum channel current required to maintain a conducting channel in the transistor.

8. The circuit of claim 1, wherein the threshold is a preset amount of charge.

9. The circuit of claim 1, wherein the threshold is a preset electrical potential.

10. The circuit of claim 1, wherein the capacitor structure is made from a MOSFET structure.

11. The circuit of claim 1, wherein the counteracting circuit is adapted to add charge to the gate.

12. The circuit of claim 1, wherein the counteracting circuit is coupled to a drain of the transistor.

13. The circuit of claim 1, wherein the counteracting circuit includes a current source.

14. The circuit of claim 14, wherein the counteracting circuit includes a transistor having a gate coupled to a reference voltage.

15. The circuit of claim 1, wherein the counteracting circuit includes:

a current sensor to monitor a drain current of the memory cell and to generate a trigger event when the threshold is reached, and

a pulse driver to add charge to the gate responsive to the trigger event.

16. The circuit of claim 15, wherein the current sensor includes:

a current sense amplifier, and

a controller to provide a control signal responsive to the trigger event, and

the pulse driver adds charge responsive to the control signal.

17. The circuit of claim 15, wherein the threshold is a preset amount of electrical current.

18. The circuit of claim 17, wherein the preset amount of electrical current is associated with a minimum channel current required to maintain a conducting channel in the transistor.

19. The circuit of claim 1, wherein the counteracting circuit includes a cutoff switch, and

a sensor to trigger the cutoff switch when the threshold is reached.

20. The circuit of claim 19, wherein the cutoff switch is arranged to prevent a high voltage from being applied to the capacitor structure.

21. The circuit of claim 19, wherein the cutoff switch is arranged to prevent a power supply from being applied to a terminal of the transistor.

22. The circuit of claim 19, wherein the cutoff switch is arranged to prevent a power supply from being applied to a well of the transistor.

23. A circuit comprising:

a first transistor with a first floating gate;

a first capacitor structure for extracting charge from the first gate;

a second transistor with a second floating gate;

a second capacitor structure for extracting charge from the second gate; and

a counteracting circuit to prevent extracting charge from the first and second gates beyond a threshold.

24. The circuit of claim 23, wherein the counteracting circuit is adapted to add charge to the first and second gates.

25. The circuit of claim 23, wherein the counteracting circuit is coupled to drains of the first and second transistors.

26. The circuit of claim 23, wherein the counteracting circuit includes a current source.

27. The circuit of claim 23, wherein the counteracting circuit includes:

a cutoff switch, and

a sensor to trigger the cutoff switch when the threshold is reached.

28. The circuit of claim 27, wherein the cutoff switch is arranged to prevent a high voltage from being applied to the first and second capacitor structures.

29. The circuit of claim 27, wherein the cutoff switch is arranged to prevent a power supply from being applied to a terminal of the first transistor and to a terminal of the second transistor.

30. The circuit of claim 27, wherein the cutoff switch is arranged to prevent a power supply from being applied to a well of the first transistor and to a well of the second transistor.

31. A memory device comprising:

means for extracting charge from a floating gate of a transistor; and

means for counteracting the extraction of charge if an extraction threshold is sensed.

32. The device of claim 31, wherein the extraction threshold is sensed by sensing a preset current.

33. The device of claim 32, wherein the preset current is associated with a minimum channel current required to maintain a conducting channel in the transistor.

34. The device of claim 31, wherein the extraction threshold is sensed by sensing a potential.

35. The device of claim 31, wherein the counteracting means adds charge to the gate.

36. The device of claim 31, wherein the extracting means applies a high voltage to a capacitor structure.

37. The device of claim 36, wherein the counteracting means switches off the high voltage.

38. The device of claim 31, wherein the counteracting means switches off power to a terminal of the transistor.

39. The device of claim 31, wherein the counteracting means switches off power to a well of the transistor.

40. A method comprising:

extracting charge from a floating gate of a transistor; and

if an extraction threshold is sensed, counteracting the extraction of charge.

41. The method of claim 40, wherein the extraction threshold is sensed by sensing a preset current.

42. The method of claim 41, wherein the preset current is associated with a minimum channel current required to maintain a conducting channel in the transistor.

43. The method of claim 40, wherein the extraction threshold is sensed by sensing a potential.

44. The method of claim 40, wherein counteracting is performed by adding charge to the gate.

45. The method of claim 40, wherein the charge is extracted by applying a high voltage to a capacitor structure.

46. The method of claim 45, wherein counteracting is performed by switching off the high voltage.

47. The method of claim 40, wherein counteracting is performed by switching off power to a terminal of the transistor.

48. The method of claim 40, wherein counteracting is performed by switching off power to a well of the transistor.

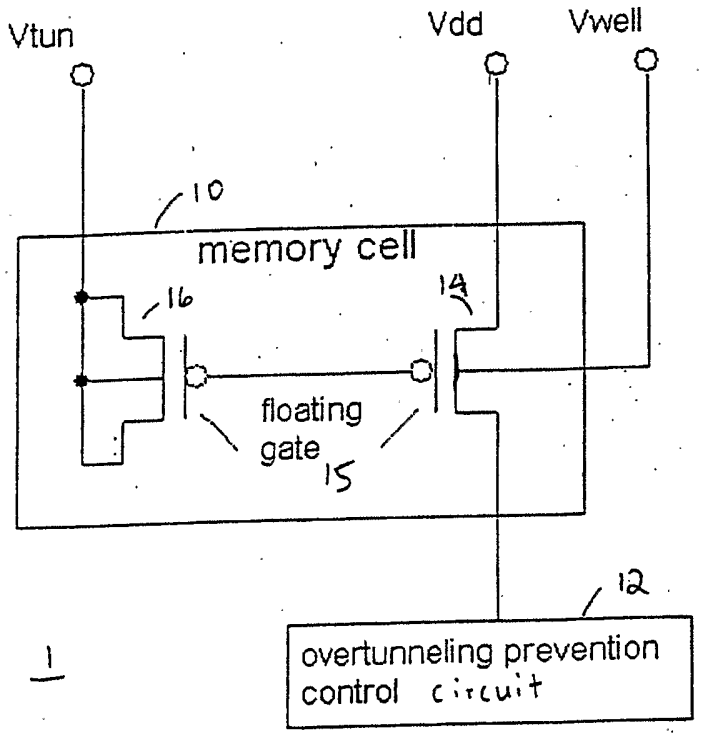
Vtun
Vdd
Vwell
10
memory cell
16
14
floating
gate
15
12
overtunneling prevention
control circuit
1

FIGURE 1

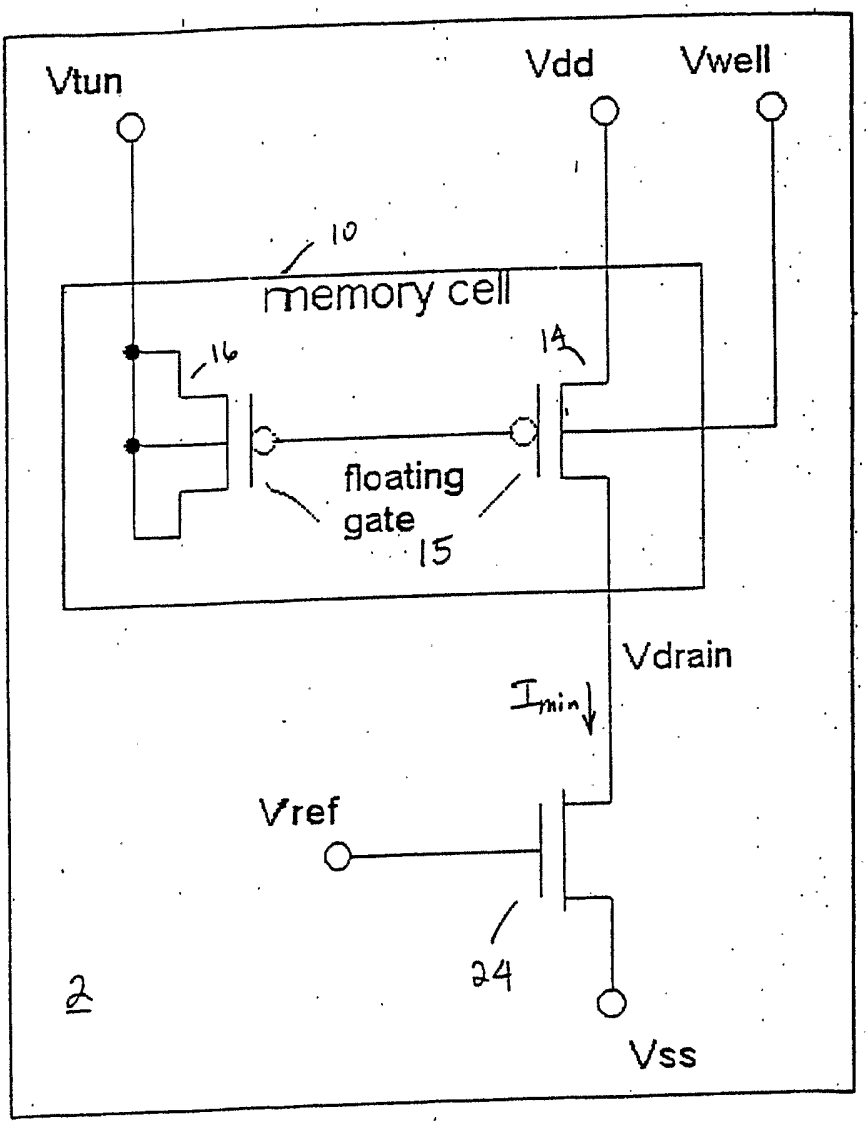
Vtun
Vdd
Vwell
10
memory cell
16
14
floating
gate
15
Vdrain
Imin
Vref
24
2
Vss

FIGURE 2

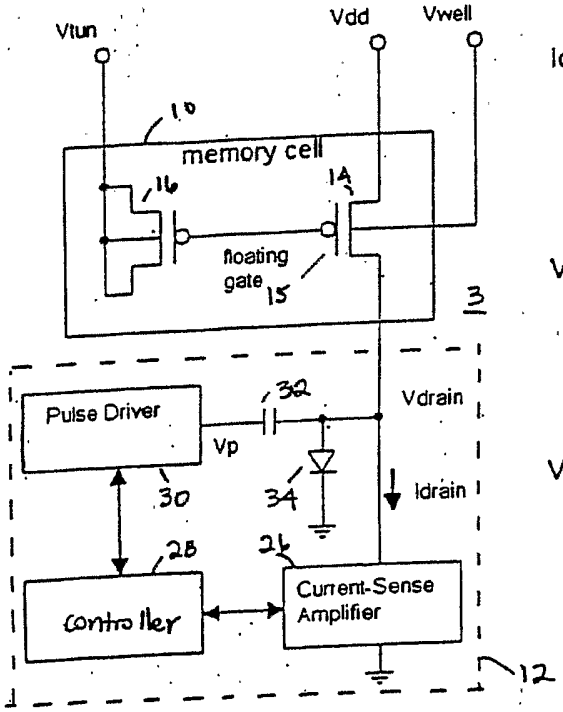

FIGURE 3A

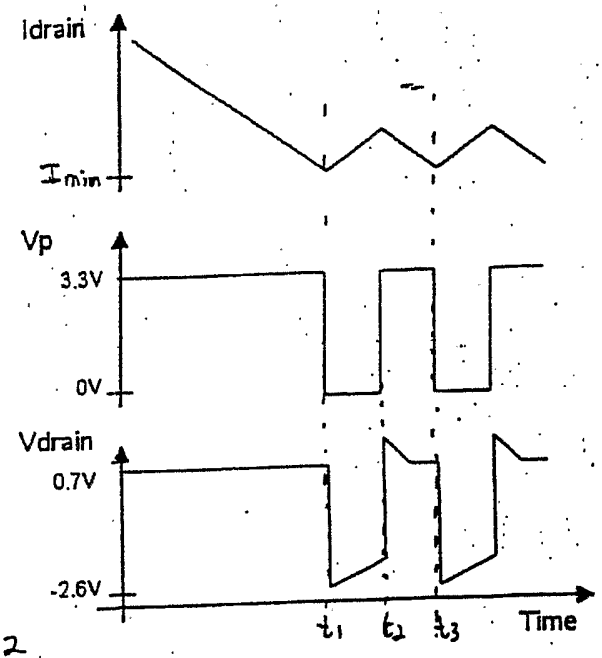

FIGURE 3B

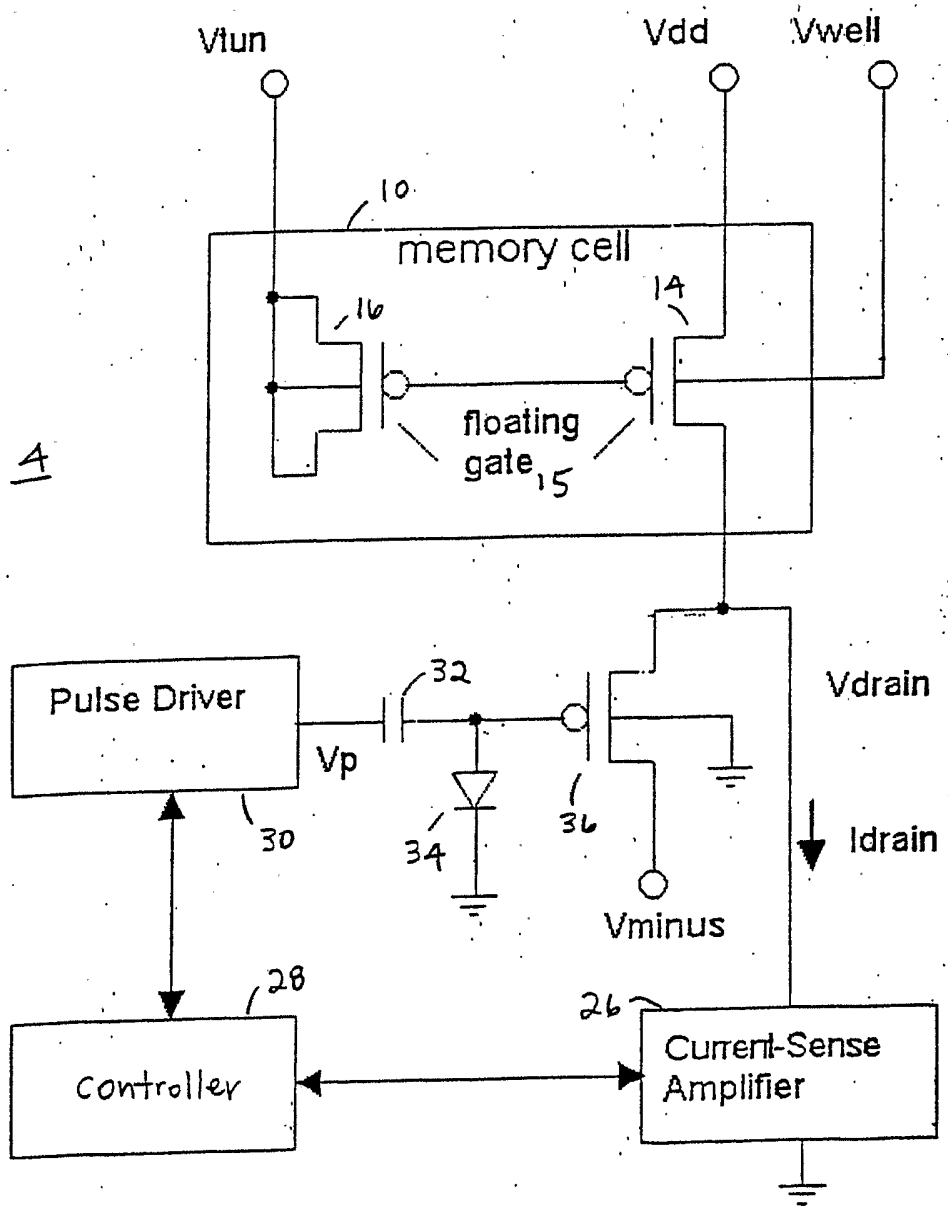
Vtun
Vdd
Vwell
10
memory cell
16
14
floating gate
15
4
Pulse Driver
32
Vp
Vdrain
30
34
36
Idrain
Vminus
28
26
Controller
Current-Sense Amplifier

FIGURE 4

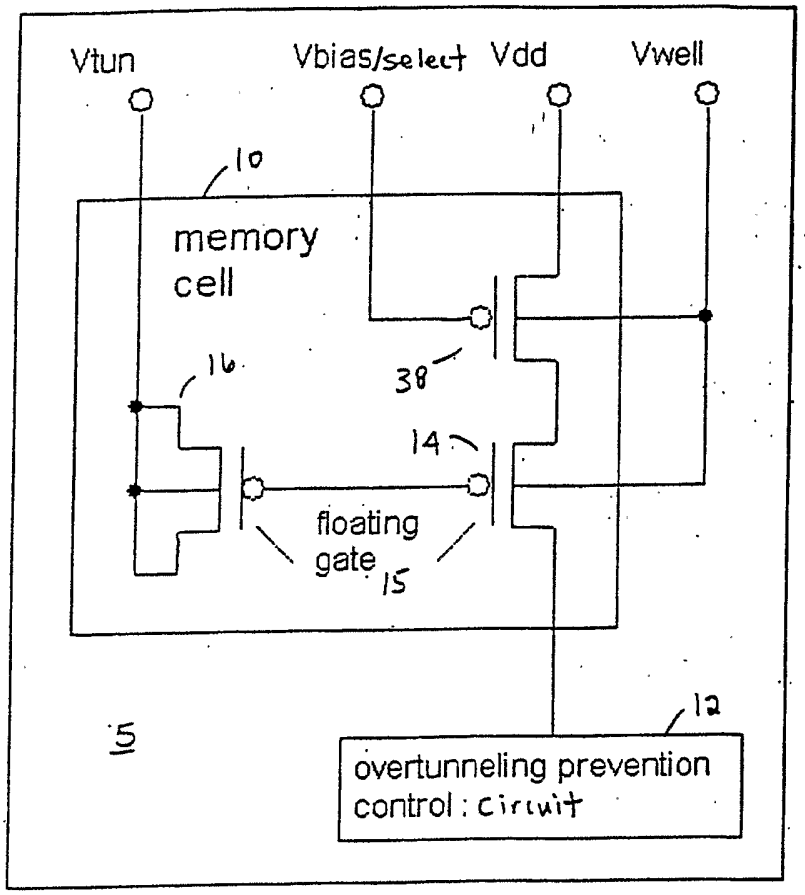
Vtun
Vbias/select
Vdd
Vwell
10
memory cell
16
38
14
floating gate
15
5
12
overtunneling prevention control : circuit

FIGURE 5

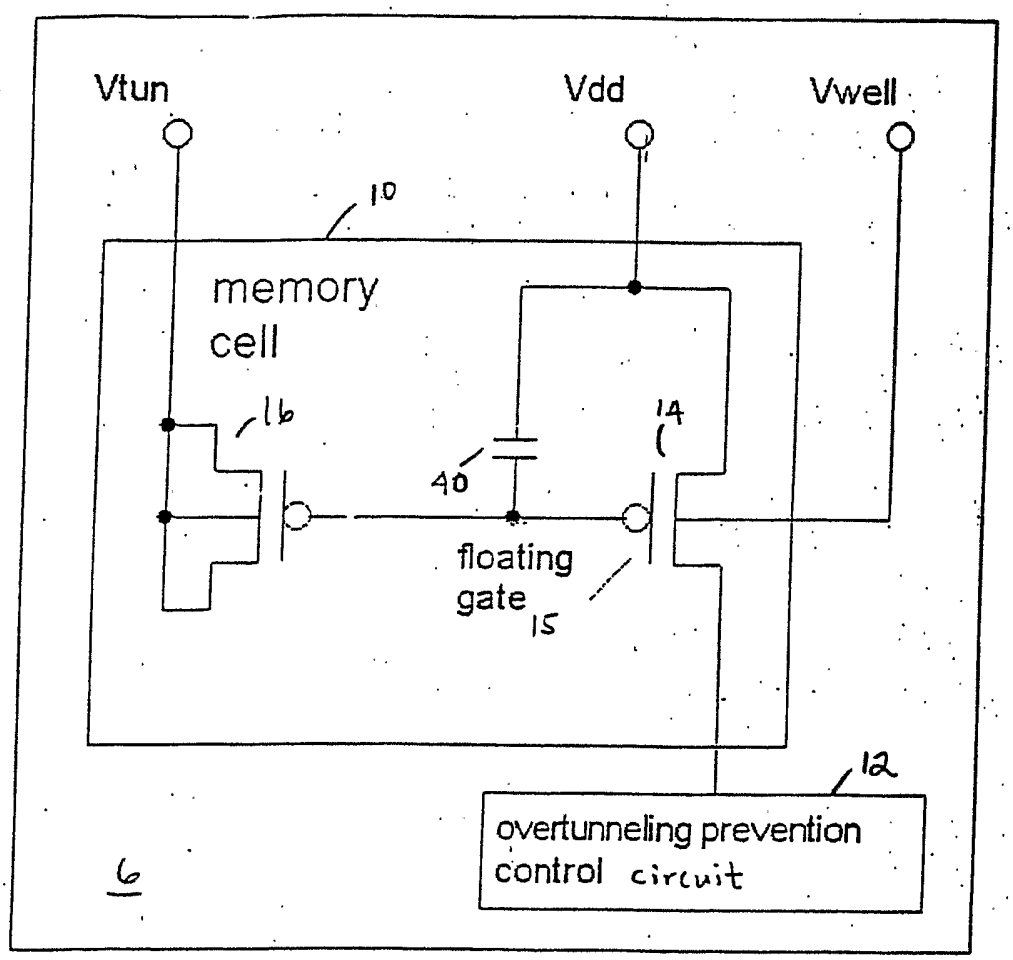
Vtun
Vdd
Vwell
10
memory cell
16
14
40
floating gate
15
12
overtunneling prevention control circuit
6

FIGURE 6

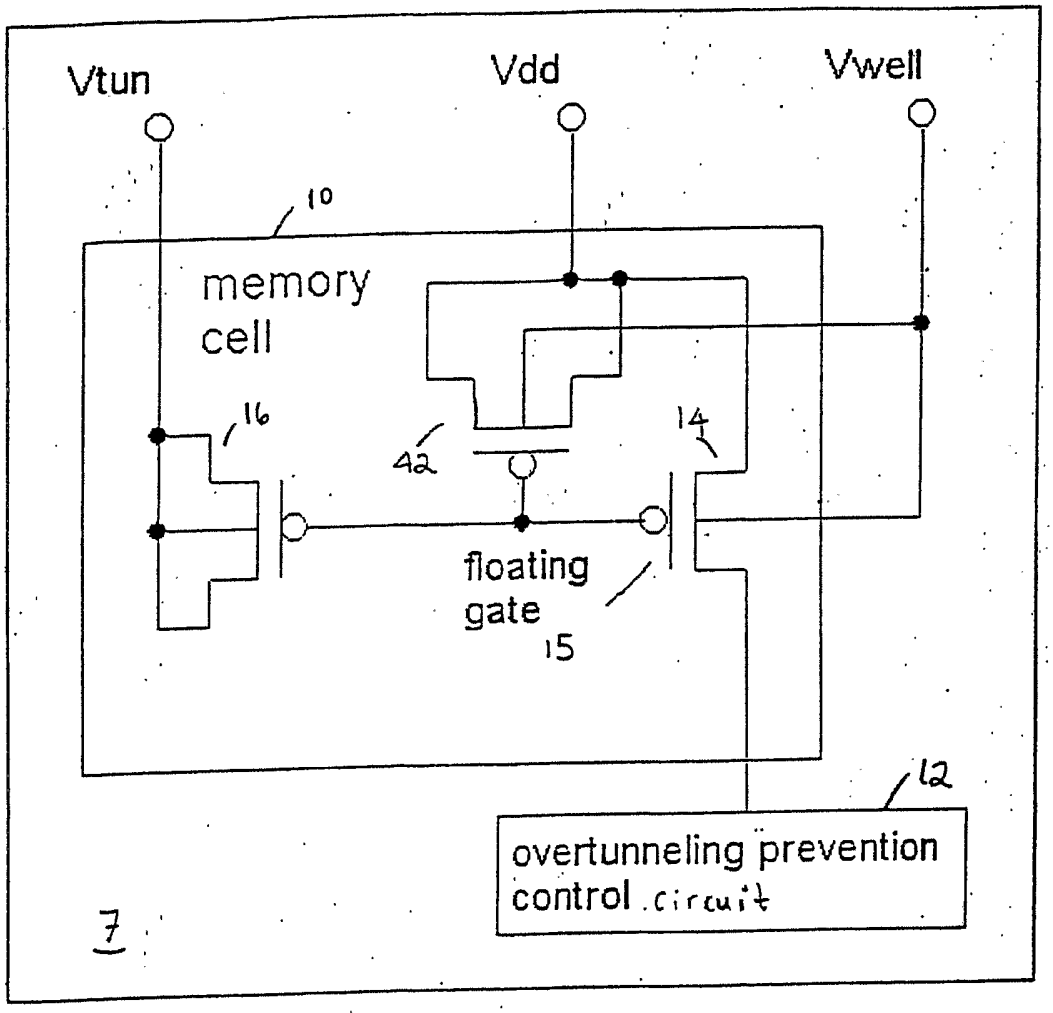
Vtun
Vdd
Vwell
10
memory cell
16
42
14
floating gate
15
12
overtunneling prevention control circuit
7

FIGURE 7

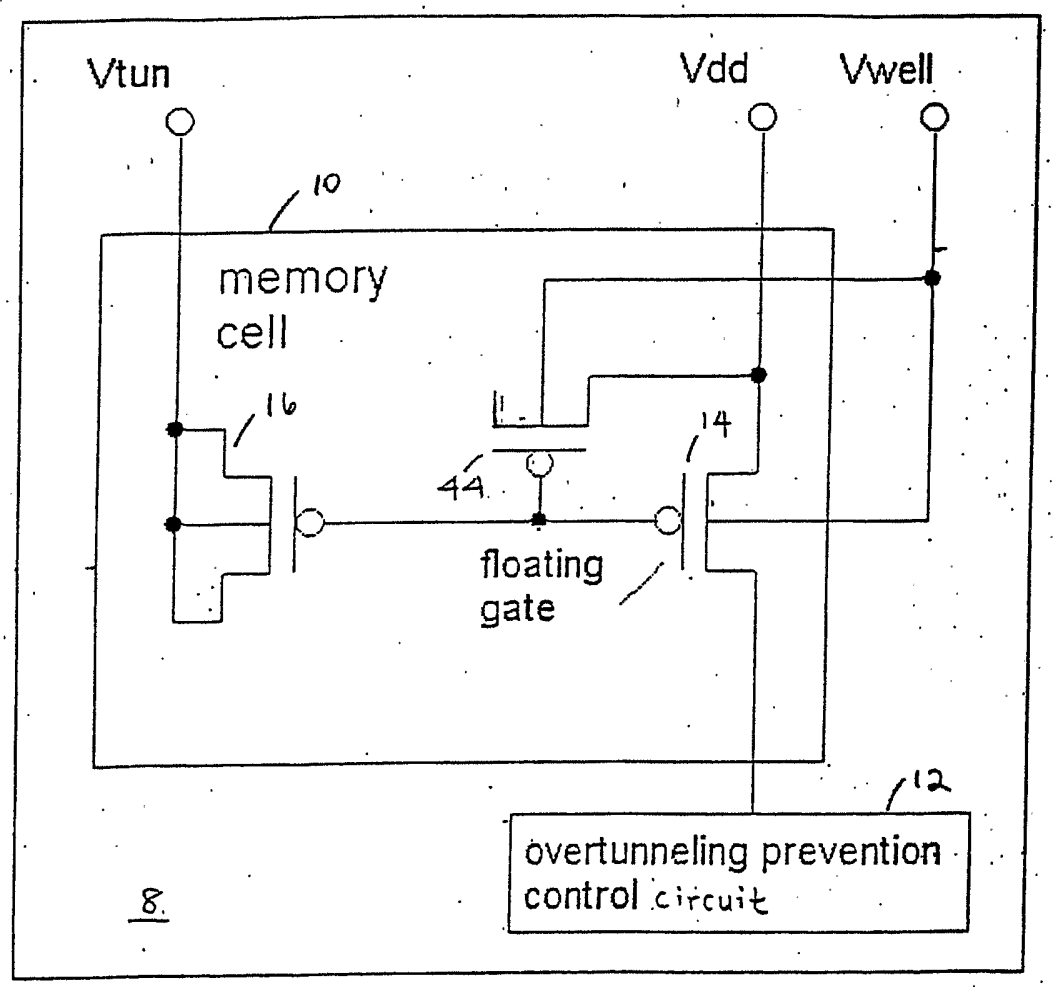
Vtun
Vdd
Vwell
10
memory cell
16
14
44
floating gate
12
overtunneling prevention control circuit
8

FIGURE 8

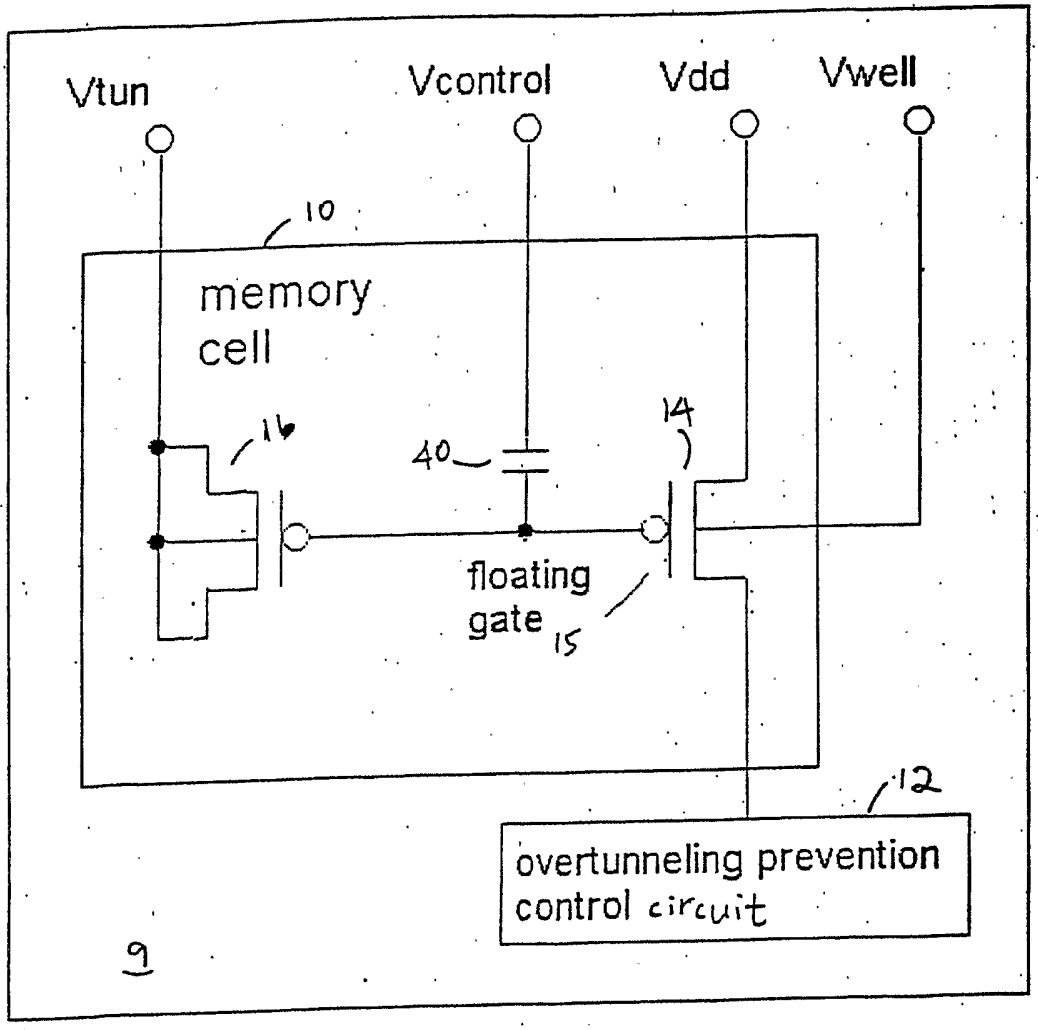
Vtun
Vcontrol
Vdd
Vwell
10
memory cell
16
40
14
floating gate
15
12
overtunneling prevention control circuit
9

FIGURE 9

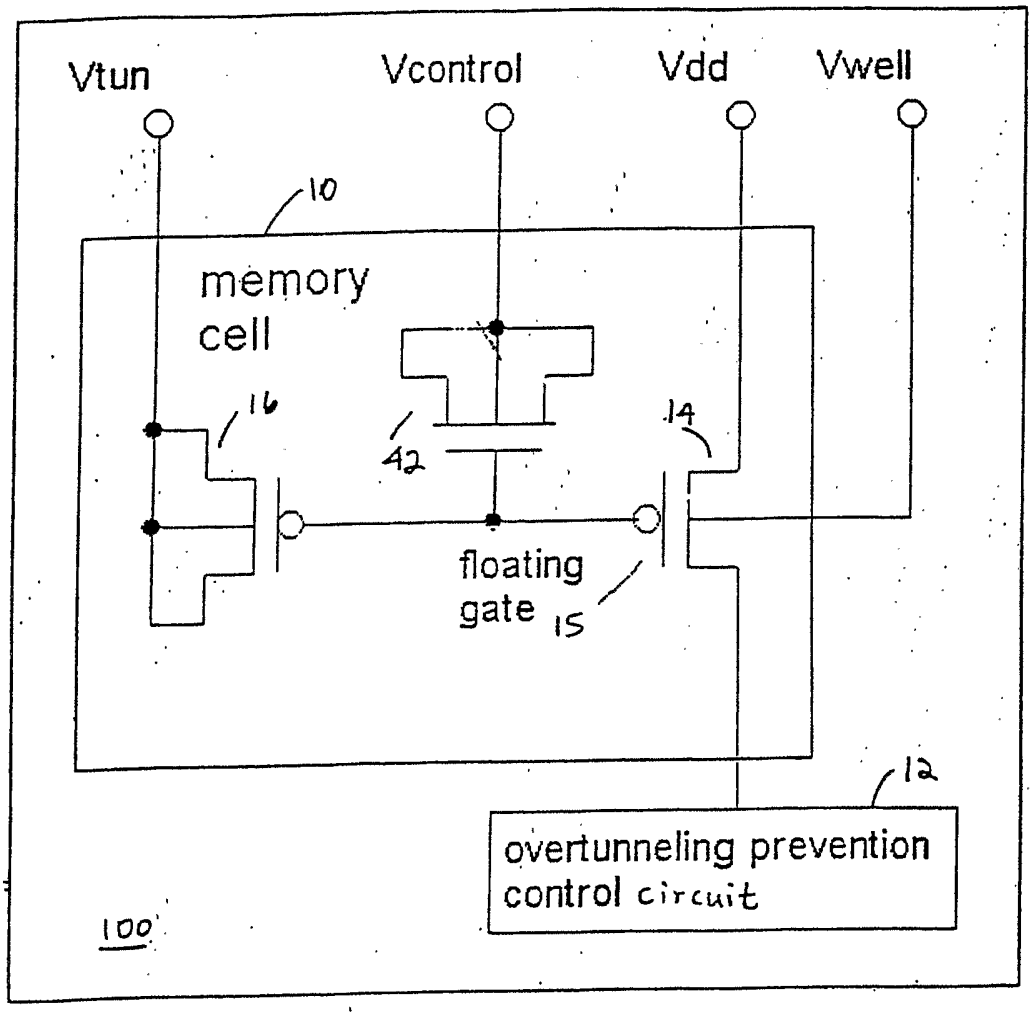
Vtun
Vcontrol
Vdd
Vwell
10
memory cell
16
42
14
floating gate
15
12
overtunneling prevention control circuit
100

FIGURE 10

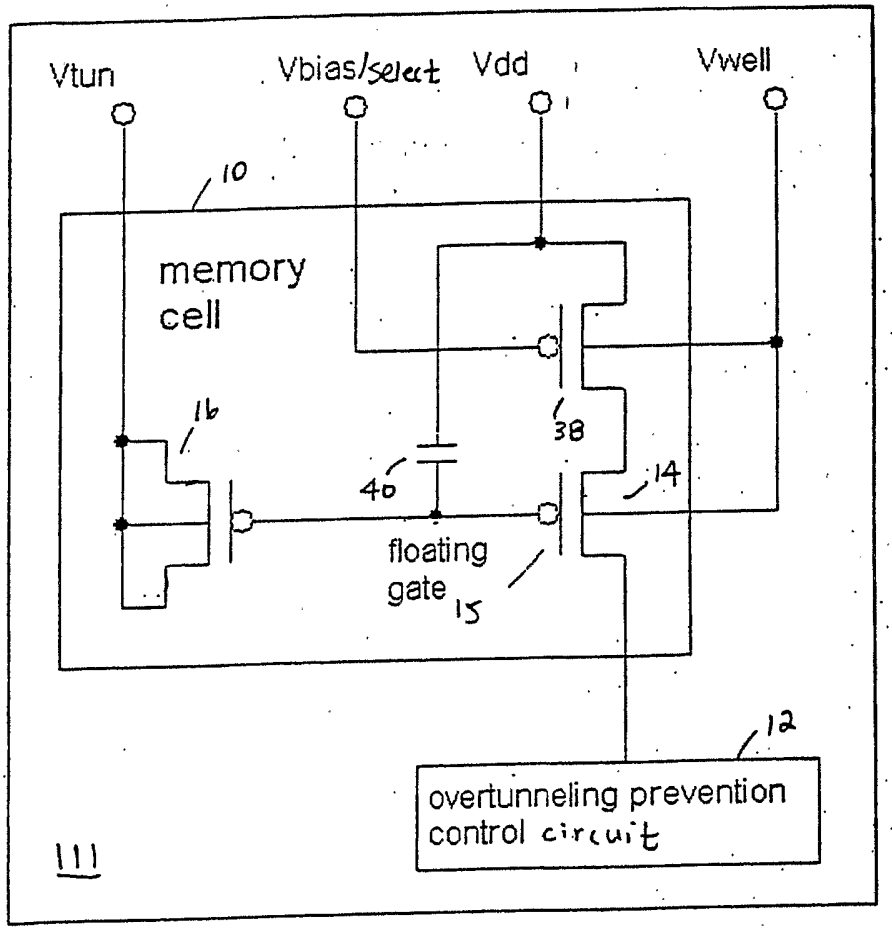
Vtun
Vbias/select
Vdd
Vwell
10
memory cell
16
38
40
14
floating gate
15
12
overtunneling prevention control circuit
111

FIGURE 11

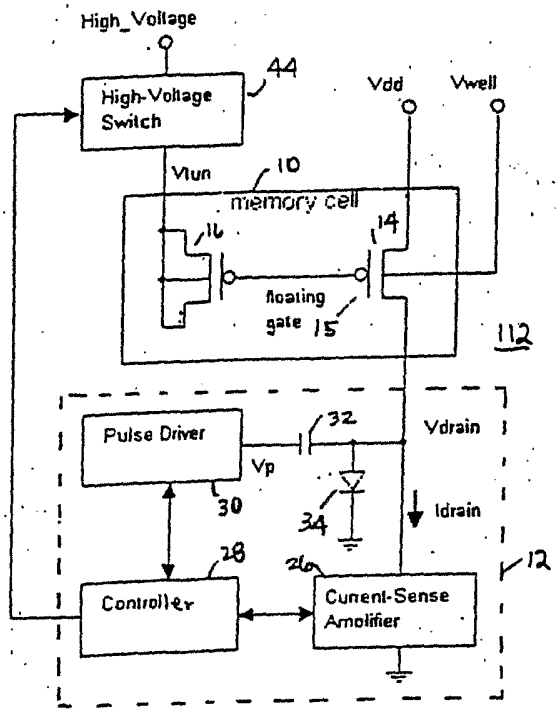

FIGURE 12A

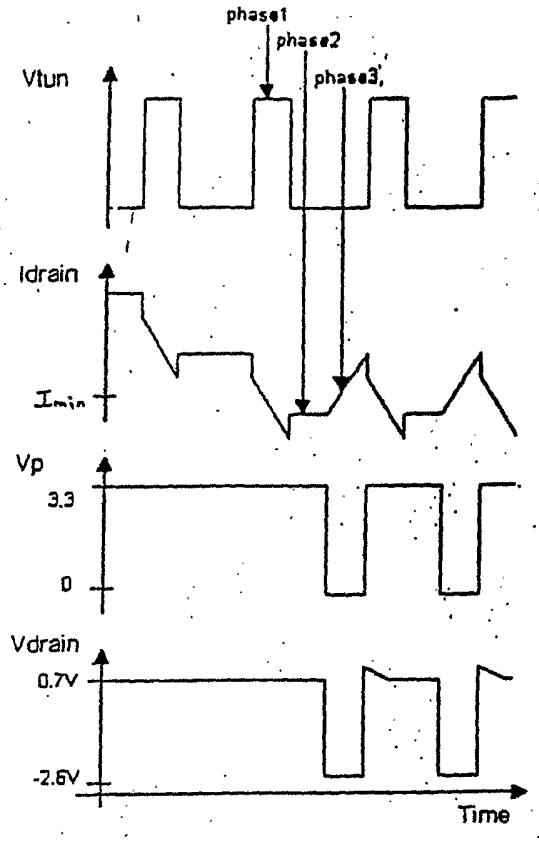

FIGURE 12B

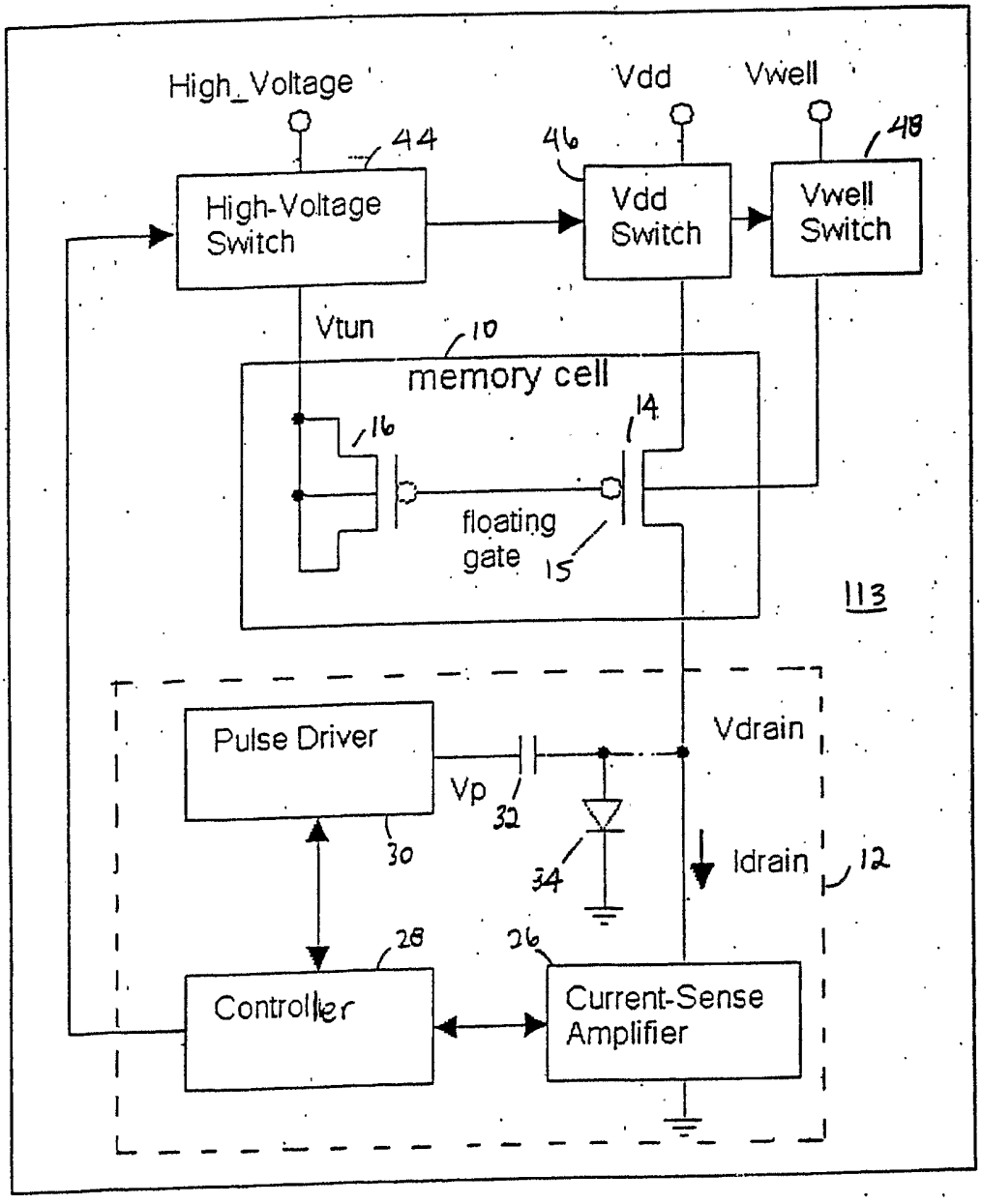
High_Voltage
Vdd
Vwell
44
46
48
High-Voltage Switch
Vdd Switch
Vwell Switch
Vtun
10
memory cell
16
14
floating gate
15
113
Pulse Driver
Vdrain
Vp
32
30
34
Idrain
12
28
26
Controller
Current-Sense Amplifier

FIGURE 13

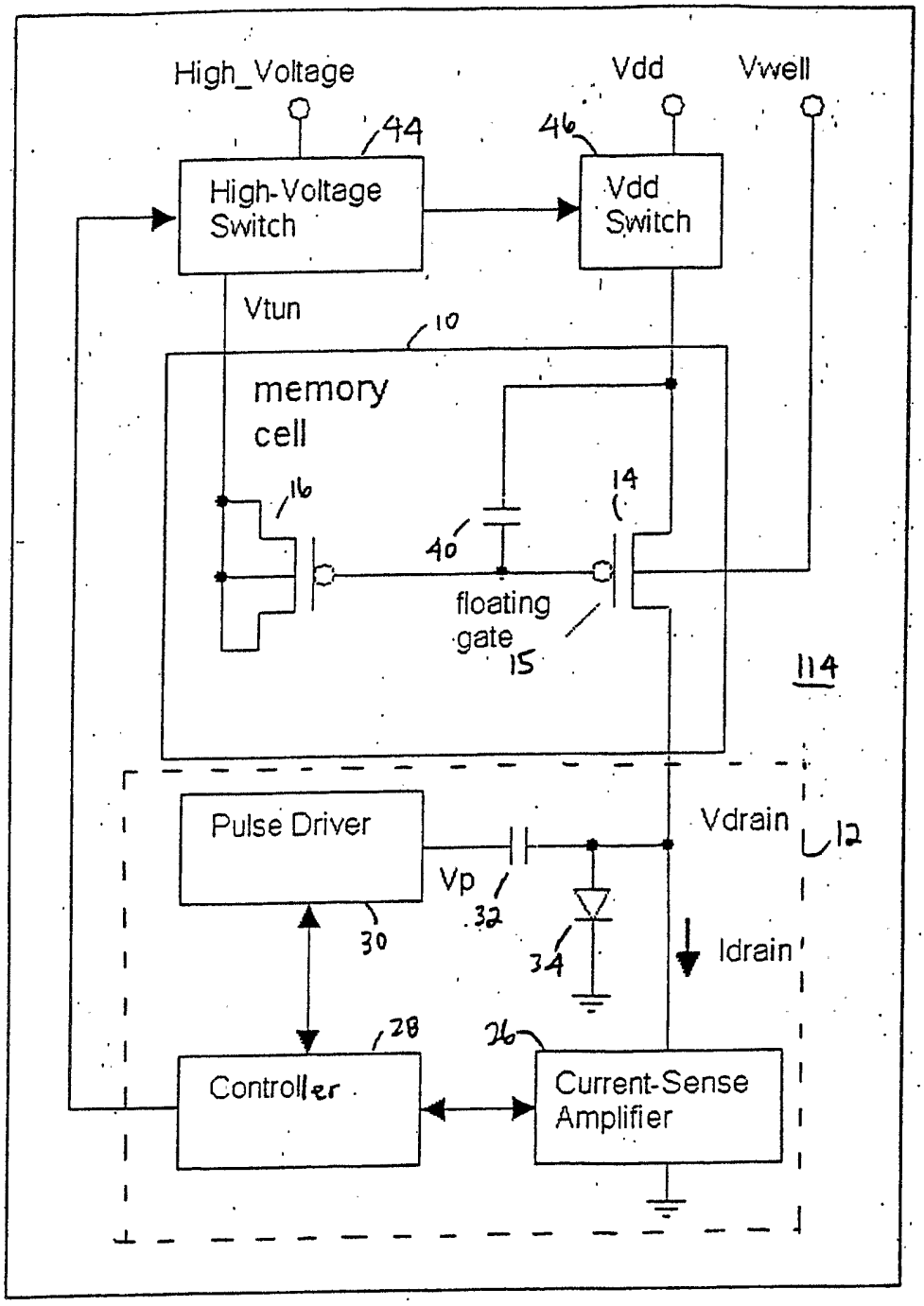
High_Voltage
Vdd
Vwell
44
46
High-Voltage Switch
Vdd Switch
Vtun
10
memory cell
16
14
40
floating gate
15
114
Pulse Driver
Vdrain
12
Vp
32
34
30
Idrain
28
26
Controller
Current-Sense Amplifier

FIGURE 14

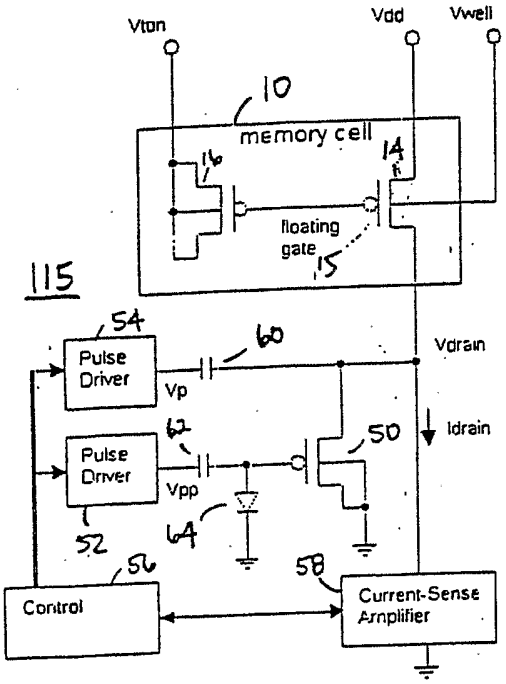

FIGURE 15A

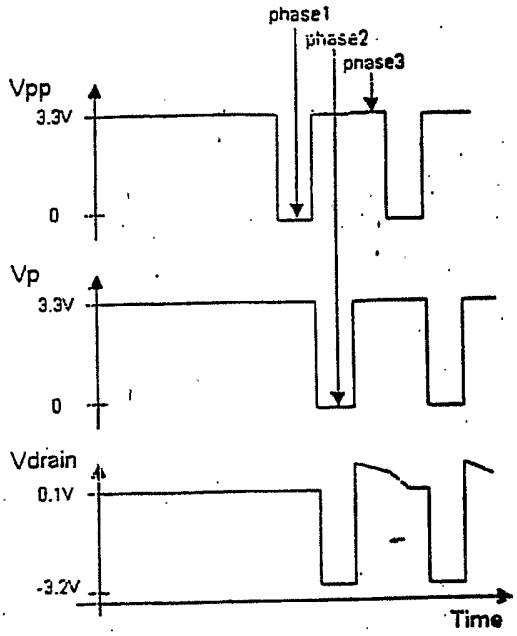

FIGURE 15B

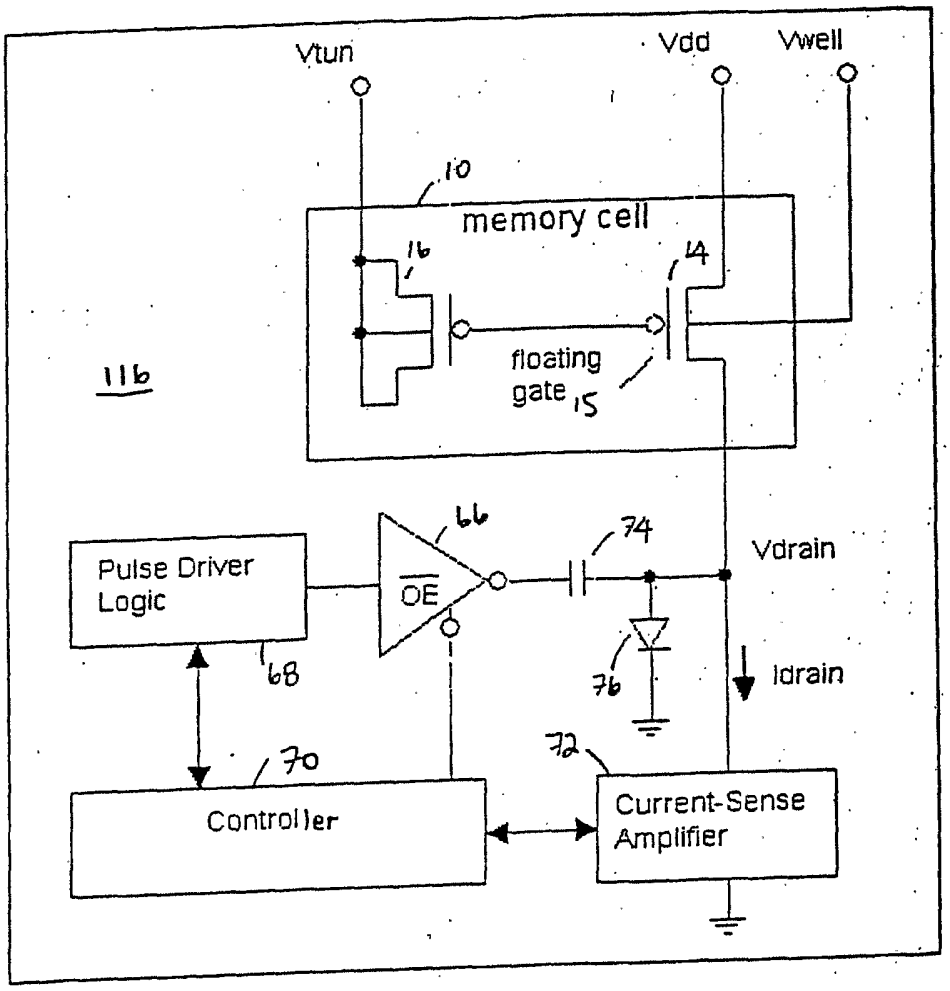
Vtun
Vdd
Vwell
10
memory cell
16
14
floating gate 15
116
66
74
Vdrain
Pulse Driver Logic
OE
68
76
Idrain
70
72
Controller
Current-Sense Amplifier

FIGURE 16

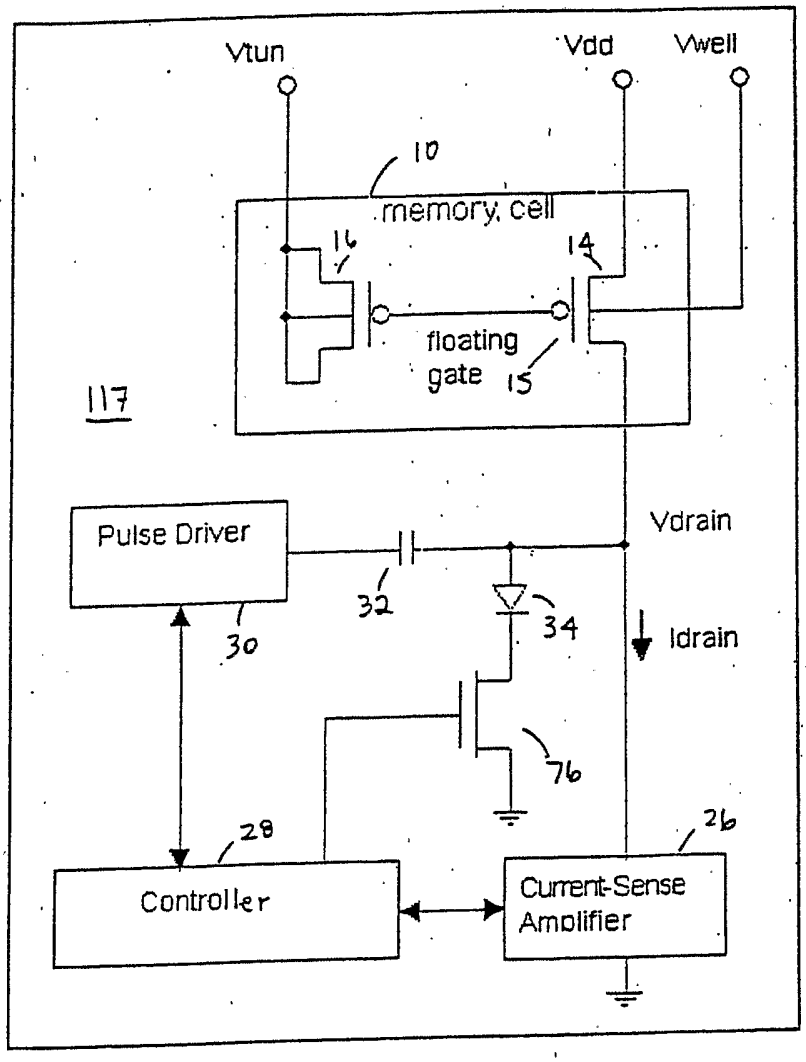
Vtun
Vdd
Vwell
10
memory cell
16
14
floating gate
15
117
Pulse Driver
Vdrain
32
34
Idrain
30
76
28
26
Controller
Current-Sense Amplifier

FIGURE 17

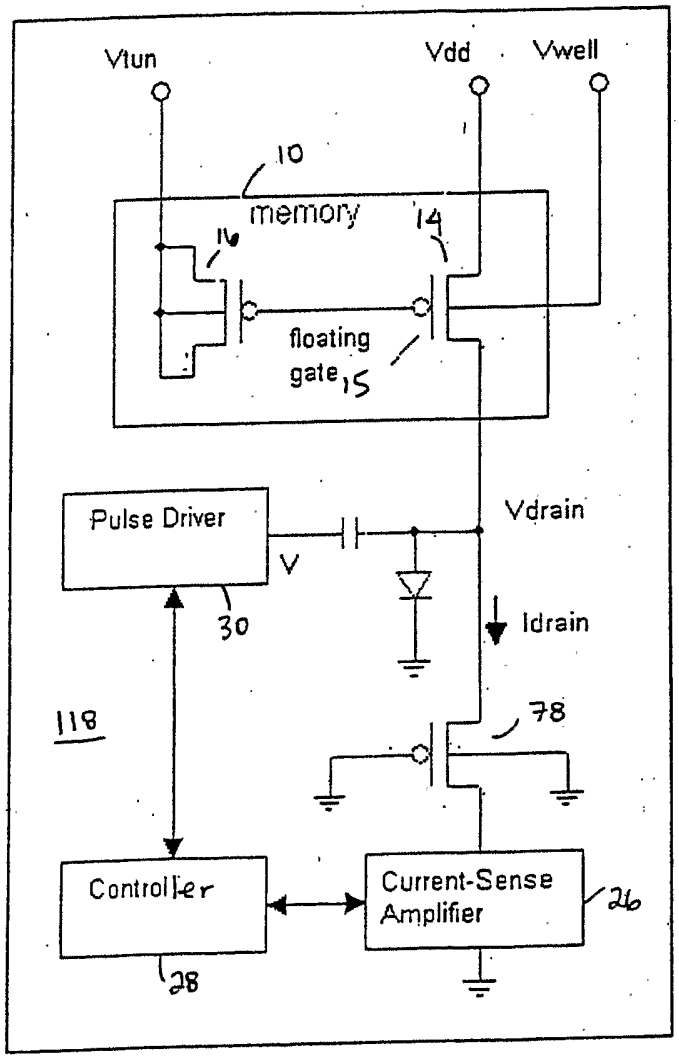
Vtun
Vdd
Vwell
10
memory
14
16
floating
gate 15
Pulse Driver
V
30
Vdrain
Idrain
118
78
Controller
28
Current-Sense
Amplifier
26

FIGURE 1B

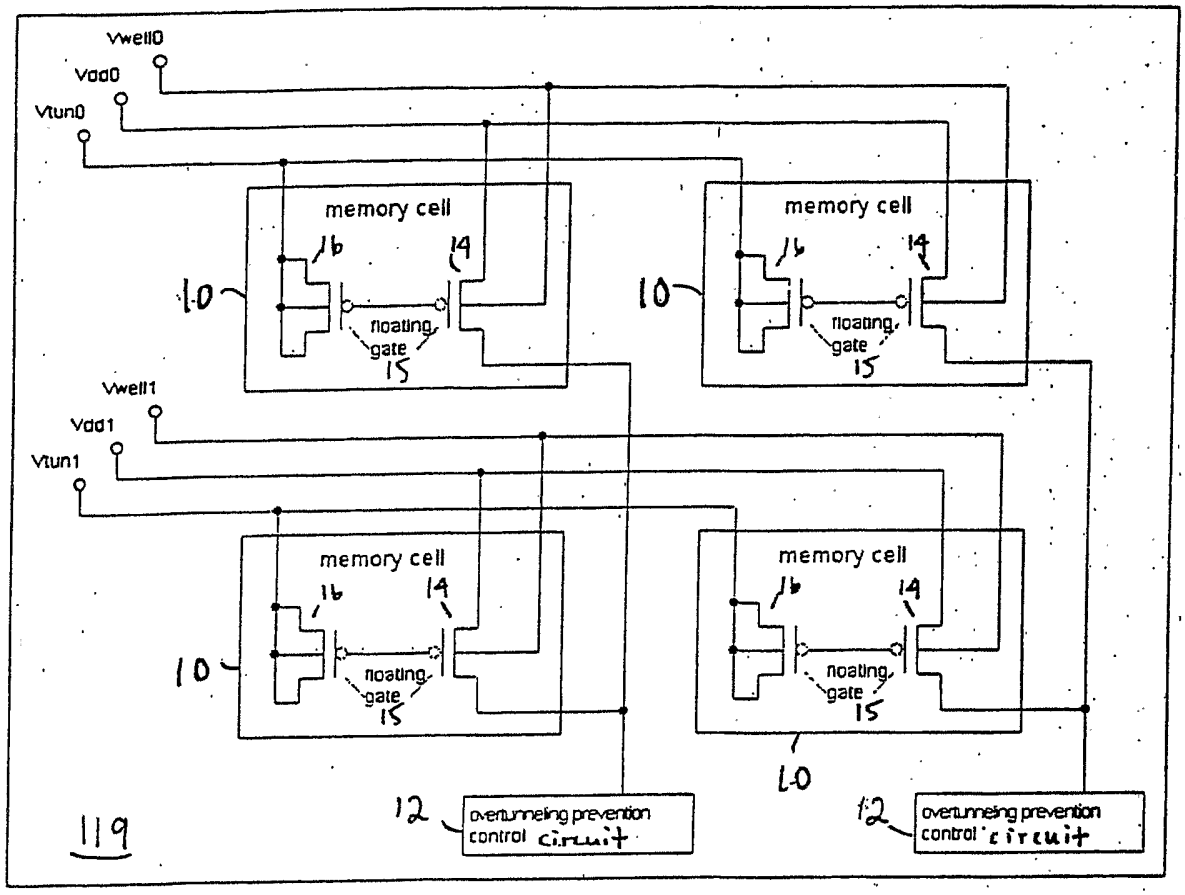
Vwell0
Vdd0
Vtun0
memory cell
16
14
10
floating gate
15
Vwell1
Vdd1
Vtun1
12
overtunneling prevention control circuit
119

FIGURE 19

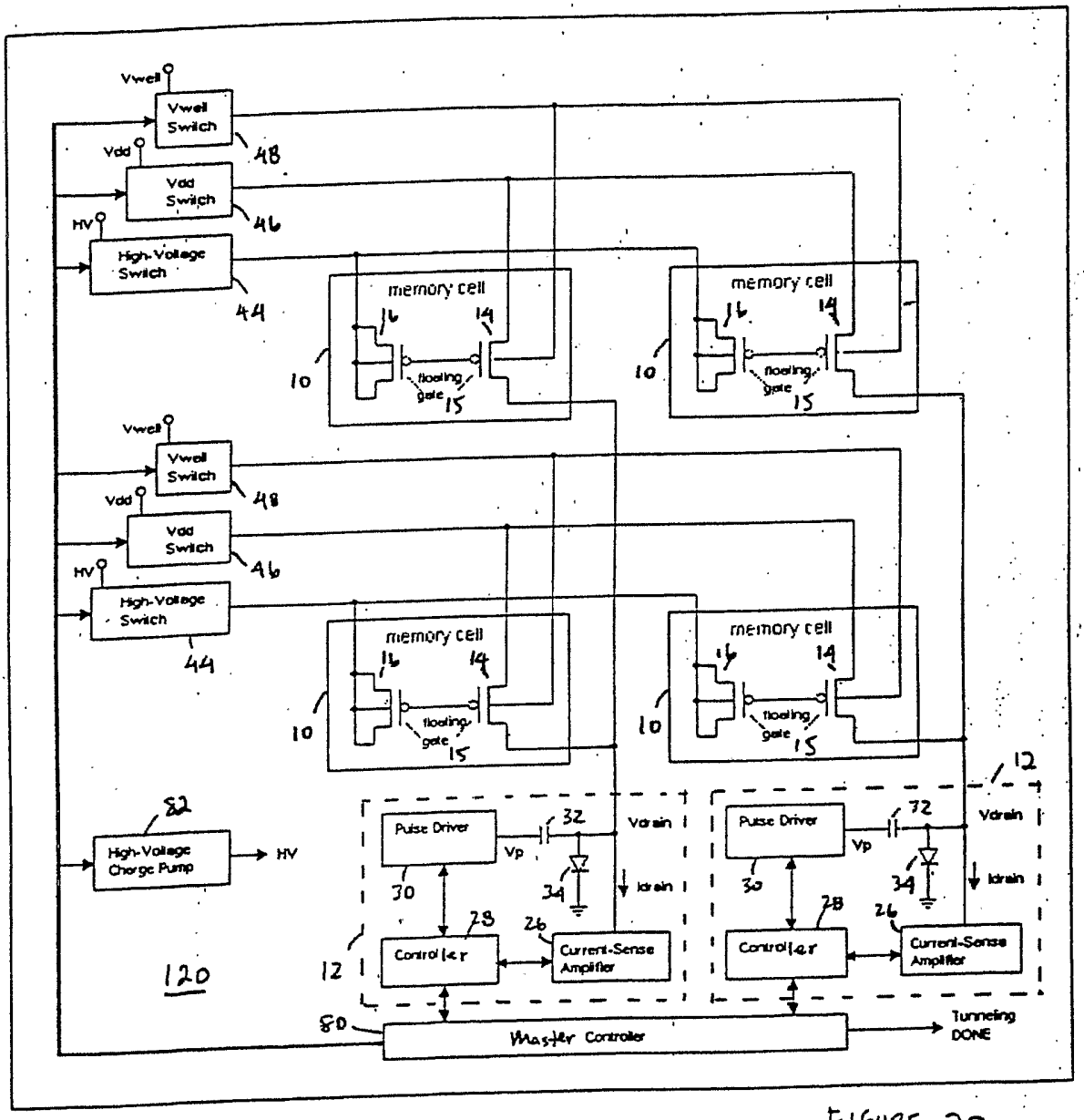
Vwell
Vwell Switch
48
Vdd
Vdd Switch
46
HV
High-Voltage Switch
44
memory cell
16
14
floating gate
15
10
High-Voltage Charge Pump
82
HV
120
Pulse Driver
32
Vp
Vdrain
Idrain
30
34
28
26
Controller
Current-Sense Amplifier
12
80
Master Controller
Tunneling DONE

FIGURE 20

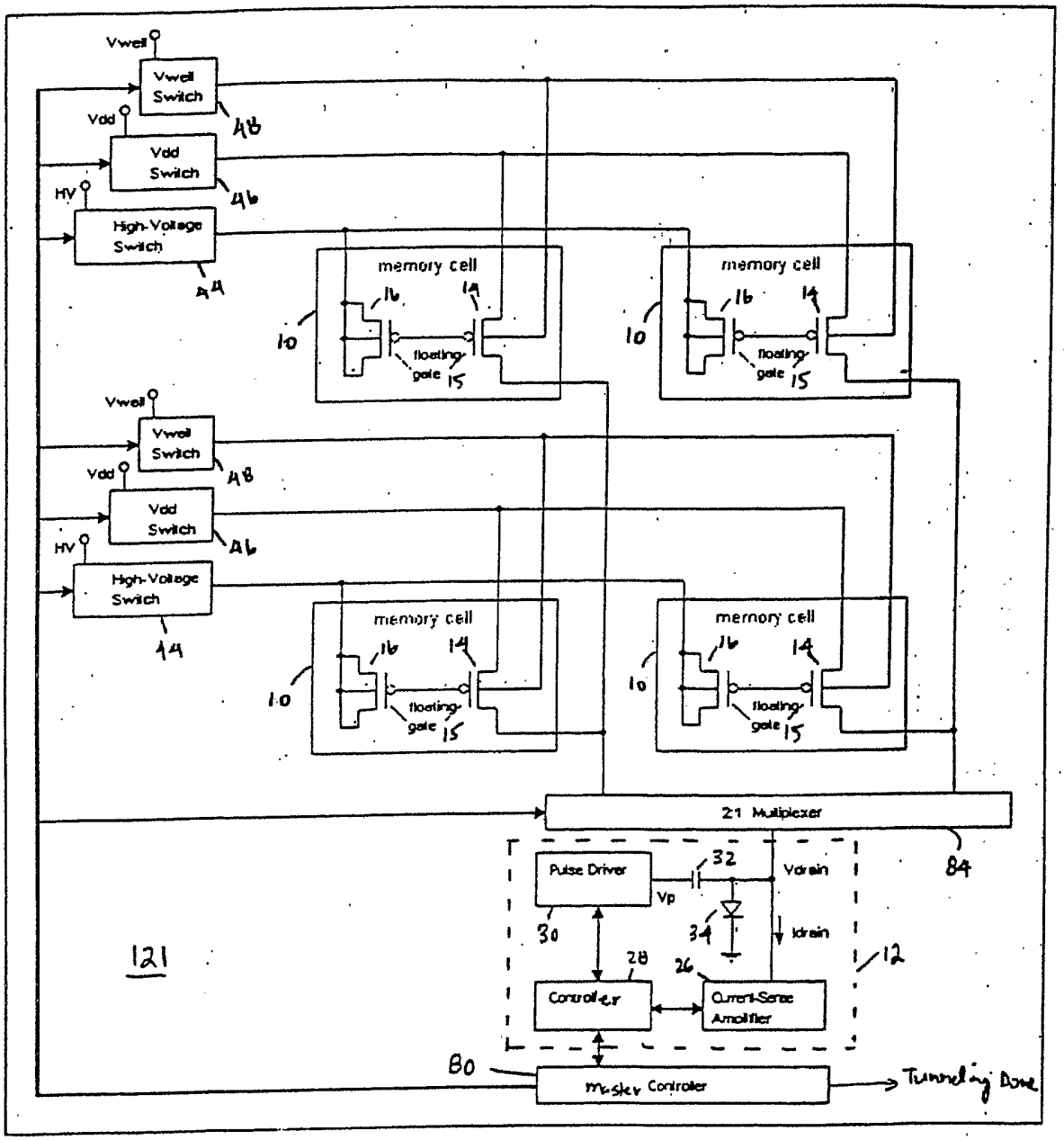
Vwell
Vwell Switch
Vdd
Vdd Switch
HV
High-Voltage Switch
memory cell
floating gate
21 Multiplexer
84
Pulse Driver
32
Vdrain
Vp
Idrain
34
30
28
26
12
Controller
Current-Sense Amplifier
80
Master Controller
Tunneling Done
121

FIGURE 21

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2005/013644

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11C16/34

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/052113 A1 (DIORIO CHRISTOPHER J ET AL) 18 March 2004 (2004-03-18) figures 2,3,13,19	1-48

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 July 2005	03/08/2005

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Vidal Verdu, J.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US2005/013644

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2004052113 A1	18-03-2004	AU 2003256994 A1	30-04-2004
		WO 2004025662 A1	25-03-2004
		US 2004195593 A1	07-10-2004
		US 2005030826 A1	10-02-2005
		US 2005030827 A1	10-02-2005