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Semiconductors, IP Department, Cross Oak Lane, Redhill
Surrey RH1 5HA (GB).

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(74) Agents: **WHITE, Andrew, G.** et al.; c/o NXP Semicon-
ductors, IP Department, Cross Oak Lane, Redhill Surrey
RH1 5HA (GB).

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(71) Applicant (*for all designated States except US*): **NXP B.V.**
[NL/NL]; High Tech Campus 60, NL-5656 AG Eindhoven
(NL).

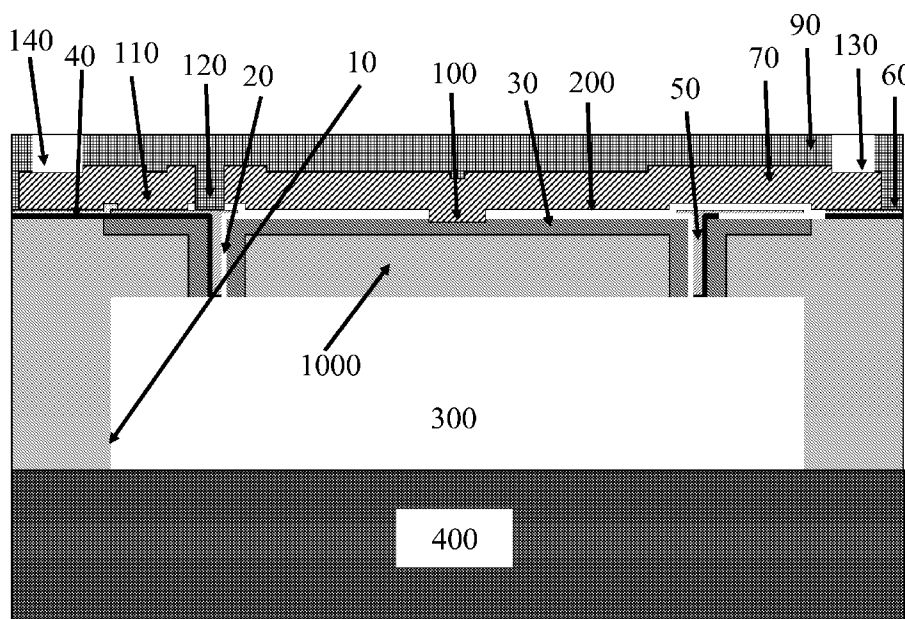
(72) Inventors; and

(75) Inventors/Applicants (*for US only*): **SWOROWSKI,**
Marc [FR/FR]; c/o NXP Semiconductors, IP Depart-
ment, Cross Oak Lane, Redhill Surrey RH1 5HA (GB).
CHEVRIE, David, D., R. [FR/FR]; c/o NXP Semicon-
ductors, IP Department, Cross Oak Lane, Redhill Surrey
RH1 5HA (GB). **PHILIPPE, Pascal** [FR/FR]; c/o NXP

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(54) Title: INTEGRATED SINGLE-CRYSTAL MEMS DEVICE



(57) Abstract: Method of manufacturing a MEMS device integrated in a silicon substrate. In parallel to the manufacturing of the MEMS device passive components as trench capacitors with a high capacitance density can be processed. The method is especially suited for MEMS resonators with resonance frequencies in the range of 10 MHz.

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DESCRIPTION

INTEGRATED SINGLE-CRYSTAL MEMS DEVICE

The invention relates to a method of manufacturing an integrated single-crystal MEMS device.

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US6,856,217B1 discloses a Micro-Electromechanical-System (MEMS) device based upon a radially or laterally vibrating disk structure and capable of vibrating at frequencies well past 100 MHz. The center of the disk is a nodal point, so when the disk resonator is supported at its center, anchor dissipation to the substrate is minimized, allowing this design to retain high-Q at high frequency. In addition, this design retains high stiffness at high frequencies and so maximizes dynamic range. Furthermore, the sidewall surface area of this disk resonator is often larger than that attainable in previous flexural-mode resonator designs, allowing this disk design to achieve a smaller series motional resistance than its counterparts when using capacitive (or electrostatic) transduction at a given frequency. The frequency and dynamic range attainable by this resonator makes it applicable to high-Q RF filtering and oscillator applications in a wide variety of communication systems. Its size also makes it particularly suited for portable, wireless applications, where if used in large numbers, such a resonator can greatly lower the power consumption, increase robustness, and extend the range of application of high performance wireless transceivers. In addition a method is disclosed to manufacture the MEMS device. Silicon on Insulator (SOI) wafers are needed in order to process the MEMS device. These SOI wafers are expensive especially if the MEMS device is a resonator devices resonating at frequencies of less than 50 MHz since thick silicon layers are needed in order to provide the mechanical stability of the resonating (disc) structure. An integration of passive components especially capacitors with high capacitance density is not possible.

It's an objective of the current invention to provide a cost effective method for manufacturing MEMS devices enabling the integration of passive

components on one substrate. The objective is achieved by means of a method of manufacturing a MEMS device, which method comprises the steps of:

- providing a device substrate with a top side and a bottom side;
- providing at least one trench in the top side of the device substrate
- 5 defining the shape of a moveable structure;
- providing at least one electrically conductive area on the top side of the device substrate and at least parts of the electrically conductive area form at least one moveable electrode attached to the moveable structure;
- providing a dielectric layer on the top side of the device substrate at least
- 10 partly covering the electrically conductive area;
- providing and structuring an electrically conductive electrode layer on the top side of the device substrate;
- providing at least one anchor point in the dielectric layer;
- providing and structuring an electrically conductive structural layer on
- 15 the top side of the device substrate and the electrically conductive structural layer anchors the moveable structure at the anchor point;
- partly removing the dielectric layer through the structured structural layer;
- removing the device substrate from the bottom side of the device
- 20 substrate in a defined area underneath the trench defining the shape of the moveable structure at least until the trench defining the shape of the moveable structure is reached and
- releasing the moveable structure.

In comparison to prior art the moveable structure is released in three

25 steps. In a first step the dielectric layer is partly removed up to a defined depth in the trenches defining the shape of the moveable structure by e.g. time controlled etching. The time is determined by the etch rate of the dielectric layer, the geometry of etch holes in the structural layer and the final thickness of the moveable structure. In a second step the device substrate is removed underneath the trenches defining the shape of the

30 moveable structure. The etching time of this second step defines the thickness of the

moveable structure. The etching of the backside and the etching of the dielectric layer have to be adapted in a way that the etchant used during backside etching doesn't reach the cavities left after the etching of the dielectric layer. The depth up to where the dielectric layer has been removed in the trenches has to be less than the final thickness of the moveable structure. In a third step the residues of the dielectric layer preventing the contamination of the cavities left after the etching of the dielectric layer with the etchant used for backside etching are removed in order to release the moveable structure. The thickness of the moveable structure can easily be adapted to the mechanical boundary conditions determined by the extension of the moveable structure since the moveable structure is formed by means of the device substrate in contrast to prior art where the moveable structure is part of the SOI layer. The extension of the moveable structure is one decisive parameter to determine the resonance frequency of the moveable structure. Other parameters are the density, Young's modulus and Poisson's ratio of material building the moveable structure. Especially at resonance frequencies below 50 MHz resulting in rather large moveable structures this method provides a decisive cost advantage in comparison to resonant MEMS devices manufactured by means of SOI wafers. The moveable structure is anchored by means of the structural layer at that area or areas where the dielectric layer has been structured in order to provide the anchor point or if more than one is needed the anchor points. The electrically conductive structural layer provides a suspension for the moveable structure on the one side and an electrically conductive connection to the moveable electrode attached to the moveable structure on the other side. The moveable electrode is in interaction with an essentially static reference electrode formed by means of parts of the structured electrode layer.

A further advantage of the method described above is that trench capacitors can be manufactured in parallel. Additional trenches can be provided on the topside of the device substrate. The surface of these trenches belongs to the conductive areas on the topside of the device substrate and forms a first electrode of the trench capacitor. The surface of the trenches is covered with the dielectric layer. The electrically conductive electrode layer fills the trenches covered with the dielectric layer forming a second electrode. These stacked structure of the first electrode, the dielectric

layer and a second electrode can be used as capacitor whereby the capacitance density is determined by the thickness of the dielectric layer and the effective area of the capacitive structure. Consequently the MEMS device can be manufactured in parallel with integrated capacitors with high capacitance density. Adding further layers of defined electrical conductivity enables the integration of resistors and inductors in addition. The combination of front side etching (etching the dielectric layer) and backside etching of the device substrate can further be used to provide through vias through the device substrate. After the trenches have been opened from the backside an electrically conductive contact layer can be provided from the backside. This contact layer is in physical contact with the electrode layer provide from the front side of the device substrate resulting in an electrically conductive connection between the front side of the device substrate and the backside of the device substrate forming a so called through via. The through vias enable the electrical connection of the MEMS device (and other passive circuit components) with further active or passive circuitry on a second substrate. The MEMS device can easily be stacked on the second substrate.

In a further embodiment of the current invention a sacrificial layer is provided after the deposition and structuring of the electrode layer. The sacrificial layer can be deposited before or after structuring of the dielectric layer. If the sacrificial layer can be removed by the same etchant as the dielectric layer it is preferably etched at a higher etching rate than the dielectric layer. The sacrificial layer is essentially removed before the dielectric layer is etched and the parts of the dielectric layer previously covered by the sacrificial layer are exposed to the etchant essentially at the same time. The part of the dielectric layer provided essentially parallel to the surface of the device substrate is etched first enabling a better control of the etching of the dielectric layer provided at the sides of the trenches (essentially perpendicular to the surface of the device substrate). The dielectric layer can be a oxide layer thermally grown on a silicon device substrate enabling excellent control about the thickness of the dielectric layer especially in the trenches and the sacrificial layer is a deposited silicon oxide layer of

lower density and consequently higher etching rate with respect to an e.g. buffered oxide etch (BOE) in comparison to the thermally grown silicon oxide.

In another embodiment of the current invention a sacrificial layer is provided that can be removed with a first etchant and the first etchant essentially doesn't remove the dielectric layer and the dielectric layer can be removed with a second etchant and the second etchant essentially doesn't remove the sacrificial layer whereby essentially doesn't remove means that the etch rate is of the layer with respect to the etchant is at least 2 decades lower. In this case the sacrificial layer is etched first until the dielectric layer covering the topside of the moveable structure is etched free. In a second etch step the dielectric layer is removed whereby the part of the dielectric layer covering the topside of the moveable structure is essentially removed first by the etchant before the dielectric layer in the trenches is exposed to the etchant. The etching time is determined by the etching of the dielectric layer in the trenches enabling an excellent control about the etching depth in the trenches that means how far is the dielectric layer removed in the trenches. The dielectric layer can again be provided by thermal oxidation of a silicon device substrate that can be etched by a buffered oxide etch whereby the sacrificial layer can be silicon nitride that can be etched by means of phosphoric acid at elevated temperature.

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In a further embodiment of the current invention the MEMS device is encapsulated on the topside of the device substrate and a vacuum is provided before a packaging substrate is bonded to the bottom side of the device substrate. The air causing damping of the moveable structure is evacuated resulting e.g. in a high-Q resonator. The encapsulation layer can be silicon oxide, silicon nitride or an organic material. The etch holes for etching the dielectric layer or the sacrificial layer and the dielectric layer have to be positioned in a way that the deposition of the encapsulation layer does not disturb the mobility of the moveable structure. Preferably no material should be deposited on top of the moveable structure. If etch holes are provided above the resonator structure in order to enable a faster etching of the dielectric layer or the sacrificial layer the etch hole have

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to be positioned around the areas where the moveable structure is anchored or suspended by means of the electrically conductive structural layer. The encapsulation layer is partly deposited around the anchor essentially without influencing the mobility of the moveable structure. As long as there is no structure on the bottom side of the device wafer or on the packaging wafer those have to be aligned, the packaging wafer is simply bonded to the device substrate by means of well-known wafer bonding techniques without special alignment. Alternatively to vacuum a protective gas can be provided.

It's further an objective of the current invention to provide a low cost MEMS device. The objective is achieved by means of MEMS devices comprising a device substrate with at least one reference electrode, a moveable structure comprising the same material as the device substrate and the moveable structure having at least one moveable electrode, the moveable structure is embedded in the device substrate and indirectly attached to the device substrate via at least one anchor essentially arranged above the device substrate, and a dielectric layer being removed locally so as to allow the moveable structure attached to the moveable electrode to be movable, and an electrical driving circuit is connected to the moveable electrode and the reference electrode. The moveable electrode and/or the reference electrode can be coherent electrodes or segmented electrodes. If e.g. the moveable electrode is segmented it's possible to independently apply a voltage to the different electrically isolated segments of the moveable electrode. The segments of the moveable electrode being on different electrical potential during operation have to be contacted by means of different anchor points electrically isolated from each other. The segmented moveable electrode can e.g. be used to stimulate different resonant modes if the moveable structure is used as a resonator. Preferably single crystal silicon is used as device substrate. Single crystal silicon is more attractive material compared to polysilicon due to its low internal friction and consequently higher mechanical quality factor, low internal stress and independence from various process parameters in comparison to SOI layers.

In a further embodiment the MEMS device is combined with a capacitive structure. The capacitive structure comprises a multitude of trenches in the device substrate. The surface of the trenches is electrically conductive e.g. doped silicon if a single crystal silicon device substrate is used forming a first electrode of the capacitive structure. The dielectric layer that is partly removed in order to release the moveable structure builds the isolating layer between the first electrode and the structured electrode layer forming the second electrode of the capacitive structure. The combination of the MEMS device together with the capacitive structure can be used to e.g. design integrated sensor circuits or oscillator circuits. In the first case the moveable structure can be e.g. a test mass for sensing acceleration. In the second case the moveable structure is a mechanical resonator structure whereby preferably one resonant mode of the resonator structure is stimulated and sensed by means of the moveable electrode and the reference electrode. The geometrical shape of the resonator structure in combination with Poisson's ratio and the Young's modulus determine the resonance frequencies of the resonator structure. Preferable geometric shapes of the resonator structure are discs or square plates.

The present invention will now be explained in greater detail with reference to the figures, in which similar parts are indicated by the same reference signs, and in which:

Figs. 1a – 1i illustrate the different stages of the method of manufacturing a MEMS device according to one embodiment of the current invention;
Fig. 2 shows a principal sketch of a top view of a MEMS device according to one embodiment of the current invention; and
Fig. 3 shows a cross section of a MEMS device according to a further embodiment of the current invention.

Fig. 1a shows a silicon device substrate 10 after a circular trench 20 is etched in the topside of the device substrate 10 by means of Deep Reactive Ion Etching

(DRIE). The lower picture in Fig. 1a shows a top view of the device substrate 10 with the trench 20 where the line A-A of the cross section shown in the upper picture of Fig. 1a is defined. The line A-A is no straight line. It comprises two straight parts meeting at the mid point of the circular trench 20 and enclosing an angle of around 20 degree. The trench 20 has a width of around 3 μm and a depth of around 20 μm . In Fig. 1b is depicted a cross section of the device substrate along the line A-A as defined in Fig. 1a after parts of the area of the topside of the silicon device substrate 10 including the surface of the trench 20 have been made conductive by means of doping. A part of this conductive area builds the moveable electrode 30. Fig. 1c shows the cross section of the device substrate 10 along line A-A after a thin dielectric layer 40 of SiO_2 (around 50 nm) have been thermally grown on the topside of the device substrate 10, and subsequently electrically conductive doped poly silicon has been deposited building the electrode layer 50. The electrode layer 50 is structured whereby the trench 20 is filled with the electrically conductive doped poly silicon building the reference electrode. Fig. 1d shows the cross section of the device substrate 10 along line A-A after a sacrificial layer 60 around 1 μm TEOS has been deposited. The sacrificial layer 60 is structured in order to provide contact openings 110 to the structured electrode layer 50. Further the sacrificial layer 60 and the dielectric layer 40 are structured together (both layers consist of silicon oxide) providing an anchor point 100 for the moveable structure. Fig. 1e shows the cross section of the device substrate 10 along line A-A after the electrically conductive structural layer 70 is deposited on the topside of the device substrate 10 and structured. The structural layer 70 consists of doped poly silicon anchoring the moveable structure at anchor point 100. Additionally the electrically conductive doped poly silicon provides contacts to the structured electrode layer 50 building the reference electrode and to the moveable electrode 30 (via the anchor point 100) whereby both electrodes are electrically isolated from each other. Further etch holes 120 are provided for etching the sacrificial layer 60 and the dielectric layer 40. Fig. 1f shows the cross section of the device substrate 10 along line A-A after a hard mask have been provided and structured. The hard mask is removed after the sacrificial layer 60 and the dielectric layer 40 have been etched as shown in Fig. 1g. The sacrificial layer 60 and the dielectric layer 40 are

etched by means of a buffered oxide etch (BOE) around the anchor point 100 via the etch holes 120. The sacrificial layer 60 etches faster than the dielectric layer 40 due to the higher density of the thermally grown silicon oxide in comparison to TEOS.

Optionally further etch holes can be provide around the anchor point 100 in order to
 5 accelerate the etching of the sacrificial layer 60. By controlling the etching time the sacrificial layer 60 and the dielectric layer 40 are removed above the moveable electrode 30 and the dielectric layer 40 is partly removed in the trench 20 that means the dielectric layer is removed up to a depth of around 15 μm from the topside of the device substrate 10 at the inner surface of the trench 20 with respect to the part of the device substrate 10
 10 circumvented by the circular trench 20. Fig. 1h shows the cross section of the device substrate 10 along line A-A after an encapsulation layer 90 has been deposited preventing short circuits. In addition contacts 130 and 140 to the electrically conductive structural layer 70 are provided through the encapsulation layer 90 in order to contact the moveable electrode 30 and the reference electrode formed by the residues of the
 15 electrode layer 50. Fig. 1i shows the cross section of the device substrate 10 along line A-A after the moveable structure 1000 has been released. First a cavity 300 is etched from the backside of the device substrate 10 underneath the area circumvented by the circular trench 20 by means of anisotropic dry etching. The etching depth of the cavity 300 is the thickness of the devices substrate 10 minus the depth of the trench 20. The
 20 trench 20 is reached but the moveable structure 1000 isn't released during backside etching. A thin residue of the dielectric layer 40 at the inner surface of the circular trench 20 protects the cavity 200 resulting from removing the sacrificial layer 60 and the dielectric layer 40. This residual of the dielectric layer 40 is removed by means of a short etch step with buffered oxide etch.

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Fig. 2 shows a principal sketch of one embodiment of the current invention. A top view of a disk resonator is shown with the contact 130 to the moveable electrode via the structured structural layer 70. Contact 140 provides the electrical contact to the reference electrode via the contact area 110 between the structured
 30 structural layer 70 and the structured electrode layer 50 building the reference electrode.

The structured parts of the structural layer 70 contacted to the reference electrode and the structured parts of the structured layer contacted to the moveable electrode are separated by means of the etch holes 120 in the structural layer. The etch holes 120 are finally filled with the encapsulation layer.

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Fig. 3 shows a cross section of the embodiment of the current invention shown in Fig. 1i where a packaging wafer 400 has been bonded to the backside of the device substrate 10. The moveable structure 1000 is isolated from the environment by means of the encapsulation layer 90 and the packaging wafer 400. A vacuum can be provided around the moveable structure or a protective gas. The moveable structure 1000 is the resonator structure of a MEMS resonator. The resonator structure has a disk shape and the theory about contour vibrations of isotropic circular plates gives the relation between material properties, dimensions and resonant frequencies of the disk:

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$$\delta \times \frac{J_0(\delta)}{J_1(\delta)} = 1 - \nu ,$$

where

$$\delta = \omega_0 \cdot R \cdot \sqrt{\frac{\rho(1-\nu^2)}{E}} ,$$

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and where R is the disk radius; $\omega_0 = 2\pi \cdot f_0$ is its angular resonance frequency; $J_n(y)$ is the Bessel function of the first kind of order n ; and ρ , ν and E are the density, Poisson's ratio and Young's modulus, respectively, e.g. of a silicon substrate.

The resonator structure is a disk fixed at its center, an reference electrode surrounding the vertical electrically conductive surface of the resonator structure building the moveable electrode 30, and an air gap between the moveable electrode and the reference electrode. As an implementation, the disk is e.g. 20 μ m thick, and has an average radius of e.g. 100 μ m. The air gap between moveable electrode and the reference electrode is

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50nm. Applying a voltage between moveable electrode and the reference electrode generates a radial force on the outer surface of the resonator structure that tends to extend it. In consequence, the vibrating mode is the expansion and the contraction of the disk. The potential of such a resonator can be demonstrated by estimating the performance according to the theory about contour vibrations of isotropic circular plates. All of them can be calculated from known parameters such as dimensions or single-crystal silicon material parameters (Table 1). The expected Q is in the range of 10000-100000.

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Parameter	Symbol	Value
Young's Modulus of single-crystal silicon	E	150 GPa
Poisson's Ratio of single-crystal silicon	ν	0.3
Density of single-crystal silicon	ρ	2330 kg/m ³
Free-space Permittivity	ϵ_0	8.854e-12 F/m
Relative Permittivity	ϵ_r	1
Disk height	h	20 μm
Disk Radius	R	100 μm
Air Gap Thickness	d	50 nm

Table 1: Parameters used in calculation. Single-crystal silicon is assumed to be isotropic.

Values of Table 1 lead to the resonance frequency of the fundamental mode of $f_0=27\text{MHz}$.

The present invention is described with respect to particular embodiments
5 and with reference to certain drawings but the invention is not limited thereto but only by the claims. Any reference signs in the claims shall not be construed as limiting the scope. The drawings described are only schematic and are non-limiting. In the drawings, the size of some of the elements may be exaggerated and not drawn on scale for illustrative purposes. Where the term “comprising” is used in the present description and claims, it
10 does not exclude other elements or steps. Where an indefinite or definite article is used when referring to a singular noun e.g. "a" or "an", "the", this includes a plural of that noun unless something else is specifically stated.

Furthermore, the terms first, second, third and the like in the description and in the claims, are used for distinguishing between similar elements and not necessarily for
15 describing a sequential or chronological order. It is to be understood that the terms so used are interchangeable under appropriate circumstances and that the embodiments of the invention described herein are capable of operation in other sequences than described or illustrated herein.

Moreover, the terms top, bottom, first, second and the like in the description
20 and the claims are used for descriptive purposes and not necessarily for describing relative positions. It is to be understood that the terms so used are interchangeable under appropriate circumstances and that the embodiments of the invention described herein are capable of operation in other orientations than described or illustrated herein.

CLAIMS

1. Method of manufacturing a MEMS device, which method comprises the steps of:
- providing a device substrate 10 with a top side and a bottom side;
 - 5 - providing at least one trench 20 in the top side of the device substrate 10 defining the shape of a moveable structure 1000;
 - providing at least one electrically conductive area on the top side of the device substrate 10 and at least parts of the electrically conductive area form at least one moveable electrode 30 attached to the movable
 - 10 structure 1000;
 - providing a dielectric layer 40 on the top side of the device substrate 10 at least partly covering the electrically conductive area;
 - providing and structuring an electrically conductive electrode layer 50 on the top side of the device substrate 10;
 - 15 - providing at least one anchor point 100 in the dielectric layer 40;
 - providing and structuring an electrically conductive structural layer 70 on the top side of the device substrate 10 and the electrically conductive structural layer 70 anchors the moveable structure 1000 at the anchor point 100;
 - 20 - partly removing the dielectric layer 40 through the structured structural layer 70;
 - removing the device substrate 10 from the bottom side of the device substrate 10 in a defined area underneath the trench 20 defining the shape of the moveable structure 1000 at least until the trench 20 defining the
 - 25 shape of the moveable structure 1000 is reached and
 - releasing the moveable structure 1000.

2. Method of manufacturing a MEMS device according to claim 1, which method comprises the additional steps of:
- providing a sacrificial layer 60 on top of the structured electrode layer 50;
 - structuring the sacrificial layer 60 and
 - partly removing the sacrificial layer 60 and the dielectric 40 layer through the structured structural layer 70.
- 10 3. Method of manufacturing a MEMS device according to claim 2, whereby the dielectric layer 40 and the sacrificial layer 60 can be removed with the same etchant and the etching rate of the sacrificial layer 60 with respect to the etchant is higher than the etching rate of the dielectric layer 40 with respect to the etchant.
- 15 4. Method of manufacturing a MEMS device according to claim 2, whereby the sacrificial layer 60 can be removed with a first etchant and the first etchant essentially doesn't remove the dielectric layer 40 and the dielectric layer 40 can be removed with a second etchant and the second etchant essentially doesn't remove the sacrificial layer 60.
- 20 5. Method of manufacturing a MEMS device according to claim 3, whereby the device substrate 10 is a silicon substrate, the dielectric layer 40 is thermally grown silicon oxide and the sacrificial layer 60 is deposited silicon oxide.
6. Method of manufacturing a MEMS device according to claim 4, whereby
- 25 the device substrate 10 is a silicon substrate, the dielectric layer 40 is thermally grown silicon oxide and the sacrificial layer 60 is deposited silicon nitride

7. Method of manufacturing a MEMS device according to any of the preceding claims, which method comprises the additional steps of:

- encapsulating the top side of the device substrate 10;
- providing a vacuum;
- 5 - providing a packaging substrate 400 and
- bonding the packaging substrate 400 to the bottom side of the device substrate 10.

8. A MEMS device comprising a device substrate 10 with at least one
10 reference electrode, a moveable structure 1000 comprising the same material as the device substrate 10 and the moveable structure 1000 having at least one moveable electrode 30, the moveable structure 1000 is embedded in the device substrate 10 and indirectly attached to the device substrate 10 via at least one anchor essentially arranged above the device substrate 10, and a dielectric layer 40 being removed locally so as to
15 allow the moveable structure 1000 attached to the moveable electrode 30 to be movable, and an electrical driving circuit is connected to the moveable electrode 30 and the reference electrode.

9. A MEMS device as claimed in claim 8 further comprising a capacitive
20 structure electrically connected to the moveable electrode 30 and/or the reference electrode, the capacitive structure comprises a multitude of trenches 20 in the device substrate, and the surface of the trenches 20 is electrically conductive forming a first electrode of the capacitive structure, and the capacitive structure further comprises the dielectric layer 40 and a second electrode comprising the same material as the reference
25 electrode.

10. A MEMS device as claimed in claim 8 or 9, characterized in that the MEMS device is a MEMS resonator.

11. A MEMS resonator as claimed in claim 10, characterized in that the moveable structure 1000 essentially has a disk shape.

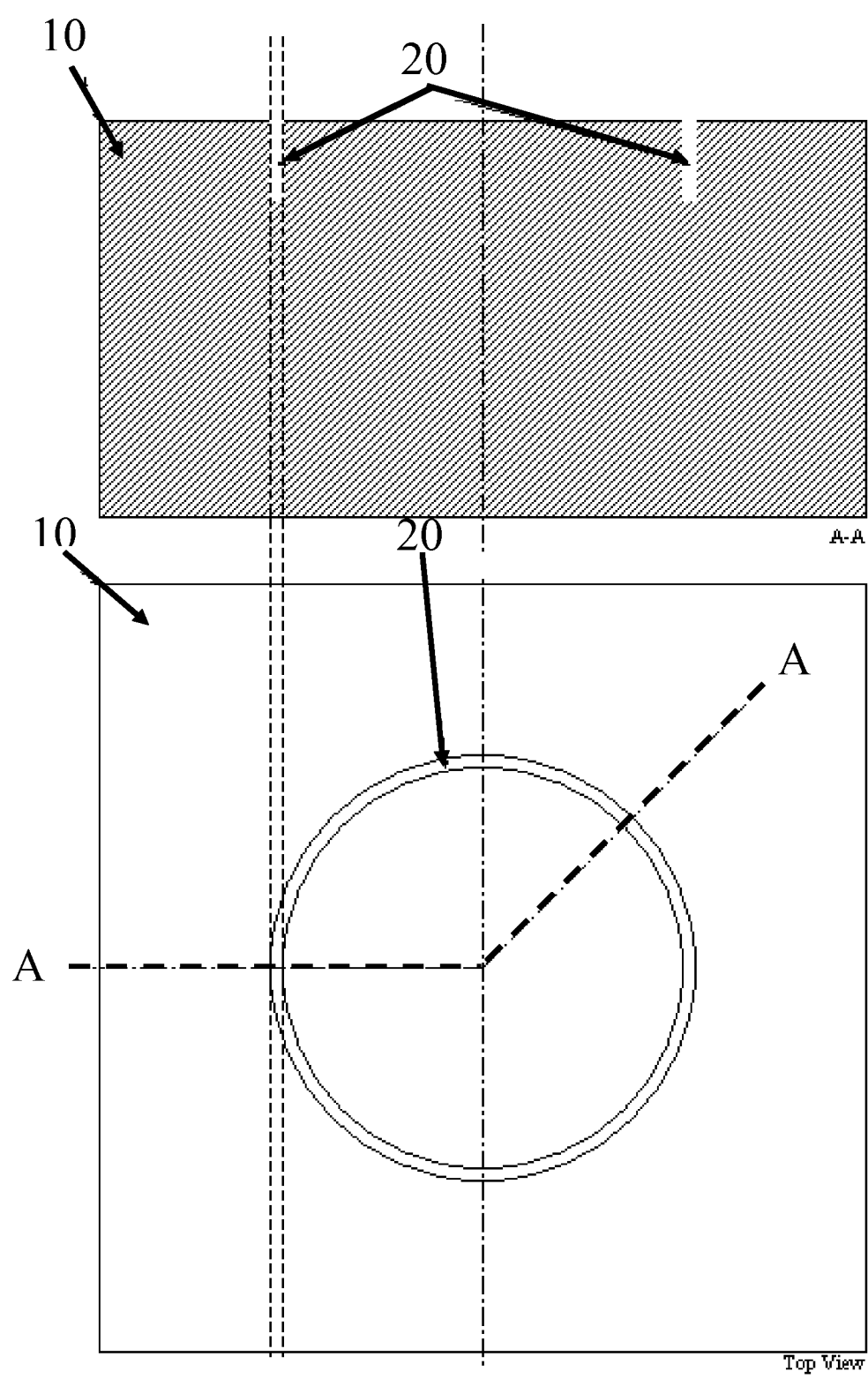


Fig.1a

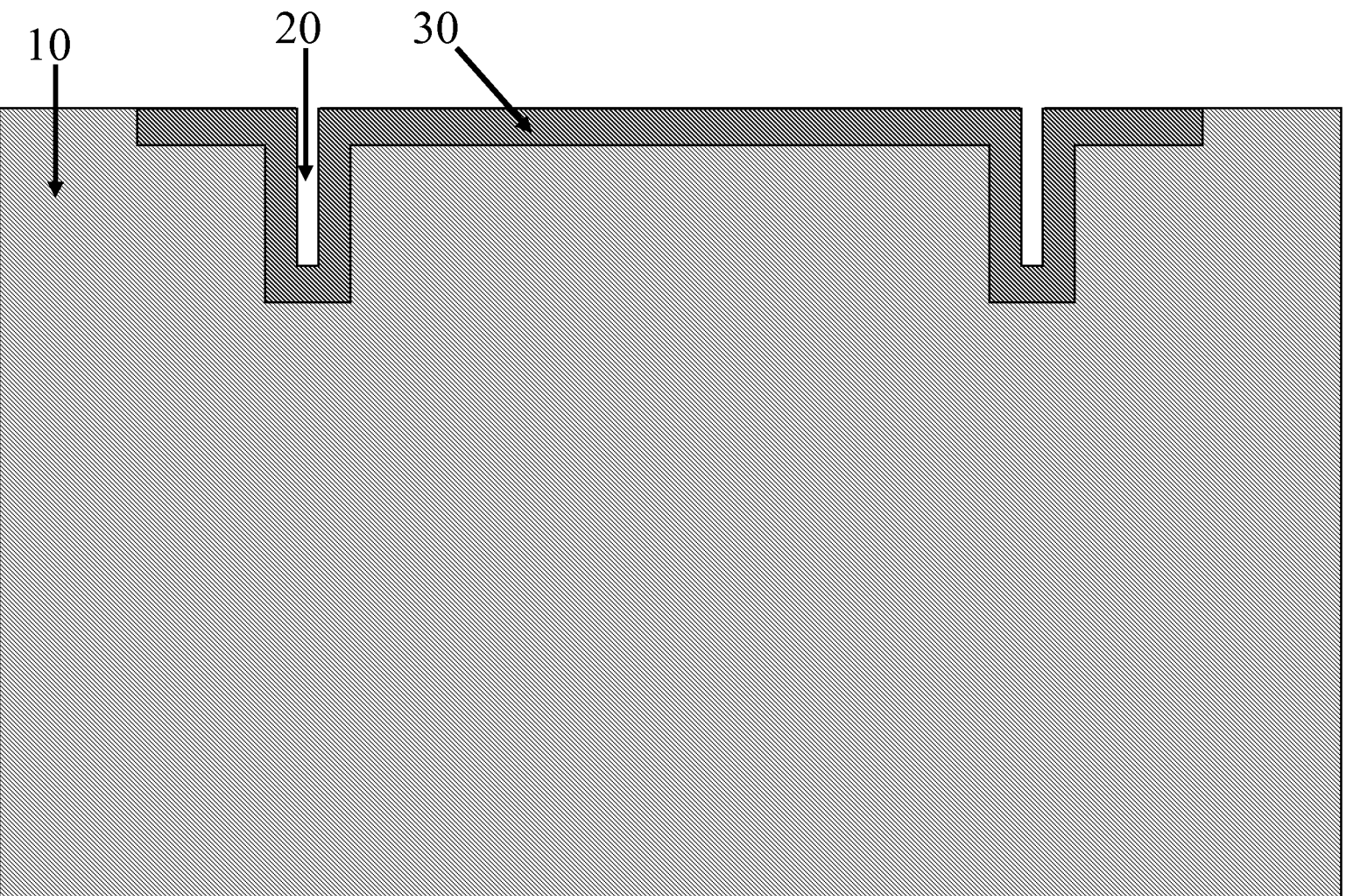


Fig. 1b

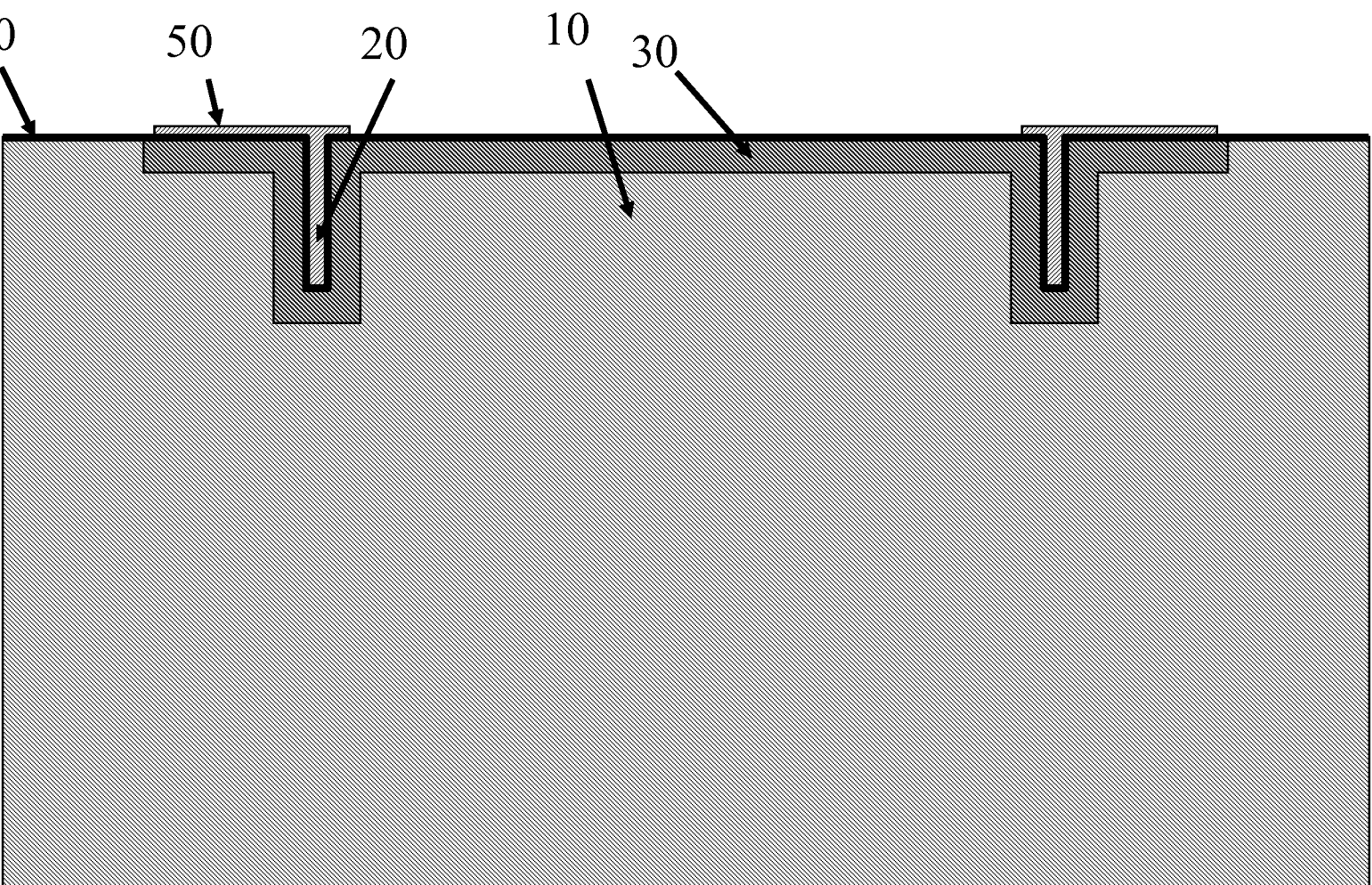


Fig. 1c

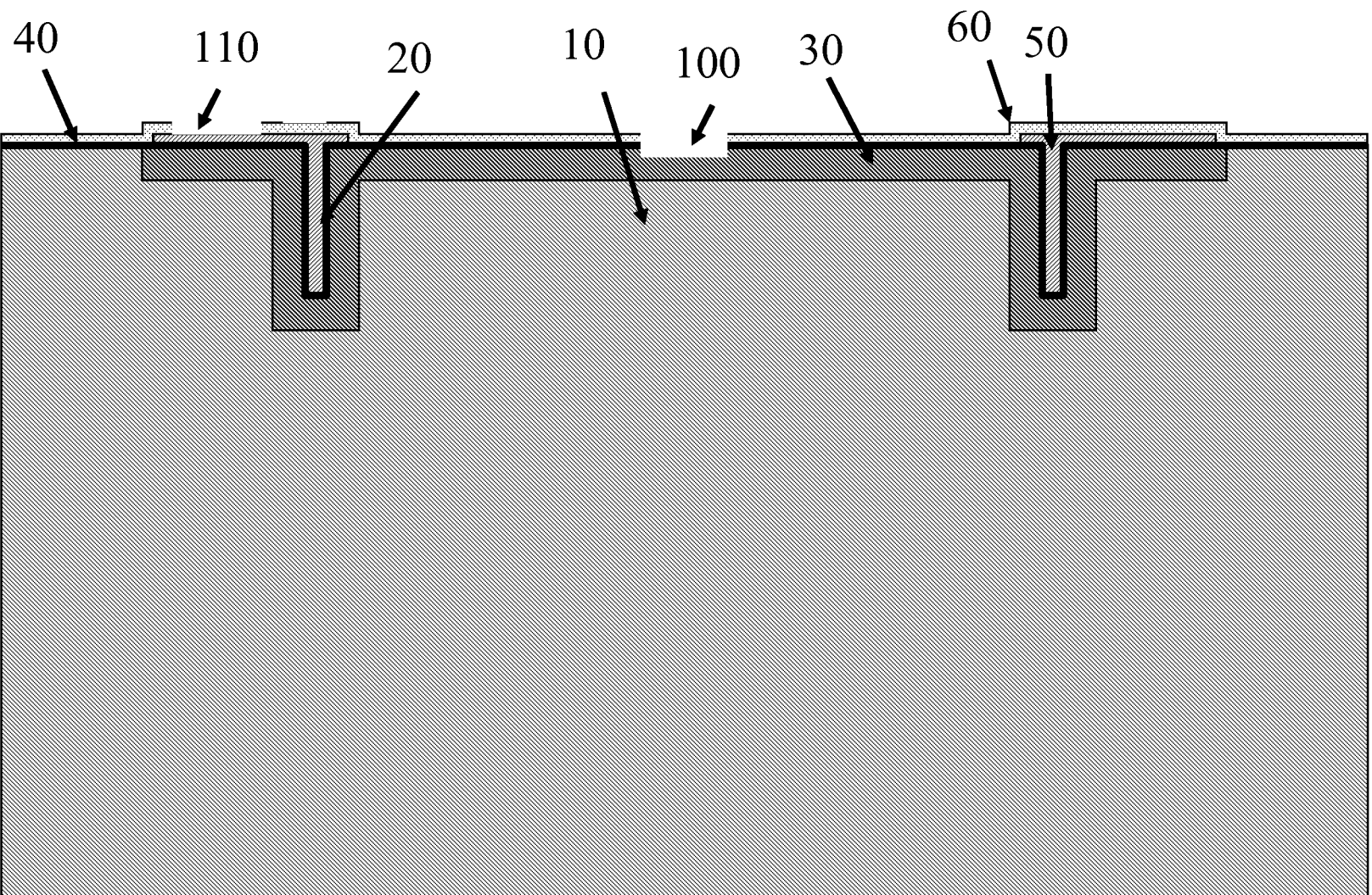


Fig. 1d

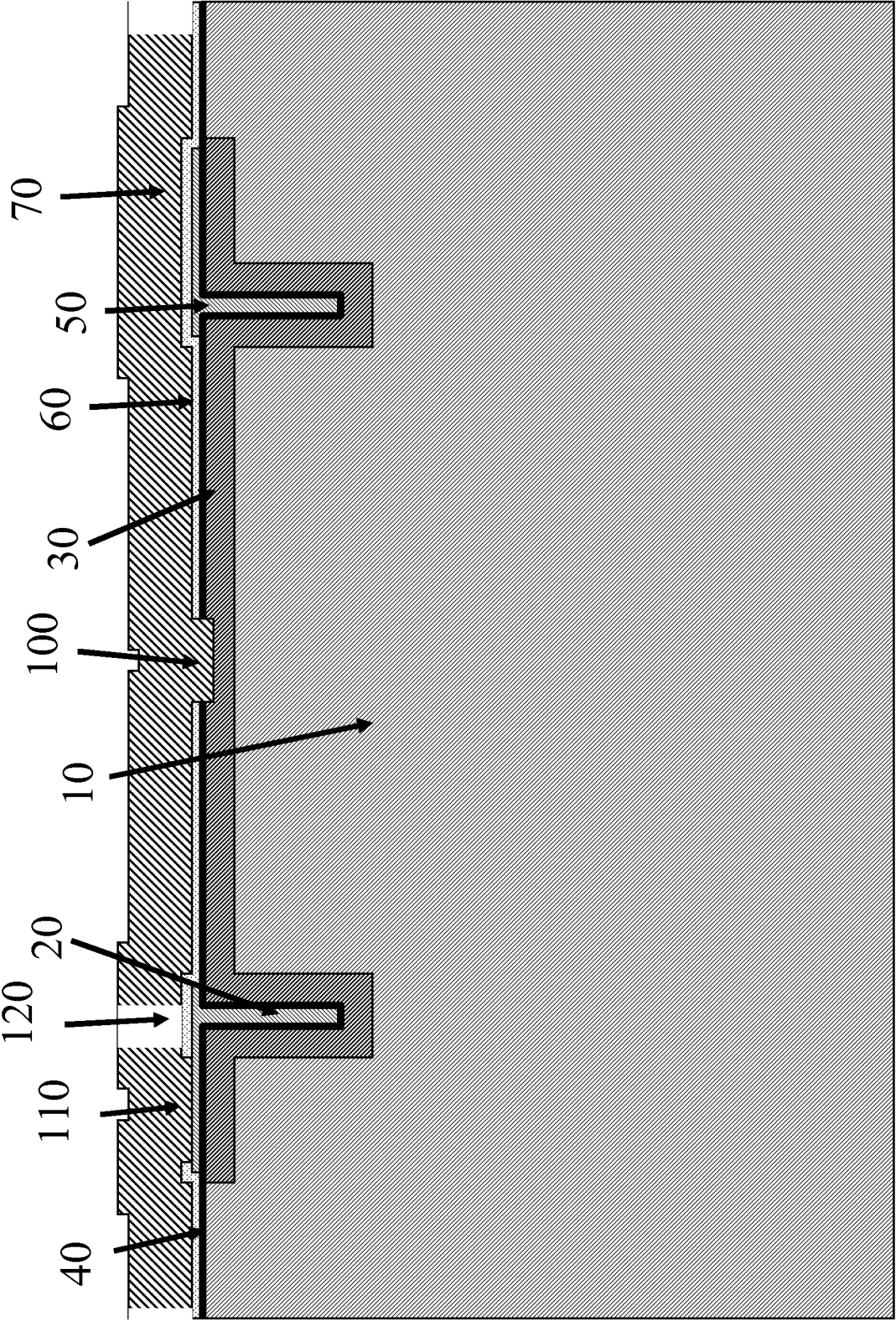


Fig.1e

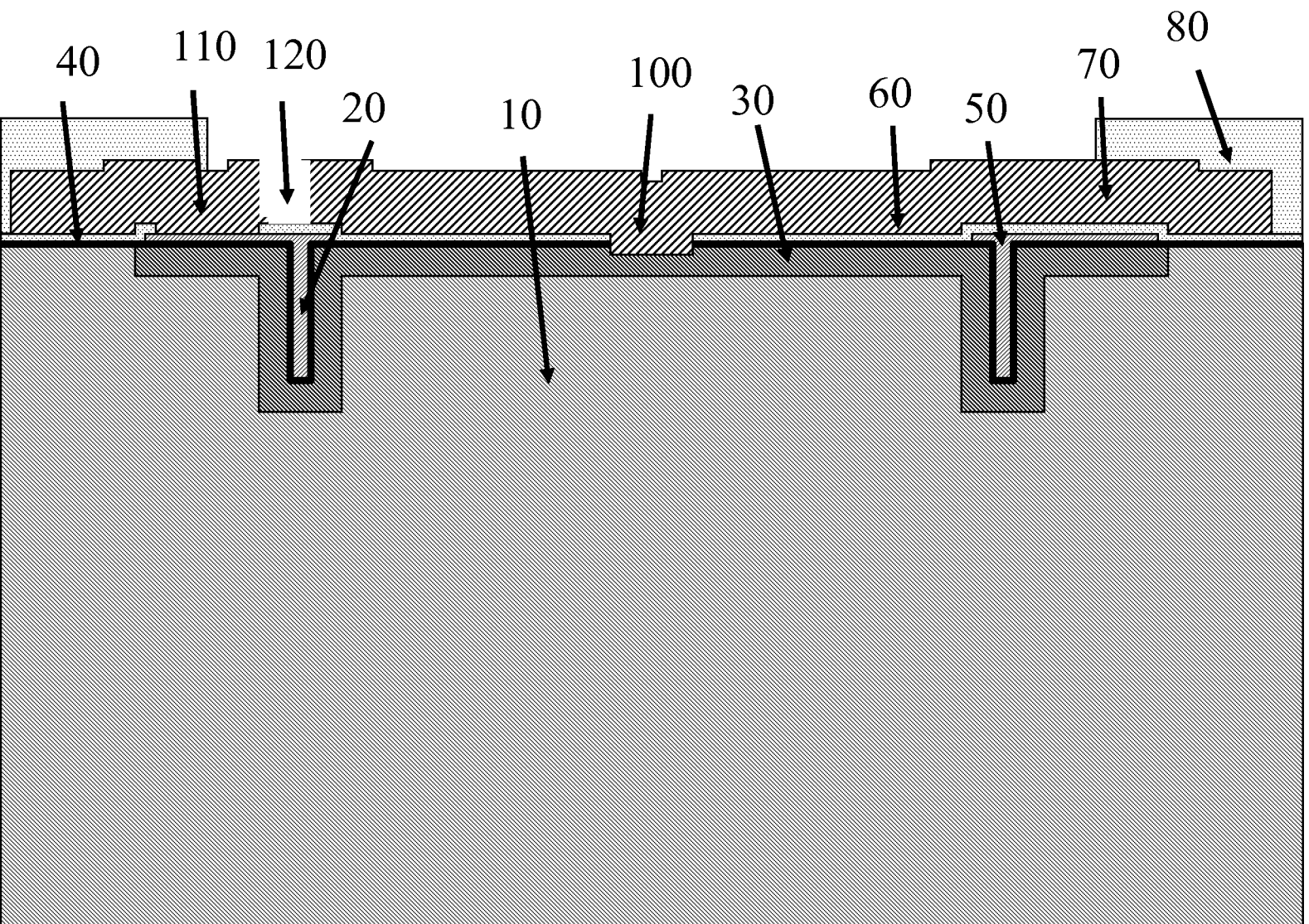


Fig.1f

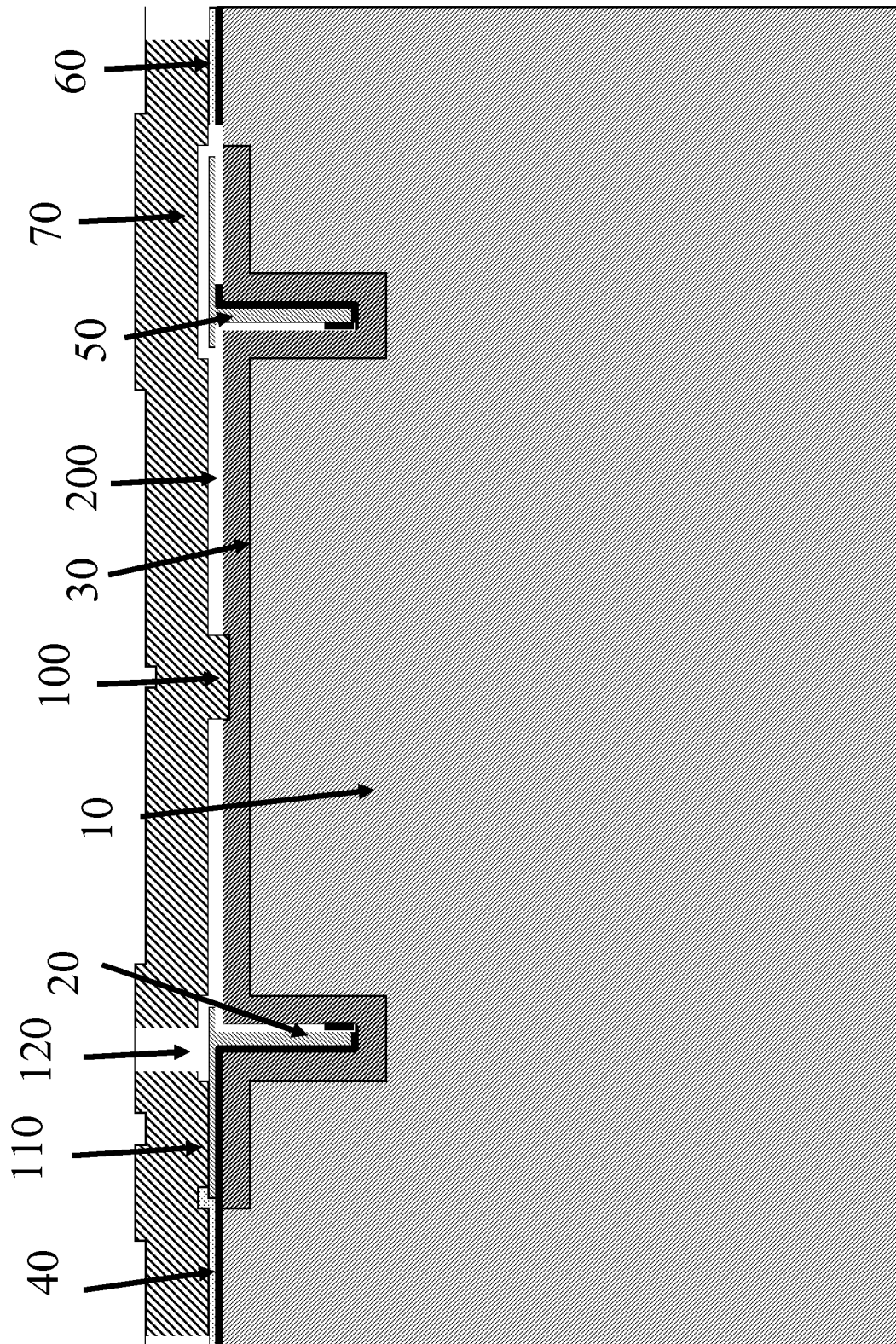


Fig.1g

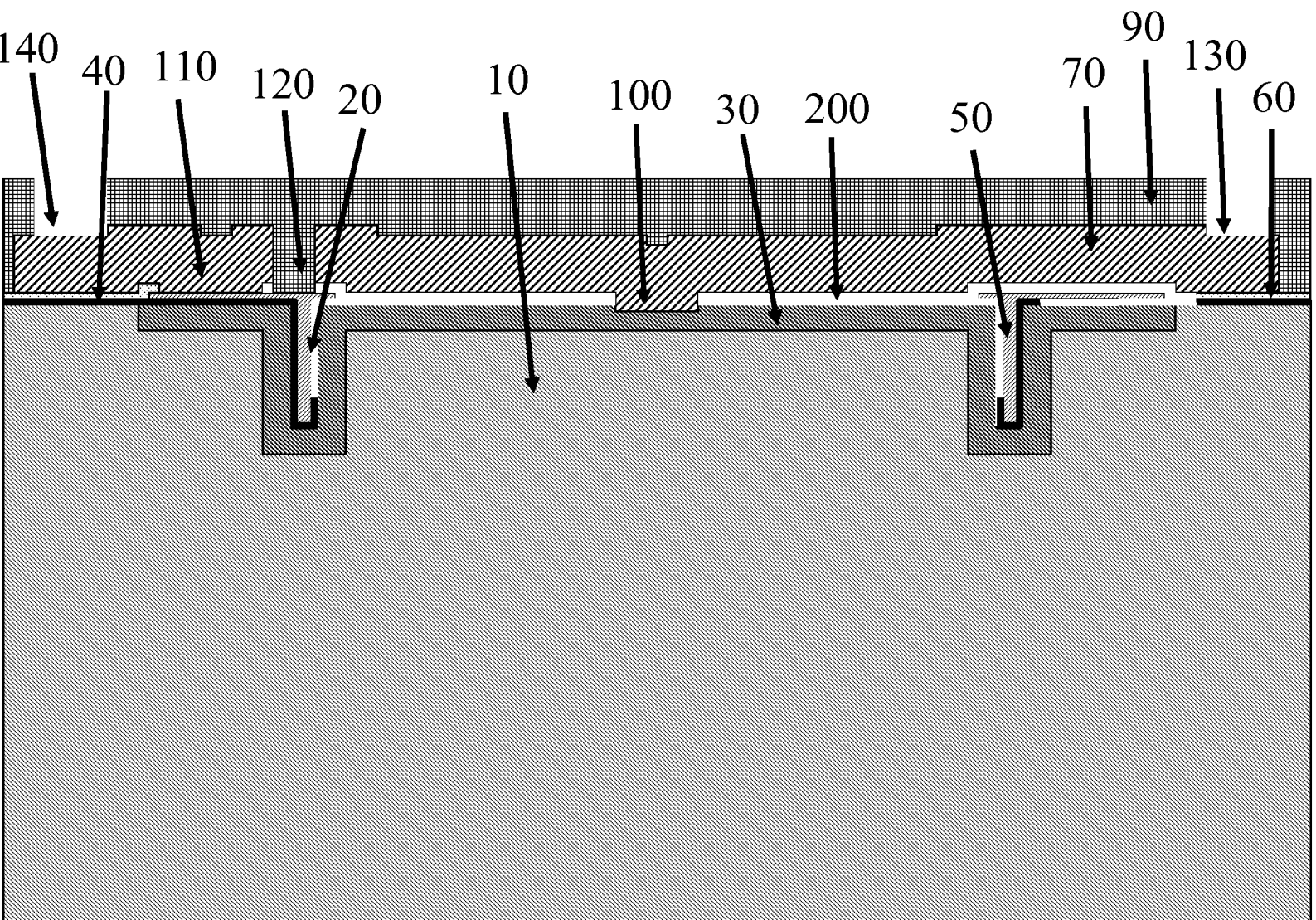


Fig. 1h

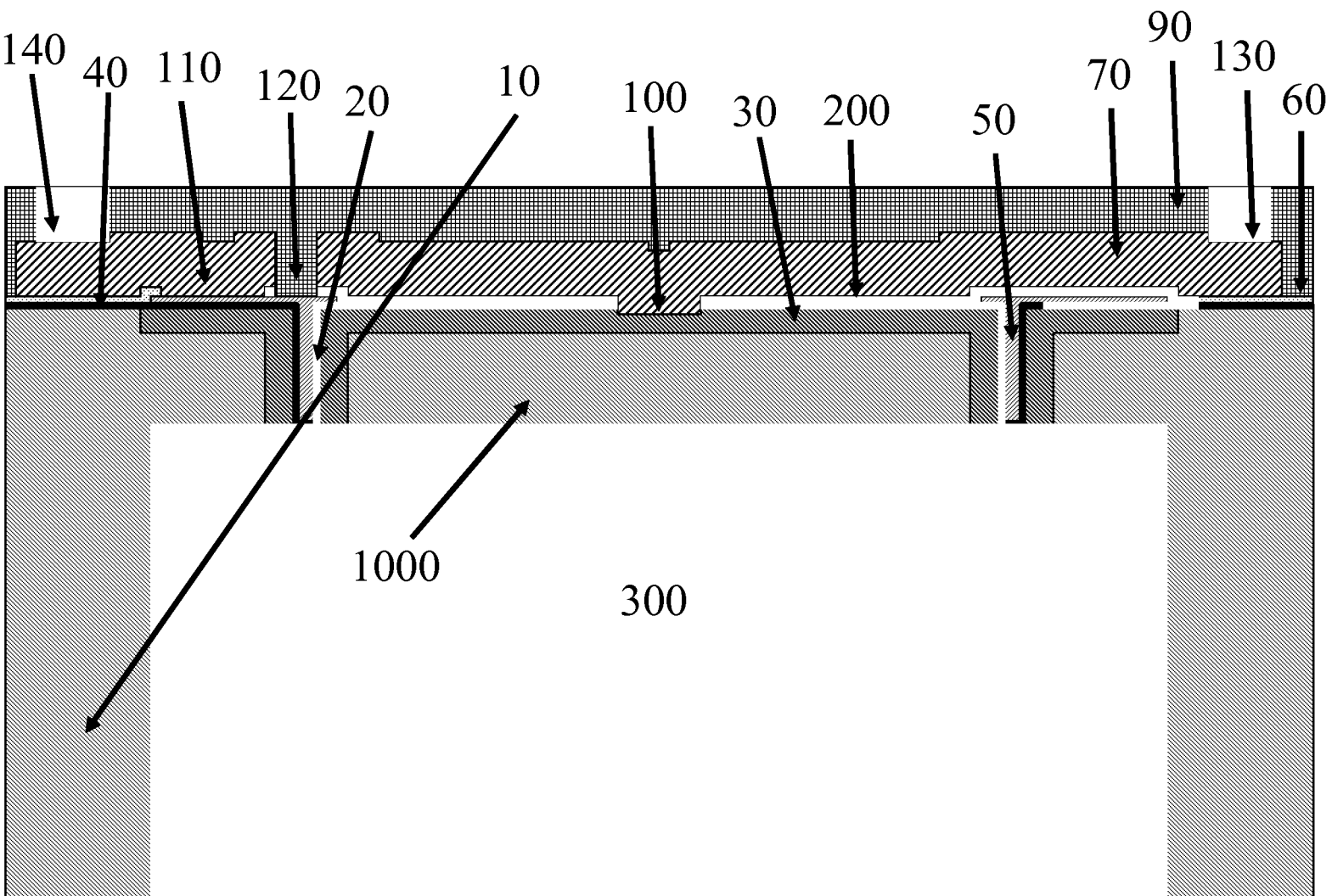


Fig. 1i

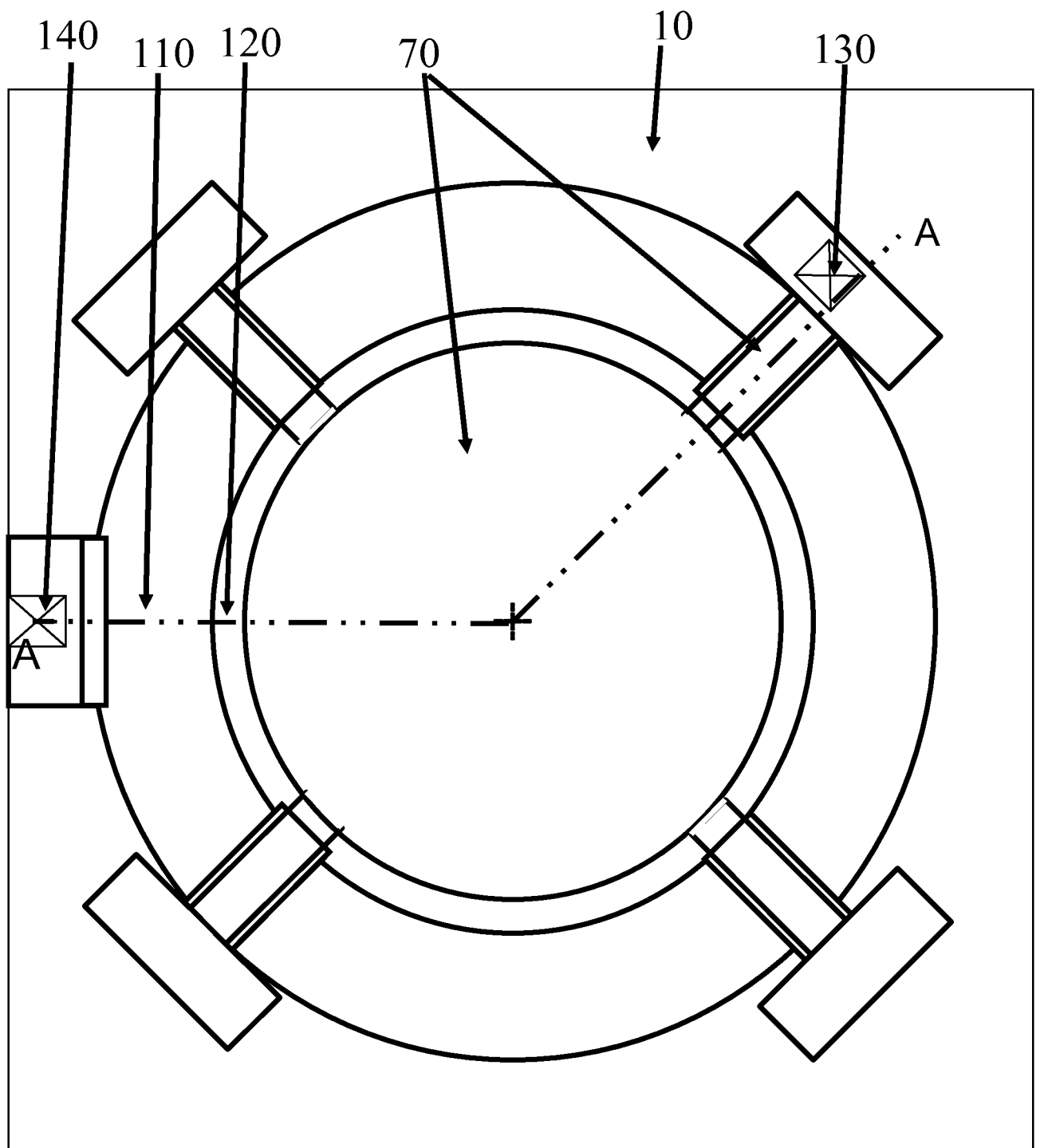


Fig.2

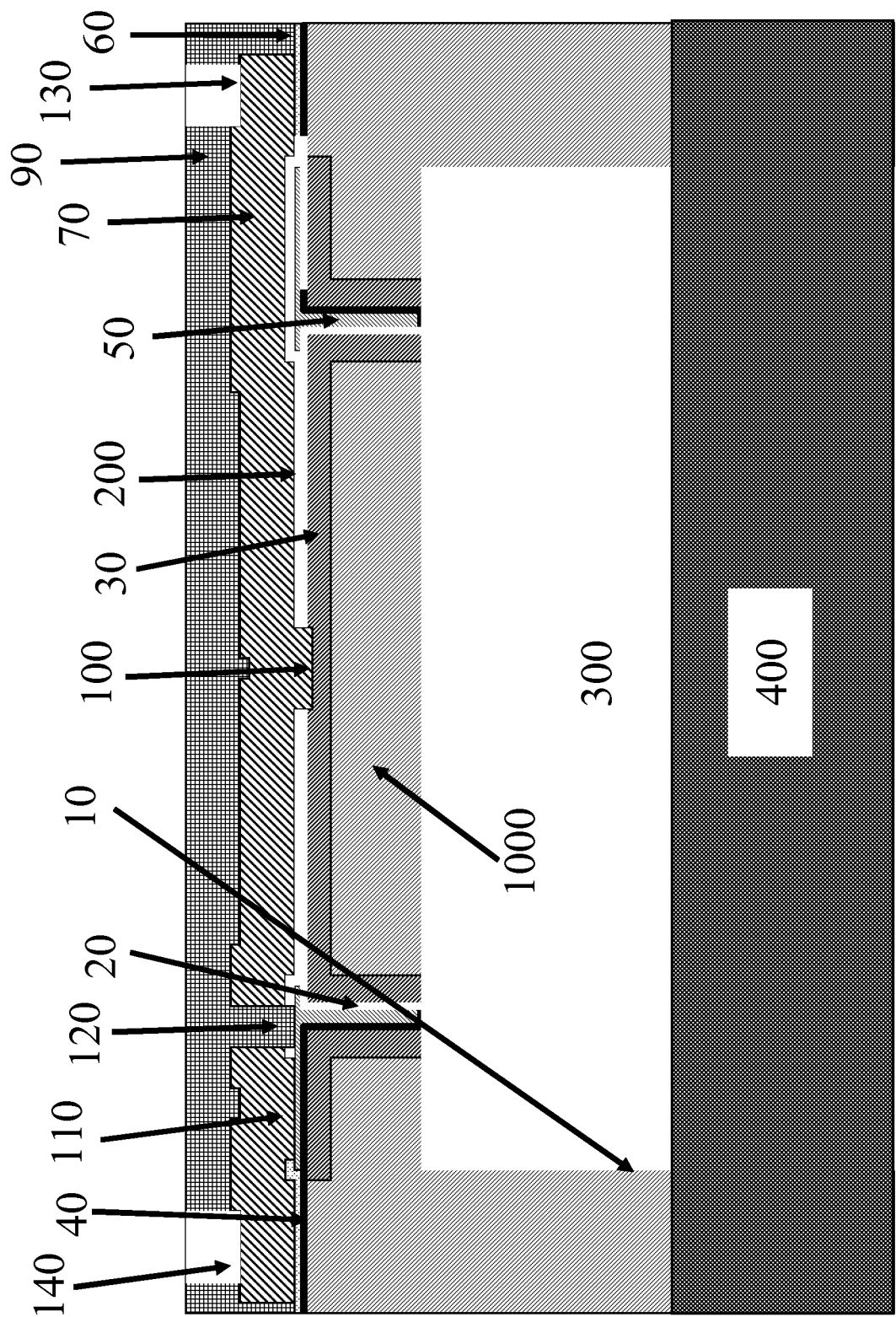


Fig.3