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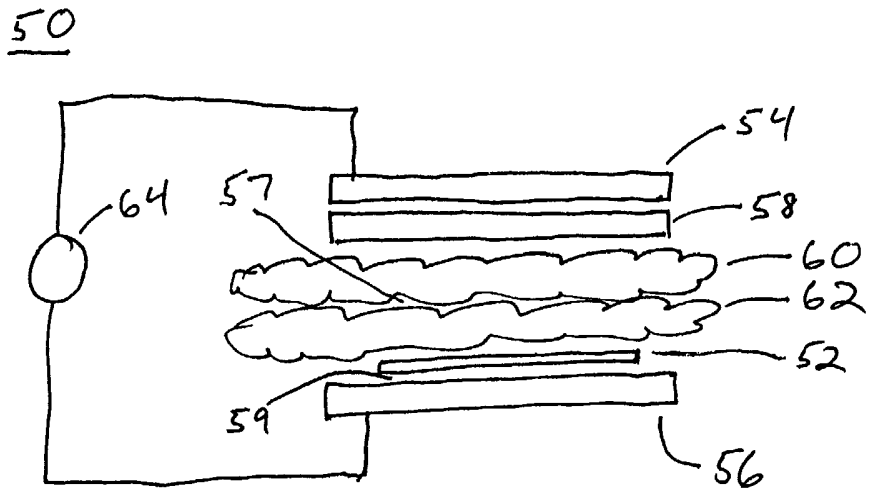
(54) Title: DIELECTRIC BARRIER DISCHARGE PROCESS FOR DEPOSITING SILICON NITRIDE FILM ON SUBSTRATES



(57) Abstract: In one embodiment, the present invention is a method of coating at least one wafer with silicon nitride. The first step in the method is assembling at least one electrode set, wherein each electrode set includes at least one dielectric barrier between a top electrode and a bottom electrode. The second step is flowing at least one purge gas and at least one reactant at least partially between the electrodes, of at least one electrode set, substantially at atmospheric pressure. The next step in the inventive method is placing a wafer between the electrodes of at least one electrode set, wherein the wafer is substantially encompassed by the flowing gas. The last step in this embodiment of the inventive method is supplying AC power to at least one electrode set thereby causing a dielectric barrier discharge.

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DIELECTRIC BARRIER DISCHARGE PROCESS FOR DEPOSITING SILICON NITRIDE FILM ON SUBSTRATES

RELATED APPLICATIONS

The present invention claims priority based on U.S. Provisional Patent Application Serial No. 60/315,098, which was filed August 27, 2001.

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FIELD OF THE INVENTION

The present invention relates to depositing thin films on substrates. Specifically, the present invention relates to the method and apparatus for using an atmospheric pressure dielectric barrier discharge process to form thin film deposits on silicon substrate surfaces for solar cell applications.

BACKGROUND OF THE INVENTION

In silicon wafers intended for solar cell application, thin film deposited silicon nitride is used for cell passivation and as an antireflection coating. Films are deposited by any of a number of different means, including plasma enhanced chemical vapor deposition ("PECVD"). In a typical PECVD process for silicon nitride on solar cells, the silicon wafer is exposed to a plasma-excited gas composition derived from SiH_4 and NH_3. The PECVD process can be used to control the refractive index of the film-coated wafer and the hydrogen content of the film. One difficulty with this process is that it normally requires a vacuum chamber to provide a low-pressure atmosphere during plasma excitation and the use of a vacuum chamber substantially slows the production of solar cell wafers.

The photovoltaic industry uses the PECVD process to deposit silicon nitride film on silicon wafers. Typical equipment utilizes a parallel plate reactor to develop low-pressure plasma between the electrodes. Reactant gases, SiH_4 and NH_3,

often mixed with inert dilute gases, flow in through a showerhead, which is also the top electrode. Plasma excitation is typically initiated using radio frequency power, which ranges from hundreds of kilohertz to thirteen megahertz, between the top electrode and the bottom electrode, on which the wafer sits. The proximity of the wafer to the electrical activity in this process can damage the wafer. This type of PECVD process is called direct PECVD because the wafer sits directly inside the plasma region.

The PECVD process has some variations. One variation of the PECVD process is called remote PECVD, as opposed to direct PECVD. Remote PECVD involves exposing only some of the gases directly to the plasma whereupon the plasma activated gases react to form the thin film of silicon nitride. The gases that are not exposed directly to the plasma will react with the activated gases. The remote PECVD process allows more control over the chemical reactions among gases involved, removes the wafer from any direct plasma exposure, and reduces the chance of wafer damage. However, the remote PECVD process is also typically operated below ambient pressure, requiring a vacuum chamber.

One of the main purposes of low-pressure operations is to stabilize the discharge plasma. Without the low-pressure environment, the discharge plasma cannot be sustained. A method of generating a thin film of silicon nitride at ambient pressure is desirable to avoid the expenses and encumbrances of using a vacuum chamber.

Dielectric barrier discharge is currently being developed as an attractive method for industrial plasma process applications because it can be performed in ambient pressure, removing the necessity of a vacuum chamber. Dielectric barrier discharge has not yet been used in any commercialized thin film process for solar cells or semiconductors. Besides obviating the need for a vacuum chamber, the difference between traditional PECVD processes and the dielectric barrier discharge process is the dielectric barrier discharge process has the ability to use of a wider range of frequencies and power. This ability in turn allows the dielectric barrier discharge process to have a large-scale, industrial adaptability whereas traditional PECVD processes have frequency and power limitations that economically limit commercial exploitation.

As the use of the dielectric barrier process to produce thin films is still being developed, some shortcomings continue to exist in the process. One of the

shortcomings is the continued use of DC power or radio frequency power (RF power) to initiate plasma excitation. Use of DC power or RF power is a technique carried over from traditional low-pressure PECVD techniques. DC power and RF power are less effective in ambient pressure because the plasma can only be sustained in a very narrow set of conditions. This set of conditions is not suitable for industrial solar cell applications. Specifically, use of low power in the discharge process inhibits large-scale production, and thereby commercialization of the process, while use of high DC or RF power in the discharge process will extinguish the plasma and fail to properly produce the desired film. A discharge process is needed that can use sufficient power to satisfy production requirements of industry without extinguishing the plasma or otherwise inhibiting the dielectric barrier discharge process.

SUMMARY OF THE INVENTION

The present invention results from the realization that thin films of silicon nitride can be deposited on silicon wafer surfaces at atmospheric pressure using dielectric barrier discharge initiated with the application of AC power. The present invention improves industrial production levels by eliminating the need for costly and time-consuming vacuum processing.

Therefore, it is an object of one embodiment of the present invention to provide a method of coating substrates at atmospheric pressure.

It is a further object of one embodiment of the present invention to provide assembly-line production of solar cell wafers.

It is a further object of one embodiment of the present invention to provide a silicon nitride thin film on a silicon wafer as an antireflection coating.

It is a further object of one embodiment of the present invention to provide a system of coating substrates that is effective for both direct and remote processes.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features and advantages of the present invention will be better understood by reading the following detailed description, taken together with the drawings wherein:

Fig. 1 is a flow diagram of one embodiment of the method characterizing the present invention.

Fig. 2 is a flow diagram of one embodiment of the method characterizing the present invention.

Fig. 3 is an apparatus for performing a batch-operation, wafer-deposition process in accordance with one embodiment of the present invention.

Fig. 4 is an apparatus for performing a continuous-production, wafer-deposition process in accordance with one embodiment of the present invention.

Fig. 5 is an apparatus for performing a wafer-deposition process in accordance with another embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In one embodiment, the present invention is a method 10 of coating at least one wafer with a film. The first step in the method 10 is assembling 12 at least one electrode set. Each electrode set includes at least one impermeable dielectric barrier and an activation space between a top electrode and a bottom electrode. The second step is flowing 14 at least one purge gas and at least one reactant gas at least partially through the activation space of at least one electrode set, substantially at atmospheric pressure. The next step in the inventive method 10 is placing 16 a wafer beneath the activation space of at least one electrode set. The last step in this embodiment of the inventive method 10 is supplying 18 AC power to at least one electrode set thereby causing a dielectric barrier discharge at least partially within the activation space from which the film descends onto the wafer.

As described, this embodiment of the invention uses an impermeable dielectric barrier. A dielectric barrier is a nonconductor of direct electric current. Some existing art in the field of the present inventive method 10 use a dielectric barrier with a plurality of apertures, essentially spacing conductive channels for creating a glow discharge. The present inventive method uses a dielectric barrier without apertures or channels or any other means for the passage of direct current, which is herein defined as an impermeable dielectric barrier.

The inventive method 10 has several narrower embodiments. One narrower embodiment includes containing 20 at least one of the electrode sets, the gases and the wafer within a process chamber. A narrower embodiment of this design would include an exit pump for pumping the gases out of the chamber after discharge.

Another narrow embodiment of the inventive method 10 involves heating 22 the wafer above ambient temperature. Heating the wafer during the coating process increases the adhesiveness of the coating to the wafer. In a narrower embodiment, the wafer is heated to approximately 400 degrees Celsius during the dielectric barrier discharge process, as this wafer temperature has been determined to be ideal for the coating process.

Another narrow embodiment of the inventive method 10 involves supplying 18 the AC power with a frequency between 1 kilohertz and 500 kilohertz, a frequency well below that utilized by glow discharge.

Another narrow embodiment of the inventive method 10 involves making the bottom electrode a conductive conveyor belt whereupon multiple wafers are carried on the belt, through an assembly line, to receive the silicon nitride coating. A narrower embodiment of this design involves flushing 24 the wafers with an inert gas curtain before and after the wafers are placed between the electrodes, thereby cleaning the wafer. Alternatively, cleaning 26 the wafers is accomplished with a dielectric barrier discharge process in an inert gas environment before the wafers are placed between the electrodes. The conveyor belt embodiment may result in assembling 28 a plurality of electrode sets, wherein the plurality of electrode sets include a plurality of top electrodes, a plurality of impermeable dielectric barriers and a single bottom electrode, said single bottom electrode comprising a metal conveyor belt. In one embodiment, the conveyor belt embodiment includes heating 22 the wafers above ambient temperature. Finally, in one embodiment, the AC supply generates 30 an electric field in the activation space with an intensity between 100 V/cm and 100 kV/cm, which is believed to be at least one magnitude greater than the fields currently achieved through glow discharge.

The present invention may also be described as an apparatus 50 for coating a substrate 52 with a film. The apparatus 50 includes at least one top electrode 54, at least one bottom electrode 56 located below the top electrode 54, wherein an activation space 57 resides substantially between the top electrode 54 and the bottom electrode 56, and at least one impermeable dielectric barrier 58 located between the electrodes 54, 56. The apparatus 50 further includes at least one substrate seat 59 for supporting the substrate 52 in a substantially horizontal position beneath the activation space 57. Also, the apparatus 50 includes at least one purge gas 60 and at least one reactant gas 62 flowing at least partially within

the activation space 57 at approximately atmospheric pressure. Finally, an AC power supply 64 is connected to at least one electrode 54, 56 whereby a dielectric barrier discharge will be caused within the activation space 57.

The inventive apparatus 50 may further include a process chamber 66 at least partially containing the electrodes 54, 56, the wafer seat 59, the dielectric barrier 58 and the gases 60, 62. The chamber 66 is maintained at atmospheric pressure or, more specifically, no specific effort is made to affect the pressure within the chamber 66 (i.e. utilizing a vacuum chamber). The central purpose of the chamber is to keep the gases 60, 62 contained between the electrodes 54, 56 and keep out other gases that would contaminate the dielectric barrier discharge process. The process chamber 66 may further include an intake pumping means 68 for pumping the gases 60, 62 into the chamber 66 and an exit pumping means 70 for pumping the gases 60, 62 out of the chamber 66.

In a narrower embodiment, the inventive apparatus 50 may include a heat source 72 for heating the substrate 52. The heat source 72 may further include a temperature sensor 74 and heat source power 76 controller whereby the temperature of the substrate 52 is definitively controlled.

Another narrower embodiment of the apparatus 50 involves the AC power supply 64 being maintained with a current frequency between about 1 kilohertz and about 500 kilohertz. This current frequency is well below the typical current frequency for glow discharge deposition apparatuses. While AC supply in some fields is understood to mean a frequency between 25 and 60 hertz, the present context only defines an AC power supply as a power supply with an alternating current.

Another narrower embodiment of the inventive apparatus 50 involves making the bottom electrode 56 a conductive conveyor belt 78 whereby multiple wafers 52 are carried on the belt 78, through an assembly line to receive the silicon nitride coating. This embodiment is further narrowed by adding an inert gas curtain 80 at a beginning 82 and an end 84 of the belt 78 thereby cleaning the wafers 52. Alternatively, this embodiment is further narrowed by having the electrodes 54, 56 and impermeable dielectric barriers 58 include a plurality of electrode sets 86, wherein an electrode set 86 include one top electrode 54, at least one impermeable dielectric barrier 58 and a shared bottom electrode 56, said shared bottom electrode 56 comprising a metal conveyor belt 78. This embodiment is further

narrowed by having beginning electrode sets 86 at a beginning 82 of the belt 78 and middle electrode sets 86 at a middle 92 of the belt 78, wherein the beginning electrode sets 86 are substantially encompassed by an inert gas and the middle electrode sets 86 are substantially encompassed by the flowing purge and reactant gases 60, 62.

Finally, in one embodiment, the activation space 57 further includes an electric field. The electric field will have an intensity between 100 V/cm and 100 kV/cm, which is at least one magnitude greater than normally achieved by the glow discharge process.

As described, the inventive method 10 and apparatus 50 can utilize either direct or remote dielectric barrier discharge. Figures 3 and 4 show one embodiment of direct dielectric barrier discharge while Figure 5 shows one embodiment of remote dielectric barrier discharge. The main difference between the two discharge systems is the location of the wafer 52 in relation to the activation space 57. In both systems, the wafer 52 is at least partially below the activation space 57. However, in the direct dielectric barrier discharge system, the wafer 57 is partially within the activation space 57, between the horizontally placed electrodes 54, 56. In the remote dielectric barrier discharge system, the wafer 52 rests below the activation space 57, which is between the vertically-placed electrodes 54,56.

Modifications and substitutions by one of ordinary skill in the art are considered to be within the scope of the present invention, which is not to be limited except by the following claims.

We claim:

1. A method of coating at least one wafer with a film, said method comprising the steps of:

assembling at least one electrode set, wherein each electrode set includes at least one impermeable dielectric barrier between a top electrode and a bottom electrode, wherein between the top electrode and the bottom electrode is an activation space;

flowing at least one purge gas and at least one reactant gas at least partially through the activation space of at least one electrode set, substantially at atmospheric pressure;

placing a wafer at least partially beneath the activation space of at least one electrode set; and

supplying AC power to at least one electrode set thereby causing a dielectric barrier discharge at least partially within the activation space from which the film descends onto the wafer.

2. The method of claim 1 wherein at least one of the electrode sets, the gases and the wafer are contained within a process chamber.

3. The method of claim 2 wherein the process chamber further comprises an exit pump for pumping the gases out of the chamber after discharge.

4. The method of claim 1 further comprising heating the wafer above ambient temperature.

5. The method of claim 4 wherein the wafer is heated to approximately 400 degrees Celsius.

6. The method of claim 1 wherein the AC power is supplied with a current frequency between about 1 kilohertz and 500 kilohertz.

7. The method of claim 1 wherein the bottom electrode is a conductive conveyor belt whereby multiple wafers are carried on the belt, through an assembly line to receive the silicon nitride coating.

8. The method of claim 7 further comprising flushing the wafers with an inert gas curtain before and after the wafers are placed at least partially beneath the activation spaces.

9. The method of claim 7 further comprising cleaning the wafers with a dielectric barrier discharge process in an inert gas environment before the wafers are placed at least partially beneath the activation spaces.

10. The method of claim 7 further comprising assembling a plurality of electrode sets, wherein the plurality of electrode sets include a plurality of top electrodes, a plurality of dielectric barriers and a single bottom electrode, said single bottom electrode comprising a metal conveyor belt.

11. The method of claim 7 further comprising heating the wafers above ambient temperature.

12. The method of claim 1 wherein the step of supplying AC power results in an electric field formed within the activation space and wherein the electric field has an intensity between about 100 V/cm and 100 kV/cm.

13. A apparatus for coating a substrate with a film, said apparatus comprising:

at least one top electrode;

at least one bottom electrode located below the top electrode, wherein an activation space resides substantially between the top electrode and the bottom electrode;

at least one impermeable dielectric barrier located between the electrodes;

at least one substrate seat for supporting the substrate in a substantially horizontal position beneath the activation space;

at least one purge gas and at least one reactant gas flowing at least partially within the activation space at approximately atmospheric pressure; and

an AC power supply connected to at least one electrode whereby a dielectric barrier discharge will be caused within the activation space.

14. The apparatus of claim 13 further comprising a process chamber at least partially containing the electrodes, the wafer seat, dielectric barrier and the gases, wherein the chamber is maintained at atmospheric pressure.

15. The apparatus of claim 14 wherein the process chamber further comprises an intake pumping means for pumping the gases into the chamber and an exit pumping means for pumping the gases out of the chamber.

16. The apparatus of claim 13 further comprising a heat source for heating the substrate within the substrate seat.

17. The apparatus of claim 16 wherein the heat source further comprises a temperature sensor and heat source power controller whereby the temperature of the substrate is definitively controlled.

18. The apparatus of claim 13 wherein the AC power supply is maintained with a current frequency between about 1 kilohertz and about 500 kilohertz.

19. The apparatus of claim 13 wherein the bottom electrode is the substrate seat and is a conductive conveyor belt whereby multiple substrates are carried on the belt, through an assembly line to receive the silicon nitride coating.

20. The apparatus of claim 19 further comprising an inert gas curtain at a beginning and an end of the belt thereby cleaning the substrates.

21. The apparatus of claim 19 wherein the electrodes and dielectric barriers further comprise a plurality of electrode sets, wherein an electrode set include one top electrode, at least one impermeable dielectric barrier and a shared bottom electrode, said shared bottom electrode comprising a metal conveyor belt.

22. The apparatus of claim 21 further comprising beginning electrode sets at a beginning of the belt and middle electrode sets at a middle of the belt, wherein the beginning electrode sets are substantially encompassed by an inert gas and the

middle electrode sets are substantially encompassed by the flowing purge and reactant gases.

23. The apparatus of claim 13 wherein the activation space further comprises an electric field with an intensity between about 100 V/cm and 100 kV/cm.

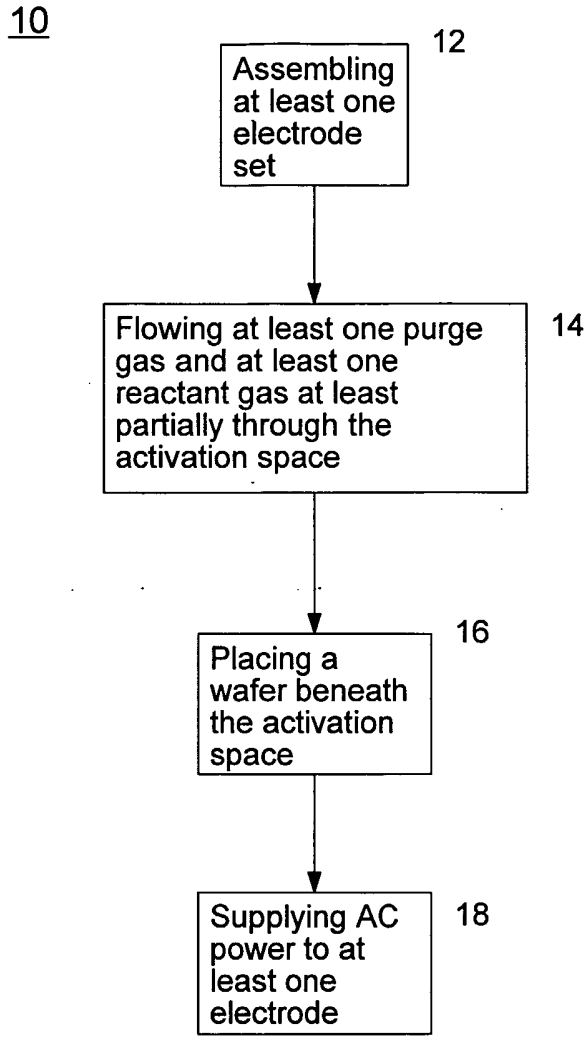
10
12
Assembling at least one electrode set
Flowing at least one purge gas and at least one reactant gas at least partially through the activation space
14
Placing a wafer beneath the activation space
16
Supplying AC power to at least one electrode
18

Figure 1

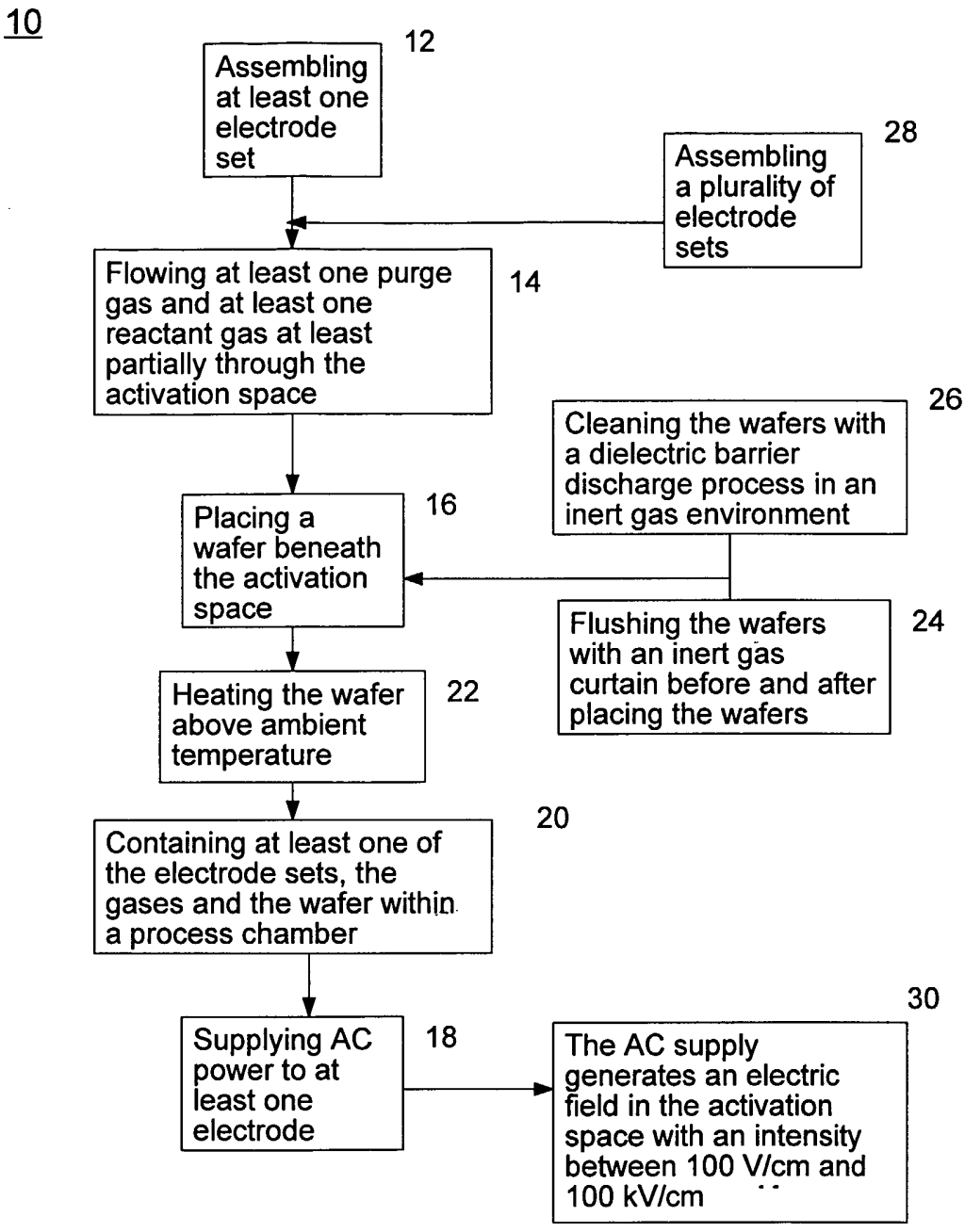
10
12
Assembling at least one electrode set
28
Assembling a plurality of electrode sets
Flowing at least one purge gas and at least one reactant gas at least partially through the activation space
14
26
Cleaning the wafers with a dielectric barrier discharge process in an inert gas environment
16
Placing a wafer beneath the activation space
24
Flushing the wafers with an inert gas curtain before and after placing the wafers
22
Heating the wafer above ambient temperature
20
Containing at least one of the electrode sets, the gases and the wafer within a process chamber
30
18
Supplying AC power to at least one electrode
The AC supply generates an electric field in the activation space with an intensity between 100 V/cm and 100 kV/cm

Figure 2

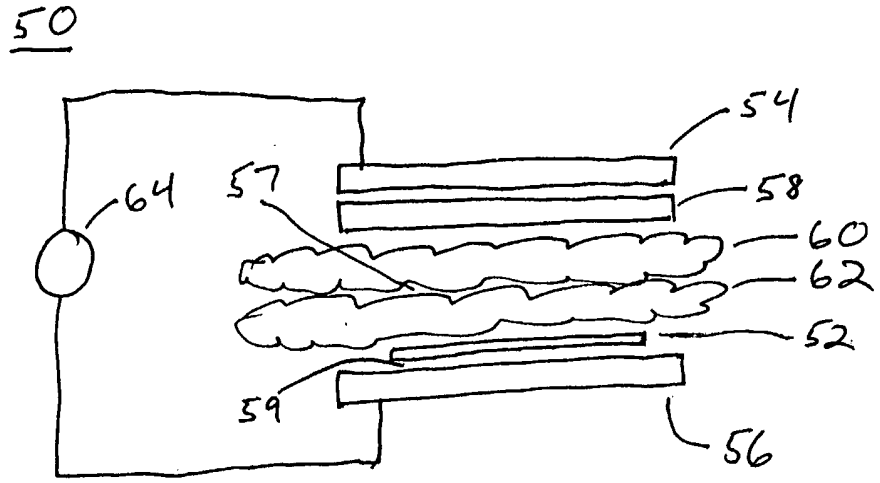

Figure 3

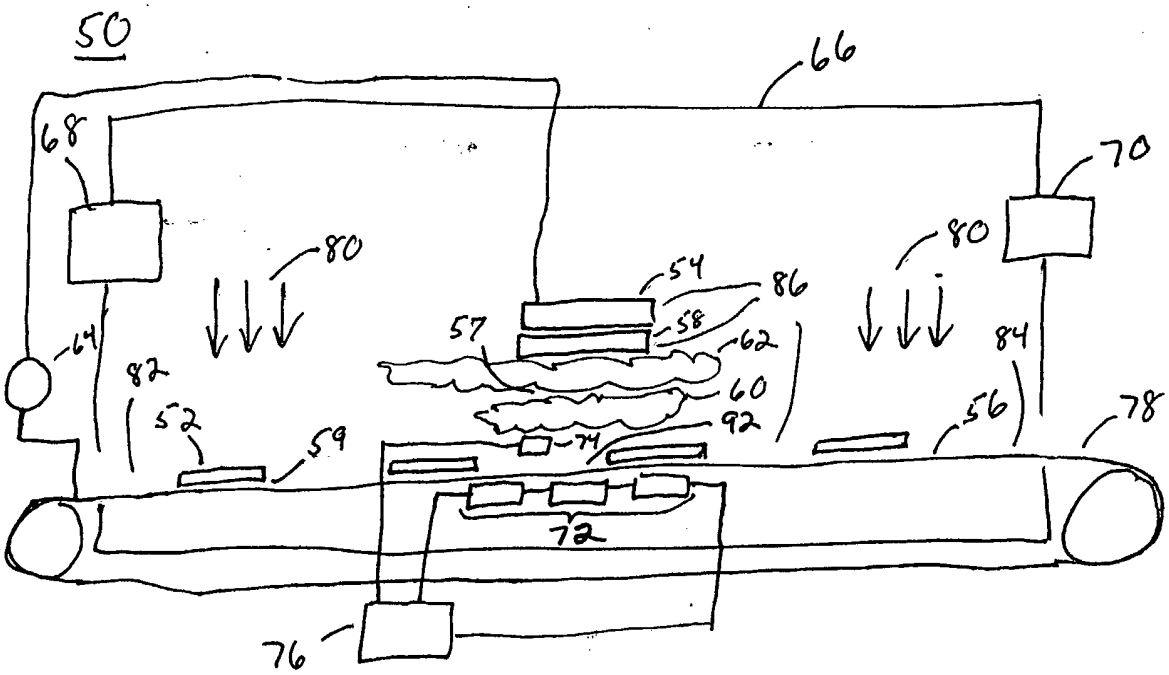

Figure 4

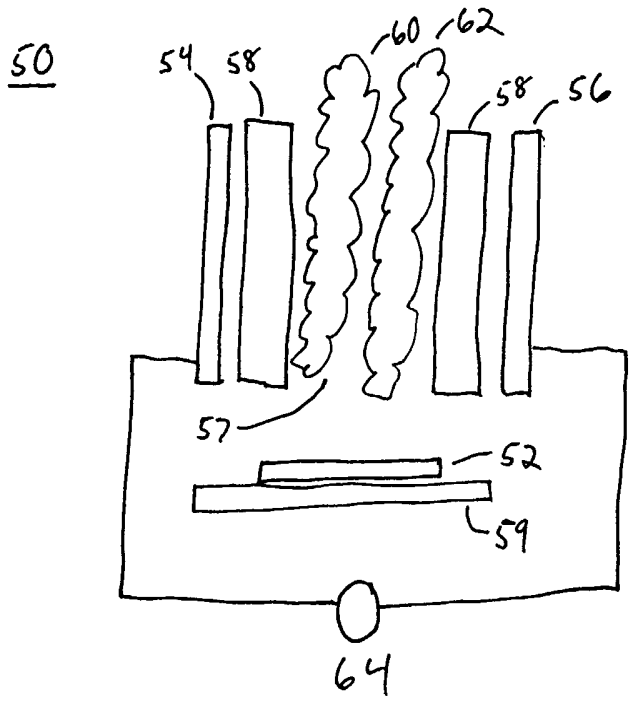

Figure 5