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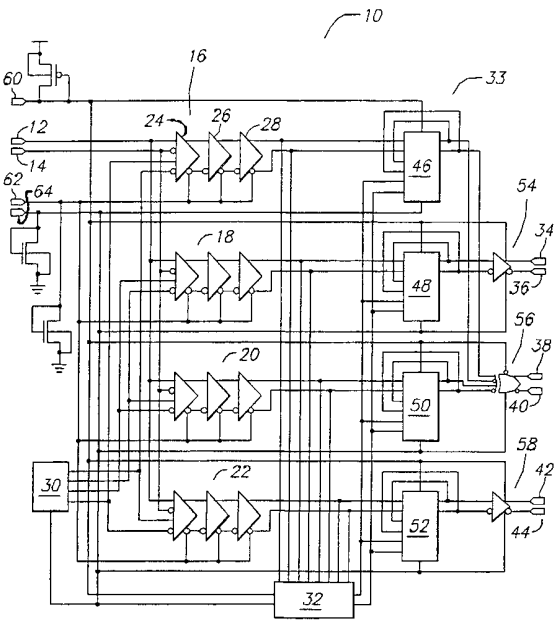
(54) Title: 5-ARY RECEIVER UTILIZING COMMON MODE INSENSITIVE DIFFERENTIAL OFFSET COMPARATOR



(57) Abstract: A signal converter is provided for converting multiple level encoded digital signals into a binary equivalent signal. The signal converter includes a reference voltage generator, a plurality of four-input differential comparators, timing recovery circuitry, and signal conversion circuitry. The reference voltage generator is operative to generate a plurality of progressively larger differential reference voltages. The plurality of differential comparators are each operative to compare magnitude of a differential input voltage with magnitude of a dedicated one of the progressively larger differential reference voltages and produce a differential output voltage having a first logical sense if the magnitude of the differential input voltage is greater than the magnitude of the differential reference voltage, and having a second logical sense if the magnitude of the differential input voltage is less than the magnitude of the differential reference voltage. Each comparator has an offset input voltage. The timing recovery circuitry is configured to receive the differential output voltages from each of the differential comparators and is operative to derive a clock via edge detection and generate a recovered clock signal. The signal conversion circuitry is coupled with the timing recovery circuitry and the differential comparators and is operative to convert the differential output voltages into a binary equivalent. A method is also provided.

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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04L25/49 H03M5/20 H03M1/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04L H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	F. MLINARSKY: "Gigabit Ethernet over Category 5" WWW.SCOPE.COM, 13 October 1997 (1997-10-13), XP002193483 page 1, line 1 -page 11, last line; figures 3,11 --- -/--	1-26

[X] Further documents are listed in the continuation of box C.

[ ] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
19 March 2002	03/04/2002

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
Y	SHIH T ET AL: "A FULLY DIFFERENTIAL COMPARATOR USING A SWITCHED-CAPACITOR DIFFERENCING CIRCUIT WITH COMMON-MODE REJECTION" IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE INC. NEW YORK, US, vol. 32, no. 2, 1 February 1997 (1997-02-01), pages 250-253, XP000722212 ISSN: 0018-9200 page 250, column 1, line 6 -column 2, line 4 page 251, column 2, line 37 -page 252, column 2, last line; figure 2 ---	1-26
A	M. HATAMIAN ET AL.: "Design Considerations for Gigabit Ethernet 1000Base-T Twisted Pair Transceivers" IEEE 1998 CUSTOM INTEGRATED CIRCUITS CONFERENCE, 11 - 14 May 1998, pages 335-342, XP010293978 Santa Clara, CA, USA figures 1,9 -----	1,12,20, 23

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