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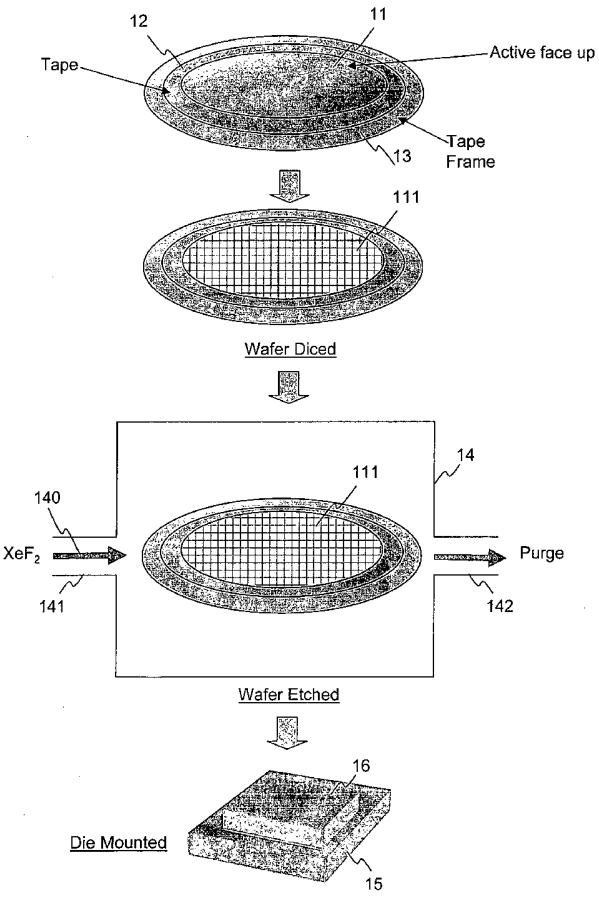
(54) Title: INCREASING DIE STRENGTH BY ETCHING DURING OR AFTER DICING



(57) Abstract: A semiconductor wafer 11 having an active layer is mounted on a carrier 13 with the active layer away from the carrier and at least partially diced on the carrier from a major surface of the semiconductor wafer. The at least partially diced semiconductor wafer is etched on the carrier from the said major surface with a spontaneous etchant 140 to remove sufficient semiconductor material from a die produced from the at least partially diced semiconductor wafer to improve flexural bend strength of the die by removing at least some defects caused by dicing.

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INCREASING DIE STRENGTH BY ETCHING DURING OR AFTER DICING

This invention relates to increasing die strength by etching during or after dicing a semiconductor wafer.

Etching of semiconductors such as silicon with spontaneous etchants is known with a high etch selectivity to a majority of capping, or encapsulation, layers used in the semiconductor industry. By spontaneous etchants will be understood etchants which etch without a need for an external energy source such as electricity, kinetic energy or thermal activation. Such etching is exothermic so that more energy is released during the reaction than is used to break and reform inter-atomic bonds of the reactants. US 6,498,074 discloses a method of dicing a semiconductor wafer part way through with a saw, laser or masked etch from an upper side of the wafer to form grooves at least as deep as an intended thickness of die to be singulated from the wafer. A backside of the wafer, opposed to the upper side, is dry etched, for example with an atmospheric pressure plasma etch of CF_4, past a point at which the grooves are exposed to remove damage and resultant stress from sidewalls and bottom edges and corners of the die, resulting in rounded edges and corners. Preferably a protective layer, such as a polyimide, is used after grooving to hold the die together after singulation and during etching and to protect the circuitry on the top surface of the wafer from etchant passing through the grooves.

However, in order to etch from the backside of the wafer it is necessary to remount the wafer, in, for example, a vortex non-contact chuck, after grooving the upper surface, in order to etch the wafer from an opposite side from that from which the wafer is grooved.

It is an object of the present invention at least to ameliorate the aforesaid shortcoming in the prior art.

According to a first aspect of the present invention there is provided a method of dicing a semiconductor wafer having an active layer comprising the steps of: mounting the semiconductor wafer on a carrier with the active layer away from the carrier; at least partially dicing the semiconductor wafer on the carrier from a major surface of the semiconductor wafer to form an at least partially diced semiconductor wafer; and etching the at least partially diced

semiconductor wafer on the carrier from the said major surface with a spontaneous etchant to remove sufficient semiconductor material from a die produced from the at least partially diced semiconductor wafer to improve flexural bend strength of the die.

Conveniently, the step of at least partially dicing the semiconductor wafer comprises dicing the semiconductor wafer completely through the semiconductor wafer; and the step of etching the semiconductor wafer comprises etching sidewalls of the die, remaining portions of the die being masked from the spontaneous etchant by portions of the active layer on the die.

Alternatively, the step of at least partially dicing the semiconductor wafer comprises partially dicing the semiconductor wafer along dicing lanes to leave portions of semiconductor material bridging the dicing lanes; and the step of etching the semiconductor wafer comprises etching sidewalls of the dicing lanes and etching away the portions of semiconductor material bridging the dicing lanes to singulate the die.

Advantageously, the semiconductor wafer is a silicon wafer.

Conveniently, the step of etching with a spontaneous etchant comprises etching with xenon difluoride.

Preferably, the step of etching with a spontaneous etchant comprises providing an etching chamber and etching the semiconductor wafer within the etching chamber.

Advantageously, the step of etching with a spontaneous etchant within the etching chamber comprises cyclically supplying the chamber with spontaneous etchant and purging the etching chamber of spontaneous etchant for a plurality of cycles.

According to a second aspect of the invention, there is provided a dicing apparatus for dicing a semiconductor wafer having an active layer comprising: carrier means on which the semiconductor wafer is mountable with the active layer away from the carrier; laser or mechanical sawing means arranged for at least partially dicing the semiconductor wafer on the carrier from a major surface of the semiconductor wafer to form an at least partially diced semiconductor wafer; and etching means arranged for etching the at least partially diced semiconductor wafer on the carrier from the said major surface with a spontaneous etchant to remove sufficient semiconductor material from a die

produced from the at least partially diced semiconductor wafer to improve flexural bend strength of the die.

Conveniently, the dicing apparatus is arranged for dicing a silicon wafer.

Advantageously, the etching means is arranged to etch with xenon difluoride.

Preferably, the dicing apparatus further comprises an etching chamber arranged for etching the semiconductor wafer mounted on the carrier means within the etching chamber.

Preferably, the etching chamber is arranged for cyclically supplying the chamber with spontaneous etchant and purging the etching chamber of spontaneous etchant for a plurality of cycles.

The invention will now be described, by way of example, with reference to the accompanying drawings in which:

Figure 1 is a schematic flow diagram of a first embodiment of the invention comprising active side up dicing followed by spontaneous etching;

Figure 2 is a schematic flow diagram of a second embodiment of the invention comprising active face up partial dicing followed by die release by spontaneous etching;

Figure 3 is a graph of survival probability as ordinates versus die strength as abscissa of a laser-cut control wafer and wafers etched to various extents according to the invention as measured by a 3-point test;

Figure 4 is a graph of survival probability as ordinates versus die strength as abscissa of a saw-cut control wafer and wafers etched to various extents according to the invention as measured by a 3-point test;

Figure 5 is a graph of survival probability as ordinates versus die strength as abscissa of a laser-cut control wafer and wafers etched to various extents according to the invention as measured by a 4-point test;

Figure 6 is a graph of survival probability as ordinates versus die strength as abscissa of a saw-cut control wafer and wafers etched to various extents according to the invention as measured by a 4-point test;

Figure 7 shows micrographs of sidewalls of a laser-cut control wafer and of laser-cut wafers etched to various extents according to the invention; and

Figure 8 is of micrographs of sidewalls of a saw-cut control wafer and of saw-cut wafers etched to various extents according to the invention.

In the Figures like reference numerals denote like parts.

Referring to Figures 1 and 2, a silicon wafer 11 on a standard dicing tape 12 and tape frame 13 is mounted on a carrier, not shown. The wafer is diced using a laser or a mechanical saw on the carrier to produce a diced wafer 111. The laser may be a diode-pumped solid-state laser, a mode-locked laser or any other laser suitable for machining the semiconductor and other materials of the wafer. Suitable laser wavelengths may be selected from infrared to ultraviolet wavelengths.

The diced wafer 111 is placed on the carrier in a chamber 14, the chamber having an inlet port 141 and an outlet port 142. Cycles of xenon difluoride (XeF_2), or any other spontaneous etchant of silicon, are input through the inlet port 141 and purged through the outlet port 142 for a predetermined number of cycles each of a predetermined duration. Alternatively, the etching may be carried out as a continuous process, but this has been found to be less efficient in terms of etch rate and etchant usage. The dies are then released from the tape 12 and mounted onto a die pad 15 or another die to form a mounted die 16.

Referring to Figure 1, in a first embodiment of the invention, a wafer 11, with an active layer uppermost, is diced followed by spontaneous etching. The wafer 11 is mounted active face up on a wafer carrier on a tape 12 and a tape frame 13, that is, with the active layer away from the carrier. The wafer is diced with a mechanical dicing saw or a laser dicing saw on the carrier to form an active side up, diced wafer 111. The diced wafer 111 is placed face up in an etching chamber 14 and a spontaneous etchant 140 of silicon is input into the chamber 14 through the inlet port 141 to come in contact with the diced wafer 111 for a pre-defined period. The etchant can be, but is not limited to, XeF_2 and can be either a gas or liquid. The diced wafer 111 is held in place in the chamber 14 by the wafer carrier, not shown, which can be made of any flexible or inflexible material that holds the wafer in place either through the use of an adhesive layer or by mechanical means such as physical, electrical or vacuum clamping. The wafer carrier can be opaque or optically transparent. After etching, singulated etched dies 16 are removed from the carrier and mounted onto a die pad 15 or another die. In this embodiment, the active layer acts as a mask to the spontaneous etchant and only the sidewalls of the dies are etched to remove a layer of silicon. The etching of the sidewall changes the physical nature of the sidewall thereby

increasing the average die strength, as measured to destruction with a three-point or four-point test.

Referring to Figure 2, in a second embodiment of the invention, a wafer 11, with an active layer uppermost is mounted active side up on a tape 12 and tape frame 13 on a wafer carrier 17. The wafer carrier 17 can be made of any optically transparent flexible or inflexible material that is suitable for holding the wafer in place either through the use of an adhesive layer or by mechanical means such as mechanical, electrical or vacuum clamping. The wafer 11 is partially diced through along dice lanes 18 with a mechanical dicing saw or a laser dicing saw to form a partially diced wafer 112. The partially diced wafer 112 is placed face up, on the carrier 17, in an etching chamber 14 to come into contact with a spontaneous etchant 140 of silicon until the etchant 140 has etched away a remaining portion of silicon in the dice lanes. The etchant can be, but is not limited to, XeF_2 and can be either a gas or liquid. As well as by a change in physical nature of the sidewall, die strength is also enhanced because the dies are diced substantially simultaneously, avoiding any stress build up which may occur in conventionally diced wafers.

The process of the invention provides the advantages over other etch processes, such as chemical or plasma etching, of being a fully integrated, dry, controllable, gas process, so that no specialist wet chemical handling is required, and clean, safe and user-friendly materials are used in a closed handling system that lends itself well to automation. Moreover, since spontaneous etching may be carried out in parallel with dicing, cycle time is of the order of dicing process time, so that throughput is not restricted. Furthermore, the invention uses a tape-compatible etch process which is also compatible with future wafer mounts, such as glass. In addition, no plasma is used, as in the prior art, which might otherwise induce electrical damage on sensitive electrical devices. Finally, the invention provides an inexpensive process which, used with laser dicing, provides a lower cost dicing process than conventional dicing processes.

EXAMPLE

Ten 125mm diameter 180μm thick silicon wafers were coated with standard photoresist. The wafers were split into two groups as shown in Table 1 with five

wafers undergoing laser dicing and five wafers undergoing dicing by mechanical saw.

Table 1. Wafer description

Wafer number	Dicing Process	Etch depth (μm)		Wafer number	Dicing process	Etch depth (μm)
1	Laser	Not etched		6	Saw	Not etched
2		2		7		2
3		3		8		3
4		4		9		4
5		25		10		25

After dicing the wafers were placed in a chamber and etched with XeF_2 for a predetermined period of time. After this period the chamber was evacuated and purged. This etch, evacuate and purge cycle was repeated for a set number of times to remove a predetermined thickness of silicon. The numbers of cycles used are given in Table 2.

Table 2. Etching parameters

Etch depth (μm)	Number of cycles	Time per cycle (sec)
Not etched	--	--
2 μm	8	10
3 μm	12	10
4 μm	16	10
25 μm	100	10

After the wafers had been etched, the die strength of each wafer was measured using 3-point and 4-point flexural bend strength testing.

The results for 3-point die strength testing are listed in Table 3 for laser-cut wafers and Table 4 for saw-cut wafers. Corresponding graphs comparing the survival probability for the control wafer with the four different etch depths used are shown in Figure 3 for laser-cut wafers, in which line 31 relates to an un-etched wafer, line 32 an etch depth of 2 μm, line 33 an etch depth of 3 μm, line 34 an

etch depth of 4 μm and line 35 an etch depth of 25 μm and in Figure 4 for saw-cut wafers in which line 41 relates to an un-etched wafer, line 42 an etch depth of 2 μm, line 43 an etch depth of 3 μm, line 44 an etch depth of 4 μm and line 45 an etch depth of 25 μm. It can be seen that for both laser-cut and saw-cut wafers the flexural strength as measured by a 3-point test generally increases with etch depth.

Table3. Laser cut wafers. 3-Point Die Strength Test

Normalised Die Strength (MPa) for Xise laser diced wafers					
	Control wafer	2 μm etched	3 μm etched	4 μm etched	25 μm etched
Average (MPa)	223	506	697	658	1381
Std Dev (MPa)	83	178	162	131	417
Max (MPa)	404	799	1077	920	2279
Min (MPa)	100	221	446	403	663
Range (MPa)	304	578	632	518	1616
Coeff. of variance	0.37	0.35	0.23	0.20	0.30

Table 4. Saw cut wafers. 3-Point Die Strength Test

Normalised Die Strength (MPa) for mechanical saw cut wafers					
	Control wafer	2 μm etched	3 μm etched	4 μm etched	25 μm etched
Average (MPa)	861	1308	1585	1427	2148
Std Dev (MPa)	181	593	623	457	601
Max (MPa)	1245	2250	2894	2119	3035
Min (MPa)	512	321	622	617	790
Range (MPa)	733	1929	2272	1502	2246
Coeff. of variance	0.21	0.45	0.39	0.32	0.28

The results for 4-point die strength testing are listed in Tables 5 and 6. Corresponding graphs comparing the survival probability for the control wafer and the four different etch tests are shown in Figures 5 for laser-cut wafers, in which line 51 relates to an un-etched wafer, line 52 an etch depth of 2 μm, line 53

an etch depth of 3 μm, line 54 an etch depth of 4 μm and line 55 an etch depth of 25 μm and in Figure 6 for saw-cut wafers in which line 61 relates to an un-etched wafer, line 62 an etch depth of 2 μm, line 63 an etch depth of 3 μm, and line 64 an etch depth of 4 μm. It can be seen that for both laser-cut and saw-cut wafers the flexural strength as measured by a 4-point test generally increases with etch depth.

Table 5. Laser cut wafers. 4-Point Die Strength Test

Normalised Die Strength (MPa) for Xise laser diced wafers					
	Control wafer	2 μm etched	3 μm etched	4 μm etched	25 μm etched
Average (MPa)	194	394	551	574	770
Std Dev (MPa)	23	81	109	101	155
Max (MPa)	234	588	743	762	1043
Min (MPa)	139	296	370	342	543
Range (MPa)	95	291	373	419	500
Coeff of variance	0.12	0.20	0.20	0.18	0.20

Table 6. Saw cut wafers. 4-Point Die Strength Test

Normalised Die Strength (MPa) for mechanical saw diced wafers					
	Control wafer	2 μm etched	3 μm etched	4 μm etched	25 μm etched
Average (MPa)	680	716	843	868	--
Std Dev (MPa)	137	425	399	357	--
Max (MPa)	863	1851	1608	1583	--
Min (MPa)	316	213	365	344	--
Range (MPa)	547	1638	1244	1240	--
Coeff of variance	0.20	0.59	0.47	0.41	--

SEM images of the laser-cut and saw-cut wafers are shown in Figures 7 and 8 respectively. Figure 7(a) shows a laser-cut un-etched die corner at x200 magnification, Figure 7(b) shows a laser-cut un-etched sidewall at x800

magnification, Figure 7(c) shows a laser-cut die corner etched 4 μm at x250 magnification, Figure 7(d) shows a laser-cut sidewall etched 4 μm at x600 magnification, Figure 7(e) shows a laser-cut die corner etched 25 μm at x250 magnification, Figure 7(f) shows a laser-cut sidewall etched 25 μm at x700 magnification. Figure 8(a) shows a saw-cut un-etched die corner at x400 magnification, Figure 8(b) shows a saw-cut un-etched sidewall at x300 magnification, Figure 8(c) shows a saw-cut die corner etched 4 μm at x300 magnification, Figure 8(d) shows a saw-cut sidewall with no resist etched 4 μm at x300 magnification, Figure 8(e) shows a saw-cut die corner etched 25 μm at x500 magnification, Figure 8(f) shows a saw-cut sidewall etched 25 μm at x300 magnification.

For both the 3-point and 4-point tests, it can be seen that for both saw-cut and laser-cut die, on average the etched dies had higher flexural strength than the un-etched dies and the flexural strength increases with depth of etch in the etch range 2 μm to 25 μm.

Although the invention has been described in relation to silicon and xenon difluoride, it will be understood that any suitable liquid or gaseous spontaneous etchant such as a halide or hydrogen compound, for example F_2, Cl_2, HCl or HBr may be used with silicon or another semiconductor.

CLAIMS

1. A method of dicing a semiconductor wafer (11) having an active layer comprising the steps of:
   a. mounting the semiconductor wafer on a carrier (13) with the active layer away from the carrier;
   b. at least partially dicing the semiconductor wafer on the carrier from a major surface of the semiconductor wafer to form an at least partially diced semiconductor wafer (111); and
   c. etching the at least partially diced semiconductor wafer on the carrier from the said major surface with a spontaneous etchant (140) to remove sufficient semiconductor material from a die (16) produced from the at least partially diced semiconductor wafer to improve flexural bend strength of the die.

2. A method as claimed in claim 1, wherein the step of at least partially dicing the semiconductor wafer comprises dicing the semiconductor wafer completely through the semiconductor wafer; and the step of etching the semiconductor wafer comprises etching sidewalls of the die, remaining portions of the die being masked from the spontaneous etchant by portions of the active layer on the die.

3. A method as claimed in claim 1, wherein the step of at least partially dicing the semiconductor wafer comprises partially dicing the semiconductor wafer along dicing lanes (18) to leave portions of semiconductor material bridging the dicing lanes; and the step of etching the semiconductor wafer comprises etching sidewalls of the dicing lanes and etching away the portions of semiconductor material bridging the dicing lanes to singulate the die.

4. A method as claimed in any of the preceding claims, wherein the semiconductor wafer is a silicon wafer.

5. A method as claimed in any of the preceding claims, wherein the step of etching with a spontaneous etchant comprises etching with xenon difluoride.

6. A method as claimed in any of the preceding claims, wherein the step of etching with a spontaneous etchant comprises providing an etching chamber (14) and etching the semiconductor wafer within the etching chamber.

7. A method as claimed in claim 6, wherein the step of etching with a spontaneous etchant within the etching chamber comprises cyclically supplying the chamber with spontaneous etchant and purging the etching chamber of spontaneous etchant for a plurality of cycles.

8. A dicing apparatus for dicing a semiconductor wafer (11) having an active layer comprising:
   a. carrier means (13) on which the semiconductor wafer is mountable with the active layer away from the carrier;
   b. laser or mechanical sawing means arranged for at least partially dicing the semiconductor wafer on the carrier from a major surface of the semiconductor wafer to form an at least partially diced semiconductor wafer; and
   c. etching means arranged to etch the at least partially diced semiconductor wafer on the carrier from the said major surface with a spontaneous etchant (140) to remove sufficient semiconductor material from a die (16) produced from the at least partially diced semiconductor wafer to improve flexural bend strength of the die.

9. A dicing apparatus as claimed in claim 8, wherein the dicing apparatus is arranged to dice a silicon wafer.

10. A dicing apparatus as claimed in claims 8 or 9, wherein the etching means is arranged to etch with xenon difluoride.

11. A dicing apparatus as claimed in any of claims 8 to 10, wherein the dicing apparatus further comprises an etching chamber (14) arranged for etching the semiconductor wafer mounted on the carrier means within the etching chamber.

12. A dicing apparatus as claimed in any of claims 8 to 10, wherein the etching chamber is arranged cyclically to supply the chamber with spontaneous etchant and to purge the etching chamber of spontaneous etchant for a plurality of cycles.

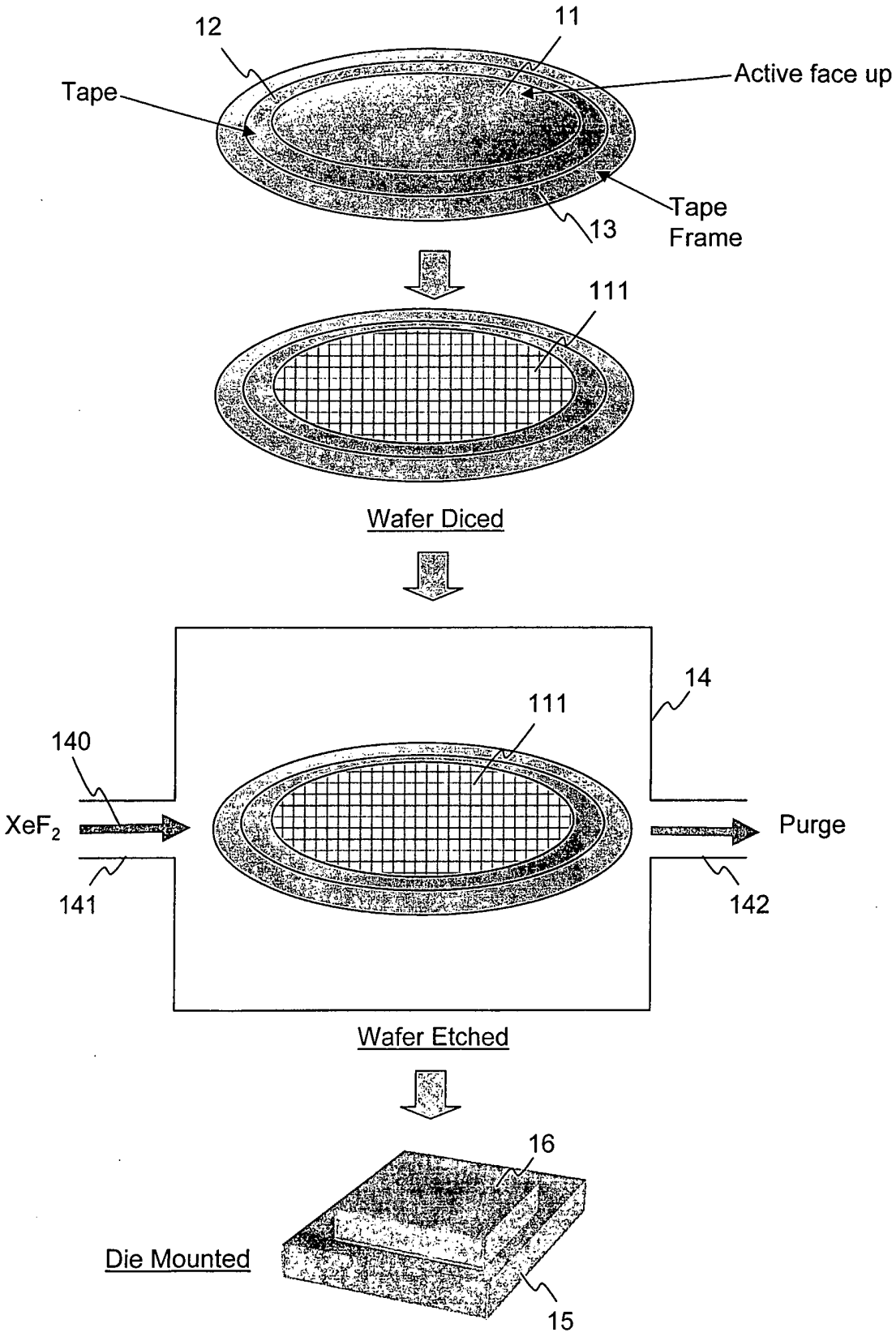
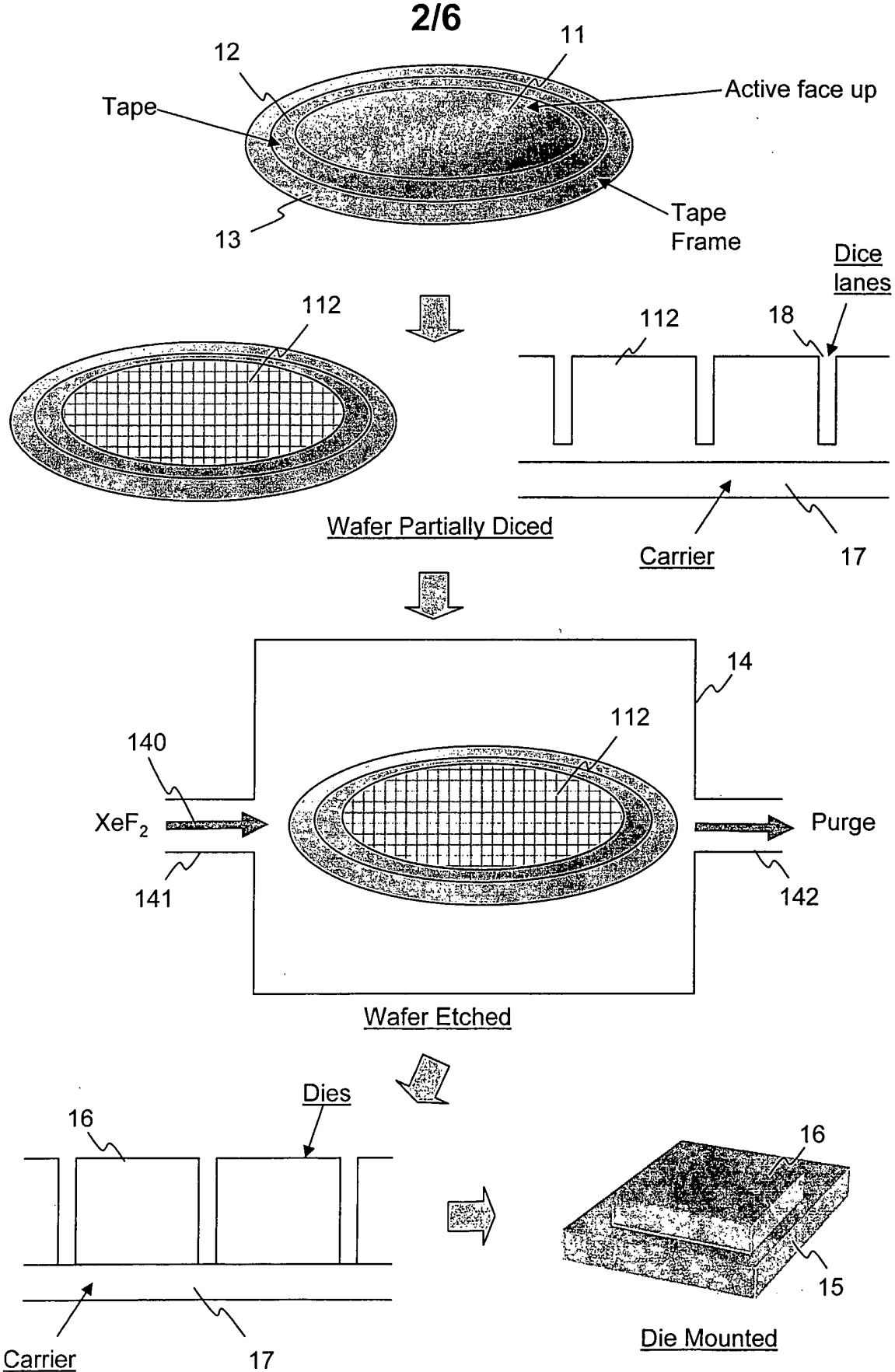

12
11
Tape
Active face up
Tape Frame
13
111
Wafer Diced
14
111
140
XeF_2
Purge
141
142
Wafer Etched
16
Die Mounted
15

Figure 1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11
Tape
Active face up
13
Tape
Frame
Dice
lanes
112
112
18
Wafer Partially Diced
Carrier
17
14
112
140
XeF_2
Purge
141
142
Wafer Etched
Dies
16
16
Carrier
17
15
Die Mounted

Figure 2

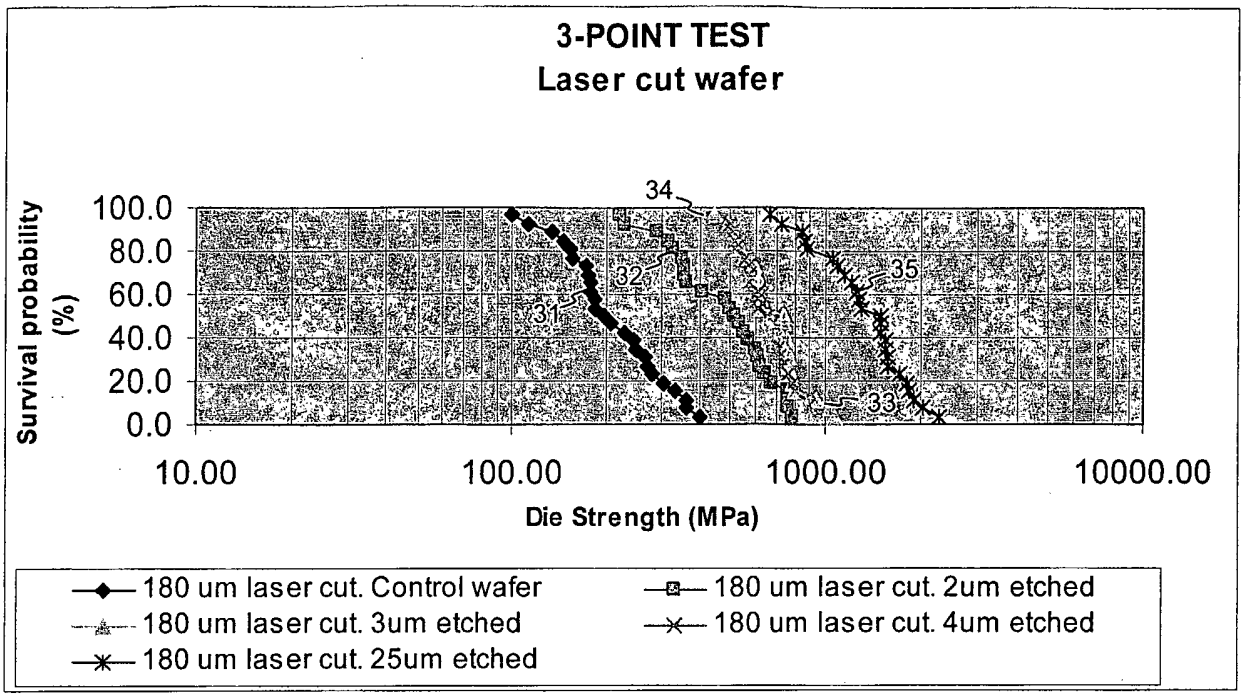

Figure 3

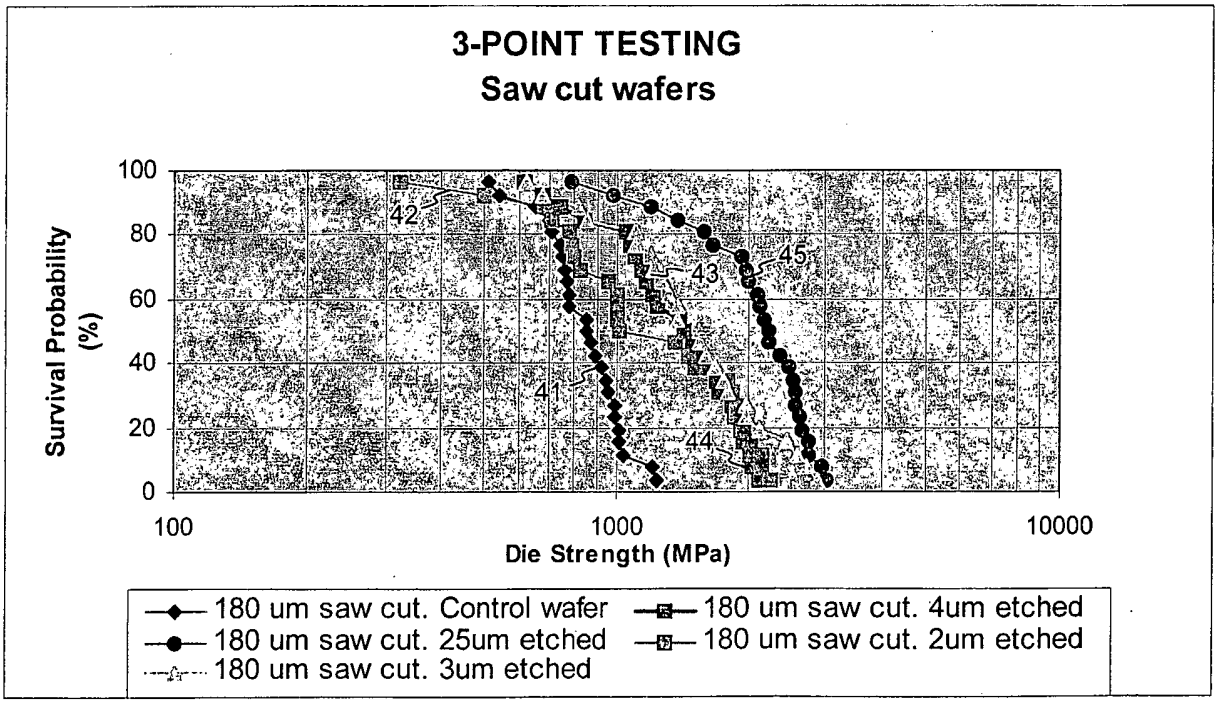

Figure 4

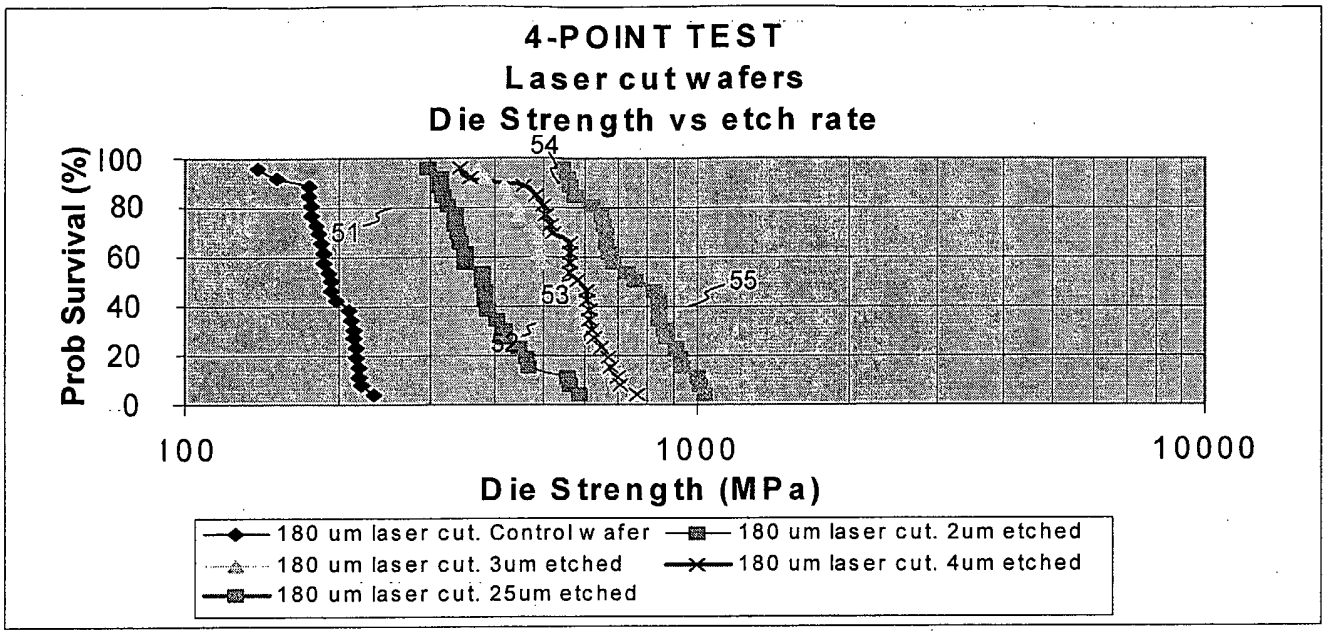

Figure 5

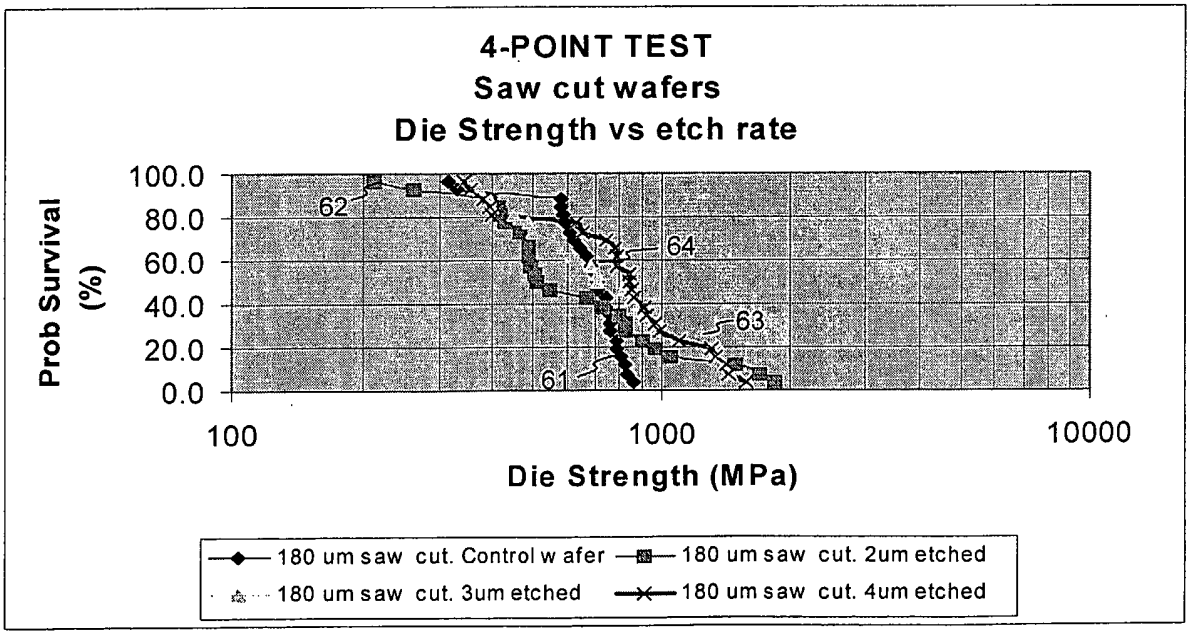

Figure 6

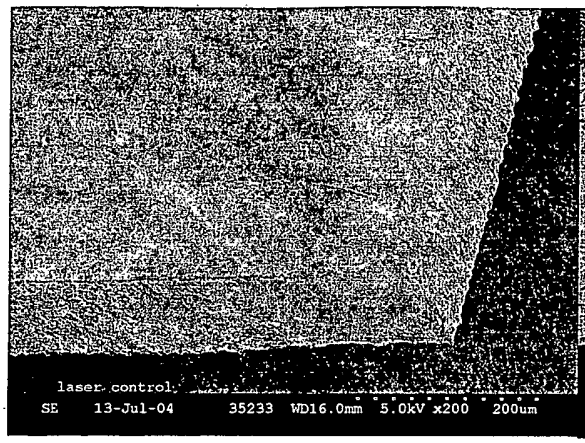

Figure 7(a)

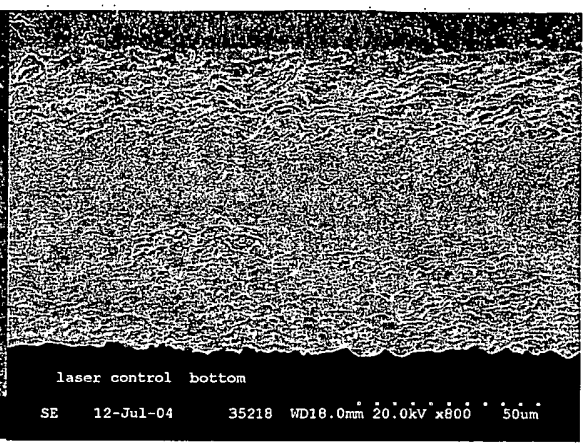

Figure 7(b)

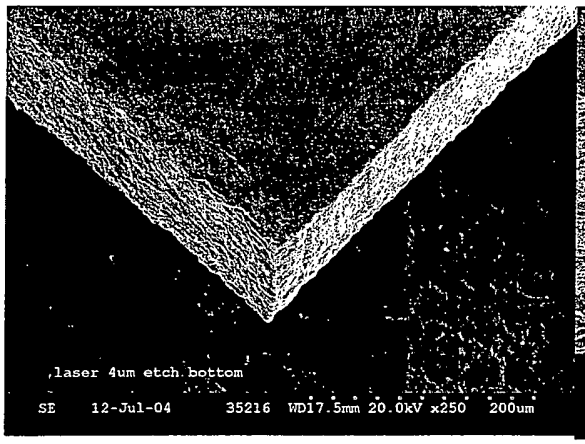

Figure 7(c)

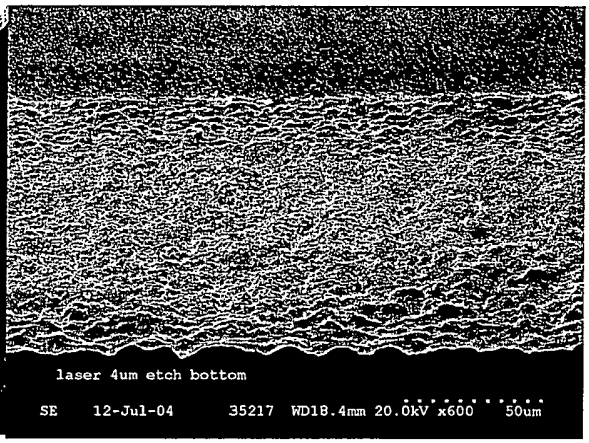

Figure 7(d)

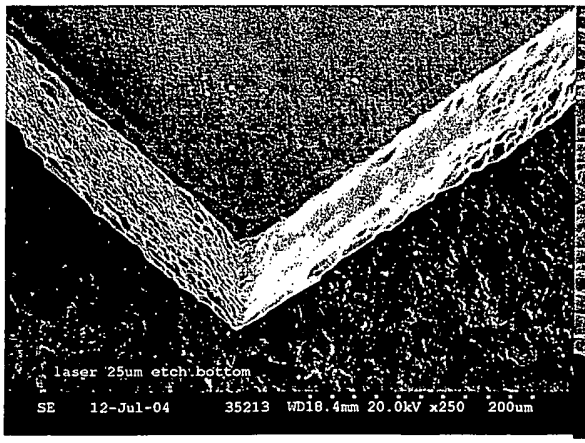

Figure 7(e)

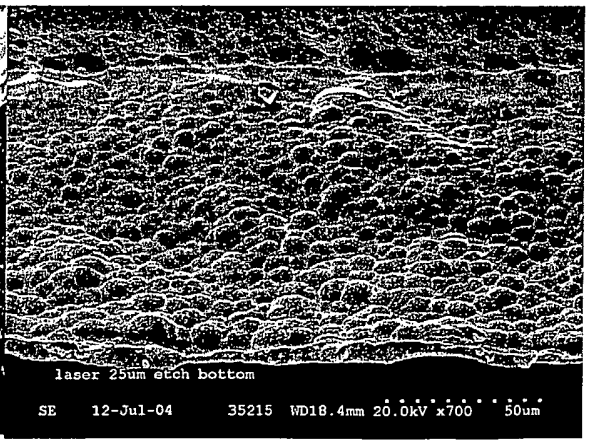

Figure 7(f)

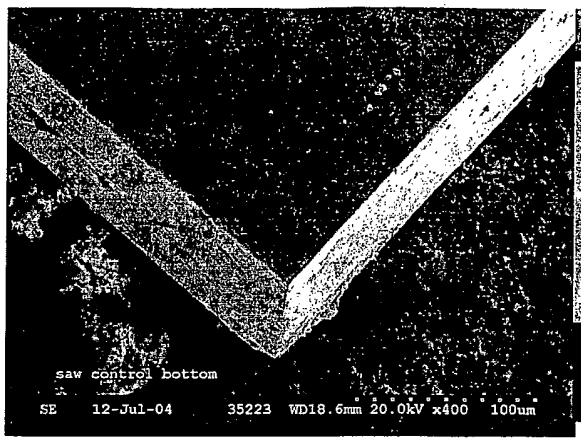

Figure 8(a)

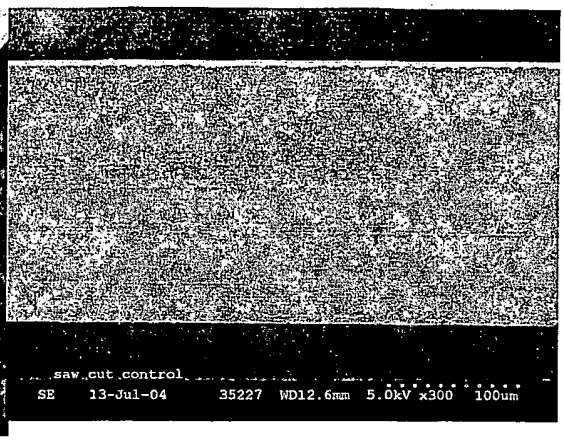

Figure 8(b)

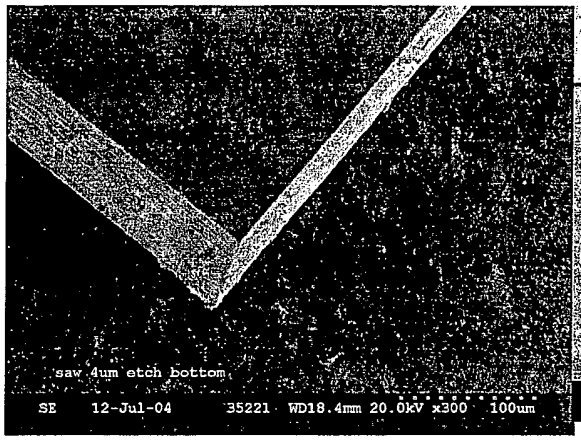

Figure 8(c)

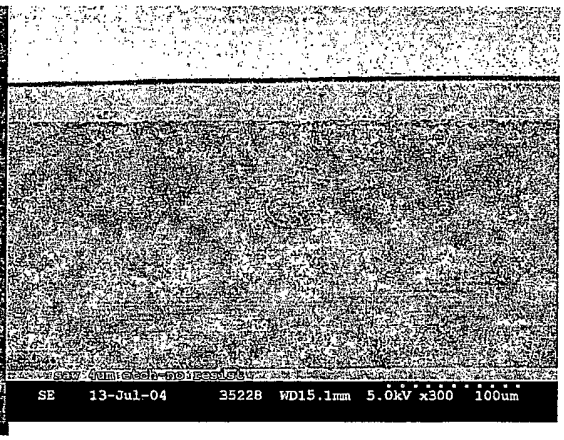

Figure 8(d)

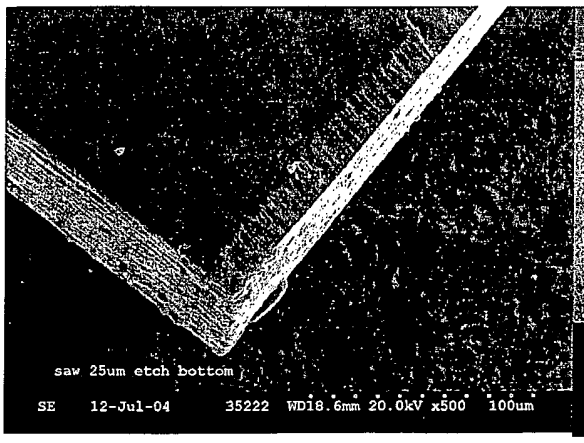

Figure 8(e)

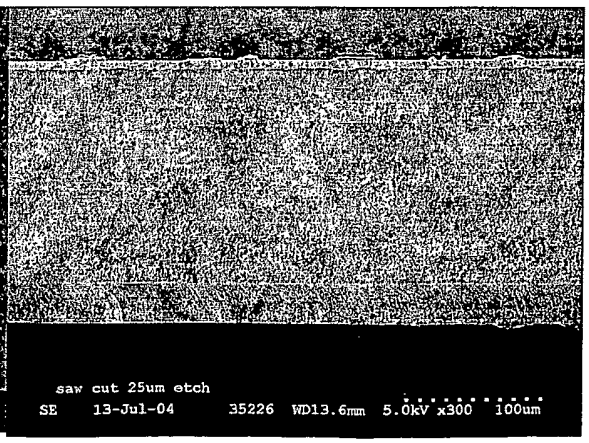

Figure 8(f)

INTERNATIONAL SEARCH REPORT

International Application No
EP2005/011671

A. CLASSIFICATION OF SUBJECT MATTER
H01L21/78 H01L21/3065

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, CHEM ABS Data, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	PATENT ABSTRACTS OF JAPAN vol. 1995, no. 11, 26 December 1995 (1995-12-26) -& JP 07 201784 A (FUJITSU LTD), 4 August 1995 (1995-08-04) abstract; figure 2	1,2,4 5
X	PATENT ABSTRACTS OF JAPAN vol. 015, no. 438 (E-1130), 8 November 1991 (1991-11-08) -& JP 03 183153 A (FUJITSU LTD), 9 August 1991 (1991-08-09) abstract; figure 1	1,3
X	US 2004/072388 A1 (SEKIYA KAZUMA) 15 April 2004 (2004-04-15) paragraph '0032! - paragraph '0044!; figures 4,9	8-12

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 January 2006	31/01/2006

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Bakker, J

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP2005/011671

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	BAHREYNI BEHRAAD ET AL: "Investigation and simulation of XeF2 isotropic etching of silicon" JOURNAL OF VACUUM SCIENCE AND TECHNOLOGY A. VACUUM, SURFACES AND FILMS, AMERICAN INSTITUTE OF PHYSICS, NEW YORK, NY, US, vol. 20, no. 6, November 2002 (2002-11), pages 1850-1854, XP012006208 ISSN: 0734-2101 page 1850	5
A	WO 03/078091 A (BECTON, DICKINSON AND COMPANY) 25 September 2003 (2003-09-25) paragraph '0065! - paragraph '0071!; figures 16,17	1-5

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/EP2005/011671

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 07201784 A	04-08-1995	NONE	
JP 03183153 A	09-08-1991	NONE	
US 2004072388 A1	15-04-2004	AU 2002354108 A1	24-07-2003
		CN 1496580 A	12-05-2004
		DE 10296522 T5	15-04-2004
		WO 03058697 A1	17-07-2003
		JP 2003197569 A	11-07-2003
WO 03078091 A	25-09-2003	AU 2003231967 A1	29-09-2003
		BR 0308319 A	28-12-2004
		CA 2478329 A1	25-09-2003
		CN 1646245 A	27-07-2005
		EP 1490191 A1	29-12-2004
		JP 2005519703 T	07-07-2005