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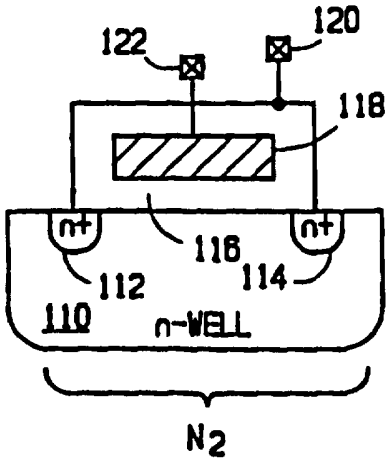

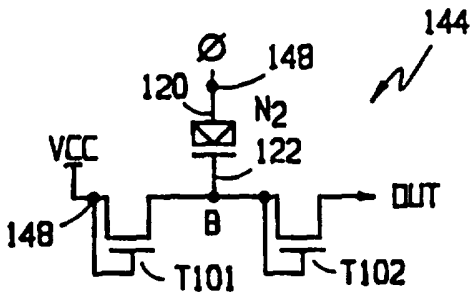

(57) Abstract

A charge pump circuit utilizing accumulation capacitors for use in EEPROM devices so as to internally pump up an external power source voltage includes a plurality of MOS transistors (T101, T102; T201, T202) and accumulation capacitors (N2, P2). The plurality of MOS transistors are connected in series between a first input voltage terminal and a higher voltage output terminal. The first input voltage terminal receives the external power source voltage. The accumulation capacitor has a first plate and a second plate. Each of the first plates of the accumulation capacitors is connected between adjacent ones of the plurality of MOS transistors. Each of the second plates of the accumulation capacitors is connected to a second input terminal for receiving a clock signal. As a result, the pump circuit can be operated effectively so as to produce a significant reduction in power consumption.

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DESCRIPTION

IMPROVED CHARGE PUMPS USING ACCUMULATION CAPACITORS

BACKGROUND OF THE INVENTION

1. Field of the Invention:

This invention relates generally to semiconductor integrated circuit memory devices, such as flash electrically erasable programmable read-only memory (EEPROM) devices and more particularly, it relates to an improved charge pump utilizing an accumulation capacitor for use in EEPROM devices so as to internally pump up a power source voltage as supplied from an external or off-chip power supply on a more effective and efficient basis.

2. Description of the Prior Art:

As is generally known, in the area of memory devices and other semiconductor integrated circuits there is often required a voltage to be internally generated that is greater than an external or off-chip power supply potential which is supplied to it. For instance, in flash electrically erasable, programmable read-only memories (EEPROM's) high voltages such as ±12 V is needed to be produced for the programming and erasing modes of operation of memory cells. As a result, the semiconductor memory devices generally also include an internal booster circuit of some type for internally boosting up the external power supply voltage. One type of internal booster circuit commonly used in flash EEPROM's is referred to as a "charge pump."

While the user of such memory devices are not required to provide a high voltage source for its operation, these memory devices do suffer from the disadvantage that the charge pumps often account for a significant percentage of the total power dissipation of such memory devices. Further, as the demand for higher and higher densities of the semiconductor memory devices

increases, there exists a general miniaturization of all of the circuit elements forming the memory devices. Thus, there has been necessitated the use of lower power supply voltages not only as a way of reducing power dissipation, but also in order to prevent danger to the miniaturized circuit elements. There exists likewise a trend of decreasing the voltage for a battery power source for portable electronic applications to about 3 V or below. However, as the battery power source is reduced the conventional charge pumps utilizing inversion capacitors fail to provide an adequate degree of operation.

In Figure 1a, there is shown the electrical symbol for a capacitor-connected N-channel MOS transistor **N1**. Figures 1b and 1c show the cross-section and top plan views of the N-channel MOS transistor **N1**, respectively. As can be seen, the reference numeral **10** designates a p-type substrate. An n-type drain region **12** and an n-type source region **14** are diffused in the surface of the substrate **10**. A thin gate oxide layer **16** is interposed between the top surface of the substrate and a conductive polysilicon gate **18**. The drain and source regions **12** and **14** are connected together and to a metal contact connection **20** defining one plate of the capacitor **N1**. The gate **18** is also joined to a metal contact connection **22** defining the other plate of the capacitor **N1**.

In Figure 2, there is illustrated a plot of the amount of capacitance value for the three operating regions (accumulation, depletion, and inversion) of the capacitor-connected MOS transistor **N1** of Figure 1b as a function of the voltage V_g applied to the polysilicon gate. As will be noted, when the capacitor is being operated in the inversion region there is the disadvantage of having the capacitance value drop off at the higher frequencies. The current output supplied from a charge pump becomes very small when the power source

voltage is made small. The output current of a charge pump is given by the following expression:

$$I \propto C \times V \times F$$

where:

C = value of pump capacitance

V = magnitude of switching power supply

F = frequency at which the voltage V is being switched

Thus, the output current of the charge pump can be made high by operating at higher frequencies. It is possible to increase the operating frequency of the capacitor operating in the inversion region by the adding of diffusion contacts **24** in the middle of the capacitor structure, as shown in Figure 1d. The diffusion contacts serve to generate a nearby supply of minority carriers and thus improves the frequency response of the capacitor. Therefore, it would be possible to further subdivide the capacitor structure so as to add more diffusion contacts **24** and further improve the frequency response. However, this approach suffers from the drawback that it also adds parasitic capacitance which reduces the efficiency of the charge pump. Moreover, there is another disadvantage that the amount of area occupied by the capacitor on a semiconductor chip is significantly increased.

Similarly, there is shown in Figure 3a the electrical symbol for a capacitor-connected P-channel MOS transistor **P1**. Figure 3b shows the cross-sectional view of the P-channel MOS transistor **P1**. The capacitor is formed of a p-type substrate **26**. An n-well region **28** is formed in the substrate **26**. A p-type source region **30** and a p-type drain region **32** are diffused in the surface

of the n-well region **28**. A thin gate oxide layer **34** is interposed between the top surface of the n-well region **28** and a conductive polysilicon gate **36**. Further, an n-well contact region **38** is formed in the n-well region **28**. The contact region **38**, source region **30**, and drain region **32** are all connected together and to a metal contact connection **40** defining one plate of the capacitor **P1**. The gate **36** is also connected to a metal contact connection **42** defining the other plate of the capacitor **P1**.

In Figure 4, there is illustrated a plot of the capacitance value for the three operating regions (accumulation, depletion, and inversion) of the capacitor-connected MOS transistor **P1** of Figure 3b as a function of the voltage V_g applied to the polysilicon gate. It will be noted again that when the capacitor **P1** is being operated in the inversion region there is the disadvantage of having the capacitance value fall off at the higher frequencies.

In Figure 7, there is depicted a schematic circuit diagram of a single stage positive voltage charge pump **44** of the prior art. The charge pump **44** includes a pair of N-channel MOS transistors **T1**, **T2** and the inversion capacitor **N1** (similar to Figure 1b). The drain and gate of the transistor **T1** are connected together and to an input voltage terminal **46** for receiving a power supply voltage source **VCC**. The gate and drain of the transistor **T2** are also connected together and to the source of the transistor **T1** and to one plate of the capacitor **N1** at node **A**. The other plate of the capacitor **N1** is connected to an input node **48** for receiving a clock signal ϕ. The source of the transistor **T2** is connected to the output terminal **OUT** of the charge pump **44**.

Referring again to the graph of Figure 2, it will be noted that for a full capacitance value in the inversion region the initial condition of the node **A** must be

greater than the threshold voltage of the capacitor-connected MOS transistor **N1**, which is approximately 1 volt. Thus, the operating voltage of the inversion capacitor cannot be reduced or lowered below 1 volt. On the other hand, the accumulation capacitor can be initialized at 0 volts as depicted in Figure 2. Another disadvantage of the inversion capacitor is that its effective threshold is increased due to the "body effect," which is caused by the differential potential applied between the source and the substrate of the transistor **N1**.

Accordingly, it would be desirable to provide an improved charge pump which overcomes the disadvantages of the prior art so as to be capable of operating reliably and effectively at lower power supply voltages (i.e., at 3 V or lower). It would be expedient that the charge pump be operated effectively so as to produce a significant reduction in power consumption. The present invention provides an improved charge pump by utilizing accumulation capacitors which is able to operate at lower voltages and with higher efficiency.

SUMMARY OF THE INVENTION

It is a general object of the present invention to provide an improved charge pump which overcomes all of the disadvantages of the prior art charge pumps.

It is an object of the present invention to provide an improved charge pump circuit utilizing accumulation capacitors for use in EEPROM devices so as to internally pump up a power source voltage on a more efficient and effective basis.

It is another object of the present invention to provide an improved charge pump circuit which is capable of operating reliably and effectively at lower power supply voltages.

It is still another object of the present invention to provide an improved charge pump which can be operated

efficiently so as to produce a significant reduction in power consumption.

In accordance with these aims and objectives, the present invention is concerned with the provision of a charge pump circuit utilizing accumulation capacitors for use in EEPROM devices so as to internally pump up an external power supply voltage. The charge pump circuit includes a plurality of MOS transistors connected in series between a first input voltage terminal and a higher voltage output terminal. The first input voltage terminal receives an external power supply voltage.

An accumulation capacitor has a first plate and a second plate. The first plate of the accumulation capacitor is connected between adjacent ones of the plurality of MOS transistors. The second plate of the accumulation capacitor is connected to a second input terminal for receiving a clock signal.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects and advantages of the present invention will become more fully apparent from the following detailed description when read in conjunction with the accompanying drawings with like reference numerals indicating corresponding parts throughout, wherein:

Figure 1a shows the electrical symbol for an N-channel MOS transistor **N1** connected so as to form an inversion capacitor for use in positive charge pumps;

Figure 1b is a cross-sectional view of the capacitor-connected N-channel MOS transistor **N1** of Figure 1a;

Figure 1c is top plan view of the capacitor-connected N-channel MOS transistor **N1** of Figure 1b;

Figure 1d is a top plan view of a capacitor-connected N-channel MOS transistor, similar to Figure 1c, which has an improved frequency response;

Figure 2 is a graph illustrating the capacitance value for the three operating regions of the capacitor-

connected N-channel MOS transistor **N1** of Figure 1b as a function of the gate voltage V_g;

Figure 3a shows the electrical symbol for a P-channel MOS transistor **P1** connected so as to form an inversion capacitor for use in negative charge pumps;

Figure 3b is a cross-sectional view of the capacitor-connected P-channel MOS transistor **P1** of Figure 3a;

Figure 4 is a graph illustrating the capacitance value for the three operating regions of the capacitor-connected P-channel MOS transistor **P1** of Figure 3b as a function of the gate voltage V_g;

Figure 5a shows the electric symbol for an n-well capacitor for use as an accumulation capacitor in positive charge pumps;

Figure 5b is a cross-sectional view of the n-well capacitor of Figure 5a, constructed in accordance with the principles of the present invention;

Figure 6a shows the electrical symbol for a p-well capacitor for use as an accumulation capacitor in negative charge pumps;

Figures 6b is a cross-sectional view of the p-well capacitor of Figure 6a, constructed in accordance with the principles of the present invention;

Figure 7 is a schematic circuit diagram of a single stage positive voltage charge pump of the prior art, utilizing an inversion capacitor similar to Figure 1b;

Figure 8 is a schematic circuit diagram of a single stage positive voltage charge pump of the present invention, utilizing an accumulation capacitor similar to Figure 5b; and

Figure 9 is a schematic circuit diagram of a single stage negative voltage charge pump of the present invention, utilizing an accumulation capacitor similar to Figure 6b.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following, there will be described the preferred embodiments of the present invention with reference to the drawings. In Figure 5a, there is shown an electrical symbol for an n-well capacitor **N2** for use as an accumulation capacitor in positive voltage charge pumps. There is illustrated in Figure 5b a cross-sectional view of the n-well capacitor of Figure 5a, which is constructed with the principles of the present invention. As can be seen, the reference numeral **110** denotes an N-well region. There are formed n-type well electrode regions **112** and **114** in the n-well region **110**. A thin gate oxide layer **116** is interposed between the top surface of the n-well region and a conductive polysilicon gate **118**. The n-type well electrode regions **112** and **114** are connected together and to a metal contact connection **120** defining one plate of the n-well capacitor **N2**. The gate **118** is also joined to a metal contact connection **122** defining the other plate of n-well capacitor **N2**.

In Figure 8, there is illustrated a schematic circuit diagram of a single stage positive charge voltage pump **144** utilizing an accumulation capacitor, constructed in accordance with the principles of the present invention. The charge pump **144** includes a pair of N-channel MOS transistor **T101, T102** and the accumulation capacitor **N2** (similar to Figure 5b). The gate and drain of the transistor **T101** are connected together and to an input voltage terminal **146** for receiving a power supply voltage source **VCC**. The gate and drain of the transistor **T102** are also connected together and to the source of the transistor **T101** and to one plate **122** of the n-well capacitor **N2** at an internal node **B**. The other plate **120** of the capacitor **N2** is connected to an input terminal **148** for receiving a clock signal ϕ. The source of the transistor **T102** is connected to the output node **OUT** of the charge pump **144**. With reference to the graph of

Figure 2, it should be clear, as previously pointed out, that since the n-well capacitor **N2** is operating in the accumulation region it can be initialized at zero volts.

Further, the power supply voltage source **VCC**, which is typically at +3.0 volts, can be reduced to approximately 2 volts so as to operate adequately in battery powered applications, thereby reducing significantly the power dissipation. As a result, the efficiency of the charge pump **144** can be increased by about 20% over the prior art charge pump **44** using the inversion capacitor. Moreover, the present charge pump **144** can be operated at a higher frequency of the switching voltage supply since the capacitance value in the accumulation region, unlike the inversion region, does not fall off at higher frequencies. In addition, the accumulation capacitors do not suffer from the "body effect" since there is no source-substrate voltage differential.

With reference to Figure 6a of the drawings, there is depicted an electrical symbol for a p-well capacitor **P2** for use as an accumulation capacitor in negative voltage charge pumps. There is shown in Figure 6b a cross-sectional structural view of the p-well capacitor of Figure 6a, which is constructed in accordance with the principles of the present invention. As can be seen, the reference numeral **210** designates a p-type substrate which has formed therein an n-well region **212**. A p-well region **214** is, in turn, formed in the n-well region **212**. There are formed a pair of p-well electrode regions **216** and **218** in the p-well region **214**. A thin gate oxide region **220** is interposed between the top surface of the p-well region and a conductive polysilicon gate **222**. Thus, the p-well region **214** is electrically insulated from the p-type substrate **210**. The p-type well electrode regions **216** and **218** are connected together and to a metal contact connection **224** defining one plate of the p-well capacitor

P2. The gate 222 is also joined to a metal contact connection 226 defining the other plate of the capacitor P2.

In Figure 9, there is illustrated a schematic circuit diagram of a single stage negative voltage charge pump 244 utilizing an accumulation capacitor, constructed in accordance with the principles of the present invention. The charge pump 244 includes a pair of P-channel MOS transistors T201, T202 and the accumulation capacitor P2 (similar to Figure 6b). The gate and source of the transistor T201 are connected together and to an input voltage terminal 246 for receiving a power supply voltage source VSS, which is typically at ground potential. The gate and source of the transistor T202 are connected together and to the drain of the transistor T201 and to one plate 226 of the p-well capacitor P2 at an internal node C. The other plate 224 of the capacitor P2 is connected to an input node 248 for receiving a clock signal ϕ. The drain of the transistor T202 is also connected to the output terminal OUT of the charge pump. With reference to the graph of Figure 4, it will again be noted that since the p-well capacitor P2 is being operated in the accumulation region, it can be likewise initialized at zero volts and has all the advantages similar to that described with respect the n-well capacitor N2.

While Figures 8 and 9 show only single stage charge pumps, it should be apparent to those skilled in the art that they could be formed as multi-stage charge pumps. In this case, a plurality of MOS transistors would be cascade-connected between the input voltage terminal and the output voltage terminal. A corresponding plurality of capacitors would have their one end connected to respective internal nodes between adjacent transistors. Further, the other ends of the adjacent capacitors would

be driven by non-overlapping two-phase clock signals $\phi 1$ and $\phi 2$.

From the foregoing detailed description, it can thus be seen that the present invention provides improved charge pumps utilizing accumulation capacitors for use in EEPROM devices so as to internally pump up a power supply voltage. The present charge pump overcomes the disadvantages of the prior art so as to be capable of operating reliably and effectively at lower power supply voltage. As a result, the charge pump of the present invention has improved efficiency since there is achieved a significant reduction in power consumption.

While there has been illustrated and described what are at present considered to be preferred embodiments of the present invention, it will be understood by those skilled in the art that various changes and modifications may be made, and equivalents may be substituted for elements thereof without departing from the true scope of the invention. In addition, many modifications may be made to adapt a particular situation or material to the teachings of the invention without departing from the central scope thereof. Therefore, it is intended that this invention not be limited to the particular embodiments disclosed as the best modes contemplated for carrying out the invention, but that the invention will include all embodiments falling within the scope of the appended claims.

CLAIMS

WHAT IS CLAIMED IS:

1. A charge pump circuit utilizing accumulation capacitors for use in EEPROM devices so as to internally pump up an external power supply voltage, comprising:

a plurality of MOS transistors (**T101, T102; T201, T202**) connected in series between a first input voltage terminal, and a higher voltage output terminal, said first input voltage terminal receiving the external power source voltage;

accumulation capacitors (**N2, P2**) each having a first plate and a second plate;

each of said first plates of said accumulation capacitors being connected between adjacent ones of said plurality of MOS transistors; and

each of said second plates of said accumulation capacitors being connected to a second input terminal for receiving a clock signal.

2. A charge pump circuit as claimed in Claim 1, wherein said plurality of MOS transistors is comprised of N-channel transistors (**T101, T102**).

3. A charge pump circuit as claimed in Claim 1, wherein said plurality of MOS transistors is comprised of P-channel transistors (**T201, T202**).

4. A charge pump circuit as claimed in Claim 2, wherein said external power source voltage is comprised of a positive potential (**VCC**), which is typically at +3.0 volts or lower.

5. A charge pump circuit as claimed in Claim 3, wherein said external power source voltage is comprised of a ground potential (**VSS**), which is typically at zero volts.

6. A charge pump circuit as claimed in Claim 4, wherein each of said accumulation capacitors is comprised of an n-well capacitor (**N2**).

7. A charge pump circuit as claimed in Claim 5, wherein each of said accumulation capacitors is comprised of a p-well capacitor (**P2**).

8. A charge pump circuit as claimed in Claim 6, wherein said n-well capacitor includes a pair of n+ electrode regions (**112, 114**) formed in an n-well region (**110**) and a gate oxide layer (**116**) disposed between the top surface of said n-well region and a polysilicon gate (**118**).

9. A charge pump circuit as claimed in Claim 7, wherein said p-well capacitor includes a pair of p+ electrode regions (**216, 218**) formed in a p-well region (**214**) within an n-well region (**212**) and a gate oxide layer (**220**) disposed between the top surface of said p-well region and a polysilicon gate (**222**), said n-well region being disposed in a p-type substrate (**210**).

10. A positive voltage charge pump circuit for use in semiconductor memory devices, comprising:

a pair of N-channel MOS transistors (**T101, T102**) connected in series between a first input voltage terminal and a higher voltage output terminal, each of said pair of N-channel MOS transistors having its gate and drain connected together, said first input voltage terminal receiving an external power source voltage;

an n-well capacitor (**N2**) functioning as an accumulation capacitor having a first plate and a second plate;

said first plate of said n-well capacitor being connected between junction of said pair of MOS transistors; and

said second plate of said n-well capacitor being connected to a second input terminal for receiving a clock signal.

11. A charge pump circuit as claimed in Claim 10, wherein said external power source voltage is comprised of a positive potential (**VCC**), which is typically at +3.0 volts or lower.

12. A charge pump circuit as claimed in Claim 11, wherein said n-well capacitor includes a pair of n+ electrode regions (**112, 114**) formed in an n-well region (**110**) and a gate oxide layer (**116**) disposed between the top surface of said n-well region and a polysilicon gate (**118**).

13. A charge pump circuit for use in a semiconductor integrated circuit device for generating at an output terminal a voltage which is pumped higher than an external power source voltage, comprising:

transistor charging means connected between the external power source voltage and said output terminal for generating the higher voltage at said output terminal; and

accumulation capacitor means connected to said transistor charging means and being responsive to clock signals for generating the higher voltage at said output terminal.

14. A charge pump circuit as claimed in Claim 13, wherein said transistor charging means is comprised of a plurality of N-channel transistors (**T101, T102**).

15. A charge pump circuit as claimed in Claim 13, wherein said transistor charging means is comprised of a plurality of P-channel MOS transistors (**T201, T202**).

16. A charge pump circuit as claimed in Claim 14, wherein said accumulation capacitor means is comprised of an n-well capacitor (**N2**).

17. A charge pump circuit as claimed in Claim 15, wherein said accumulation capacitor means is comprised of a p-well capacitor (**P2**).

18. A charge pump circuit as claimed in Claim 16, wherein said n-well capacitor includes a pair of n+ electrode regions (**112, 114**) formed in an n-well region (**110**) and a gate oxide layer (**116**) disposed between the top surface of said n-well region and a polysilicon gate (**118**).

19. A charge pump circuit as claimed in Claim 17, wherein said p-well capacitor includes a pair of p+ electrode regions (**216, 218**) formed in a p-well region (**214**) within an n-well region (**212**) and a gate oxide layer (**220**) disposed between the top surface of said p-well region and a polysilicon gate (**222**), said n-well region being disposed in a p-type substrate (**210**).

FIG. 1a

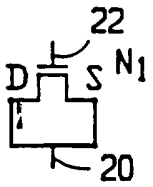


FIG. 1b

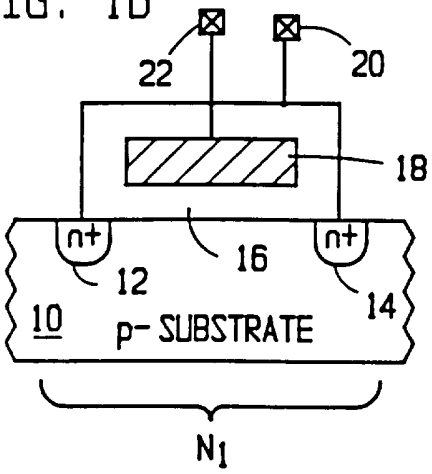


FIG. 1c

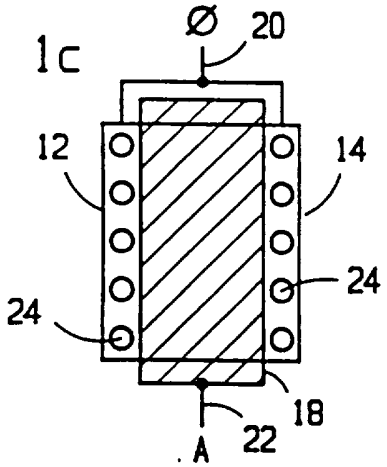


FIG. 1d

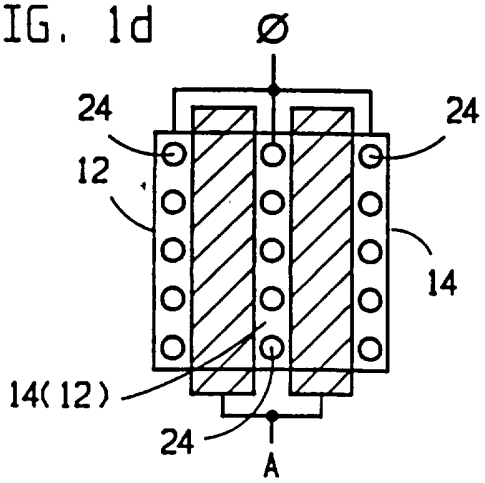


FIG. 3a

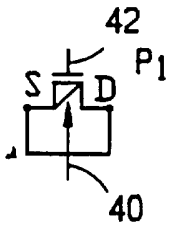


FIG. 3b

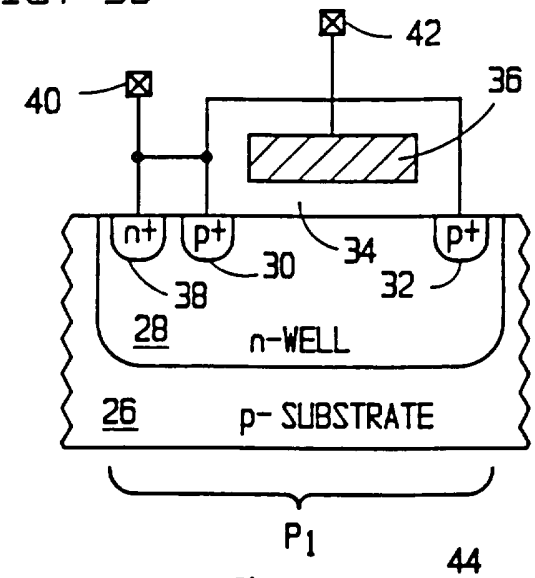


FIG. 7

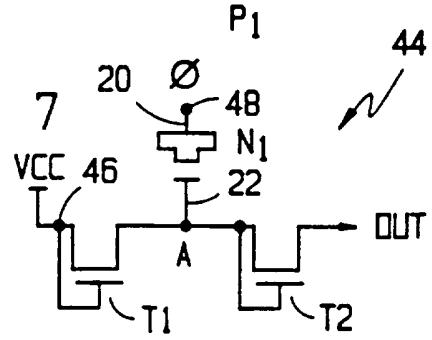


FIG. 8

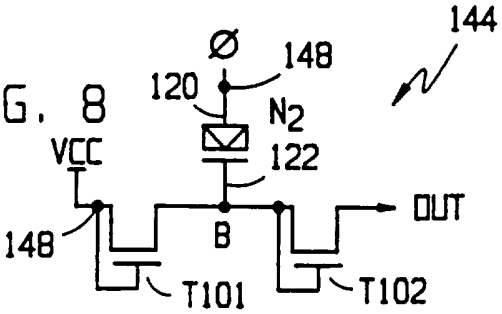
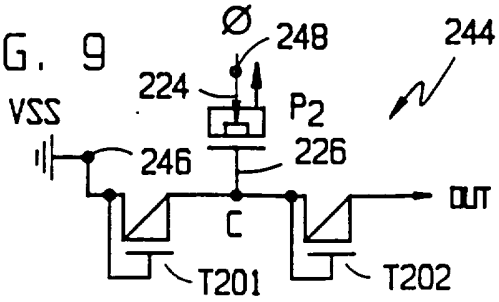
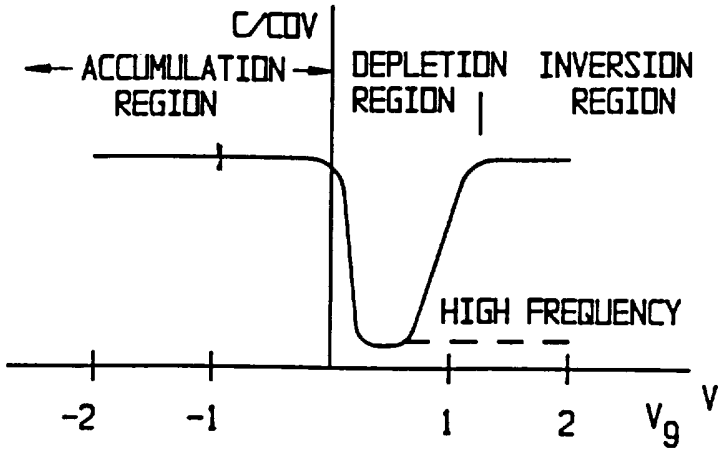


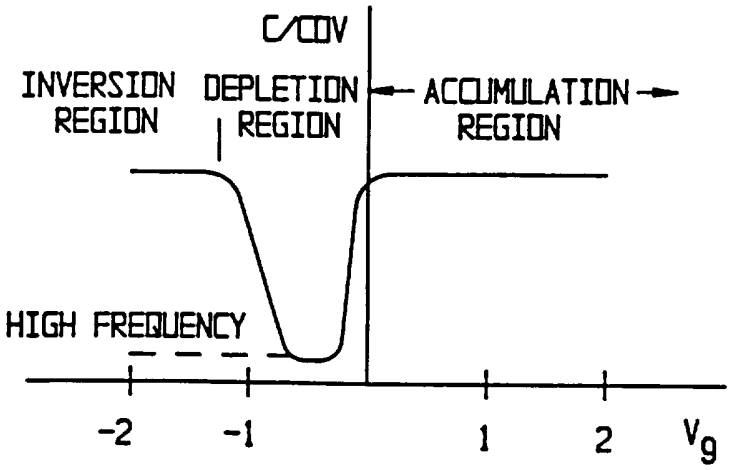
FIG. 9





CAPACITANCE VS V_g FOR N-CHANNEL TRANSISTOR

FIG. 2



CAPACITANCE VS V_g FOR P-CHANNEL TRANSISTOR

FIG. 4

FIG. 5a

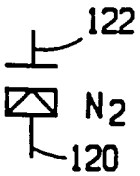


FIG. 5b

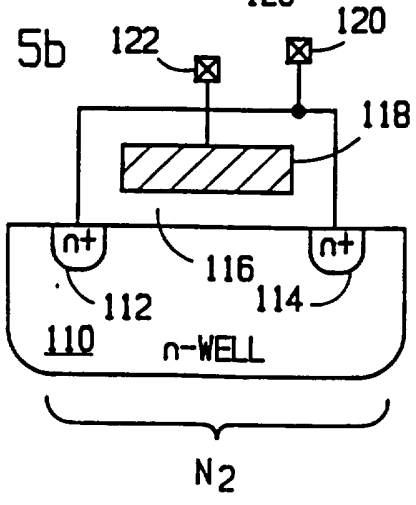


FIG. 6a

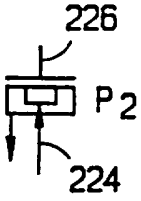
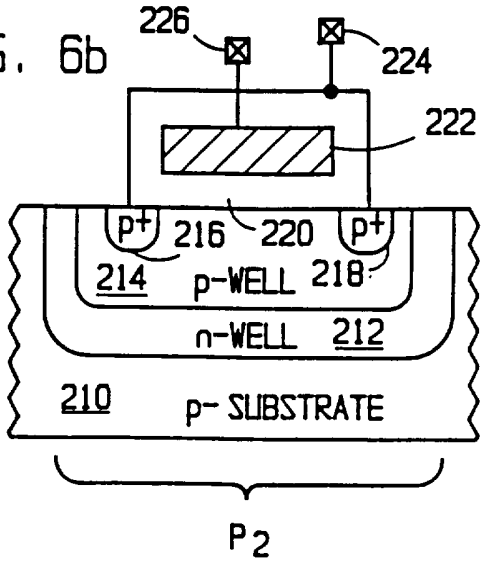


FIG. 6b



INTERNATIONAL SEARCH REPORT

Inte ɔnal Application No
PCT/US 96/12122

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L27/02 G05F3/20 H01L29/94

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L G05F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP,A,0 638 984 (ADVANCED MICRO DEVICES INC) 15 February 1995 see the whole document ---	1-19
Y	EP,A,0 581 702 (SGS THOMSON MICROELECTRONICS) 2 February 1994 see the whole document ---	1-19
A	EP,A,0 062 894 (TOKYO SHIBAURA ELECTRIC CO) 20 October 1982 see page 5, line 7 - page 8, line 1; figures 3,4 -----	1-3,5, 10,13-15

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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1

Date of the actual completion of the international search	Date of mailing of the international search report
29 October 1996	21. 11. 96
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax (+ 31-70) 340-3016	Authorized officer Albrecht, C

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter ›nal Application No
PCT/US 96/12122

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