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(54) Title: BROADBAND TERMINATION RESISTANCE INTEGRATED IN A GENERIC PHOTONIC FOUNDRY PLATFORM

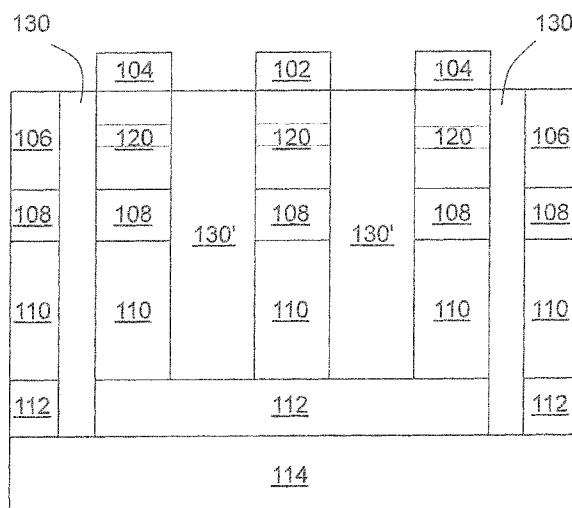


FIG. 1C

(57) Abstract: We provide a new type of broadband 50 Ohm termination resistance that is easily integrated into an existing generic photonic integration platform. The main idea is to use the epitaxially grown p-i-n layers (112,110,108,120) underneath signal (102) and ground (104) electrodes in a load area which is insulated by trenches (130,130') to form capacitive (across intrinsic semiconductor layer 110) and resistive (in doped semiconductor layer 112) elements. The device demonstrates DC blocking and a wideband impedance match to a 50 Ohm line. This approach is well suited for co-integration with high-speed electro-absorption and Mach-Zehnder modulators in order to prevent electrical signal reflections.

Broadband Termination Resistance Integrated in a  
Generic Photonic Foundry Platform

by

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FIELD OF THE INVENTION

This invention relates to providing on-chip radio frequency (RF) terminations, especially in connection with optoelectronic devices.

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BACKGROUND

One of the main drivers for photonic integrated circuits (PICs) are applications in the field of optical communications, where the demand for transmitter and receiver capacity steadily increases but at the same time cost reduction is of utmost importance. The generic foundry approach to photonic integration is well suited for producing low-cost high performance transmitter PICs for optical interconnect and transport applications. To further improve on integration density, operation speed and cost reduction, advancements in the foundry's capabilities on the device level are required.

Traveling-wave electro-absorption modulators (EAM) and Mach-Zehnder modulators (MZM) are often used components in high-capacity transmitter PICs and need to be properly designed for high-speed operation. This requires matched electrical terminations at the modulator's end in order to reduce undesired RF signal reflections. Monolithically integrated termination loads are preferred over discrete

off-chip solutions as they can be conveniently utilized in large-scale integrated modulator arrays, reducing footprint and packaging complexity. Up until now, integrated load terminations in combination with EAMs have been realized  
5 using evaporated NiCr as the resistive element. For MZ modulators in InP the InGaAs contact layer can be used to form the termination and for modulators on silicon substrate, TiN resistors are usually used as loads.

It would be an advance in the art to provide improved  
10 on-chip RF terminations for optoelectronic devices.

#### SUMMARY

High speed optical modulators need to have proper electrical termination of the input RF signals in order to  
15 reduce/eliminate undesirable RF reflections. On-chip terminations are more desirable than off-chip terminations because they are more conducive to large scale integration. However, on-chip terminations that have been demonstrated to date tend to lack a DC blocking capability. Such DC  
20 blocking is needed to operate the optical modulator in reverse electrical bias, which is usually the desired operating mode.

In this work a DC blocking, on-chip RF termination for optical modulators is provided. The basic idea is to  
25 provide an RF load having an impedance that can be controlled via semiconductor fabrication. The RF signal and ground electrodes are connected to this load via vertical stacks of semiconductor materials that have a highly doped layer next to the metal electrodes (to make  
30 electrical contact), and which include an intrinsic/undoped layer (to provide the DC blocking). RF signals are able to pass through the intrinsic/undoped layer to reach the RF

load. As used herein, "radio frequency" (RF) refers to electromagnetic radiation having a frequency in the range from 3 kHz to 300 GHz.

## 5 BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a top view of an embodiment of the invention.

FIGS. 1A-C show cross sections through the structure of FIG. 1.

10 FIG. 2 shows a top view of an embodiment of the invention.

FIGS. 2A-C show cross sections through the structure of FIG. 2.

15 FIG. 3A shows a top view of a Mach-Zehnder modulator lacking an on-chip RF termination.

FIG. 3B shows a top view of a Mach-Zehnder modulator having an on-chip RF termination.

FIG. 4 shows an equivalent circuit for the RF termination in an experiment.

20 FIG. 5 shows calculated impedance vs. frequency for an exemplary on-chip RF termination according to principles of the invention. The geometrical parameters in the legend of this plot are defined on FIG. 2.

25 FIG. 6 shows simulated reflection (S11) at 10 GHz for various load geometries. Parameters of fabricated devices are shown with numbered circles. Here 'separation' is sep as shown on FIG. 2.

FIG. 7A shows simulated and measured S11 reflection coefficient for fabricated RF terminations.

FIG. 7B shows measured I-V curves for fabricated RF terminations.

FIG. 7C shows measured input impedance vs. frequency for fabricated RF terminations.

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#### DETAILED DESCRIPTION

Section A describes general principles relating to embodiments of the invention. Section B describes an exemplary experimental demonstration.

10

#### A) General principles

FIG. 1 shows a top view of an embodiment of the invention. FIGs. 1A-C show cross sections through the structure of FIG. 1 along sections A-C respectively. In the epitaxial structure, 114 is a semiconductor substrate, 112 is a first doped semiconductor region disposed on substrate 114, and 110 is an intrinsic semiconductor region disposed on first doped semiconductor region 112. Here an RF transmission line is formed by signal electrode 102 and ground electrodes 104 and is disposed above the intrinsic semiconductor region. Zero or more intervening regions separate the electrical transmission line from the intrinsic semiconductor region 110. The optional intervening layers of this example are described below.

25 A first insulating trench 130 extends vertically from the substrate 114 to the electrical transmission line and laterally encircles a load region (112 on FIG. 1, dashed lines) of the electrical termination structure. A second insulating trench (130' on FIG. 1C) within the load region extends vertically from the first doped semiconductor region 112 to the electrical transmission line, and

30

separates ground and signal electrical contacts of the electrical transmission line, as shown on FIG. 1C.

The load region (112 on FIG. 1) of the electrical termination structure makes RF (radio frequency) electrical contact between signal and ground of the electrical transmission line laterally through the first doped semiconductor region 112, and vertically through at least the intrinsic semiconductor region (110 on FIG. 1C).

Dimensions of the first doped semiconductor region, dimensions of the intrinsic semiconductor region, and dimensions of the second insulating trench are preferably configured to provide an RF load impedance of about 50  $\Omega$  in the load region.

The zero or more intervening regions can include a second doped semiconductor region, e.g., 108 on FIGs. 1A-C. The zero or more intervening regions outside the insulating trench can include a passivation structure, e.g., passivation layer 106 as shown on FIGs. 1 and 1A. The zero or more intervening regions within the insulating trench can include an electrical contact structure, e.g., contact 120 on FIG. 2C. This electrical contact structure can include a heavily doped semiconductor layer. Here "heavily doped" refers to a doping level sufficient to put the electron Fermi level into the conduction band (or put the hole Fermi level into the valence band). For electrons in InGaAs, this corresponds to a doping level of  $1.8 \times 10^{17} \text{ cm}^{-3}$  or greater.

Preferably the first and second insulating trenches are filled with an insulator. Suitable insulators for this include, but are not limited to: insulating polymers such as polyimide.

The example of FIGs. 1 and 1A-C relates to a simplified layer structure. However, the same principles can be applied to a more realistic example, such as the example of FIGs. 2 and 2A-C. The epitaxial structure of this example includes a p-i-n diode and optical waveguide structure suitable for optical modulators, and is also the epitaxial structure of the experiments of section B.

FIG. 2 shows a top view of an embodiment of the invention. FIGs. 2A-C show cross sections through the structure of FIG. 2 along sections A-C respectively. In the epitaxial structure of this example, 214 is a semiconductor substrate, 212 is a first doped semiconductor region (n-InP) disposed on substrate 214, 210 is an intrinsic semiconductor layer (i-InGaAsP) disposed on first doped semiconductor region 212, and 208 is an intrinsic layer (i-InP) disposed on layer 210. Here layers 208 and 210 together form an intrinsic region as described above (e.g., 110 on FIGs. 1A-C). An RF transmission line is formed by signal electrode 102 and ground electrodes 104 and is disposed above the intrinsic semiconductor region.

The optional intervening layers of this example include a second doped semiconductor region 206 (p-InP), a polyimide layer 204 and an SiO<sub>2</sub> layer 202. Layers 202 and 204 provide passivation for this example. Within the load region, passivation layers 202 and 204 are replaced with contact layer 220 under the electrodes of the RF transmission line, as shown on FIG. 2C.

An optical modulator layer stack 216 (i.e., optical waveguide + p-i-n diode) is formed by these epitaxial layers as follows. InGaAsP layer 210 is the waveguide core, and InP layers 206, 208 and 212 provide the cladding surrounding the waveguide core. Layers 208 and 210 are

intrinsic, layer 206 is p-type and layer 212 is n-type, thereby forming a p-i-n diode.

A first insulating trench 230 extends vertically from the substrate 214 to the electrical transmission line and laterally encircles a load region (212 on FIG. 2, dashed lines) of the electrical termination structure. A second insulating trench (230' on FIG. 2C) within the load region extends vertically from the first doped semiconductor region 212 to the electrical transmission line, and separates ground and signal electrical contacts of the electrical transmission line, as shown on FIG. 2C.

The load region (212 on FIG. 2) of the electrical termination structure makes RF (radio frequency) electrical contact between signal and ground of the electrical transmission line laterally through the first doped semiconductor region 212, and vertically through the intrinsic semiconductor region (208 and 210 on FIG. 2C), the second doped semiconductor region (206 on FIG. 2C), and the contact structure (220 on FIG. 2C). Contact structure 220 can include one or more heavily doped semiconductor layers.

Dimensions of the first doped semiconductor region, dimensions of the intrinsic semiconductor region, and dimensions of the second insulating trench are preferably configured to provide an RF load impedance of about 50  $\Omega$  in the load region.

Preferably the first and second insulating trenches are filled with an insulator. Suitable insulators for this include, but are not limited to: insulating polymers such as polyimide.

The above-described structures can be readily fabricated using standard semiconductor fabrication

technology. Although specific materials are described in relation to the example of FIG. 2, practice of the invention does not depend critically on the materials employed. These ideas are expected to be applicable to any  
5 device that needs to have an on-chip RF termination, especially optical modulators.

## B) Experimental example

### B1) Introduction

10 In this work, we provide a new design for an integrated termination resistance that uses the bottom n-doped InP cladding layer and also has DC blocking capability. The device can be fabricated within a common generic photonic foundry process which is based on semi-  
15 insulating substrate. We first describe the device structure, then deal with design considerations and device simulation and finally present measurement results of the fabricated device.

### 20 B2) Device Structure

One of the limiting factors for optical transmitter PICs has been the interface to the high-speed electronics. Frequently PICs have an arrangement as schematically shown on FIG. 3A, where RF transmission lines 308 and 310 are  
25 both input to and output from PIC chip 302, e.g., to drive optical modulator 306. In this approach, referred to as off-chip termination, RF signals are brought off-chip to provide their proper termination. This approach becomes increasingly difficult when the number of modulators  
30 increases in multi-channel large-scale PICs.

It is preferable to have on-chip termination, e.g., as on FIG. 3B, where on-chip terminations 312 and 314 terminate transmission lines 308 and 310 respectively. By utilizing on-chip integrated termination loads the number of RF feeds and connections to PIC chips can be reduced by half, thereby facilitating electronic packaging. However, it is required for the termination to incorporate DC blocking, as the majority of high-speed modulators are operated in reverse bias and no DC current flow is desired.

Section A describes a new termination device that fulfills both functions. It conveniently connects to coplanar RF tracks and utilizes the epitaxially grown layers in such a way that DC current is blocked by the depletion layer capacitance and the overall impedance between the central signal metal and the two ground metals equals  $50\ \Omega$ . In the example of FIGs. 2 and 2A-C, the resistance is formed through the contact resistance  $R_C$  of contact 220, the sheet resistance  $R_P$  of the p-doped layer 206 and the sheet resistance  $R_N$  of the n-doped layer 212. An island of n-doped material 212 is formed by etching a trench around the device to assure electrical isolation to the rest of the chip, whereas trenches until the n-layer depth between signal and ground metal are etched to remove the p-doped and intrinsically doped InP. These trenches can be filled with an insulator, e.g., polyimide.

The resulting structure placed on a semi-insulating InP substrate can be represented by the equivalent circuit shown in FIG. 4. Here  $C_J$  is the junction capacitance formed by intrinsic layers 208 and 210, and the equivalent circuit accounts for different parameter values for the signal line (unprimed) and ground lines (primed).

## B3) Design and Simulation

The total impedance of the device can be calculated from the equivalent circuit according to

$$Z_{tot} = R_P + R_C + X_J + \frac{1}{2}(R'_P + R'_C + X'_J + R_N), \quad (1)$$

5 where the frequency dependent reactances are from the depletion layer capacitance□

$$X_J = \frac{1}{j\omega C_J} \quad X'_J = \frac{1}{j\omega C'_J}. \quad (2)$$

The DC blocking functionality is realized by this capacitance which takes values of 1 pF and 1.6 pF  
 10 respectively for the parameters specified in Table 1. The calculated total impedance is shown in FIG. 5, indicating that proper dimensioning of the geometrical parameters can yield a broadband 50 Ω load.

| Parameter                  | Value                                         |
|----------------------------|-----------------------------------------------|
| contact (220) resistivity  | $2 \times 10^{-4} \text{ } \Omega\text{cm}^2$ |
| p-layer (206) thickness    | 300 nm                                        |
| i-layer (208) thickness    | 150 nm                                        |
| Q-layer (210) thickness    | 500 nm                                        |
| n-layer (212) thickness    | 1.1 μm                                        |
| contact (220) conductivity | $23 \times 10^3 \text{ S/m}$                  |
| p-layer (206) conductivity | 120 S/m                                       |
| i-layer (208) permittivity | 10                                            |
| Q-layer (210) conductivity | $16.4 \times 10^3 \text{ S/m}$                |
| n-layer (212) conductivity | $13 \times 10^3 \text{ S/m}$                  |

Table 1: Material parameters for the analytical and CST®  
 15 simulations. Here reference numbers refer to FIG. 2C.

For a more accurate analysis, we utilize the full-wave electromagnetic solver package CST® MWS® (Computer Simulation Technology Microwave Studio) to simulate the scattering parameters of the device. The 3D model  
5 incorporates the exact epitaxial layer structure and also includes the RF tracks leading to the device. FIG. 6 shows the simulated reflection magnitude at 10 GHz for varying signal metal widths  $W_{sig}$  and its separation to the ground metal. A low reflection magnitude corresponds to a good  
10 match to the reference impedance of 50  $\Omega$ . Based on the results, we fabricated devices with different geometries also indicated on FIG. 6. It is evident that the separation distance influences the reflection magnitude more than the signal width, as the majority of the resistive path lies in  
15 the n-doped layer 212 and its length determines the total impedance.

#### B4) Measurement Results

The fabricated devices were characterized using a  
20 vector network analyzer and RF probes. The reflection coefficient S11 of the device can be directly measured and indicates how much of the incident electrical signal is reflected. The best performing device shows reflection magnitudes below -10 dB from 1.8 GHz until 67 GHz as can be  
25 seen in FIG 7A. DC blocking is realized in reverse bias through the diode under the signal metal whereas in forward bias it occurs because of the diode below the ground metal. FIG. 7B shows that this DC blocking is observed from -15 V to +20 V with a small leakage current of 1 mA at +20 V.  
30 Given the reference impedance of 50  $\Omega$  during measurement, the input impedance to the device can be directly derived from the S11 measurements and is shown in FIG. 7C. The

impedance value seen from the RF line input to the device is close to 50 Ohms so that reflections are kept at a low level.

Previous simulations showed that the optimum  
5 separation distance is at 110  $\mu\text{m}$ , leading to the lowest reflection magnitude. The optimum device found in measurement has a separation of 75  $\mu\text{m}$ . Differences between the simulation and measurement can be attributed to the  
10 actual fabricated devices, where the optimum is shifted to lower separation distances.

#### B5) Conclusion

We have demonstrated a new design for an integrated  
15 termination resistance that has been fabricated within a generic photonic integration process with semi-insulating substrate. It is based on the n-doped cladding layer that forms the resistive element and on the depletion layer that forms a DC block. The measurement results indicate that  
20 impedance values close to 50  $\Omega$  can be achieved in a broad bandwidth range and that DC currents are blocked for a reasonable voltage span. It will be advantageous to use the presented device in combination with EAMs and MZ modulators to save on device footprint and packaging complexity in  
25 transmitter PIC applications.

## CLAIMS

1. An electrical termination structure for an opto-electronic device, the termination comprising:

5       a semiconductor substrate;

          a first doped semiconductor region disposed on the semiconductor substrate;

          an intrinsic semiconductor region disposed on the first doped semiconductor region;

10       an electrical transmission line disposed above the intrinsic semiconductor region, wherein zero or more intervening regions separate the electrical transmission line from the intrinsic semiconductor region;

          a first insulating trench extending vertically from  
15 the substrate to the electrical transmission line and laterally encircling a load region of the electrical termination structure;

          a second insulating trench within the load region and extending vertically from the first doped semiconductor  
20 region to the electrical transmission line, wherein the second insulating trench separates ground and signal electrical contacts of the electrical transmission line;

          wherein the load region of the electrical termination structure makes RF (radio frequency) electrical contact  
25 between signal and ground of the electrical transmission line laterally through the first doped semiconductor region, and vertically through at least the intrinsic semiconductor region.

30 2. The electrical termination structure of claim 1, wherein dimensions of the first doped semiconductor region,

dimensions of the intrinsic semiconductor region, and dimensions of the second insulating trench are configured to provide an RF load impedance of about 50  $\Omega$  in the load region.

5

3. The electrical termination structure of claim 1, wherein the zero or more intervening regions outside the insulating trench include a passivation structure.

10 4. The electrical termination structure of claim 3, wherein the passivation structure includes a layer of silicon oxide on top of a polymer layer.

15 5. The electrical termination structure of claim 1, wherein the zero or more intervening regions within the insulating trench include an electrical contact structure.

20 6. The electrical termination structure of claim 5, wherein the electrical contact structure comprises one or more heavily doped semiconductor layers.

7. The electrical termination structure of claim 1, wherein direct current (DC) blocking is provided by the intrinsic region.

25

8. The electrical termination structure of claim 1, wherein the zero or more intervening regions comprise a second doped semiconductor region.

9. The electrical termination structure of claim 8, wherein the first doped semiconductor region, the intrinsic semiconductor region and the second doped semiconductor region are configured to provide a p-i-n diode.

5

10. The electrical termination structure of claim 9, wherein the first doped semiconductor region, the intrinsic semiconductor region and the second doped semiconductor region are configured to provide an optical waveguide.

10

11. The electrical termination structure of claim 9, wherein direct current (DC) blocking is provided by the p-i-n diode.

15

12. The electrical termination structure of claim 1, wherein the first insulating trench is filled with an insulating polymer.

20

13. The electrical termination structure of claim 1, wherein the second insulating trench is filled with an insulating polymer.

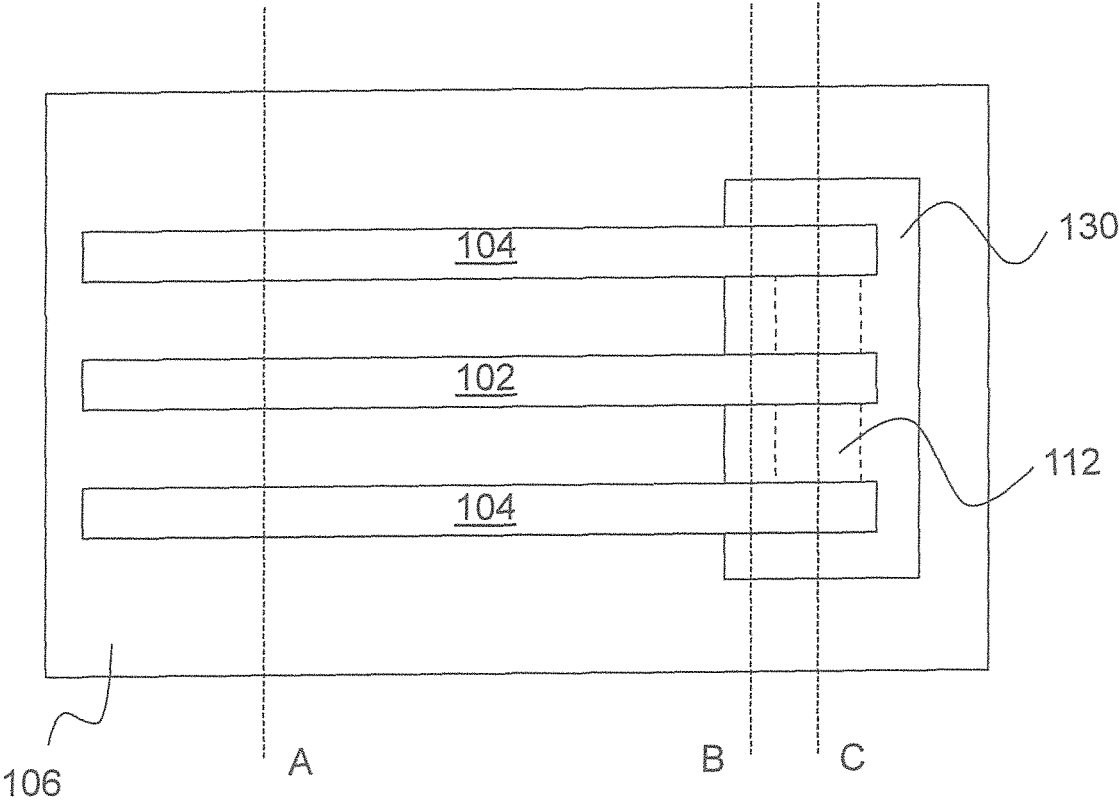


FIG. 1

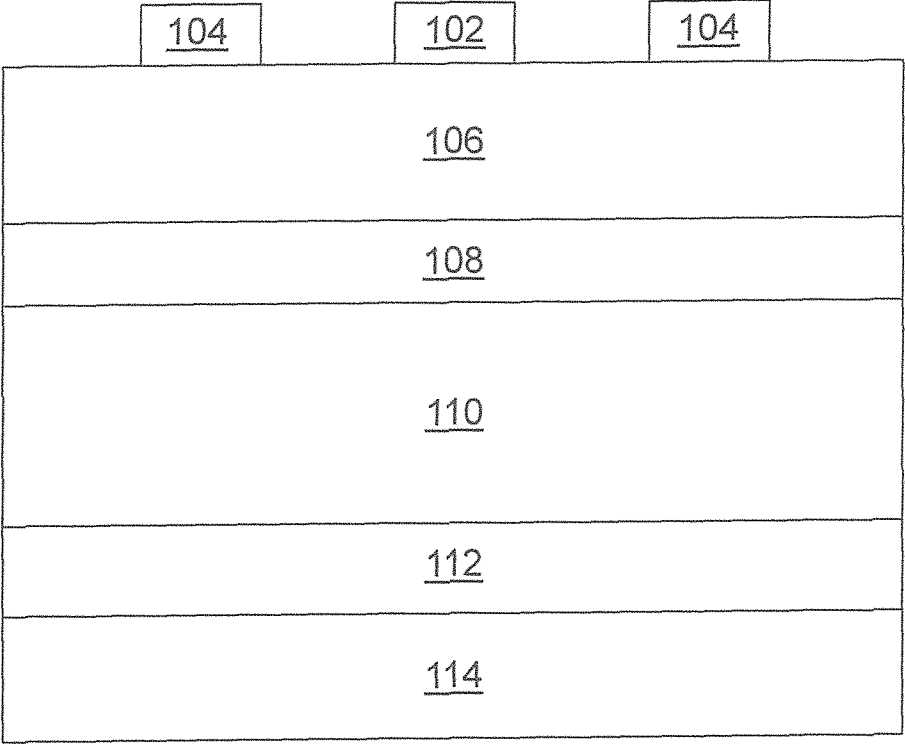


FIG. 1A

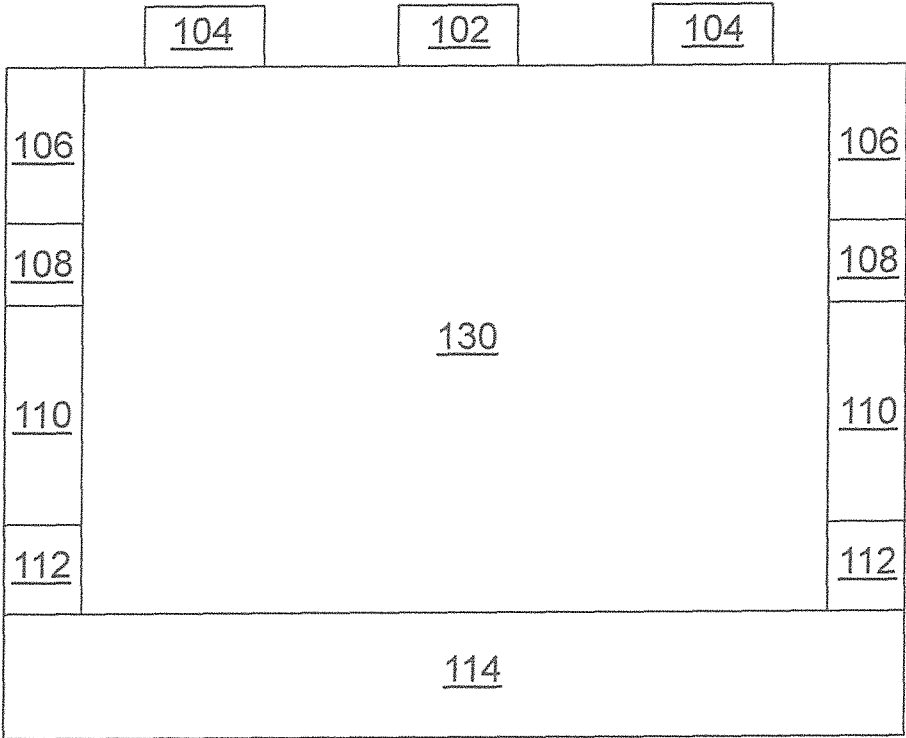


FIG. 1B

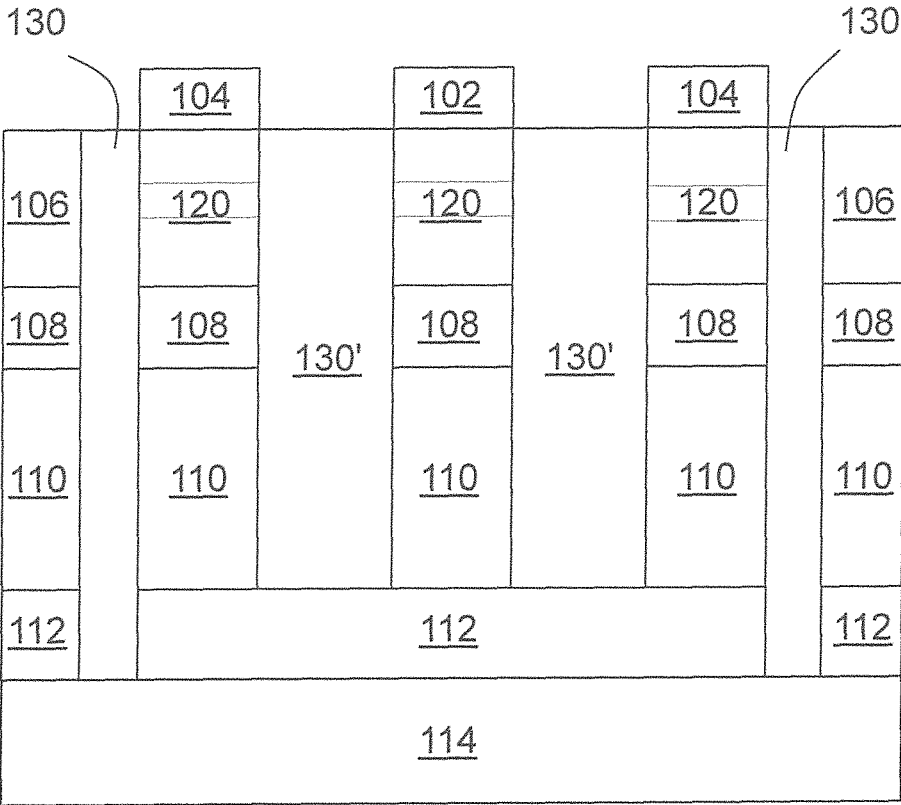


FIG. 1C

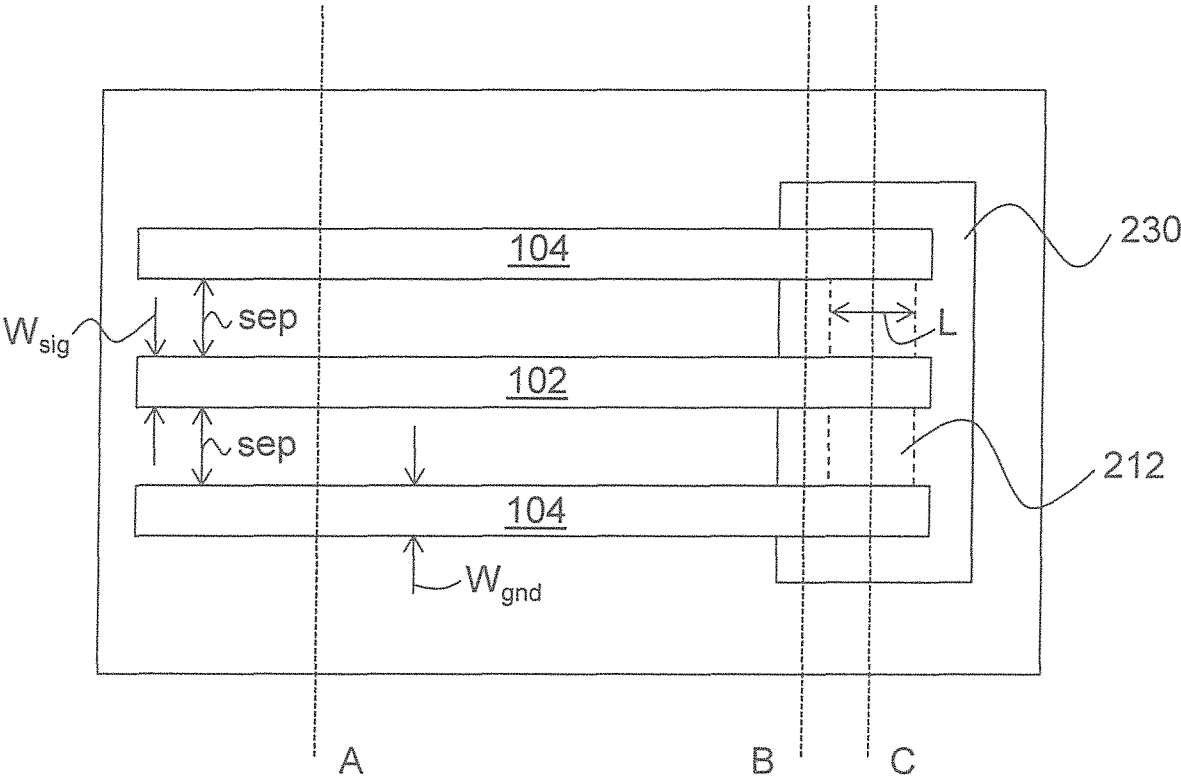


FIG. 2

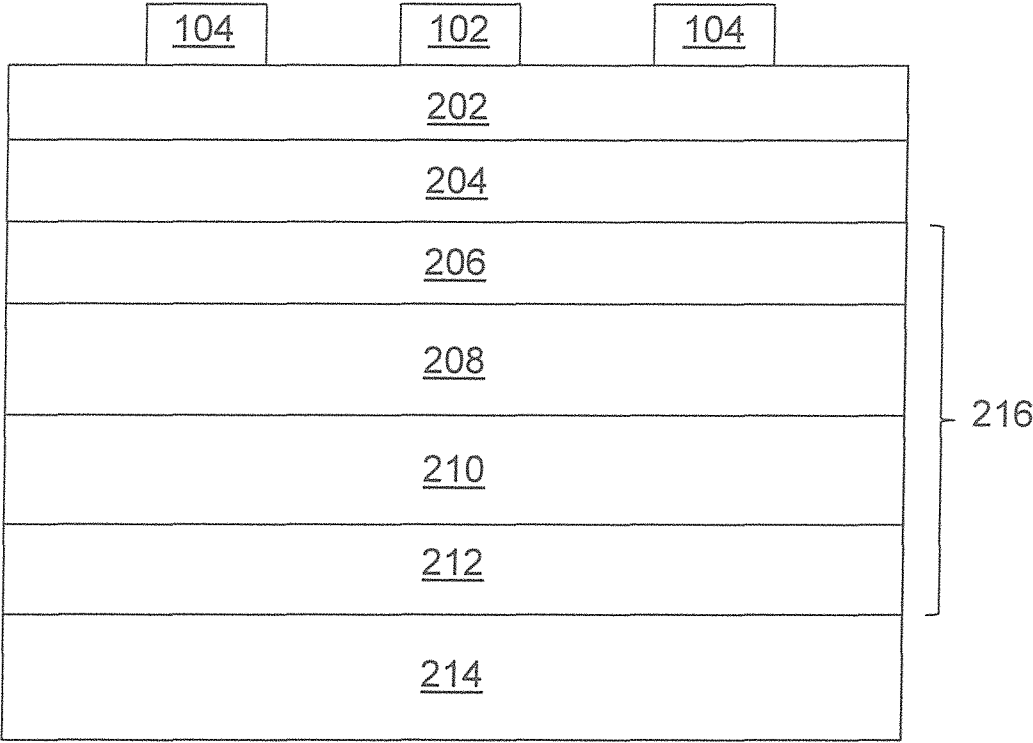


FIG. 2A

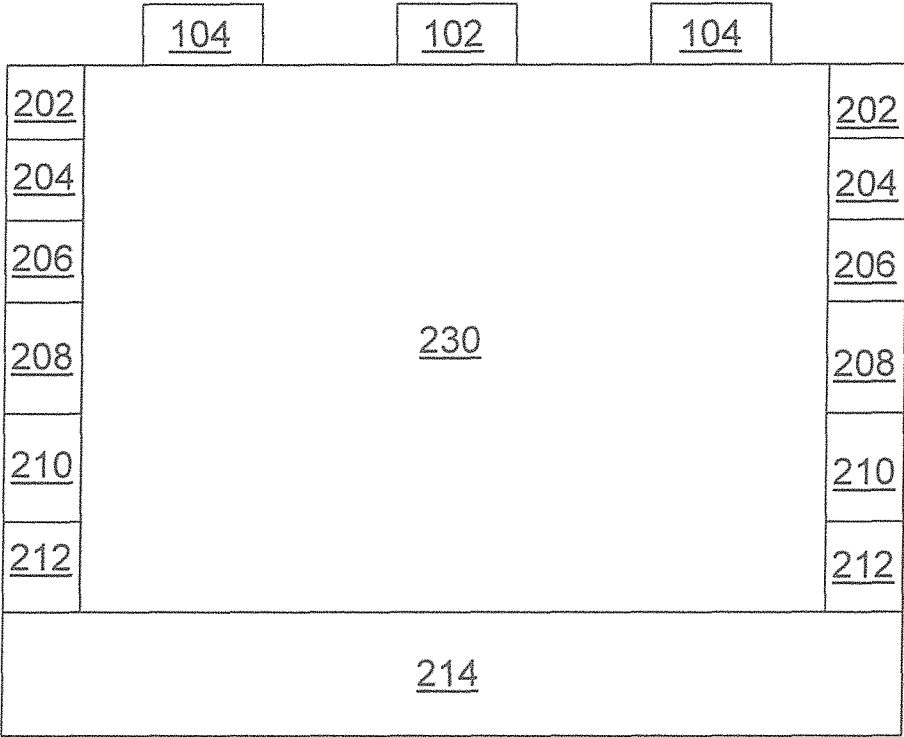


FIG. 2B

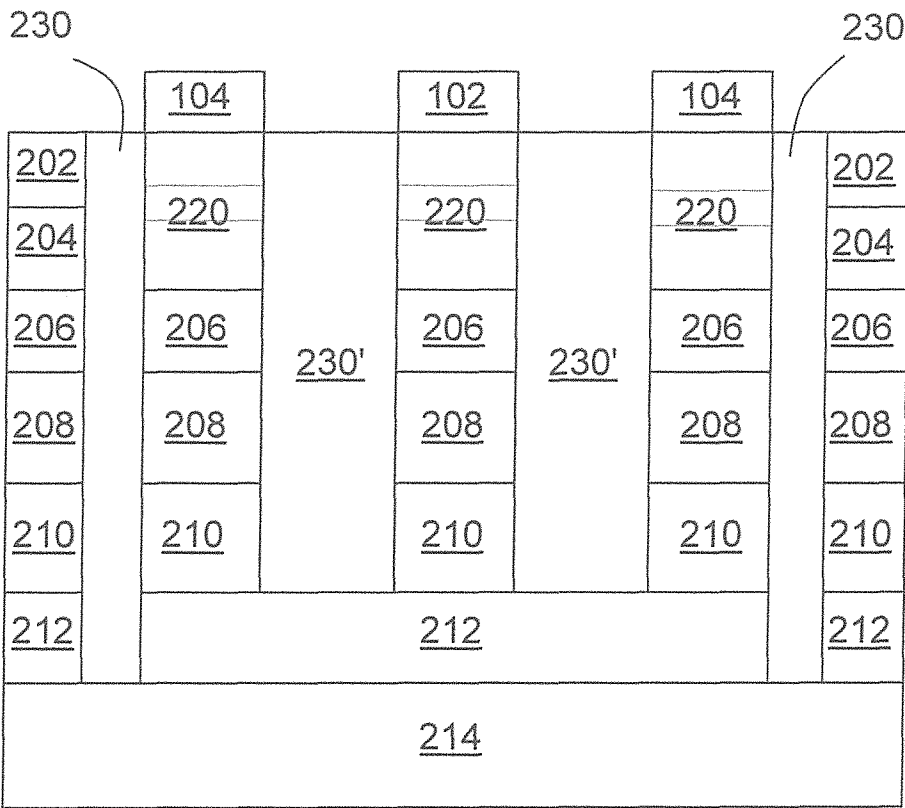


FIG. 2C

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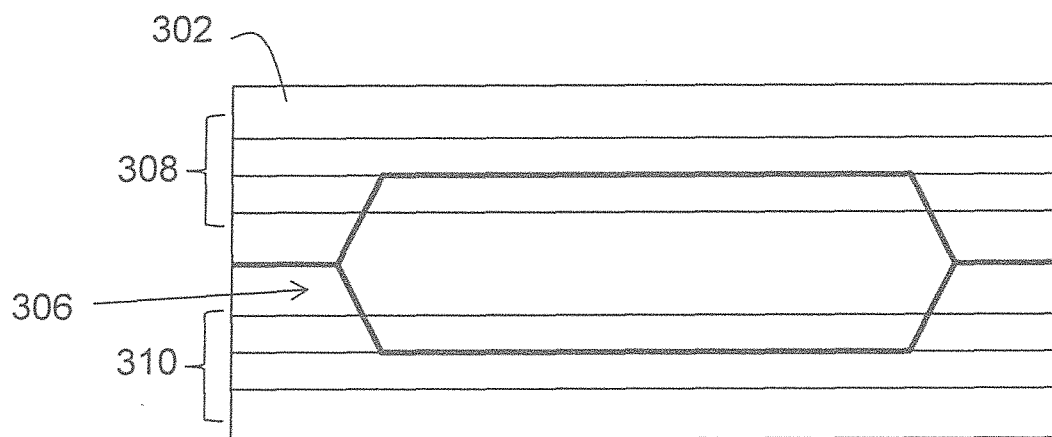


FIG. 3A

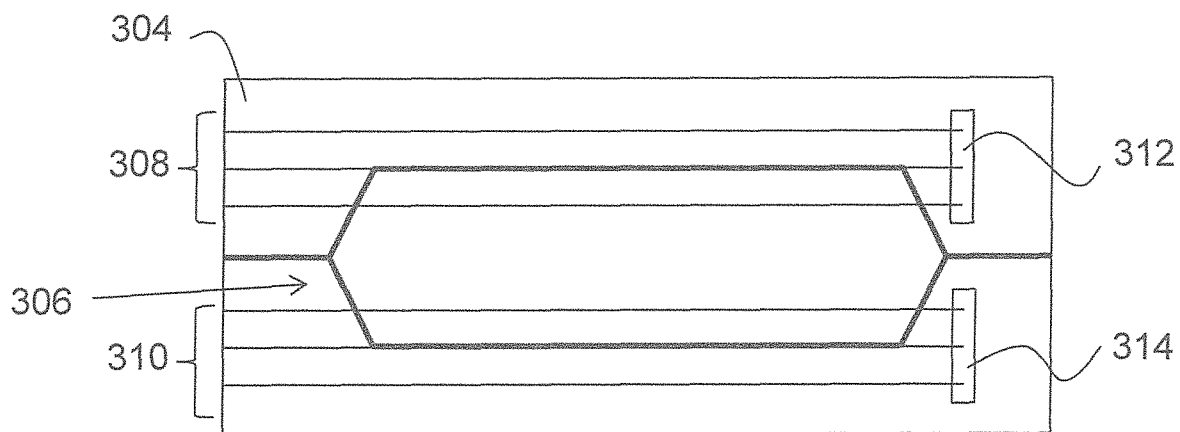


FIG. 3B

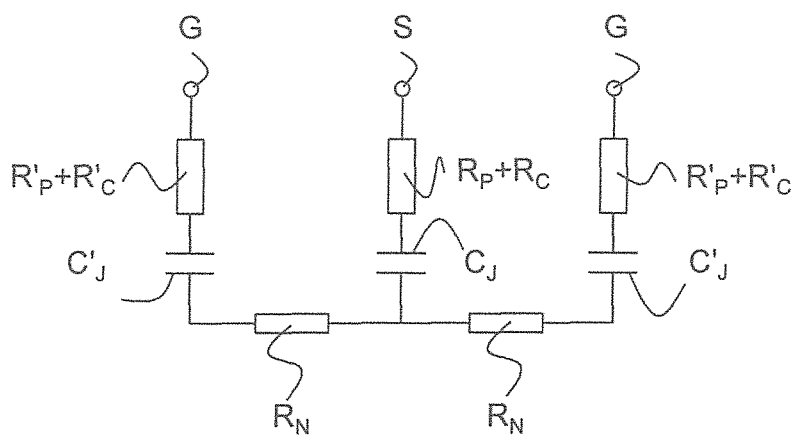


FIG. 4

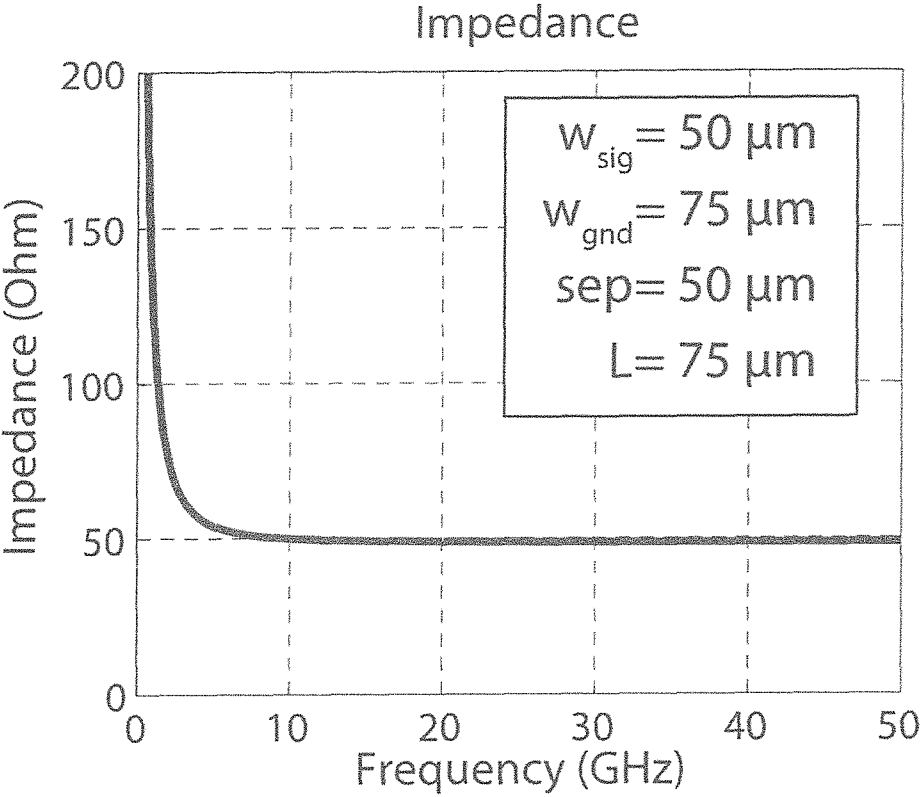


FIG. 5

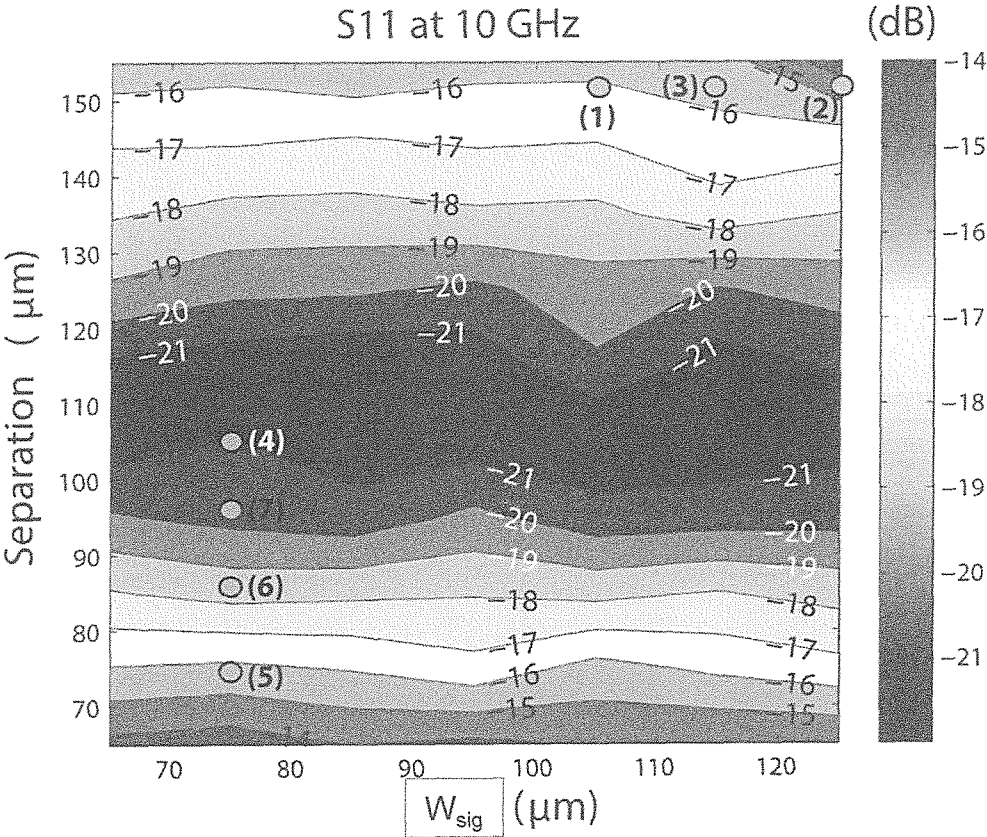


FIG. 6

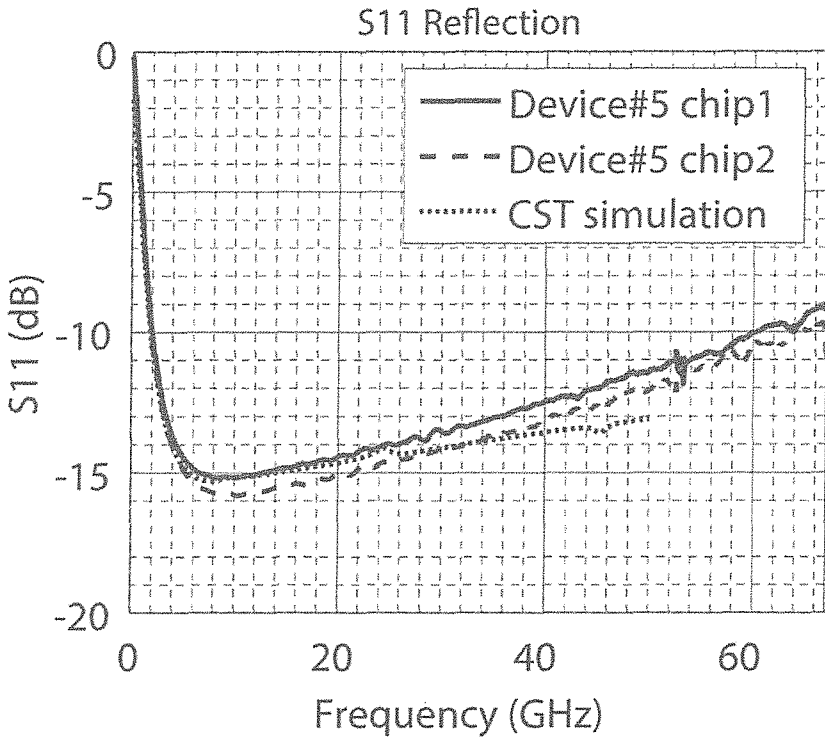


FIG. 7A

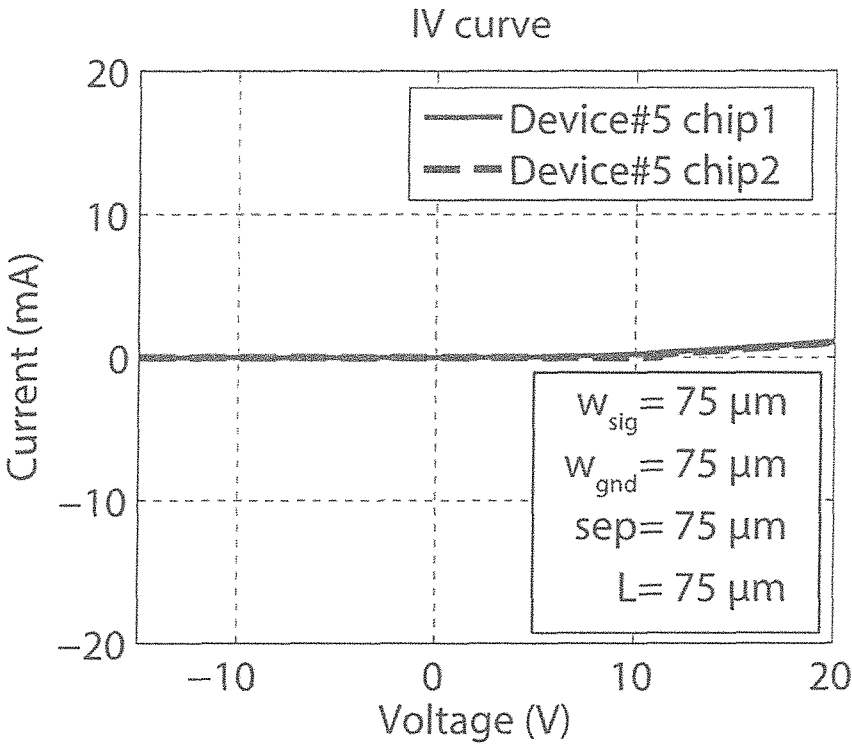


FIG. 7B

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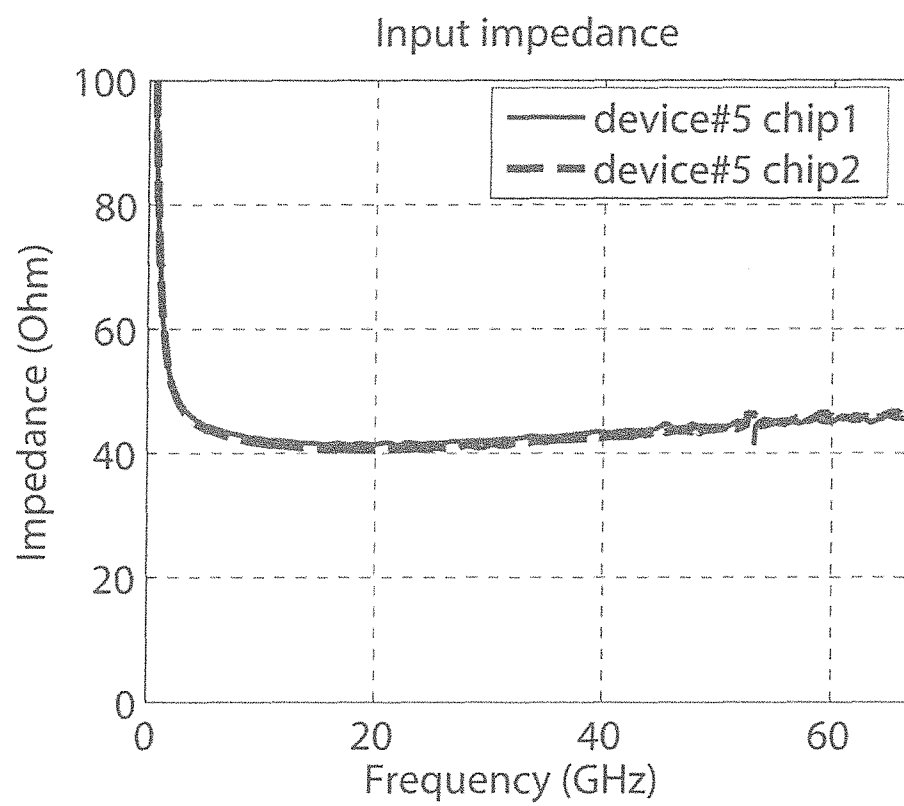


FIG. 7C

# INTERNATIONAL SEARCH REPORT

International application No  
PCT/EP2016/076686

## A. CLASSIFICATION OF SUBJECT MATTER

INV. G02F1/01 G02F1/025 G02F1/225 H01L23/66  
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G02F H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, COMPENDEX, INSPEC, WPI Data

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                                                                                                                                                                                                                                                   | Relevant to claim No. |
|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| A         | MATTHEW M. DUMMER ET AL:<br>"Selectively-undercut traveling-wave<br>electroabsorption modulators incorporating<br>a p-InGaAs contact layer",<br>OPTICS EXPRESS,<br>vol. 16, no. 25,<br>8 December 2008 (2008-12-08), pages<br>20388-20394, XP055337178,<br>ISSN: 2161-2072, DOI: 10.1364/OE.16.020388<br>section 4;<br>figure 4<br><br>-----<br>-/-- | 1-13                  |



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

24 January 2017

Date of mailing of the international search report

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                                                                                                                                                                                                                                                                                                                                                          | Relevant to claim No. |
|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
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