

[54] CONTROL APPARATUS FOR SUPPLYING
OPERATING POTENTIALS

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[22] Filed: Dec. 8, 1972
[21] Appl. No.: 313,448

[52] U.S. Cl. 315/169 TV, 315/169 R
[51] Int. Cl. H05b 37/00
[58] Field of Search..... 315/169 R, 169 TV

[56] References Cited
UNITED STATES PATENTS

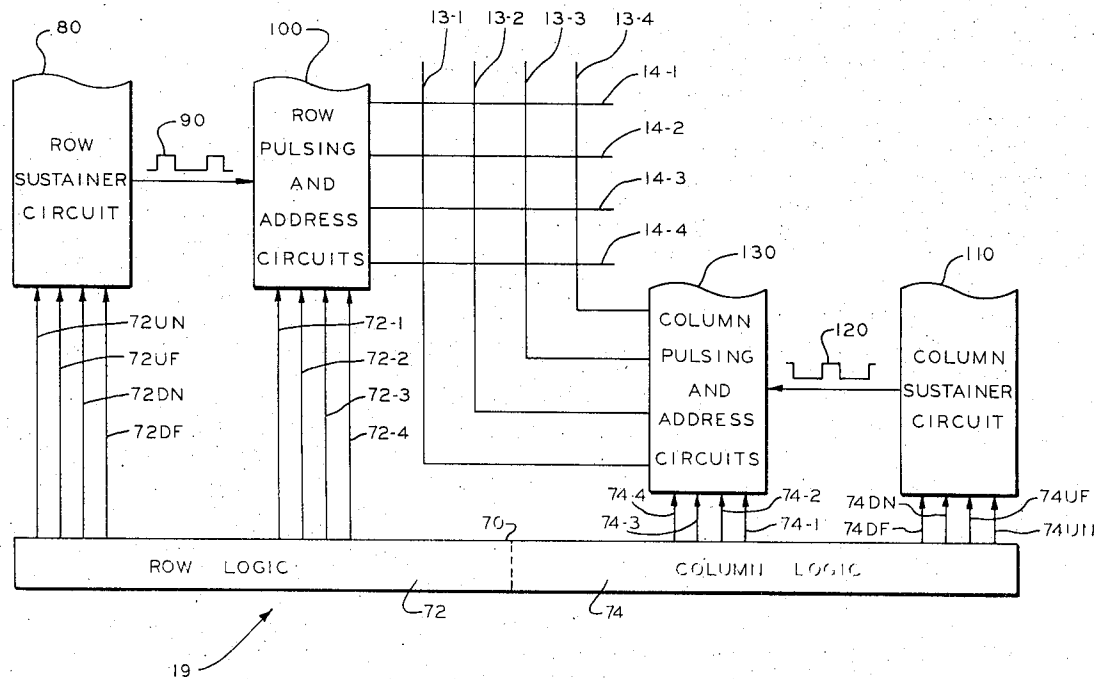
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[57] ABSTRACT

There is disclosed a system for supplying operating potentials which is particularly useful with load devices wherein at least two transversely oriented conductors are dielectrically isolated from a gaseous discharge medium between the conductors. The system utilizes wave form generators for supplying sustainer potentials and an addressing matrix for combining manipulating pulses with the sustainer potentials. Novel transistor-diode clamping means are provided to reverse bias the collector-base junctions of output transistors in the addressing circuits which are normally driven to a saturated condition except when a particular discharge site is being addressed. The reverse bias system is used to provide a reverse bias signal, in series opposition with the continuously applied turn-on signal, which will both bring the transistor out of saturation and turn it off quickly.

5 Claims, 4 Drawing Figures



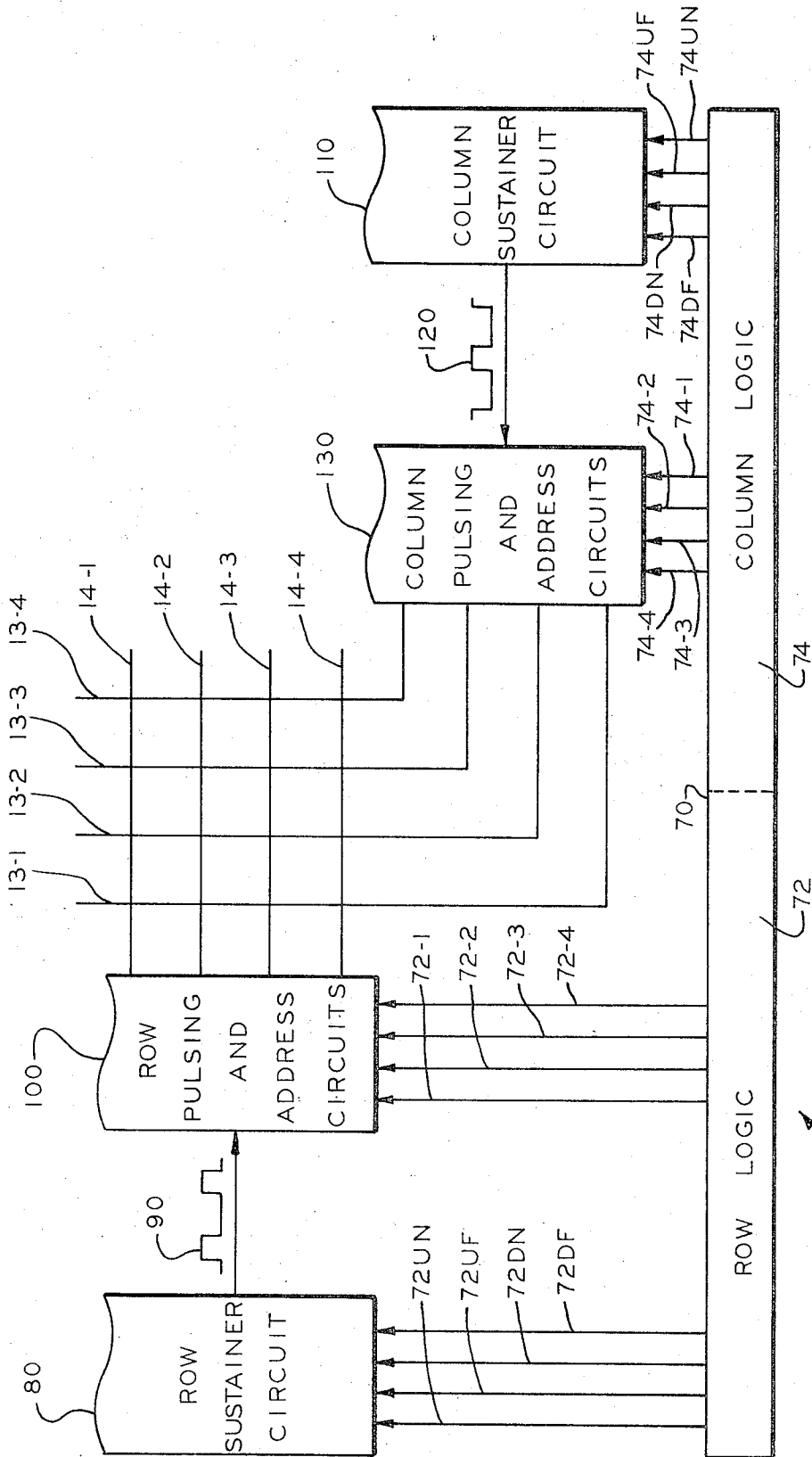


FIG. 3

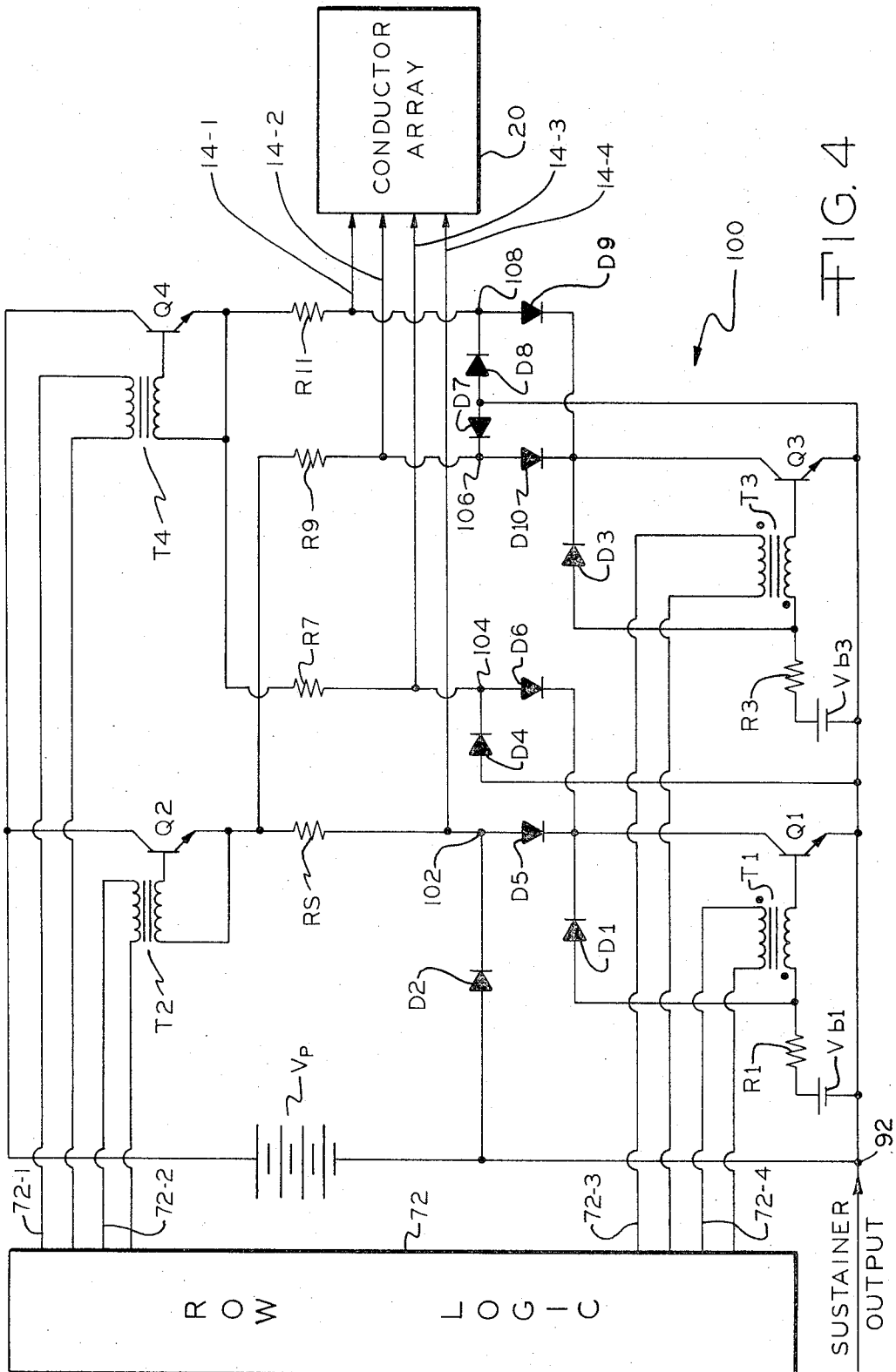


FIG. 4

CONTROL APPARATUS FOR SUPPLYING OPERATING POTENTIALS

BACKGROUND OF THE INVENTION

In the Baker, et al. U.S. Pat. No. 3,499,167, issued Mar. 3, 1970, there is disclosed a multiple discharge display and/or memory panel which may be characterized as being of the pulsing discharge type having a gaseous medium, usually a mixture of two gases at a relatively high gas pressure in a thin gas chamber or space between opposed dielectric charge storage members which are backed by conductor arrays. The conductor arrays backing each dielectric member are transversely oriented to define or locate a plurality of discrete discharge volumes or sites and constitute a discrete discharge unit. In some cases, the discharge units may be additionally defined by physical structures such as perforated glass plates and the like and in other cases capillary tubes and like structures may be used. In the above-identified patent application of Baker, et al., physical barriers and isolation members for discrete discharge sites have been eliminated. In such devices charges (electrons and ions) produced upon ionization of the gas at a selected discharge site or conductor crosspoint, when proper operating potentials are applied to selected conductors thereof, are stored upon the surface of the dielectric at the selected locations or sites and constitute an electrical field opposing the electrical field which created them. After a firing potential has been applied to initiate a discharge, the electrical field created by the charges stored upon the dielectric members aids in initiating subsequent momentary or pulsing discharges on succeeding half cycles of an applied sustaining potential so that the applied potential, and hence the storage charges indicate the previous discharge condition of a discharge unit or site and can constitute an electrical memory.

In dynamic operation, in addition to the sustaining voltages, writing and erasing pulses may be superimposed on and algebraically added to the sustaining wave forms applied to selected transverse conductor pairs in the conductor arrays to manipulate discharge conditions of discharges sites. Some of the preferred types of circuits for supplying the sustaining potentials, and for generating the manipulating pulses to be added to the sustaining potentials, utilize output transistors which are driven into deep saturation to abruptly switch the wave form from one potential level to another. Difficulties have been encountered in the past, in that when a transistor is turned "on" and driven into deep saturation, it is difficult to bring the transistor out of saturation and turn it "off" quickly. If, to prevent this problem, less driving current is applied to the transistor then control of the shape of the leading and trailing edges of the wave form is difficult, it may interfere with the proper addition or subtraction of manipulating pulses, etc., and is undesirable. Clamping circuits, using diodes alone, have been proposed and are useful in certain applications for bringing the transistor out of saturation within the time limits of those applications. However, as switching speeds increase and as the type of wave forms applied as sustaining potentials and as manipulating pulses become more complex, the diode clamping circuit is not suitable for all applications.

Accordingly, it is an object of this invention to provide an improved system for supplying operating poten-

tials to load devices, particularly wherein the load devices are of the gas discharge display/memory type.

It is another object of this invention to provide improved voltage wave form generating means particularly useful in pulsing and addressing circuits for gas discharge display/ memory devices.

It is a further object of this invention to provide improved control apparatus for transistors in which novel transformer-diode clamping means may be utilized to bring a normally "on" transistor out of saturation and permit the transistor to be turned "off" more quickly.

SUMMARY OF THE INVENTION

The invention is disclosed and described herein in a system for supplying operating potentials to a gas discharge display/memory device of the type described hereinbefore. There is shown a load sustaining potential having at least two different potential levels being applied to one of the transverse conductors of the load device via a parallel path having at least two branches. A first branch of the path has a first unidirectional device connected therein for permitting current flow in a first direction along the path. A second branch has a second unidirectional device connected therein for permitting current flow in a second direction along the path. A load signal potential is applied across the end connections of the parallel path.

A transistor means having an emitter-collector circuit is connected in one of the branches of the parallel path, to permit current flow in the same direction as the unidirectional device in that branch, to control current flow in the branch. Means are provided for applying a turn-on signal to a base electrode of the transistor, the signal having a magnitude which is sufficient to drive the transistor into saturation and allow current flow through the emitter-collector circuit.

Means are provided for establishing a reverse bias on the collector-base junction of the transistor including means for applying a reverse bias signal to the base electrode of the transistor, isolating rectifier means, and means for connecting a reverse bias source to the reverse bias applying means. The isolating rectifier is connected to prevent current flow between the collector electrode and the base electrode in response to potential differences establishing a forward bias across the collector-base junction, while permitting flow of current from the reverse bias signal across the collector-base junction in a reverse direction to discharge the minority carriers from the saturated junction and to enable the transistor to turn "off" quickly.

The reverse bias applying means may include a transformer having primary and secondary windings. The secondary winding is connected to the base electrode of the transistor, and the primary winding is connected to receive current from the reverse bias source and induce a reverse bias signal on the secondary winding. In the embodiment shown the secondary winding is connected in series with the turn-on signal.

In the embodiment shown in the drawings the turn-on signal is applied continuously. The reverse bias signal is then applied to the base electrode in series opposition to the turn-on signal and has a magnitude sufficient to inhibit application of a resultant turn-on signal to the transistors. As shown herein the secondary winding is connected in series with the turn-on signal being applied to the base electrode of the transistor.

The means for applying a load signal potential may include means for selectively applying pulses to the end connections of the parallel path. As noted, the means for applying a turn-on signal to a base electrode may include means for continuously supplying a turn-on signal to the base electrode which has a magnitude sufficient to drive the transistor into deep saturation.

The means for establishing a reverse bias on the collector-base junction of the transistor may then further include means for selectively applying the reverse bias signal to the base electrode after a load signal pulse has been initiated and for terminating the reverse bias signal before the termination of the load signal pulse. The reverse bias signal has a polarity and a magnitude sufficient to inhibit application of the resultant turn-on signal to the base electrode thereby rapidly bringing transistor out of saturation and turning it off. The termination of the reverse bias signal allows the transistor to be rapidly driven back into saturation. There is thus provided a load signal pulse, which is particularly useful as a manipulating pulse for changing the discharge state of an individual cell, which has steep leading and trailing edges for combination with sustaining potential wave forms.

The reverse bias establishing means disclosed herein may be generically described as having at least one of the primary and secondary windings connected in a circuit across the collector-base junction of the output transistor with the isolating rectifier means. The isolating rectifier means is connected to prevent current flow between a collector electrode and a base electrode of the transistor through windings of the transformer in response to potential differences establishing a forward bias across the collector-base junction. The primary winding of the transformer is generically described as being connected to receive from a reverse bias source which will induce a potential on the secondary winding which will cause current flow through the isolating rectifier in a forward direction and through the collector-base junction in a direction to reverse bias the collector-base junction and discharge the minority carriers from the saturated junction to enable the transistor to turn "off" quickly.

Other objects, features, and advantages will become apparent from the following description when taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a partially cut-away plan view of a gaseous discharge display/memory panel as connected to a diagrammatically illustrated source of operating potentials;

FIG. 2 is a cross-sectional view (enlarged, but not to proportional scale since the thickness of the gas volume, dielectric members and conductor arrays have been enlarged for purposes of illustration) taken on lines 2 — 2 of FIG. 1;

FIG. 3 is a diagrammatic layout of a system for supplying sustaining and manipulating voltages for a gaseous discharge display/memory panel; and

FIG. 4 is a schematic diagram of a circuit embodying the teachings of this invention for supplying manipulating pulses to the row conductors of the panel.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The gaseous discharge display/memory device, as fully disclosed in the hereinbefore referenced Baker, et

al. patent, utilizes a pair of dielectric films 10 and 11 shown in FIGS. 1 and 2 as separated by a thin layer or volume of a gaseous discharge medium 12, the medium 12 producing a copious supply of charges (ions and electrons) which are alternately collectable on the surfaces of the dielectric members at opposed or facing elemental or discrete areas X and Y defined by the conductor matrix on non-gas-contacting sides of the dielectric members, each dielectric member presenting large open surface areas and a plurality of pairs of elemental X and Y areas. While the electrically operative structural members such as the dielectric members 10 and 11 and conductor matrixes 13 and 14 are all relatively thin (being exaggerated in thickness in FIGS. 1 and 2) they are formed on and supported by rigid non-conductive support members 16 and 17 respectively.

Typically, one or both of nonconductive support members 16 and 17 pass light produced by discharge in the elemental gas volumes. Usually, they are transparent glass members and these members essentially define the overall thickness and strength of the panel. For example, the thickness of gas layer 12 as determined by spacer 15 is usually under 10 mils and typically about 4 to 6 mils, dielectric layers 10 and 11 (over the conductors at the elemental or discrete X and Y areas) are usually between 1 and 2 mils thick; and conductors 13 and 14 about 8,000 angstroms thick. However, support members 16 and 17 are much thicker (particularly in large panels) so as to provide as much ruggedness as may be desired to compensate for stresses in the panel. Support members 16 and 17 also serve as heat sinks for heat generated by discharges and thus minimize the effect of temperature on operation of the device. If it is desired that only the memory function be utilized, then none of the members need be transparent to light.

Except for being nonconductive or good insulators the electrical properties of support members 16 and 17 are not critical. The main function of support members 16 and 17 is to provide mechanical support and strength for the entire panel, particularly with respect to pressure differential acting on the panel and thermal shock. As noted earlier, they should have thermal expansion characteristics substantially matching the thermal expansion characteristics of dielectric layers 10 and 11. Ordinary ¼ inches commercial grade soda lime plate glasses have been used for this purpose. Other glasses such as low expansion glasses or transparent devitrified glasses can be used provided they can withstand processing and have expansion characteristics substantially matching expansion characteristics of the dielectric coatings 10 and 11. For given pressure differentials and thickness of plates, the stress and deflection of plates may be determined by following standard stress and strain formulas (see R. J. Roark, Formulas for Stress and Strain, McGraw-Hill, 1954).

Spacer 15 may be made of the same glass material as dielectric films 10 and 11 and may be an integral rib formed on one of the dielectric members and fused to the other members to form a bakeable hermetic seal enclosing and confining the ionizable gas volume 12. However, a separate final hermetic seal may be effected by a high strength devitrified glass sealant 15S. Tubulation 18 is provided for exhausting the space between dielectric members 10 and 11 and filling that space with the volume of ionizable gas. For large panels small bead-like solder glass spacers such as shown at

15B may be located between conductor intersections and fused to dielectric members 10 and 11 to aid in withstanding stress on the panel and maintain uniformity of thickness of gas volume 12.

Conductor arrays 13 and 14 may be formed on support members 16 and 17 by a number of well-known processes, such as photoetching, vacuum deposition, stencil screening, etc. In one embodiment, the center-to-center spacing of conductors in the respective arrays is about 17 mils. Transparent or semi-transparent conductive material such as tin oxide, gold or aluminum can be used to form the conductor arrays and should have a resistance less than about 1,000 ohms per linear inch of conductor line, usually less than about 50 ohms per inch. Narrow opaque electrodes may alternately be used so that discharge light passes around the edges of the electrodes to the viewer. It is important to select a conductor material that is not attacked during processing by the dielectric material.

It will be appreciated that conductor arrays 13 and 14 may be wires or filaments of copper, gold, silver or aluminum or any other conductive metal or material. For example 1 mil wire filaments are commercially available and may be used in the invention. However, formed in situ conductor arrays are preferred since they may be more easily and uniformly placed on and adhered to the support plates 16 and 17.

Dielectric layer members 10 and 11 are formed of an inorganic material and are preferably formed in situ as an adherent film or coating which is not chemically or physically effected during bake-out of the panel. One such material is a solder glass such as Kimble SG-68 manufactured by and commercially available from the assignee of the present invention.

This glass has thermal expansion characteristics substantially matching the thermal expansion characteristics of certain soda-lime glasses, and can be used as the dielectric layer when the support members 16 and 17 are soda-lime glass plates. Dielectric layers 10 and 11 must be smooth and have a dielectric strength of about 1,000 volts per mil and be electrically homogeneous on a microscopic scale (e.g., no cracks, bubbles, crystals, dirt, surface films, etc.) In addition, the surfaces of dielectric layers 10 and 11 should be good photoemitters of electrons in a baked-out condition. Alternatively, dielectric layers 10 and 11 may be overcoated with materials designed to produce good electron emission, as in U.S. Pat. No. 3,634,719, issued to Roger E. Ernsthausen. Of course, for an optical display at least one of dielectric layers 10 and 11 should pass light generated on discharge and be transparent or translucent and, preferably, both layers are optically transparent.

The preferred spacing between surfaces of the dielectric films is about 4 to 6 mils with conductor arrays 13 and 14 having center-to-center spacing of about 17 mils.

The ends of conductors 14-1 . . . 14-4 and support member 17 extend beyond the enclosed gas volume 12 and are exposed for the purpose of making electrical connection to interface and addressing circuitry 19. Likewise, the ends of conductors 13-1 . . . 13-4 on support member 16 extend beyond the enclosed gas volume 12 and are exposed for the purpose of making electrical connection to interface and addressing circuitry 19.

As described in detail in the Baker, et al. U.S. Pat. No. 3,499,167, the entire gas volume can be initially conditioned for subsequent operation at substantially uniform firing potentials by the use of internal or external radiation to supply free electrons throughout the gas medium 12.

Normal operation of a panel of the type described herein will be described with reference to FIGS. 1, 2, and 3, the interfacing and addressing circuit indicated generally at 19 in FIG. 1 being shown in more detail in FIG. 3. Potentials having the wave forms 90 and 120 as shown in FIG. 3 are supplied from row and column sustainer circuit generators 80, 110 via row and column pulsing and addressing circuits 100, 130 to conductor arrays 14, 13 in response to control pulses from row and column sections 72, 74, respectively of the logic control circuit 70. The resultant or composite potential wave form appearing across each cell is indicated at 140 in FIG. 3 as a periodic wave form of an alternating character. The wave form 140 is derived for the purpose of analysis of the operation of the panel by assuming that the wave forms 90 and 120 are spaced 180° apart or arc oppositely phased within the cycles of the periodic composite wave form 140, and that the wave form 120 is subtracted from the wave form 90.

In the examples set forth in FIG. 3, the wave form 90 is a square wave with a duration of less than one-half of the cycle defined by the composite wave form 140 and with a magnitude of +Vcc. Thus, more than 180° of the cycle of the composite wave form 140 elapses between occurrences. The wave form 120 is a square wave with a duration of less than one-half of the cycle defined by the composite wave form 140, and with a magnitude of +Vcc, since the sustainer 110 may be identical to the sustainer 80. The logic inputs to the sustainers 80 and 110 are phased 180° apart with respect to the cycle of the composite wave form 140. Therefore the positive wave 120 is produced when the positive wave 90 is not being produced. When the positive wave form 120 is subtracted from the positive wave form 90, the wave form 120 appears to be negative in the composite wave form 140.

The voltage 90 from sustainer 80 constitutes approximately one-half of the sustaining voltage necessary to operate the panel, the remaining ½ which is necessary being supplied by voltage 120 phased 180° as noted above with respect to the voltage 90. Thus, ½ of the sustainer potential 140 is applied to each of the row conductors 14 and ½ of the sustainer potential 140 is applied to each of the column conductors 13. The sustainer circuits 80 and 110 advantageously have a common ground so that the panel 10 floats with respect to ground.

Individual cells or discharge sites located by the crossing of selected conductors or conductor arrays 14, 13 are manipulated by algebraically adding unidirectional voltage pulses at the proper time to each of the sustaining voltages on the selected conductors, which, when combined, are sufficient to exceed the firing potential for the selected cells and to initiate a sequence of discharges, one for each half-cycle of the applied composite sustaining potential 140. By also properly timing such unidirectional voltage pulses and applying them at a different portion in a cycle of the composite sustaining potential 140 to each of the sustaining voltages on the selected conductors, the sequence of discharges may be terminated. Thus, any individual dis-

charge site may be manipulated "ON" or "OFF," by manipulation of the times of occurrences of the unidirectional voltage pulses.

The unidirectional voltage pulses are algebraically added to the sustainer voltages 90, 120 on the selected conductors by the row and column pulsing and addressing circuits 100, 130 in response to logic signals from the logic control circuit 70 via leads 72-1 through 72-4 and 74-1 through 74-4, respectively, to select the conductor pairs for the individual cells.

The circuits for generating the unidirectional voltage pulses for manipulating the discharge conditions of individual cells or sites usually utilize output power transistors in a switching mode. In the specific embodiment shown in the drawings, the transistor is connected to at least one, and usually more, of the conductors in a selection matrix. The transistors are normally "on" and are turned "off" only when a pulse output for a particular conductor is desired.

It is desirable to be able to turn the power transistors "on" and "off" as quickly as possible so that the transition slope in the wave form being controlled is as steep as possible. To turn a power transistor "on" quickly it is necessary to drive it with a comparatively large current pulse which will drive the transistor into deep saturation. The further the transistor is driven into saturation, the smaller the internal resistance will be to the circuit it is controlling. This decrease in internal resistance is an important factor in being able to properly operate lighted display/memory devices of the type described herein because of the high current demand.

Difficulties have been encountered, however, in that when the transistor is driven into deep saturation to reduce the wave form alternation to and below a desired level, it takes a longer time to turn the transistor "off." This decreases the slope of the wave form being produced and may delay or slow a voltage transition to a point which will interfere with proper panel operation. Moreover, this effectively decreases the width of an output pulse.

Referring now to FIG. 4 there is illustrated in detail a schematic diagram of the row pulsing and address circuit 100 of FIG. 3 to provide unidirectional manipulating pulses for the conductors 14 of the gaseous discharge display/memory unit indicated at 20. A similar circuit may be used to produce manipulating pulses for the circuit 130 and the column conductors 13.

A sustainer output from the row sustainer circuit 80 having the wave form indicated at 90 in FIG. 3 is received at an input terminal 92 of the row pulsing and address circuit 100. The sustaining potential 90 has two different operating levels and, when applied to individual intersections of the conductors in conjunction with the wave form 120 from the column sustainer circuit 110, the composite wave form 140 is seen by each individual cell or discharge site.

The input terminal 92 is connected to each end of a row conductor by a parallel path having two branches. A first branch of the parallel path has a first rectifier or unidirectional device connected therein for permitting current flow in a first direction. A second branch has a second unidirectional device connected therein for permitting current flow in the opposite or second direction.

Thus, as shown in FIG. 4 the terminal 92 is connected to the terminal 102 at the end of a row conductor 14-4 by a first branch of a parallel path which includes diode

D2 conducting in a first direction, and by a second branch of the parallel path which includes diode D5 conducting in a second direction and the collector-emitter circuit of the power transistor Q1. Similarly, the terminal 92 is connected to the terminal 104 of the conductor 14-3 by a first branch which includes diode D4 conducting in a first direction, and a second branch which includes diode D6 conducting in the second direction and the collector-emitter circuit of the transistor Q1. The terminal 92 is connected to the terminal 106 of the conductor 14-2 by a first branch which includes a diode D7 conducting in a first direction, and a second branch which includes diode D10 conducting in a second direction and the collector-emitter circuit of the transistor Q3. The terminal 92 is connected to the terminal 108 of the conductor 14-1 by the first branch of a parallel path which includes a diode D8 conducting in the first direction, and a second branch of the parallel path which includes diode D9 conducting in a second direction and the collector-emitter circuit of the transistor Q3.

Means are provided for applying a load signal potential across the end connections of each of the parallel paths. A voltage source V_p is connected across the ends 92, 102 of the parallel path for the conductor 14-4 via the collector-emitter circuit of the transistor Q2 and a resistor R5. The voltage source V_p is connected across the ends 92, 104 for the row conductor 14-3 via the collector-emitter circuit of the transistor Q4 and the resistor R7. The voltage V_p is connected across the ends 92, 106 of the path to the conductor 14-2 via the emitter-collector circuit of the transistor Q2 and the resistor R9. The voltage V_p is connected across the ends 92, 108 of the parallel path of the row conductor 14-1 via the collector-emitter circuit of the transistor Q4 and the resistor R11.

As noted in the description above the load signal applying transistors Q2 and Q4 may serve more than one conductor. Similarly, the transistors Q1 and Q3 which control the voltage is applied to a conductor, may serve more than one conductor. In a normal operation the transistors Q2, Q4 are normally "off" and are pulsed on upon receipt of signals via leads 72-2 and 72-1 from the row logic control unit 72. The transistors Q1 and Q3 are biased by voltage sources V_{b1} , V_{b3} through resistors R1, R3, respectively, to be normally "on." Turn-off signals are supplied to the transistors Q1, Q3 through leads 72-4 and 72-3 from the row logic unit 72.

In operation, in order to address a particular conductor and apply a unidirectional pulse thereto one of the load signal applying transistors Q2, Q4 must be turned "on" while one of the voltage controlling transistors Q1, Q3 must be turned "off." For example, assume that it is desired to algebraically add a manipulating pulse to the sustainer output connected to the terminal 92 for the row conductor 14-4. A turn-on signal is supplied from the row logic unit 72 via the lead 72-2 to the transformer T2 to turn the transistor Q2 "on." Voltage from the source V_p will be connected through the now-conducting emitter-collector circuit of the transistor Q2 to the pairs of end terminals 92, 102 and 92, 106. However, at this point in time both of the voltage controlling transistors Q1 and Q3 are still saturated so the application of the voltage from V_p to the pairs of terminals 92, 102 and 92, 106 has no effect.

Simultaneously with the initiation of the voltage pulse through the transistor Q2 a turn-off signal is supplied on lead 72-4 to the primary winding of the transformer T1 connected to the base electrode of the transistor Q1. A turn-off signal, which is also a reverse bias signal as will be explained hereinafter, is induced on the secondary winding of the transformer T1 with a polarity which is opposite to the polarity of the voltage and current supplied by the turn-on signal from the source Vb1, and with a magnitude which is greater than the turn-on signal from Vb1. The resultant signal at the base of Q1 is negative and the transistor Q1 is turned off.

Thus, the branch of the parallel path between the terminals 102 and 92 via the diode D5 can no longer conduct and the voltage from the source Vp appears across the terminals 92, 102 of the parallel path since the other diode D2 in the other branch is reverse biased by the voltage Vp.

The signal on the lead 72-4 is terminated along with the termination of the signal on the lead 72-2 so that, with the novel transformer-diode clamping circuit arrangement herein, a unidirectional, manipulating voltage pulse may be selectively initiated and terminated.

The novel reverse bias circuit of this invention for the collector-base junction of the transistor Q1 includes the transformer T1 having primary and secondary windings for applying a reverse bias signal to the base electrode, isolating rectifier means D1, and means for connecting a reverse bias source to the reverse bias applying means, the latter including the row logic unit 72 and the lead 72-4 from the unit 72 to the primary winding of the transformer T1.

The isolating rectifier D1 is connected to prevent current flow between the collector electrode and the base electrode in response to potential differences that would establish a forward bias across the base-emitter junction. The isolating rectifier D1 permits flow of current from the reverse bias signal supplied across the collector-base junction by the secondary winding of the transformer T1 to discharge the minority carriers from the saturated junction to enable the transistor Q1 to turn "off" quickly.

In operation, then, the means for applying a load signal potential may include means for selectively applying pulses to the end connections of the parallel path. The means for applying a turn-on signal to a base electrode of the transistor Q1 includes the voltage source Vb1, which continuously supplies a turn-on signal to the base electrode and which has a magnitude sufficient to drive the transistor Q1 into deep saturation.

Means for establishing a reverse bias on the collector-base junction of the transistor Q1 includes means for selectively applying a turn-off signal to the base electrode after a load signal pulse has been initiated, and for terminating the turn-off signal before the termination of the load signal pulse. The turn-off signal also acts as the reverse bias signal in this instance, and has a polarity and magnitude sufficient to inhibit application of a resultant turn-on signal to the base electrode, thereby rapidly bringing the transistor Q1 out of saturation and turning it "off." The termination of the turn-off (reverse bias) signal allows the transistor to be rapidly driven back into deep saturation. Therefore, a unidirectional load signal pulse of longer time duration is

produced for combination with the sustaining potential 90 on the conductor 14-4.

The conductors 14-1 through 14-3 are similarly supplied with unidirectional voltage pulses by the remaining circuitry which is identical in operation to that just described.

The novel control apparatus, including the novel transformer-diode clamping means, has been shown as particularly useful with a turn-on signal which is continuous. However, it should be noted that the novel circuit is also useful in different applications where the turn-on signal is selectively, rather than continuously, applied to the transistors.

In the specific circuit shown the voltage Vb1 represents means for continuously supplying a turn-on signal to the base electrode of the transistor Q1, the signal having a magnitude sufficient to drive the transistor into deep saturation and allow current flow through the collector-emitter circuit. It is obvious, however, that the turn-on signal may be intermittent, or be selectively, or otherwise discontinuously applied to the base electrode.

The novel transformer-diode clamping is then useful to bring the transistor Q1 out of saturation and the reverse bias signal need not be of sufficient magnitude to overcome a continuously applied turn-on signal. For example, if the turn-on signal in the circuit layout illustrated in FIG. 4 were selective rather than continuous, then after a turn-on signal to the base electrode has been removed a reverse bias signal may be induced by the primary winding of the transformer T1 on the secondary of the transformer T1. This would cause a current flow in the forward direction through the diode D1 to being the collector-base junction out of saturation. As noted above, the reverse bias signal induced on the secondary winding of D1 in this instance would not have to have the magnitude of a "turn-off" signal necessary if the circuit it used with a continuous turn-on signal as shown in FIG. 4.

There has thus been described and disclosed novel apparatus for producing improved manipulating pulses. A novel transformer-diode clamping circuit may be used to turn output power transistors "off" after, or even during, a heavy turn-on driving current to the transistor. This enables the transistor to be turned "off" in a fraction of the normal storage time for such devices. It also enables an addressing and pulsing circuit performance which meets and matches the very fast switching speed and high current requirements of display/memory panels now being developed, and to improve the performance of prior art panels.

What is claimed is:

1. In a system for supplying operating potentials to a load device wherein at least two transversely oriented conductors are dielectrically isolated from a gas discharge medium between said two conductors, comprising

a. means for applying a load sustaining potential having at least two different potential levels to one of the transverse conductors including a parallel path having at least two branches, a first branch having a first unidirectional device connected therein for permitting current flow in a first direction, a second branch having a second unidirectional device connected therein for permitting current flow in a second direction;

- b. means for applying a load signal potential across the end connections of said parallel path;
 - c. transistor means having a base-emitter junction, a collector-base junction, a collector electrode, a base electrode, and an emitter-electrode and having an emitter-collector circuit connected in one of said branches to permit current flow in the same direction as the unidirectional device in that branch so as to control current flow in said one branch;
 - d. means for applying a turn-on signal to the base-emitter junction of the transistor means having a magnitude which is sufficient to drive said transistor means into saturation and allow current flow through the emitter-collector circuit thereof; and
 - e. means for establishing a reverse bias on the collector-base junction of said transistor means including means for applying a reverse bias signal to said base-emitter junction, isolating diode means connected to prevent current flow between the collector electrode and the base electrode of the transistor means in response to collector potentials that would establish a forward bias across said base-emitter junction and permitting flow of current from said reverse bias signal across said collector-base junction in a reverse direction to discharge the minority carriers from said saturated junction to enable said transistor means to turn off quickly, and means for connecting a reverse bias source to said reverse bias applying means.
2. A system as defined in claim 1 in which
- a. said reverse bias applying means includes a transformer having primary and secondary windings,
 - b. said secondary winding being connected to said base electrode of said transistor means, and said primary winding being connected to receive current from said reverse bias source and induce a reverse bias signal on said secondary winding.
3. A system as defined in claim 1 in which
- a. said means for applying a load signal potential includes means for selectively applying pulses to the end connections of said parallel path, and in which
 - b. said means for applying a turn-on signal to a base electrode of said transistor means includes means for continuously supplying a turn-on signal to said base electrode which has a magnitude sufficient to drive said transistor means into deep saturation, and in which
 - c. said means for establishing a reverse bias on the collector-base junction of said transistor means includes means for selectively applying said reverse bias signal to said base electrode after a load signal pulse has been initiated and for terminating said reverse bias signal before the termination of said load signal pulses, with the reverse bias signal having a polarity and a magnitude sufficient to inhibit application of a resultant turn-on signal to said base electrode thereby rapidly bringing said transistor means out of saturation and turning it off, the termination of said reverse bias signal allowing the transistor to be rapidly driven back into saturation,

- thus providing a load signal pulse having steep leading and trailing edges for combination with said sustaining potential.
4. In a system for supplying operating potential to a load device wherein at least two transversely oriented conductors are dielectrically isolated from a gaseous discharge medium between said two conductors, comprising
- a. voltage wave form generating means adapted to be connected to a transverse conductor;
 - b. said voltage wave form generating means including means for applying a potential to said transverse conductor, and transistor means having a base-emitter junction, a collector-base junction, a collector electrode, a base electrode, and an emitter-electrode and having an emitter-collector circuit connected to said conductor for controlling the applied potential;
 - c. means for applying a turn-on signal to the base-emitter junction of the transistor means having a magnitude sufficient to drive said transistor into saturation; and
 - d. means for establishing a reverse bias on the collector-base junction of said transistor means including means for applying a reverse bias signal to said base-emitter junction, isolating diode means connected to prevent current flow between the collector and base electrodes in response to potential differences that would establish a forward bias across said base-emitter junction and permitting flow of current from said reverse bias signal across said collector-base junction in a reverse direction to discharge the minority carriers from the saturated junction to enable said transistor means to turn off quickly, and means for connecting a reverse bias source to said reverse bias applying means.
5. A system as defined in claim 4 in which
- a. said means for applying a potential includes means for selectively applying pulses to said transverse conductor; and in which
 - b. said means for applying a turn-on signal to a base electrode of said transistor means includes means for continuously supplying turn-on signal to said base electrode which has a magnitude sufficient to drive said transistor means into deep saturation; and in which
 - c. said means for establishing a reverse bias on the collector-base junction of said transistor means includes means for selectively applying said reverse bias signal to said base electrode after a potential pulse has been initiated and for terminating said reverse bias signal before the termination of said potential pulse, with the reverse bias signal having a polarity and a magnitude sufficient to inhibit application of a resultant turn-on signal to said base electrode thereby rapidly bringing said transistor means out of saturation and turning it off, the termination of said reverse bias signal allowing the transistor to be rapidly driven back into saturation, thus providing a resultant potential pulse on said conductor having steep leading and trailing edges.
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