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(54) **Title:** METHOD FOR DIGITIZING AN ANALOGUE SIGNAL FOR FURTHER DEMODULATION IN A RADIO RECEIVING DEVICE

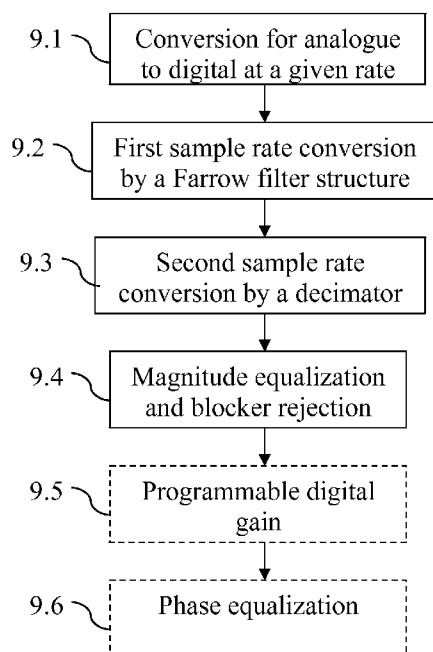


Fig. 9

(57) **Abstract:** The invention proposes a digital receiving architecture wherein the sample rate converter is designed based on a first stage consisting of a Farrow structure followed by a decimator. This way, it is possible to use the same decimator for a given RAT mode regardless the actual ADC sample rates. The Farrow structure compensates for ADC sampling rate variations by delivering data at a fixed rate at the decimator. Considering that the distortion is introduced by the decimator and not the Farrow structure as long as the latter is used in a reasonable range of conversion ratio, the potentially high number of configurations that have to be taken into account by the equalization stage is considerably reduced.



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Method for digitizing an analogue signal for further demodulation in a radio receiving device

5 The present invention generally relates to radio receiving devices and more particularly to reconfigurable receiving digital data path architecture with flexible input/output sampling rates. It relates to the digital design of the receiving segment comprising rate conversion, filtering and gain operations between the analogue to digital conversion and the modem.

10 Fig. 1 illustrates the receiving part of a wireless mobile device 1.1. It contains radio-frequency integrated circuit 1.2. A signal from antenna 1.3 passes duplex filter 1.4 and low-noise amplifier 1.5.

After conversion to baseband by mixer 1.6, the signal is filtered by analogue baseband filter 1.8 and digitized by analogue to digital converter (ADC) 1.9.

15 The sampling rate of ADC 1.9 depends on the input signal bandwidth and on radio-frequency performance requirements. Therefore, a resampling stage 1.10 implements a variable bitrate conversion resulting in a signal at a fixed output rate for the modem 1.12.

Equalizer 1.11 compensates linear distortion introduced by both analogue stages and digital stages and especially by the bitrate conversion, and the resulting signal is passed to the modem 1.12.

5 An opposite path exists from the modem to the antenna for emission. The emitting chain is not described in here. We concentrate in this document on the receiving chain.

Today, the number of mobile Radio Access Technologies (RAT) corresponding to different standards is growing rapidly, which creates a demand for versatile hardware able to adapt to a large number of RATs preserving size and consumption advantages, in comparison to software processing. For handling this diversity, it is possible to increase number of receiving chains for the different RATs, but advantageously the different receiving chains share as many hardware modules as possible.

For each RAT, the design of the receiving chain should take into account different modes. Each of these modes fixes the sample bitrate at the input of the modem. For example, considering the 3G RAT (3rd generation mobile telecommunications, such as 3G FDD, 3G TD-SCDMA or 4G with 6 different bandwidth modes (1.4, 3, 5, 10, 15, 20 MHz)), the sample rate depends on the number of cells corresponding to the mode, in example single-cell, dual-cell, tri-cell mode.

20 The ADC sampling rate (or equivalently output rate) is determined by both the used RAT mode and radio-frequency performance requirements. For example Local oscillator and ADC sampling rate generate RF spurious tones liable to fall back into in-band signal. By adjusting these block parameters the damaging effect can be mitigated. The range of possible sample rates is not very large and the actual value used for a given RAT mode depends on the radio frequency performance requirements.

Considering this, each mode within each RAT determines a given sample rate at the output of the ADC and the target sample rate at the input of the modem. Thus, it determines the ratio of the sample rate converter to bring the sample stream at the output of the ADC to the target sample rate at the input of the modem.

30 Rate conversion is classically performed by Poly-phase, CIC (Cascaded integrator-Comb) or Farrow structure with the drawback of generating potentially as many different spectrum magnitude shapes as the rate conversion parameterization

changes. These distortions should be compensated by the equalization. The equalization is typically performed by FIR (Finite Impulse Response) filters.

5 Multiplying the number of RATs that the receiver is able to receive leads to a combinatorial multiplication of the number of filters that should be implemented to handle all these distortions. *A priori* one different filter configuration is required for each combination of ADC sampling rate and RAT mode. This is rendering the design of modern and flexible radio receiving chain complex.

10 The invention aims at solving these problems by a digital receiving architecture wherein the sample rate converter is designed based on a first stage consisting of a Farrow structure followed by a decimator. This way, it is possible to use the same decimator for a given RAT mode regardless the actual ADC sample rates. The Farrow structure compensates for ADC sampling rate variations by delivering data at a fixed rate at the decimator. Considering that the distortion is introduced by the decimator and not the Farrow structure as long as the latter is used in a reasonable range of conversion ratio, the potentially high number of configurations that have to be taken into account by the equalization stage is considerably reduced.

The invention concerns a method for digitizing an analogue signal for further demodulation in a radio receiving device, said method causing the device to perform:

- 20 - converting the analogue signal to a digital signal at a sample rate using an analogue to digital converter;
- applying to the digital signal a first sample rate conversion by a Farrow structure to bring the sample rate to an intermediate sample rate;
- applying to the digital signal sampled at the intermediate sample rate a second sample rate conversion by a decimator to bring the signal from the intermediate sample rate to a target sample rate required by the demodulation;
- 25 - filtering the digital signal for magnitude equalization and/or blocker rejection.

The invention concerns also a method for configuring a sample rate converter in a reconfigurable receiving digital data path within a radio receiving device, said method causing the device to perform:

- 30 - determining a sample rate of an analogue to digital converter depending on radio-frequency performance requirements;
- determining a target sample rate required for demodulation;
- determining a conversion ratio to configure the sample rate converter comprising a Farrow structure and a decimator to convert a sample rate of a signal

provided by the analogue to digital converter to the target sample rate required for modulation;

- obtaining a conversion ratio of the Farrow structure to convert the sample rate of the ADC to an intermediate sample rate for further rate conversion by the decimator;

- obtaining a conversion ratio of the decimator to convert the intermediate sample rate to the target sample rate required for modulation.

The invention concerns also a radio receiving device for digitizing an analogue signal for further demodulation, the device comprising circuitry causing the device to implement:

- means for converting the analogue signal to a digital signal at a sample rate using an analogue to digital converter;
- means for applying to the digital signal a first sample rate conversion by a Farrow structure to bring the sample rate to an intermediate sample rate;
- means for applying to the digital signal sampled at the intermediate sample rate a second sample rate conversion by a decimator to bring the signal from the intermediate sample rate to the target sample rate required by the demodulation;
- means for filtering the digital signal for magnitude equalization and/or blocker rejection.

The invention concerns also a radio receiving device for configuring a sample rate converter in a reconfigurable receiving digital data path within a radio receiving device, the device comprising circuitry causing the device to implement:

- means for determining a sample rate of an analogue to digital converter depending on radio-frequency performance requirements;
- means for determining a target sample rate required for demodulation;
- means for determining a conversion ratio to configure the sample rate converter comprising a Farrow structure and a decimator to convert a sample rate of a signal provided by the analogue to digital converter to the target sample rate required for modulation;
- means for obtaining a conversion ratio of the Farrow structure to convert the sample rate of the ADC to an intermediate sample rate for further rate conversion by the decimator;
- means for obtaining a conversion ratio of the decimator to convert the intermediate sample rate to the target sample rate required for modulation.

The present invention also concerns, in at least one embodiment, a computer program that can be downloaded from a communication network and/or stored on a medium that can be read by a computer or a processing device. This computer program comprises instructions for causing implementation of the aforementioned method, or any of its embodiments, when said program is run by a processor.

The present invention also concerns an information storage means, storing a computer program comprising a set of instructions causing implementation of the aforementioned method, or any of its embodiments, when the stored information is read from said information storage means and run by a processor.

The characteristics of the invention will emerge more clearly from a reading of the following description of an example embodiment, the said description being produced with reference to the accompanying drawings, among which:

Fig. 1 illustrates the receiving part of a wireless mobile device.

Fig. 2 illustrates the architecture of the proposed digital receiving chain according to a particular embodiment of the invention.

Fig. 3 illustrates the Farrow frequency responses according to a particular embodiment of the invention.

Fig. 4 illustrates the Farrow frequency responses according to a particular embodiment of the invention, it is a detail of the preceding figure.

Fig. 5 illustrates the method to configure the sample rate converter in a reconfigurable receiving digital data path according to a particular embodiment of the invention.

Fig. 6 illustrates an order 5 Lagrange Interpolation based Farrow structure according to a particular embodiment of the invention.

Fig. 7 illustrates a possible implementation of the CIC decimator.

Fig. 8 schematically represents an architecture of a receiver device in which the present invention may be implemented.

Fig. 9 illustrates the method to digitize the analogue signal for demodulation.

Fig. 2 illustrates the architecture of the proposed digital receiving chain. The first block 2.1 consists in the analogue filter bank. It receives the baseband signal. This filtered signal enters then the analogue to digital converter ADC (2.2). The core of the invention comes from the rate converter following the ADC. According to the invention, the rate converter first applies a Farrow structure based rate conversion 2.3

followed by a decimator stage 2.4. Prior art usually does the opposite and does first a decimation followed by a fine adjustment by a poly-phase or Farrow structure. The sample rate converter 2.3 and 2.4 is followed by a stage 2.5 comprising a magnitude equalizer and/or blocker rejection filter. The signal is then amplified by the programmable digital gain 2.6 followed by a filter for phase equalization 2.7. Then the signal is ready to be demodulated by the modem.

To come back to the sample rate converter, it is typically built using two stages. Given an input sample rate, let's call it F , and a target output sample rate, let's call it F' , the target conversion ratio is given by F'/F . To achieve this ratio several known sample rate converter types that can be used.

Some coarse grain rate converters are known. An exemplary coarse grain rate converter is a CIC (Cascaded integrator-Comb) converter, known for example from document "An Economical Class of Digital Filters for Decimation and Interpolation" by Eugene B. HOGENAUER in IEEE TRANSACTIONS ON ACOUSTICS, SPEECH, AND SIGNAL PROCESSING, VOL. ASSP-29, NO. 2, APRIL 1981. The CIC is able to apply a conversion ratio expressed by a ratio U/D where U and D are integer values. The value of U is typically 1 or 2 while the value of D is typically between 1 and several tens.

The decimator stage 2.5 is advantageously implemented as a CIC for flexibility, but it could be something else, such as a FIR filter implemented as a decimator. The invention is not limited to the use of CIC as a decimator.

Another example of a sample rate converter is a Farrow structure that is able to apply a conversion ratio close to unity. The Farrow structure could be seen as a fine grain rate converter. It is a multi-rate filter structure which offers the option of continuously adjustable resample ratio. Several Farrow structures are known in the art. The one we used in this example preserves the in-band signal spectrum flatness. It is based on Lagrange interpolation, but a Hermite interpolation based Farrow structure could also work.

The rate conversion should also take into account aliases that are introduced in the receiving chain. Typically three sources of aliases could be present in the signal. The first source comes from the input signal. This is due to the fact that the rate conversion is basically an up-sampling stage followed by a down-sampling stage. The up-sampling stage brings some replica of the input signal at frequencies multiple of the input frequencies, while the down-sampling stage fold these replicas over in band.

A second source of alias comes from quantization noise. This noise is due to the truncation operations performed on the digitized signal. A third source of alias comes from blockers. Blockers are strong interference signals in a frequency band close to the useful band of the input signal. When present in the signal, the rate conversion will introduce some aliases of these blockers within the signal.

In the prior art, the decimator is always used before a Farrow structure. The target rate conversion is approached by the decimator, the Farrow structure being used to adjust the rate conversion to the exact target value. These modules are used in this order because the decimator is known to allow the resolution of aliases problems.

A thorough analysis of the behaviour of a rate converter based on a Farrow structure stage followed by a decimator stage as proposed by the invention leads to the conclusion that this solution allows to reduce the complexity of equalization needed to correct the distortion due to the rate conversion.

Furthermore, in some embodiment, the proposed architecture allows to take care of the three kinds of aliases produced. This is the case if the Farrow structure conversion ratio is kept in a range close to one.

There is an innovative association of Lagrange Interpolation-based Farrow and a decimator, advantageously a CIC, which extends the ADC capabilities with the following properties.

The first property is that an arbitrary sampling rate is affordable while aliases of input signal and quantization noise are controlled.

Let's consider the rate conversion operated by a Farrow-based structure as depicted on Fig. 3.

The unit of the horizontal axis is the input sampling frequency of the Farrow structure 2.3 and the horizontal axis represents the power of samples expressed in dB. In the up-sampling phase, input signal spectral replicas are centred on the multiples of the input sampling frequency of the Farrow structure 2.3, say F , and fall in the notches of the filter associated to the specific Farrow structure. Therefore, when aliased in the down-sampling phase, *i.e* translated at the output frequency of the Farrow structure 2.3, say F' , the resulting contributions interfering with the input signal, spectrally centred on 0, are attenuated. And the narrower the input signal bandwidth, the stronger the attenuation. As could be seen on Fig. 3, an input band $B=F/2$, thus being half the input sampling frequency, ensures around 40dB minimum attenuation on the first replica for an order 5 Lagrange interpolation based Farrow structure.

When the output frequency F' is significantly lower than the input frequency F , the quantization noise in the spectrum range $[F', F]$ is weakly filtered and the down-sampling phase translates it around the frequency 0 potentially interfering strongly with the input signal. As an example, in for an order 5 case, with a conversion ratio
5 larger than 0.6 for the quantization noise alias contribution is 16dB below the initial contribution.

Another property of the proposed architecture is the in-band spectrum insensitivity toward ADC sampling rate changes.

With this structure, the in-band input signal spectrum remains mostly unchanged
10 when the ADC output frequency is varying.

Indeed, if we consider an order 5 Farrow structure and an input signal of bandwidth B less than 0.42 times the ADC output frequency, Fig. 4 shows that the spectrum distortion is at most 0.1 dB on the edges. It allows a fixed Farrow output rate with ADC frequency variations (typically +/- 10%) without signal spectrum
15 modification.

Therefore any fixed final rate F' can be achieved with a fluctuating ADC output frequency, using a cascade of Farrow with fluctuating conversion ratio and fixed CIC. And the resulting spectrum modification is fixed since, as recalled above, the CIC filtering spectrum shape depends on the output frequency F' , the decimation factor
20 and the order.

The converse combination consisting of a CIC followed by Lagrange Interpolation-Based Farrow does not have obviously this property.

What is achieved by the proposed architecture is a sample rate converter where the coarse grain decimator is fixed for a given RAT mode, which implies that the
25 equalization which is needed is also fixed for a given RAT mode. The variation in the ADC output frequency due to radio-frequency performance requirements are compensated by the Farrow structure 2.3 with no modification of the decimator 2.4.

Therefore the potentially high number of configurations to be equalized is greatly reduced. The number of equalization filters to be implemented is reduced
30 leading to a much simpler implementation.

The proposed solution has also the benefit that it introduces only small cumulated group delay. The rate change is done without phase distortion, due to linear-phase filtering, and at the expense of a small group delay. Let T_{in} the Farrow

structure input period and T_{out} the CIC decimator output period. The delay groups associated to Farrow and CIC stages can be calculated respectively:

$$T_G^{Farrow} = \left(\frac{Order + 1}{2} \right) T_{in};$$

$$T_G^{CIC} = \left(\frac{N \left(1 - \frac{1}{D} \right)}{2} \right) T_{out};$$

Where the conversion ratio of the CIC is U/D , $Order$ is the order of the Farrow structure and N is the order of the CIC.

For example, if the order of the Farrow structure order is small, for example equal to 5, largest group delays occur in large decimation cases and are approximated by $\pm N/4 T_{out}$, where T_{out} is the output sampling period.

For example, if the order of the CIC N is typically equal to 2, the group delay is comparable to T_{out} , which is an attractive value.

Above mentioned orders are given as an example of realization, other orders may be used in the present invention.

It has to be noted here that the conversion ratio of the Farrow structure may be predetermined and obtained from non-volatile memory of the receiver device and only the conversion ratio of the decimator is determined or the conversion ratio of the decimator may be predetermined and obtained from non-volatile memory of the receiver device and only the conversion ratio of the Farrow structure is determined or the conversion ratios of the Farrow structure and the decimator are obtained from a table stored in non-volatile memory of the receiver device using the determined conversion ratio of the rate converter as input key or the conversion ratio of the Farrow structure and the conversion ratio of the decimator are determined according to the determined for the sample rate. Regarding synchronization, the Farrow-based rate conversion structure 2.3 allows fractional sampling, as well as CIC with coarser accuracy, which provides a re-synchronization with arbitrary time offset. With a conversion ratio $\eta_{Farrow} = p/q$ and an input sampling period T_{in} , the offset can be set to any multiple of T_{in}/p .

Whereas in the prior art, magnitude and phase equalization are done altogether with asymmetric FIR, the invented structure allows a separate and simplified magnitude and phase filtering.

Advantageously, the magnitude equalizer and blocker rejection filter 2.5 does the magnitude filtering. The in-band spectrum insensitivity toward the ADC sample rate property makes it possible to considerably limit the number of different blocker rejecter and magnitude equalizer designs while extending the RFIC sampling frequency range. Both magnitude equalization and blocker rejection can be performed by the same filter, with suitable filter design. Filter may be designed to satisfy both the in-band constraints for equalization and the out-band constraints for blocker detection or may be designed to satisfy the in-band constraints for equalization or the out-band constraints for blocker detection. Practical design of filters as such is known in the art, and it is therefore not described here in detail.

The phase equalization module 2.7 performs advantageously the phase equalization at a fixed rate. It is possible since phase distortions are only due to analogue impairments, the rate change and magnitude filtering are equivalent to a linear phase filtering, and then induce a fixed group delay, independent of the input frequency, i.e. the ADC sampling rate. The phase equalizer can be switched off, for example, for 2G RAT, in-band phase distortion induced by RF and analogue are negligible and phase equalization is not required.

The programmable digital gain 2.6 is applicable only after the magnitude equalization and blocker rejection module 2.5. It is advantageously applied before phase equalization since it decreases the quantization constraints on the IIR phase equalizer.

The proposed architecture also provides the advantage that the parameterization is completely flexible and the path can be configured by software for any desired Radio Access Technology (RAT). These parameters are typically the rate converters, filter taps, gain tables, etc.

AGC (Automatic Gain Control), DC-offset cancellation, base-band I and Q paths mismatch correction or inter-modulation of order 2 correction function could be added easily to the above described architecture. These functionalities are well known in the art and not drawn for clarity.

Fig. 9 illustrates the method to digitize the analogue signal for demodulation.

In step 9.1, the analogue signal that has advantageously been filtered before, is converted from analogue to digital by the ADC. The digital signal comes out from the ADC with a given sample rates which depends on radio-frequency performance requirements.

In step 9.2, the digital signal is then subject to a first sample rate conversion by a Farrow structure. This rate conversion brings the sample rate to an intermediate sample rate.

5 The intermediate sample rate is for example and in a non limitative way, chosen as the mean value of the ADC sampling rate range.

In step 9.3, the digital signal sampled at the intermediate sample rate is then subject to a second sample rate conversion by a decimator. This second rate conversion brings the digital signal rate from the intermediate sample rate value to the target rate required by the demodulation. This target rate value depends on the RAT
10 mode of the signal transmission.

In step 9.4, the signal is then subject to a magnitude equalization to compensate the distortion due to the rate conversion and/or the signal is filtered for blocker rejection. Blockers are strong interference signals at frequency close to the frequency of the meaningful signal.

15 In step 9.5, optionally, if needed, the signal is then subject to a programmable digital gain to bring the signal to the required level.

In step 9.6, optionally if needed, the signal is then filtered for phase equalization.

The signal is then ready for demodulation by the modem 1.12.

20 Fig. 5 illustrates the method to configure the sample rate converter in a reconfigurable receiving digital data path by determining the distribution of the conversion ratio between the Farrow structure and the decimator. This method is used for the configuration of the reconfigurable receiving data path architecture as defined in this document.

25 In a step 5.1, the ADC sample rate is determined. The ADC sample rate is given by radio-frequency performance requirements, for example spurs.

In a step 5.2, the target sample rate required for demodulation is determined. The target sample rate depends on the RAT mode used. For example, for 3G single-cell mode, a sample rate of 7.68 MHz is required. In a step 5.3, the conversion ratio is
30 determined to configure the sample rate converter comprising a Farrow structure and a decimator to convert a sample rate of a signal provided by the analogue to digital converter to the target sample rate required for modulation.

In a step 5.4, the conversion ratio of the Farrow structure is obtained to convert the sample rate of the analogue to digital converter for further rate conversion by the

decimator. Regarding the implementation of the Farrow structure, it could be advantageously done using an order 5 Lagrange Interpolation based Farrow structure as illustrated on Fig. 6. This implementation is preferable to a poly-phase based implementation because it offers the following properties : the in-band spectrum is flat
 5 as explained above, the coefficients are simple, the control is simple and the size is small, typically 20-25 kGates for order 5.

Advantageously, considering a rate conversion ratio p/q , p and q being positive integers, X_n being the input samples, Y_m being the output samples, the interpolation parameter μ is controlled according to the following pseudo-code:

```

10   counter=0 ;
      while (1)
          load next input  $X_n$ ;
          while (counter < p)
              compute:  $\mu = \text{counter} \cdot (1 / p)$ ;
15          compute and output interpolated sample:  $Y_m$  ;
              counter = counter + q;
          endwhile
      counter = counter - p;
      endwhile
  
```

20

Re-synchronization is performed by setting *counter* value to a desired value. An integer increment Δ on *counter* delays the output signal of $(\frac{\Delta}{p})T_{in}$, where T_{in} is the CIC input sampling period.

25 In a step 5.5, the conversion ratio of the decimator is obtained to convert the intermediate sample rate to the target sample rate required for modulation.

The conversion ratio of the decimator is done by choosing a ratio U/D , with U and D being integers, U being 1 or 2, and D being between 1 and several tens. U and D are chosen to bring the intermediate sample rate to the target sample rate required for modulation.

30

It has to be noted here that the conversion ratio of the Farrow structure may be predetermined and obtained from non-volatile memory of the receiver device and only the conversion ratio of the decimator is determined or the conversion ratio of the decimator may be predetermined and obtained from non-volatile memory of the receiver device and only the conversion ratio of the Farrow structure is determined or

the conversion ratios of the Farrow structure and the decimator are obtained from a table stored in non-volatile memory of the receiver device using the determined conversion ratio of the rate converter as input key or the conversion ratio of the Farrow structure and the conversion ratio of the decimator are determined according to the determined the sample rate(s).

Fig. 7 illustrates a possible implementation of the CIC decimator. The order N is a parameter. Indeed, the “Int/Comb” block 7.1 implements a first block 7.2 for up-sampling by a ratio U , followed by a succession of $N_{max} > N$ integrators 7.3, followed by decimation of factor D 7.4, followed by a succession of $N_{max} > N$ combs 7.5. The hardware easily bypasses part of the N_{max} steps allowing for only N order.

Re-synchronization can be performed in the decimation step by factor D in the “Int/Comb”. The step nominally keeps one data every D data. Every additional skipped data delays the output signal of T_{in}/U , where T_{in} is the input sampling period.

The “Int/Comb” block is followed by a first coarse gain 7.6, typically of a factor of 2^{-S} , S being an integer having the value $\lceil \log_2(G_{CIC}) \rceil$, and where :

$$G_{CIC} = \frac{D^N}{U} = \frac{2^S}{SF}.$$

The fine gain 7.7 having a factor of SF .

The proposed architecture has no disadvantages relating to prior art because it simplifies previous designs dedicated to specific radio features, without adding complexity. It solves the technical problem to reduce the number of equalization filter required to compensate distortion due to the rate conversion. We achieve a reconfigurable receiving data path architecture which adapts to potentially all narrow-band systems.

By keeping the conversion ratio of the Farrow structure within a reasonable conversion ratio range around unity, the three kinds of aliases are controlled. The exact range of conversion ratio of the Farrow structure will depend on the radio technology and the input signal. For example, if strong blockers are present close to the used frequency, the actual range for the Farrow will be narrower than for a signal without blocker. In our test, the range $[0.6, 1.2]$ provides a good control of aliases.

Fig. 8 schematically represents an architecture of a receiver device in which the present invention may be implemented.

According to the shown architecture, the receiver 8.1 device comprises the following components interconnected by a communications bus 8.7: a processor,

microprocessor, microcontroller or CPU (*Central Processing Unit*) 8.2; a RAM (*Random-Access Memory*) 8.3; a ROM (*Read-Only Memory*) 8.4; an SD (*Secure Digital*) card reader 8.5, or any other device adapted to read information stored on storage means; a communication interface 8.6.

5 The communication interface 8.6 allows the receiver device to wirelessly communicate with a transmitter device.

CPU 8.2 is capable of executing instructions loaded into RAM 8.3 from ROM 8.4 or from an external memory, such as an SD card. After the receiver device has been powered on, CPU 8.2 is capable of reading instructions from RAM 8.3 and
10 executing these instructions. The instructions form one computer program that causes CPU 8.2 to perform some or all of the steps of the algorithms described hereafter with regard to Figs. 5 and/or 9.

Any and all steps of the algorithms described hereafter with regard to Figs. 5 and/or 9 may be implemented in software by execution of a set of instructions or
15 program by a programmable computing machine, such as a PC (*Personal Computer*), a DSP (*Digital Signal Processor*) or a microcontroller; or else implemented in hardware by a machine or a dedicated component, such as an FPGA (*Field-Programmable Gate Array*) or an ASIC (*Application-Specific Integrated Circuit*).

In other words, the receiver device includes circuitry, or a device including
20 circuitry, causing the receiver device to perform the steps of the algorithms described hereafter with regard to Figs. 5 and/or 9. Such a device including circuitry causing the receiver device to perform the steps of the algorithms described hereafter with regard to Figs. 5 and/or 9 may be an external device connectable to the receiver device. Such receiver device may also be installed as part of another device. In example, this kind
25 of installation would be useful when the receiver device is in form of a chip, a chipset, or a module. Alternatively, instead of being installed in or connected to a dedicated communication device, the receiver device according to the invention may provide communication capability to any suitable device, such as a computer device, a machine, in example, a vending machine, or a vehicle like a car or truck, where the
30 device may be installed in or connected to for this purpose. The term circuitry refers either to hardware implementation, consisting in analogue and/or digital processing, or to a combination of hardware and software implementation, including instructions of computer program associated with memories and processor causing the processor to

perform any and all steps of the algorithms described hereafter with regard to Figs. 5 and/or 9.

CLAIMS

1/ A method for digitizing an analogue signal for further demodulation in a radio receiving device, said method causing the device to perform:

- 5 - converting the analogue signal to a digital signal at a sample rate using an analogue to digital converter;
- applying to the digital signal a first sample rate conversion by a Farrow structure to bring the sample rate to an intermediate sample rate;
- applying to the digital signal sampled at the intermediate sample rate a second
10 sample rate conversion by a decimator to bring the signal from the intermediate sample rate to a target sample rate required by the demodulation;
- filtering the digital signal for magnitude equalization and/or blocker rejection.

2/ A method according to claim 1, characterized in that it further causes the
15 device to perform:

- applying a programmable digital gain after the filtering.

3/ A method according to any of claims 1 to 2, characterized in that it further causes the device to perform:

- 20 - further filtering the digital signal for phase equalization after the filtering.

4/ A method according to any of claims 1 to 3, characterized in that the first conversion ratio and/or the second conversion ratio is/are determined based on the sample rate and the target sample rate.

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5/ A method for configuring a sample rate converter in a reconfigurable receiving digital data path within a radio receiving device, said method causing the device to perform:

- determining a sample rate of an analogue to digital converter depending on
30 radio-frequency performance requirements;
- determining a target sample rate required for demodulation;
- determining a conversion ratio to configure the sample rate converter comprising a Farrow structure and a decimator to convert a sample rate of a signal

provided by the analogue to digital converter to the target sample rate required for modulation;

- obtaining a conversion ratio of the Farrow structure to convert the sample rate of the analogue to digital converter to an intermediate sample rate for further rate conversion by the decimator;

- obtaining a conversion ratio of the decimator to convert the intermediate sample rate to the target sample rate required for modulation.

6/ A method for configuring a sample rate converter according to claim 5, characterized in that the conversion ratio of the Farrow structure and/or the conversion ratio of the decimator is/are determined based on the sample rate and the target sample rate.

7/ A computer program characterized in that it comprises program code instructions which can be loaded in a programmable device for implementing the method according to any one of claims 1 to 6, when the program code instructions are run by the programmable device.

8/ Information storage means, characterized in that they store a computer program comprising program code instructions which can be loaded in a programmable device for implementing the method according to any one of claims 1 to 6, when the program code instructions are run by the programmable device.

9/ A radio receiving device for digitizing an analogue signal for further demodulation, the device comprising circuitry causing the device to implement:

- means for converting the analogue signal to a digital signal at a sample rate using an analogue to digital converter;

- means for applying to the digital signal a first sample rate conversion by a Farrow structure to bring the sample rate to an intermediate sample rate;

- means for applying to the digital signal sampled at the intermediate sample rate a second sample rate conversion by a decimator to bring the signal from the intermediate sample rate to the target sample rate required by the demodulation;

- means for filtering the digital signal for magnitude equalization and/or blocker rejection.

10/ A device according to claim 9, characterized in that it further comprises circuitry causing the device to implement:

- means for applying a programmable digital gain after the filtering.

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11/ A device according to any of claims 9 to 10, characterized in that it further comprises circuitry causing the device to implement:

- means for further filtering the signal for phase equalization after the filtering.

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12/ A device according to any of claims 9 to 11, characterized in that it further comprises circuitry causing the device to implement:

- means to determine the first conversion ratio and/or the second conversion ratio based on the sample rate and the target sample rate.

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13/ A radio receiving device for configuring a sample rate converter in a reconfigurable receiving digital data path within a radio receiving device, the device comprising circuitry causing the device to implement:

- means for determining a sample rate of an analogue to digital converter depending on radio-frequency performance requirements;

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- means for determining a target sample rate required for demodulation;

- means for determining a conversion ratio to configure the sample rate converter comprising a Farrow structure and a decimator to convert a sample rate of a signal provided by the analogue to digital converter to the target sample rate required for modulation;

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- means for obtaining a conversion ratio of the Farrow structure to convert the sample rate of the analogue to digital converter to an intermediate sample rate for further rate conversion by the decimator;

- means for obtaining a conversion ratio of the decimator to convert the intermediate sample rate to the target sample rate required for modulation.

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14/ A device according to claim 13, further comprising circuitry to cause the device to implement:

- means for determining the conversion ratio of the Farrow structure and/or the conversion ratio of the decimator based on the sample rate and the target sample rate.

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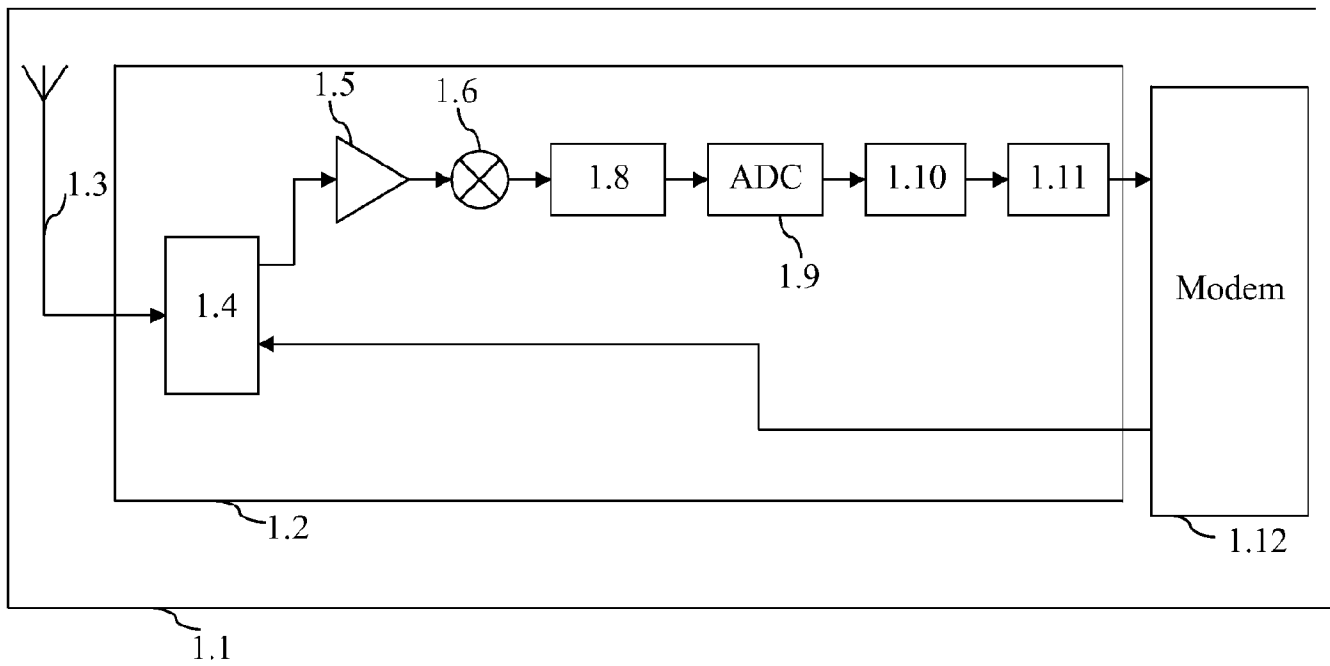


Fig. 1

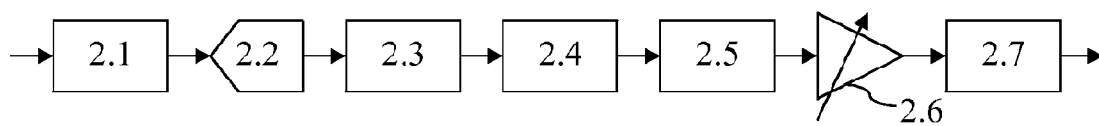


Fig. 2

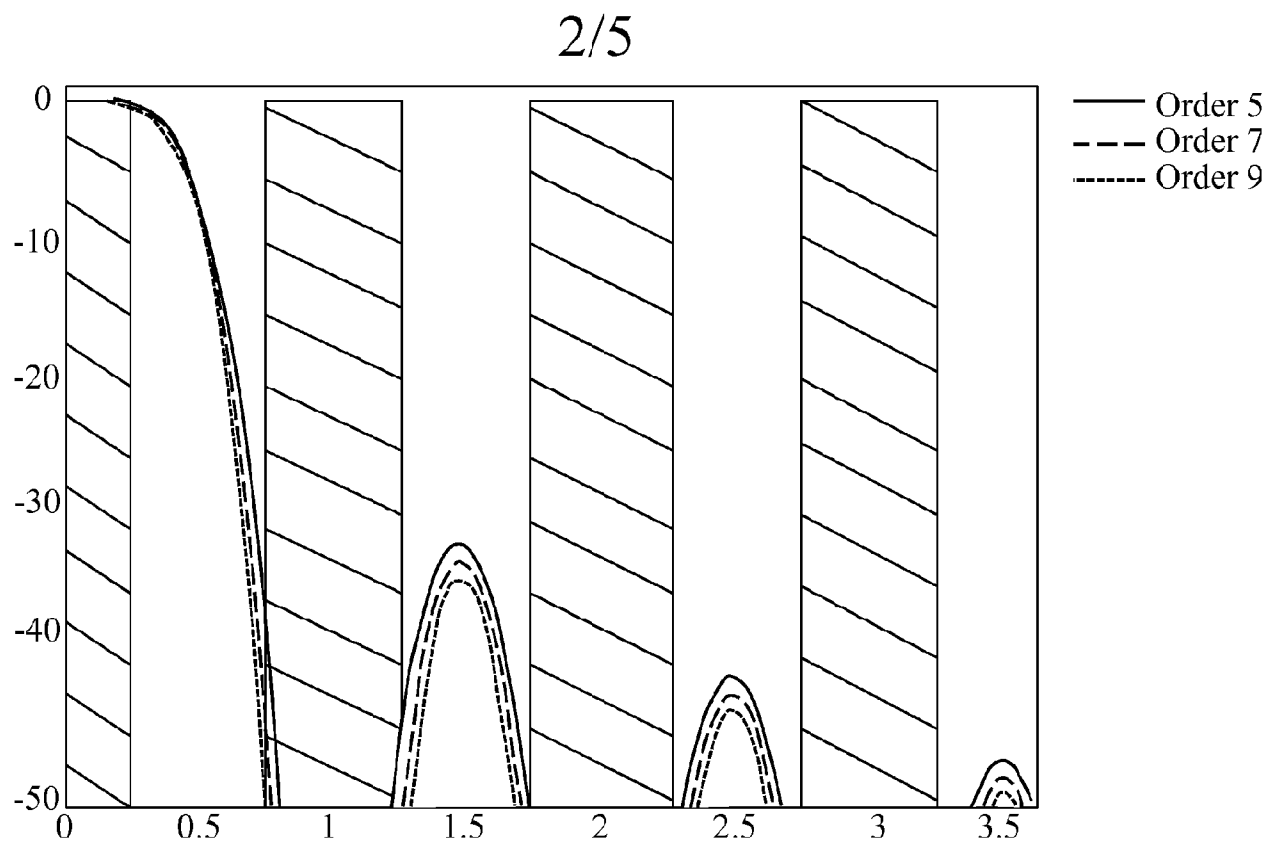


Fig. 3

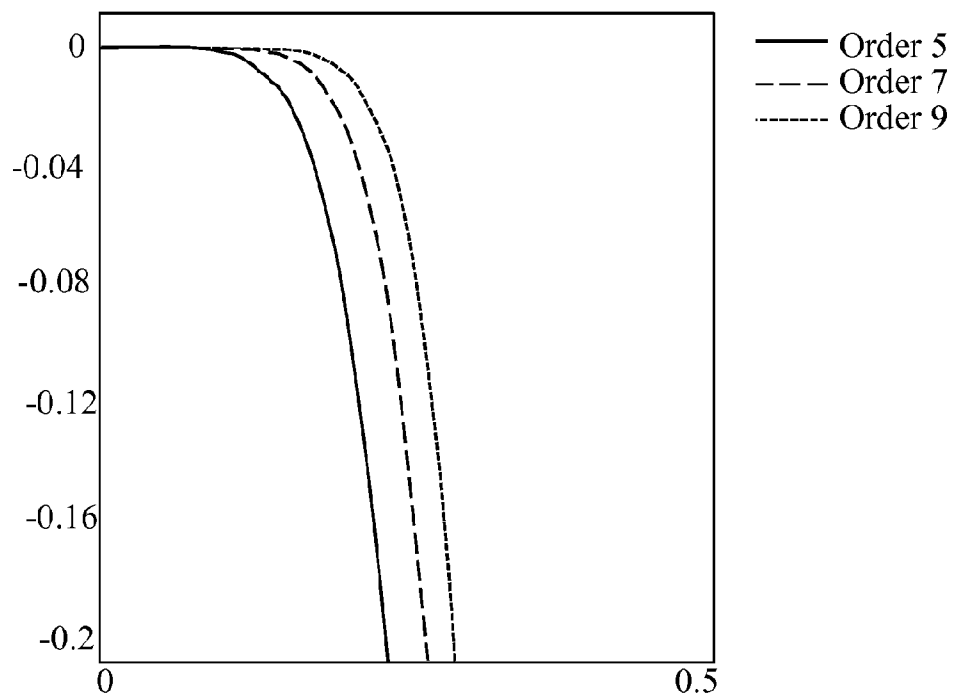


Fig. 4

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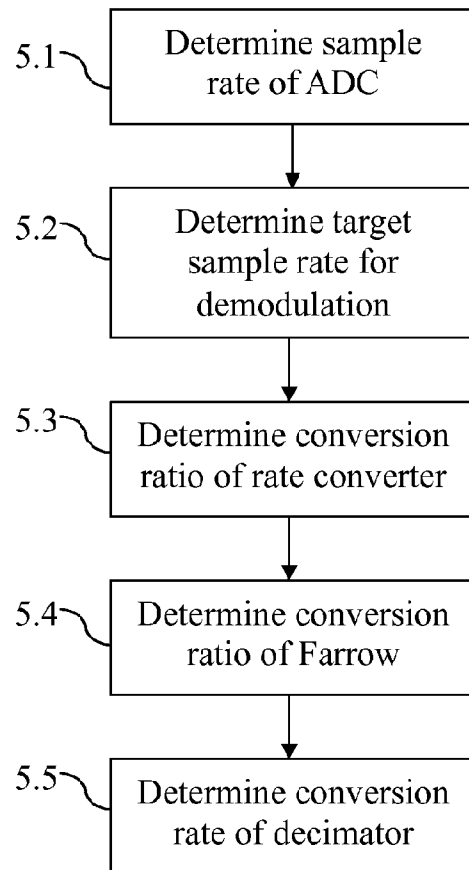


Fig. 5

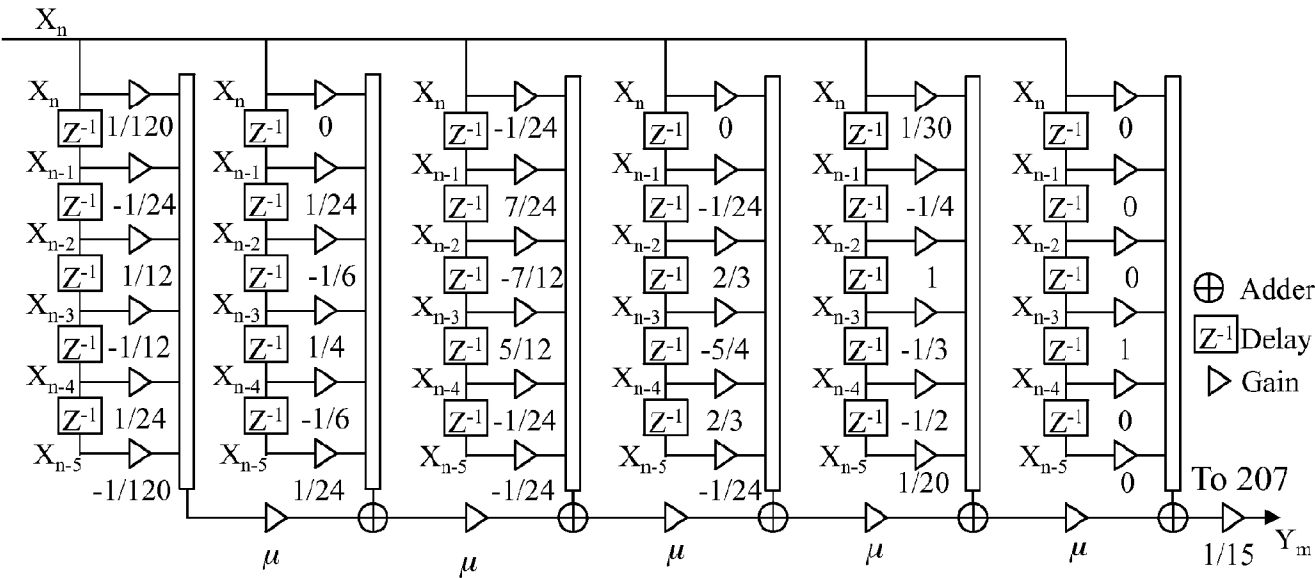


Fig. 6

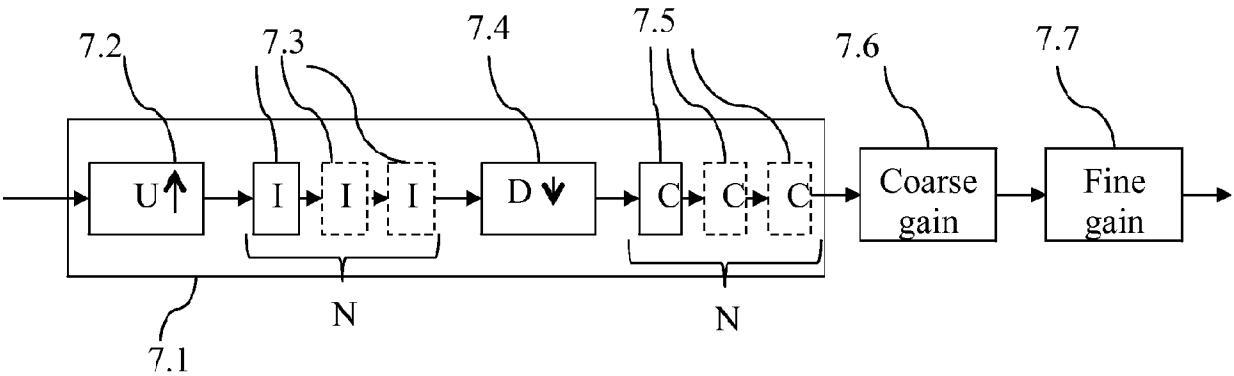


Fig. 7

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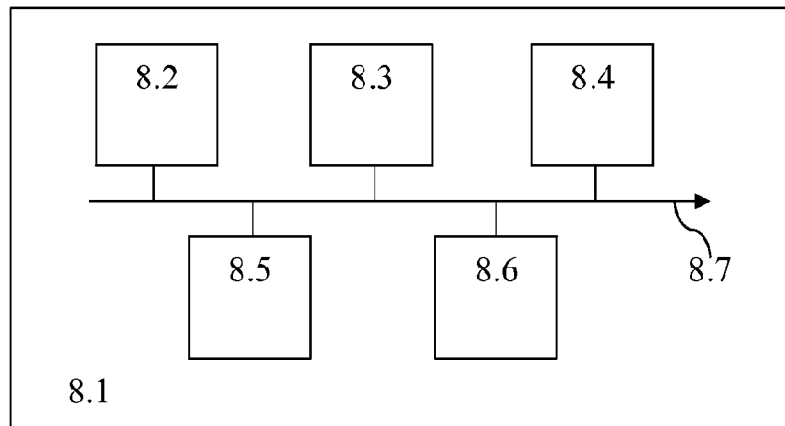


Fig. 8

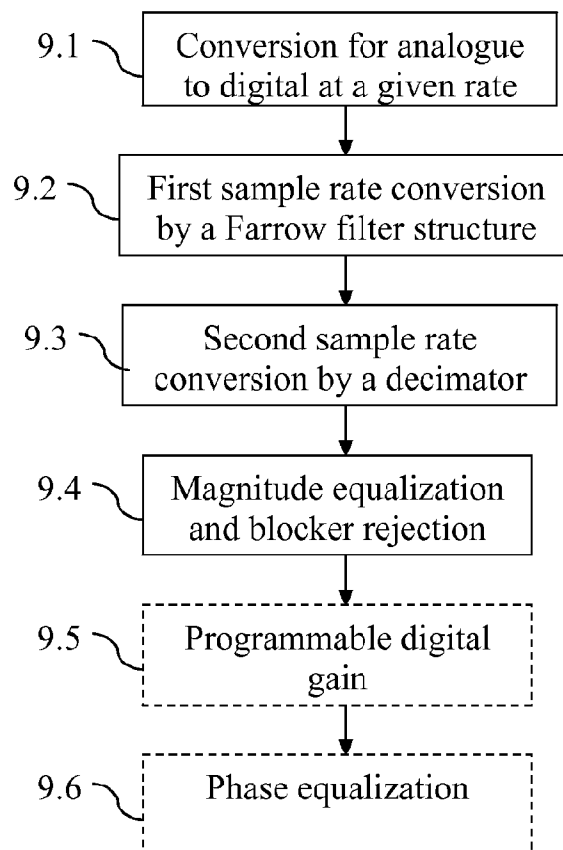


Fig. 9

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2012/002222

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03H17/02 H03H17/06
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	BABIC D ET AL: "Decimation by non-integer factor in multistandard radio receivers", SIGNAL PROCESSING, ELSEVIER SCIENCE PUBLISHERS B.V. AMSTERDAM, NL, vol. 85, no. 6, 1 June 2005 (2005-06-01), pages 1211-1224, XP027670893, ISSN: 0165-1684 [retrieved on 2005-06-01] abstract; figure 3	1-14
Y	US 2008/226001 A1 (GENG JIFENG [US] ET AL) 18 September 2008 (2008-09-18) paragraphs [0031] - [0034]; figure 4 ----- -/--	1-14



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

17 July 2013

Date of mailing of the international search report

30/07/2013

Name and mailing address of the ISA/

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Authorized officer

De La Pinta, Luis

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2012/002222

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	TIM HENTSCHEL ET AL: "Sample Rate Conversion for Software Radio", IEEE COMMUNICATIONS MAGAZINE, IEEE SERVICE CENTER, PISCATAWAY, US, vol. 38, no. 8, 1 August 2000 (2000-08-01), pages 142-150, XP011091342, ISSN: 0163-6804 abstract; figure 5 -----	1-14
A	NAVIN MICHAEL ET AL: "Design of Multistandard Channelization Accelerators for Software Defined Radio Handsets", IEEE TRANSACTIONS ON SIGNAL PROCESSING, IEEE SERVICE CENTER, NEW YORK, NY, US, vol. 59, no. 10, 1 October 2011 (2011-10-01), pages 4767-4780, XP011360118, ISSN: 1053-587X, DOI: 10.1109/TSP.2011.2161301 paragraph [III.C] -----	1-14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2012/002222

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☒ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/IB2012/002222

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008226001 A1	18-09-2008	CN 101636921 A	27-01-2010
		EP 2127101 A2	02-12-2009
		JP 2010521893 A	24-06-2010
		KR 20090117961 A	16-11-2009
		TW 200847665 A	01-12-2008
		US 2008226001 A1	18-09-2008
		WO 2008112928 A2	18-09-2008

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-4, 9-12(completely); 7, 8(partially)

Method for digitizing an analogue signal for further demodulation in a radio receiving device and corresponding radio receiving device for digitizing an analogue signal for further demodulation

2. claims: 5, 6, 13, 14(completely); 7, 8(partially)

Method for configuring a sample rate converter in a reconfigurable receiving digital data path within a radio receiving device and corresponding radio receiving device for configuring a sample rate converter in a reconfigurable receiving digital data path
