THIN FILM THERMOELECTRIC DEVICES FOR POWER CONVERSION AND COOLING

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Abstract:
A thermoelectric device having at least one thermoelectric unit including at least one thermoelectric pair of n-type and p-type thermoelements, a first header coupled to one side of the thermoelectric pair, and a second header coupled to a second side of the thermoelectric pair. The thermoelectric pair has a thermal conduction channel area smaller than an area of the first header or the second header such that the thermal conduction area is a fraction of the area of the first header or the second header.
FIG. 3
FIG. 4
### FIG. 5

**TABLE 2**

<table>
<thead>
<tr>
<th>Stage</th>
<th>ZTave</th>
<th>Efficiency (%)</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>UPPER PROJECTION</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Stage 1 (Bi2Te3-based SL)</td>
<td>2.5</td>
<td>11.4%; 0T = 150C</td>
<td>10.8%; 0T = 150C</td>
</tr>
<tr>
<td>Stage 2 (with PbTe/PbSe SL)</td>
<td>1.5</td>
<td>6.9%; 0T = 175C</td>
<td>7.4%; 0T = 200C</td>
</tr>
<tr>
<td>Stage 3 (with Si/Ge SL)</td>
<td>1.5</td>
<td>5.9%; 0T = 200C</td>
<td>5.5%; 0T = 200C</td>
</tr>
<tr>
<td><strong>Total Efficiency and Power Density for 3-stage Cascade Module</strong></td>
<td></td>
<td>24.2%</td>
<td>23.7%</td>
</tr>
<tr>
<td><strong>MID-RANGE PROJECTION</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Stage 1 (Bi2Te3-based SL)</td>
<td>2.25</td>
<td>10.8%; 0T = 150C</td>
<td>10.2%; 0T = 150C</td>
</tr>
<tr>
<td>Stage 2 (with PbTe/PbSe SL)</td>
<td>1</td>
<td>5.3%; 0T = 175C</td>
<td>5.7%; 0T = 200C</td>
</tr>
<tr>
<td>Stage 3 (with Si/Ge SL)</td>
<td>1</td>
<td>4.5%; 0T = 200C</td>
<td>4.2%; 0T = 200C</td>
</tr>
<tr>
<td><strong>Total Efficiency and Power Density for 3-stage Cascade Module</strong></td>
<td></td>
<td>20.6%</td>
<td>20.1%</td>
</tr>
<tr>
<td><strong>LOWER PROJECTION</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Stage 1 (Bi2Te3-based SL)</td>
<td>2</td>
<td>10.2%; 0T = 150C</td>
<td>9.6%; 0T = 150C</td>
</tr>
<tr>
<td>Stage 2 (use only thin-substrate bulk)</td>
<td>0.75</td>
<td>4.3%; 0T = 175C</td>
<td>4.7%; 0T = 200C</td>
</tr>
<tr>
<td>Stage 3 (use only thin-substrate bulk)</td>
<td>0.75</td>
<td>3.7%; 0T = 200C</td>
<td>3.4%; 0T = 200C</td>
</tr>
<tr>
<td><strong>Total Efficiency and Power Density for 3-stage Cascade Module</strong></td>
<td></td>
<td>18.2%</td>
<td>17.7%</td>
</tr>
</tbody>
</table>
Voc vs T in one P-N coupler and 16-couple Mini-module

Mini-module: \(7.5169 \times 10^{-3} + 0.01579 \times \Delta A_0\)

\(P_{\text{in}} = 0.9871\)

1 couple: \(0.476x - 0.8427\)

\(R' = 0.9995\)

\(\Delta T, (K)\)

0 30 60 90 120 150

FIG. 6B(1)

Electrical Power vs \(\Delta T\) in one P-N couple and 16-couple Mini-module

Mini-module: \(2.039 \times 10^{-2} + 1.496 \times 10^{-1} \times \Delta A_0\)

\(R' = 9.997 \times 10^{-1}\)

1 couple: \(2.039 \times 10^{-3} + 1.579 \times 10^{-1} \times \Delta A_0\)

\(R' = 9.778 \times 10^{-1}\)

\(\Delta T, (K)\)

0 30 60 90 120 150

FIG. 6B(2)
Electrical Power Density vs $\Delta T$ in one P-N couple and 16-couple Mini-module

$F I G, 6 B(3)$
Table 4

<table>
<thead>
<tr>
<th>Structure and Comments on Measurement</th>
<th>Configuration</th>
<th>Best Observed ZT</th>
<th>Typical ZT</th>
<th>Potential ZT</th>
</tr>
</thead>
<tbody>
<tr>
<td>P-type Element with two contacts</td>
<td><img src="image1" alt="Diagram" /></td>
<td>&gt;3.5</td>
<td>2.5 to 3.0</td>
<td>3.5 to 4.0</td>
</tr>
<tr>
<td>N-type Element with two contacts</td>
<td><img src="image2" alt="Diagram" /></td>
<td>2.0</td>
<td>1.0 to 1.5</td>
<td>2.0 to 2.5</td>
</tr>
<tr>
<td>Invented P-N Couple</td>
<td><img src="image3" alt="Diagram" /></td>
<td>2.0</td>
<td>1.2 to 1.8</td>
<td>2.0 to 2.5</td>
</tr>
<tr>
<td>Mini-module: Flipped, Inverted P-N Couple with one interconnect and two leads on bottom header (adiabatic conditions difficult plus exact thermal-electrical matching between two legs needed to maximize ZT observed by Hermann method)</td>
<td><img src="image4" alt="Diagram" /></td>
<td>~1.6 (limited by lead resistances on the bottom header)</td>
<td>~1.8 (limited by lead resistances on the bottom header)</td>
<td>&gt;2.0</td>
</tr>
<tr>
<td>Mini-module: Flipped, inverted P-N Couple with one interconnect and two leads on bottom header (power mode where ZT is exacted from electrical power and heat flow through SL elements; no need for adiabaticity and thermal matching of legs less stringent (as one leg does not pump on other as in cooling mode when mismatched)</td>
<td><img src="image5" alt="Diagram" /></td>
<td>~1.6 (limited by lead resistances on the bottom header)</td>
<td>~1.6 (limited by lead resistances on the bottom header)</td>
<td>&gt;2.0</td>
</tr>
</tbody>
</table>

**FIG. 6C**
FIG. 9
FIG. 15
THIN FILM THERMOELECTRIC DEVICES FOR POWER CONVERSION AND COOLING

RELATED APPLICATIONS

[0001] The present application claims the benefit of priority as a continuation-in-part of U.S. application Ser. No. 11/406, 100 filed on Apr. 18, 2006 which claims priority as a continuation-in-part of International Application No. PCT/US2004/041431 (designating the United States) filed on Dec. 13, 2004, which claims the benefit of priority from U.S. Provisional Application No. 60/528,479 filed Dec. 11, 2003. U.S. application Ser. No. 11/406,100 also claims the benefit of priority from U.S. Provisional Application No. 60/672,330 filed Apr. 18, 2005. The present application thus claims the benefit of priority from U.S. application Ser. No. 11/406,100; International Application No. PCT/US2004/041431; U.S. Provisional Application No. 60/528,479; and U.S. Provisional Application No. 60/672,330. The disclosures of each of the above referenced U.S. Utility, U.S. Provisional, and International PCT Applications are hereby incorporated herein in their entirety by reference.

CROSS-REFERENCE TO RELATED DOCUMENTS

[0002] This application is related to U.S. Provisional Application No. 60/572,139 entitled “Thermoelectric device technology utilizing double-sided Peltier junctions” filed on Apr. 15, 2002, the entire contents of which is incorporated herein by reference. This application is related to U.S. Pat. No. 6,300,150 entitled “Thin-film thermoelectric device and fabrication method of same” issued Oct. 9, 2001, the entire contents of which is incorporated herein by reference. This application is related to U.S. Pat. No. 6,071,351 entitled “Low temperature chemical vapor deposition and etching apparatus and method” issued Jun. 6, 2002, the entire contents of which is incorporated herein by reference. This application is related to U.S. Pat. No. 6,505,468 entitled “Cascade cryogenic thermoelectric cooler for cryogenic and room temperature applications” issued Jan. 14, 2003, the entire contents of which is incorporated herein by reference. This application is also related to U.S. Provisional Application No. 60/253,743 entitled “Spontaneous emission enhanced heat transport method and structures for cooling, sensing, and power generation”, filed Nov. 29, 2000, the entire contents of which is incorporated herein by reference, and subsequently filed as PCT Application No. PCT/US01/44517 filed Nov. 29, 2001. This application is related to U.S. Provisional Application No. 60/428,753, “Three-Thermal-Terminal (T³) Trans-Thermoelectric Device”, filed Nov. 25, 2002, the entire contents of which is incorporated herein by reference.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH

[0003] The U.S. Government, by the following contracts, may have a paid-up license in this invention and the right in limited circumstances to require the patent owner to license others on reasonable terms, as provided for by the terms in High-Performance Thin-film Thermoelectric Devices for Cooling and Power Generation, DARPA/ONR Contract No. N00014-97-C-0211, Thin-film Thermoelectric Palm Power Technologies, DARPA/ARO Contract No. DAAD 19-01-C-0070, and Meta-Material Structures for Super-Radiant Structures, DARPA/AIRFORCE Contract No. F49620-01-C-0038.

DISCUSSION OF THE BACKGROUND

[0004] 1. Field of the Invention

[0005] This invention relates to thermoelectric devices for power conversion and cooling which utilize thin film thermoelectric materials.

[0006] 2. Background of the Invention

[0007] A thermoelectric device can produce electrical energy when a heat flux flows through opposite conductivity types of a thermoelectric material. Furthermore, a thermoelectric device can cool an attached object when a current is flown in an appropriate direction through the thermoelectric material. In a thermoelectric generator, for example, a Seebeck voltage generated across a thermoelectric device can be used to drive a current in a connected load circuit. Indeed, thermoelectric generators can generate power from a variety of heat sources. For example, a thermoelectric power device can be connected to a wall of a combustion chamber and therefore generate power from the heat flux flowing from the combustion wall. In this example, a fuel is burnt to produce the heat flux for thermoelectric power generation; however, other heat sources applicable for thermoelectric generators include solar-heated sources, radiotiscope-heated sources, and nuclear reactor waste heat sources. Thermoelectric generators typically include external electronic circuitry such as a DC-DC conversion circuits or DC-AC converters for receiving power from the thermoelectric elements at a low voltage and for delivering power at higher voltages.

[0008] In conventional thermoelectric devices, the efficiency of thermoelectric conversion is at about 6 to 8%. Accordingly, there is a drawback that thermoelectric conversion efficiency is low as compared with the other direct energy conversion systems such as for example a fuel cell device. If thermoelectric devices had higher conversion efficiencies, then thermoelectric thermoelectric power conversion devices could be effectively employed even in automobiles to increase the total fuel efficiency of the automobile by converting waste heat spent from the combustion process into electrical power.

[0009] Low efficiencies have also limited the application of thermoelectric devices in cooling and refrigeration applications. Chen et al. in U.S. Pat. No. 5,713,208, the entire contents of which are incorporated by reference, describe a thermoelectric cooling apparatus which includes a plurality of thermoelectric coolers each having a hot side connected to a heat sink and a cold side coupled to an object to be cooled. While Chen et al. describe that thermoelectric coolers may be any suitable thermoelectric coolers such as those supplied by Melcor under catalog number CP 2-127-06L, the efficiency of these coolers, like those of the afore-mentioned power conversion thermoelectric devices, are limited.

[0010] The dimensionless thermoelectric figure of merit (ZT) is a measure of the effectiveness of the material for both cooling and power conversion applications. The Seebeck coefficient (S) is a measure of how readily electrons (or holes) convert thermal to electrical energy as the electrons move across a temperature gradient. At a given temperature, the thermoelectric figure of merit ZT for a given material is maximized at an optimum doping level. In most materials, the thermoelectric figure of merit ZT is maximized at doping levels of approximately 10¹⁹ cm⁻³. Currently, the best non-superlattice thermoelectric materials have a maximum ZT of approximately 1. Today, bulk thermoelectric materials based...
on p-Bi$_2$Sb$_3$Te$_3$ and n-Bi$_2$Te$_3$Se$_2$ do not have a sufficient figure-of-merit (ZT) to allow economical application in many power conversion situations. [0011] In contrast to bulk materials, the thermal properties of superlattice structures can be improved over that of the thermal properties of bulk materials. Superlattice structures in thermoelectric materials have been investigated as structures whose engineered properties can lead to better semiconductor and thermoelectric properties. The fabrication of a superlattice by molecular beam epitaxy (MBE), or other known epitaxial growth techniques, is generally known. The choice of materials and the relative amounts of the materials which make up the superlattice are factors in determining the characteristics of the superlattice. For use as a thermoelectric material, it is desirable to choose the materials, and their relative amounts, so that the thermoelectric figure of merit (ZT) and Seebeck coefficient (S) are maximized. Thus, superlattice materials are expected to have higher ZT values than bulk-materials. Despite the higher ZT of superlattice thin-film materials, thin film thermoelectric devices are presently limited by thermal mismatch and temperature gradient issues and also are practically limited by the high cost of thin-film superlattice materials.

SUMMARY

[0012] One object of some embodiments of the present invention is to provide a thermoelectric device structure utilizing high ZT thermoelectric materials.

[0013] Another object of some embodiments of the present invention is to utilize a thermoelectric device structure in which the thermoelectric properties of the device are not contravened by inadvertent heat flux around the active thermoelectric elements in the device.

[0014] A further object of some embodiments of the present invention is to provide a thermoelectric device structure for cooling power-dissipating devices.

[0015] Still another object of some embodiments of the present invention is to provide a thermoelectric device which can convert power from a wide variety of moderate to high temperature heat sources, including but not limited to fuel sources.

[0016] Accordingly, one object of some embodiments of the present invention is to provide a multi-stage thermoelectric device for power conversion from heat sources at temperatures of 600 to 850 K.

[0017] Still another object of some embodiments of the present invention is to provide a thermoelectric device which can be converted from a power conversion device to a heat pump device should coolant to a heat sink of the thermoelectric device be interrupted.

[0018] Yet another object of some embodiments of the present invention is to provide a thermoelectric device which utilizes both bulk thermoelectrics and superlattice thermoelectric films to exploit for each respective thermoelectric material those thermoelectric properties in operational temperature ranges most suitable for each.

[0019] Accordingly, one object of some embodiments of the present invention is to provide a thermoelectric device in which there is a high internal heat-flux within an individual thermoelectric stage and a low external heat-flux across the entirety of the thermoelectric device.

[0020] Various of these and other objects of some embodiments of the present invention are accomplished in several embodiments of the present invention.

[0021] One exemplary embodiment includes a novel thermoelectric device having at least one thermoelectric unit including a thermoelectric pair of n-type and p-type thermoelements, a first header coupled to one side of the thermoelectric pair, a second header coupled to a second side of the thermoelectric pair, and a thermal impedance increasing device disposed between the thermoelectric pair and one of the first and second headers.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] A more complete appreciation of the present invention and many attendant advantages thereof will be readily obtained as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings, wherein:

[0023] FIG. 1A is a schematic of one embodiment of a thermoelectric device according to some embodiments of the present invention;

[0024] FIG. 1B is a schematic of a thermoelectric device according to some embodiments of the present invention operating in a High Active Flux-Low Input-Output Flux mode;

[0025] FIG. 2 is a schematic of a multi-stage thermoelectric device according to some embodiments of the present invention;

[0026] FIG. 3 is a graph depicting variations of ZT with temperature for various material systems useful in some embodiments of the present invention;

[0027] FIG. 4 is a graph depicting state-of-the-art ZT vs carrier concentration for p and n-type Bi$_2$Te$_3$-based superlattice elements;

[0028] FIG. 5 is a table of estimated design efficiencies for a three-stage thermoelectric device of some embodiments of the present invention;

[0029] FIG. 6A is a schematic illustration depicting a thermoelectric device module of some embodiments of the present invention integrating a series of p-n couples on a single stage;

[0030] FIG. 6B (1)-(3) depict tests on p-n couple devices of some embodiments of the present invention for open-circuit voltage (Voc), power (P), and power density (PD) in W/cm$^2$;

[0031] FIG. 6C is a table illustrating the inverted processing approach of some embodiments of the present invention;

[0032] FIG. 7A is a schematic depicting the attachment of a pre-fabricated thermoelectric device of some embodiments of the present invention onto a semiconductor device chip;

[0033] FIG. 7B is a schematic depicting the attachment of a thermoelectric device of some embodiments of the present invention onto a semiconductor device chip;

[0034] FIG. 7C is a schematic depicting the sequential formation of a thermoelectric device on some embodiments of the present invention onto a semiconductor device chip;

[0035] FIG. 8 is a schematic of a multi-stage thermoelectric device of some embodiments of the present invention employing resonant thermal energy transfer using Purcell-cavity enhancement effects and proximity-coupling of IR modes between various stages;

[0036] FIG. 9 is a plot of apparent emission intensity as a function of the surface temperature of different engineered structures according to some embodiments of the present invention;
FIG. 10 is a schematic arrangement of a three stage of thermoelectric device of some embodiments of the present invention with a split-header to provide thermal expansion relief;

FIG. 11 is an electrical diagram showing a configuration for operating a thermoelectric device of some embodiments of the present invention in either a cooling mode or a heat pump mode;

FIG. 12A is a schematic depicting a coupling structure for coupling a thermoelectric device to a semiconductor device chip;

FIG. 12B is a schematic depicting another coupling structure for coupling a thermoelectric device to a semiconductor device chip;

FIG. 13 is a schematic depicting another coupling structure for coupling a thermoelectric device to a semiconductor device chip;

FIG. 14 is a schematic depicting a coupling structure including via for electrical connections to the thermoelectric devices; and

FIG. 15 is a schematic depicting a coupling structure including high thermal conductivity materials in a heat sink plate.

DETAILED DESCRIPTION

Referring now to the drawings, wherein like reference numerals designate identical, or corresponding parts throughout the several views, and more particularly to FIG. 1A thereof, FIG. 1A depicts a schematic of one embodiment of a thermoelectric device according to some embodiments of the present invention. As shown in FIG. 1A, a thermoelectric device 1 of some embodiments of the present invention includes a thermoelectric pair of n and p-type thermoelements 2a and 2b, respectively. The thermoelectric pair is connected thermally in parallel for heat conduction and electrically in series for electrical conduction. The thermoelectric pair of n and p-type thermoelements 2a and 2b are electrically adjoined together on the side coupled to an upper side header 3 by electrical connection 6, and are electrically connected separately on the side coupled to a lower side header 4 by electrical connection 7. As shown illustratively in FIG. 1A, the thermoelectric pair of n and p-type thermoelements 2a and 2b can be coupled to the upper side header 3 by a heat pipe 5 made of high thermal conductivity materials such as Si, SiC, Mn, etc. In this example of some embodiments of the present invention, heat flowing in the thermoelectric device 1 is channeled in the heat pipe 5 into the thermoelectric pair of n and p-type thermoelements 2a and 2b.

In some embodiments of the present invention, due to the different thermoelectric properties of the n and p-type materials of the thermoelements 2a and 2b, electrons and holes in these materials diffuse at different rates across the respective n and p-type thermoelements, thereby creating a voltage difference across the pair of n and p-type thermoelements. In this embodiment, a cooling device (not shown) is coupled to the lower side header 4 to permit dissipation of heat. Otherwise, the upper side header 3, the pair of n and p-type thermoelements 2a and 2b, and the lower side header 4 would all come to nearly equivalent temperatures. As a consequence, the electrons and holes in the n and p-type thermoelements 2a and 2b would stop diffusing to the lower side header.

In other embodiments of the present invention, electron and hole current can driven through the n and p-type thermoelements 2a and 2b by an applied voltage to thereby cool the upper side header 3. Owing to electrical barriers existing between electrical connection 6 and the pair of n and p-type thermoelements 2a and 2b, the electron and hole current will preferentially transport those electrons and holes having a higher thermal energy, thereby cooling the upper side header 3. A heat dissipation device (not shown) coupled to the lower side header 4 permits dissipation of heat from the device, else the lower side header 4 would come to a temperature such that heat, via diffusion of phonons, would flow back to the upper side header 3 at a rate equal to the heat being carried from the upper-side header 3 by the electron and hole current, thereby eliminating the cooling.

The optional heat pipe 5 represents a mechanism to increase the thermal impedance (through the gap) between the upper side header 3 and the lower side header 4 to a value significantly larger (by a factor of 100 or more) than the thermal impedance across the thermoelectric pair 2a and 2b. As shown in FIG. 1A, the heat pipe 5 is elongated in a direction transverse to the thermoelectric device 1 (i.e., normal to the upper side header 3). The heat pipe 5 has a cross-sectional area smaller than that of an area of the upper side header 3. The heat pipe 5 of some embodiments of the present invention provides an offset, spacing apart the upper side header 3 from the lower side header 4. The offset permits for example thin-film thermoelements to be used without thermal conduction from the upper side header 3 to the lower side header 4 shunting across the gap between the headers, thereby forcing heat flux to flow through the thermoelements 2a and 2b. The offset in some embodiments of the present invention is at least 0.25 μm and more preferably in the range of 250 to 500 μm. As such, the offset produces a thermal impedance across a gap, where thermoelectric elements do not exist, between the upper side header 3 and the lower side header 4 whose value is at much larger than the thermal impedance across the pair of thermoelements 2a and 2b. For example, a thermal impedance across an air gap is greater than the thermal impedances for the thermoelements 2a and 2b, typically by a factor of 500 to 1000, for similar areas of air gap and thermoelectric materials. Thus, the offset allows this ratio to increase, using the high thermal conductivity of the offset relative to the air-gap. The thickness of the offset can be reduced as the pressure level in the gap is reduced i.e., with a high vacuum level, the thermal conductivity of the gap is reduced and so we need less of the offset thickness. For many applications, the offset will be at least 10 μm, and for other applications in a range of 100-500 μm.

Regardless of the heat pipe, the thermoelectric devices of some embodiments of the present invention conduct a high active heat flux, while maintaining a much lower flux through the surfaces 1 and 4, through the pair of thermoelements which permits some embodiments of the present invention to realize ultra-high specific power in the pair of n and p-type thermoelements 2a and 2b. Thus, some embodiments of the present invention operates with a high active flux through each of the thermoelements while having a low input/output flux across the entirety of the thermoelectric device. As described herein, this aspect of some embodiments of the present invention is referred as High Active Flux-Low Input-Output Flux (HAF-LIOF). This aspect is illustrated pictorially in FIG. 1B. In this aspect, the heat flux through the heat gatherer (e.g. an upper side header 3) and the heat spreader (e.g. an lower side header 4) is smaller than the heat flux through the n and p-type thermoelements 2a and 2b due to the
reduced packing fraction of the thermoelements. A packing fraction of the thermoelements relative to the area of the heat spreader(s) permits the utilization of thinner thermoelements, thereby reducing the fabrication costs that would be involved should for example thicker sections of high ZT materials be required to maintain the requisite $\Delta T$ across the thermoelectric device.

The packing fraction of thermoelements (i.e., the fraction of area occupied by the pair of n and p-type thermoelements $2a$ and $2b$ relative to a unit area of for example the upper side header 3) in some embodiments of the present invention is less than 50%, less than 20%, and can be significantly lower, 0.5-1% for example. A unit area for the heat spreader is defined as that fraction of the total area of the heat spreader which principally conducts heat into one of the associated pairs of n and p-type thermoelements attached to the heat spreader. For the single pair of n and p-type thermoelements shown in FIG. 1b, the unit area would be the entire area of the upper side header 3. For instance, while the total heat flux into upper-side header 3 and out the lower-side header 4 can be on the order of 10-30 W/cm², the heat flux through each thermoelectric pair $2a$ and $2b$ can be as much as a factor of 100 times higher.

The preferred packing fraction is a function of the heat flux available at the heat-source, the required $\Delta T$ needed across the thermoelement to achieve the maximum efficiency, and the heat-flux that can be dissipated at the heat-sink. For example, if the required heat-flux through the device element is 2500 W/cm² to generate a requisite $\Delta T$, then the heat flux that can be efficiently dissipated at the heat-sink is 25 W/cm², then a packing fraction of 1% will be used (i.e. 25/2500 x 100%). However, if the heat flux that can be efficiently dissipated at the sink is only 2.5 W/cm², then a packing fraction needed would be 0.1% for the same heat flux of 2500 W/cm² through each thermoelectric pair. A smaller packing fraction, however, can result in increased parasitic thermal transfer losses through any medium (such as air, Nitrogen, Helium) between the hot and cold-sides of the thermoelectric module.

Therefore, in thermoelectric devices of some embodiments of the present invention, besides using a heat pipe, other thermal impedance increasing devices can be employed. For example, a partial vacuum (i.e. 1 Torr) as a low thermal impedance medium can be used in a module (e.g. the module containing thermoelectric devices shown in FIG. 6a) containing the thermoelectric devices. Alternatively, the module 10 can be filled with a low conductivity gas such as for example Ar.

The headers and heat pipes of some embodiments of the present invention have thermally conducting properties. Examples of suitable materials for the headers and heat pipes include for example AlN, SiC, and diamond. These materials have relatively high thermal conductivities (e.g. 5-20 W/cm-K) and offer the advantage of being electrically insulating. Alternatively, metallic or other semiconductor materials can be used for the headers and heat pipes of some embodiments of the present invention provided a suitable electrical insulating layer 8 is added to the surface of those materials. The thermal conductance through the electrical insulating layer preferably presents no substantial impedance to vertical heat flow through the pair of n and p-type thermoelements $2a$ and $2b$.

For example, the headers of some embodiments of the present invention can be made from a Si substrate of a thermal conductivity of $1.2$ to $1.6\ W/cm-K$ having a thin (i.e. $10\ nm$ to $1000\ nm$) $SiO_2$ or $Si_N_x$ layer of a thermal conductivity of $0.015\ W/cm-K$ deposited thereon. For example, the headers of some embodiments of the present invention can also be made from a Cu substrate of a thermal conductivity of $4\ W/cm-K$ having a thin (i.e. $100\ nm$ to $1000\ nm$) $SiO_2$ or $Si_N_x$ layer of a thermal conductivity of $0.015\ W/cm-K$ deposited thereon. If a SiC header or heat pipe is used that is electrically conducting (e.g. a doped SiC material), a similar insulating layer can be applied as well.

Since the thermoelements are low voltage, high current devices, the electrical connections are preferably highly conductive having a low resistance (preferably $10^{-6}$ or less than that of the Ohmic resistance of the thermoelements). A low conductance for the electrical connections will undermine the efficiency of the thermoelectric stage by resistive losses in current flow through the thermoelectric device.

Accordingly, in general, some embodiments of the present invention may include a thermoelectric device having a first header (e.g. the upper side header 3) coupled to a heat source, a pair of n-type and p-type thermoelements (e.g. the pair of n and p-type thermoelements $2a$ and $2b$) coupled to the first header and configured to conduct heat from the first header, a second header (e.g. the lower side header 4) coupled to the pair of n-type and p-type thermoelements and configured to conduct heat from the thermoelectric pair, and a heat pipe coupled to the pair of n-type and p-type thermoelements (e.g. the heat pipe 15 connected to the thermoelectric pair $2a$ and $2b$) and elongated in a transverse direction across the thermoelectric device to separate the first header from the second header.

In some embodiments of the present invention, the thermoelectric devices cool the first header (and thus can cool heat dissipating devices coupled thereto) by the flow of an electrical current through electrical connections 6 and 7 through the thermoelements $2a$ and $2b$, thus transporting heat in the electrical carriers (i.e., the electrons and holes) and thereby cooling the first header. In other embodiments of the present invention, the thermoelectric devices generate electrical power by the development of a voltage on the electrical connections 6 and 7 as heat flows from the first header (coupled to a heat source) through the thermoelements $2a$ and $2b$ to the second header (coupled to a heat sink).

Further, some embodiments of the present invention may not be limited to single stage and/or single pair thermoelectric devices but can utilize multiple stages and/or multiple pairs of thermoelements in a single stage.

FIG. 2 depicts a multi-stage embodiment of the present invention. Specifically, FIG. 2 is an illustrative schematic of a multi-stage or multi-unit thermoelectric device of some embodiments of the present invention including three thermoelectric stages or units. The device depicted in FIG. 2 is shown by way of example in a configuration for thermoelectric power conversion and, for simplicity, is discussed below only in a context of power conversion. However, the features of some embodiments of the present invention depicted in FIG. 2 and utilizing multiple stages and/or multiple pairs of thermoelements in a stage are, according to some embodiments of the present invention, applicable to thermoelectric cooling as well. Further, the number of stages and the number of thermoelectric pairs per stage in some embodiments of the present invention are not restricted to that illustrated in FIG. 2.

As shown in FIG. 2, an upper header 12 is coupled to a heat source 14 and includes at least one upper thermoelec-
tric stage 16 coupled to the upper header 12. Of the thermoelectric stages 16,17, and 18 depicted in FIG. 2, at least one of the depicted thermoelectric stages is dimensioned such that area for thermal conduction in the thermoelectric stage through a pair of thermoelements 20a and 20b, herein referred to as the active thermal conduction channel area, is smaller than above-noted unit area of header 22 to which the pair of thermoelements 20a and 20b are coupled to. Such dimensioning as discussed with regard to FIG. 1 establishes the HAF-LIOF aspect for the multi-stage thermoelectric device of FIG. 2. As shown in FIG. 2, the upper thermoelectric stage 16 is coupled to at least one lower thermoelectric stage, e.g. stage 17. The lower thermoelectric stage 17 like the upper thermoelectric stage 16 has an active thermal conduction channel area through the pair of thermoelements 20a and 20b that is smaller in area than the unit area of header 22. In the device depicted in FIG. 2, heat is dissipated from the lowermost thermoelectric stage 18 by a heat sink 24 coupled thereto. Accordingly, heat pipes in the various stages also have at least one thermal conduction channel area that is smaller than the unit area of the associated headers.

In the multi-stage thermoelectric device depicted in FIG. 2, a high internal heat-flux exists within the individual thermoelectric stages (e.g., ~1800 W/cm² for a AT across each stage of 85 K to as high as ~2300 W/cm² with a AT across each stage of 107 K). Meanwhile, a low external heat-flux exists across the entirety of the thermoelectric device (e.g., a range from 15 to 30 W/cm²). In a multi-stage device, the packing fraction and hence the active flux through each stage can be different or similar to the active heat flux in other stages.

More specifically, the multi-stage thermoelectric device as illustrated in FIG. 2 can include a high-temperature thermoelectric conversion stage (i.e. the upper thermoelectric stage 16), for example an N-SiGe/P-TAGS thermoelement pair (e.g., with a ~100 µm active region thickness). TAGS refers to a Tellurium, Antimony, Germanium, and Silver (TAGS) alloy composition. TAGS compositions are in general denoted by (Ag5SbTe3) (GeTe)11. In an optimal composition according to some embodiments of the present invention for x, the GeTe mole fraction, is ~0.80 to 0.85. As illustrated in FIG. 2, the high-temperature thermoelectric conversion stage is coupled to a mid-temperature thermoelectric conversion stage (i.e. stage 17), for example an N-PbTe/P-TAGS thermoelement. As illustrated in FIG. 2, the mid-temperature thermoelectric conversion stage is coupled to a lower temperature thermoelectric conversion stage (i.e. the thermoelectric stage 18), for example an n-type and p-type Bi2Te3 superlattice-thin-film thermoelement pair having a 5 to 10 µm in thickness. As shown in FIG. 2, the lower header 23 constitutes a split-header having slits formed partially (in the top side and correspondingly at certain locations on bottom side not shown) in a body of the lower header 23 to provide thermal expansion relief. In some embodiments of the present invention, the splits are preferably not located near the devices.

The three-stage thermoelectric device depicted in FIG. 2 has a design efficiency in a range of 20% and electrical power density in excess of 5 W/cm², and is capable of power conversion in a range of tens of mWatts to as high as 1 MWatt when coupled to a heat source at temperatures approaching 875 K. Design efficiencies in excess of 20% and the capability to operate with hot-sides in the range of 675 to 875 K permit flexibility and adaptability to real-world systems. With hot-sides in the range of 675 to 875 K, higher Carnot efficiencies are available then would be available for example in thermoelectric devices restricted to hot-sides of 375 K to 575 K. In turn, higher Carnot efficiency provides for higher system efficiencies which in turn facilitates load balancing by reducing the number of modules (i.e., the number of thermoelectric pairs) required to convert a given heat flux into electrical power.

Materials Selection

While the concepts of some embodiments of the present invention are not restricted to any particular family of thermoelectric materials, the use of superlattice materials improves thermoelectric device efficiency of the multi-stage thermoelectric device of some embodiments of the present invention. Conventional bulk Bi2Te3 thermoelectric devices offered by Hi-Z Inc. (San Diego, Calif.) exhibits a power density of 0.34 W/cm² at a ΔT of 200 K for a specific power of about 0.165 W/gm. Yet, even unoptimized thin-film Bi2Te3 superlattice mini-module devices fabricated by the HAF-LIOF aspect of some embodiments of the present invention, even without the mid and high temperature thermoelectric power conversion stages discussed above, have demonstrated a power density of 0.7 W/cm², with a ΔT of 77 K, and a specific power of 16.7 W/gm. Specific power is defined as the power produced per unit weight of the thermoelectric device. Both the specific power and the power density levels would increase with the addition of mid and high-temperature stages and further optimization of the low-temperature superlattice stage. Accordingly, thermoelectric devices of some embodiments of the present invention may realize a specific power greater than 1 W/gm and a power density greater than 0.5 W/cm².

On the other hand, specific powers in a range of less than 0.0001 W/gm, 0.001 W/gm, and 0.01 W/gm, are possible with some embodiments of the present invention and are applicable to applications such as for example bio-medical devices. In these applications, the HAF-LIOF devices could be used for heat gathering from low temperature sources in a range of about 30-40° C, such as the human body for the powering of pacemakers or neuro-stimulators used to alleviate symptoms of Parkinson’s disease or other neurological disorders.

FIG. 3 is a graph depicting variations of ZT with temperature for various material systems useful in some embodiments of the present invention. Knowledge of the variation of ZT with temperature in suitable temperature-stable material systems, such as shown in FIG. 3, permits appropriate materials selection for the above-described multi-stage design. The material selections should, according to some embodiments of the present invention, provide a material for each thermoelectric stage which is robust in the temperature range in which the thermoelectric stage is intended to operate. For example, devices in PbTe/PbSe and Si/Ge superlattice material systems would be useful for a temperature range of 475 K-675 K and 675 K-875 K, respectively, in some embodiments of the present invention.

The relevant properties, the lattice-mismatch and the bandgaps, of the PbTe/PbSe superlattice system are shown in Table 1.
Both materials PbTe and PbSe have similar thermal expansion coefficients, so that lattice mismatch at higher temperatures would be similar to that at 300K. Also, K(T) at the temperatures of 500 to 650 K is about 0.05 eV, comparable to or larger than the bandgap difference between PbTe and PbSe. Thus, no barriers or quantum confinement effects will be present within the material, but a significant thermal conductivity reduction is expected in these superlattice materials.

Regarding the SiGe materials family, Si/Ge superlattice materials, according to some embodiments of the present invention, are attractive for high temperature applications (i.e., 650 K to 850 K). For example, Si/Ge superlattice materials deposited at about -1000 K have shown a dramatic reduction in thermal conductivity and concomitantly an enhancement in ZT. Although Si/Ge superlattices may only offer a ZT of only about -0.8 at 300 K, significantly below that of a Bi$_2$Te$_3$/Sb$_2$Te$_3$ superlattice or a Bi$_2$Te$_3$/Bi$_2$Te$_3$/Se$_2$ superlattice, the Si/Ge superlattices are likely to offer a much higher ZT at the higher temperatures employed in the upper thermoelectric stages depicted in FIG. 2. Further, the SiGe superlattices will have higher ZT values than associated SiGe alloys of the same Ge concentration, leading to higher efficiencies. Indeed, development of high ZT thin films in the PbTe/PbSe and in the SiGe material systems have been described by M. Lee et al. in Appl. Phys. Lett., 70, 2957 (1997) and R. Venkatasubramanian, Phys. Rev. B 61, p. 3901 (2000) and by R. Venkatasubramanian et al. in Proc. of 17th International Conference on Thermoelectrics, 191 (1998), the entire contents of which are incorporated herein by reference.

In addition to superlattices, other quantum-confined structures and structures can be utilized according to some embodiments of the present invention in which a strong thermal conductivity reduction is obtained while at the same time maintaining electrical conduction across the thermoelectric stages. For example, PbTe-based quantum-dot superlattices (QDSL) are suitable materials for the n and p-type thermoelements according to some embodiments of the present invention. ZT values for these materials are achievable in a range of 1.5 to 2, in the temperature range of 450 K-550 K.

Furthermore, even ZnSb and skutterudides, (i.e., materials with a known ZT >1 over a temperature range suitable for power conversion) are also applicable according to some embodiments of the present invention provided these materials are in thin substrate form (i.e., in a thickness of 1.00 to 200 μm) and are used in a temperature range of 500 K to 900 K. Thus, the HA-F-LOF, high-power density, multi-stage power conversion device concept according to some embodiments of the present invention is not limited to Bi$_2$Te$_3$-superlattice/PbTe/SiGe material combinations. Indeed, superlattices of Si/Ge, PbTe/PbSe, ZnSb/CdSb, InAs/InSb, CdTe/HgCdTe, Ga$_n$In$_{1-n}$As/Ga$_n$In$_{1-n}$As can be used in the high-temperature and mid-temperature thermoelectric conversion stages, discussed above, thus providing a cascade thermoelectric device utilizing all superlattice materials.

For the lower temperature thermoelectric conversion stages according to some embodiments of the present invention and for single stage cooling devices operating near room temperature, superlattice stages of Bi$_2$Te$_3$—Sb$_2$Te$_3$ can be used. FIG. 4 is a graph depicting state-of-the-art ZT vs carrier concentration for p and n-type Bi$_2$Te$_3$-based superlattice elements. FIG. 4 shows a ZT in -3.5 in p-type superlattices and -2.0 in n-type. According to some embodiments of the present invention, by control and engineering of dopant carrier levels, the 500 K figure-of-merit (ZT) achievable with p-type Bi$_2$Te$_3$/Sb$_2$Te$_3$, and n-type Bi$_2$Te$_3$/Bi$_2$Te$_3$/Se$_2$ superlattice device elements is improved from previously known values of -2.4 and -1.2 to values greater than 3.5 and -2, respectively. The carrier levels in the p-type materials as shown in FIG. 4 are controlled by varying the organometallic Tellurium flow-rate during growth, for a fixed growth rate of the superlattices which in turn can be controlled by the flow-rate of the organometallic Bismuth for Bi$_2$Te$_3$, and organometallic Sb for Sb$_2$Te$_3$. The carrier levels, for a constant growth rate, can also be controlled by control of growth temperature over a limited range. For the n-type materials, the doping levels as shown in FIG. 4 can be controlled by the growth rates of Bi$_2$Te$_3$, and Bi$_2$Te$_3$/Se$_2$/Sb$_2$Te$_3$ layers in the superlattice as well as the growth temperatures. A value of peak ZT of about ~2.9 demonstrated according to some embodiments of the present invention for a 10 Å/(Angstrom)/50 Å/(Angstrom) p-type Bi$_2$Te$_3$—Sb$_2$Te$_3$ superlattice is one of the highest peak ZT values observed at 300 K for the p-type Bi$_2$Te$_3$—Sb$_2$Te$_3$ superlattice material system. Such improvements in ZT may permit improved power conversion efficiencies and cooling efficiencies for the thermoelectric devices according to some embodiments of the present invention.

#### Device Performance

In some embodiments of the present invention, the advances in ZT for the p and n-type superlattice materials have been incorporated into fabricated p-n thermoelement couples. By flipping the fabricated p-n couples onto a split semi-infinite Cu-plate as opposed to flipping the fabricated p-n couples onto a header with a limited-thickness metallization, a more accurate measure of the thermoelectric properties of the fabricated p-n thermoelement couples is possible. For instance, each one of the p-n thermoelement couples potentially carries a high-current (i.e., several Amps of current) and is a low-voltage thermoelectric device. Parasitic lead resistances can therefore affect the measured device efficiencies. Properties of the p-n thermoelement couples have been developed by fabrication and analysis of the p-n thermoelement couples on a split semi-infinite Cu-plate. In the fabricated thermoelectric devices, electrical contact resistances in the thermoelectric devices may be reduced and/or minimized between the metallizations and the p-n thermoelement couples, providing adequate electrical interfacing.

In addition to managing electrical contact resistances, thermal interface resistances may be reduced in the metal-to-dielectric interfaces according to some embodiments of the present invention by deep-anneling of a metal into the dielectric bulk or by utilizing an AlN-diffused Al—Cu interface.

Further, high aspect-ratio thermoelectric devices (either with thicker superlattice films or smaller-area devices) are provided by appropriate patterning and etching of the p-n couples (e.g., the thermoelectric pair 2a and 2b). An aspect ratio of the element is defined as the ratio of thickness/area of...
element in units of cm\(^{-1}\). Typical thickness of thermoelectric elements in the low-temperature stage can be about 5 μm to 20 μm (microns), while the mid and high temperature stages can have thicknesses ranging from 50 μm to 250 μm (microns). The aspect ratio, hence the area of each element of the various stages, are based on the thermal conductivity of the materials (noting that the thermal conductivities of the p and n-type elements within a stage can be different and so their aspect ratios to allow same ΔT (temperature differential) across both p and n-type elements of each stage can be different) of the various stages and the required ΔT (temperature differential) for each stage for increasing and/or maximizing the efficiency of the overall set of stages. The ΔT (temperature differential) of each stage is inversely proportional to thermal conductivity of the material and directly proportional to the aspect ratio. Hence, according to some embodiments of the present invention, the total heat flux through each stage is same; thus the aspect ratio (and the associated packing fraction) in each stage is adjusted with this criterion to meet the design ΔT for each stage.

**[0075]** Power conversion efficiencies achievable in, for example, the three-stage thermoelectric devices according to some embodiments of the present invention are calculable based on known equations. The maximum efficiency is obtained when the load ratio \(r\), defined as \(R_L/R_s\), with \(R_s\) being the load resistance and \(R_L\) being the thermoelectric device internal resistance, is optimized for a given ΔT over the entire temperature range, \(T_{\text{MN}}\). See, for example, H. J. Goldsmid, Electronic Refrigeration, Pion Limited, (1986).

**[0076]** Once \(r\) is known as per eqn. (1) shown below, the device efficiency \(\eta\) can be obtained by eqn. (2), shown below for a given \(\Delta T\) (temperature differential), and mean operating temperature \(T_{\text{MN}}\):

\[
r = (1 + \frac{\Delta T}{T_{\text{MN}}})^{1/2}
\]

\[
\eta = \frac{\Delta T}{(r + 1)(r - 1)T_{\text{MN}} + \Delta T/2}
\]

**[0077]** Power conversion efficiency estimates are shown in Table 2 of FIG. 5, for a range of ZT values for each stage. The power conversion efficiency estimates shown are in a range from upper to midrange to lower projected values. The projections in Table 2 indicate that an efficiency in the range of 9.6% to 11.4% for a ΔT (temperature differential) of 150°C in the low-temperature \(Bi_2Te_3\)-SL-based stage can be realized for a ZT value of 2.5. An efficiency in the range of 4.3% to 4.7% for a ΔT (temperature differential) of 175 to 200°C in the \(n\)-\(PbTe/p\)-TAGS-based thin-substrate high-temperature stage can be realized for a ZT of 0.75. An efficiency in the range of 3.4 to 3.7% for a ΔT (temperature differential) of 200°C in the \(n\)-\(SiGe/p\)-TAGS thin-substrate high-temperature stage can be realized for a constant ZT of 0.75. Thus, according to some embodiments of the present invention, a thermoelectric efficiency of about 19.4% to 17.7% and a power density in excess of 5 W/cm\(^2\) may be obtainable in three-stage thermoelectric power conversion devices.

**[0078]** Indeed, Table 2 illustrates the performance of various stages of a three-stage thermoelectric device according to some embodiments of the present invention as a function of ZT and the efficacy of thermal management at the heat-sink. The calculations in Table 2 are based on a module size of approximately 33 cm\(^2\). For these examples, a heat flux of about 30 W/cm\(^2\) is assumed to flow from the heat-source (i.e., the upper-most header) to the heat-sink (i.e., the lower-most header), yielding a heat-flux dissipation range of about 24.7 to 22.7 W/cm\(^2\) at the heat-sink. The power densities are calculated assuming a 5 μm thick superlattice element in the low-temperature \(Bi_2Te_3\)-super lattice stage and assuming a 100 μm thin-substrate for bulk thermoelements in the mid and high temperature stages. Table 2 indicates that higher ZT materials for both the mid-stage (460 K to 660 K) and high-stage (670 K to 890 K) may be advantageous.

**[0079]** For a given heat flow \(Q\) in Watts, the aspect ratio determines the ΔT. The efficiency is a function of ΔT (temperature differential) and ZT. The power generated \(P\), in Watts, is a product of Q times efficiency. Thus, power density, \(P_d\), is a function of both area, thickness, ZT and Q. Hence, according to some embodiments of the present invention, one approach to achieve power densities of greater than 20 W/cm\(^2\) is to use thinner sections of thermoelement materials (e.g., preferably less than 300 μm).

**[0080]** Calculations of thermal-to-electrical conversion efficiency, corrected for lead resistances, versus internal ΔT across the flipped inverted p-n couple, and the ZT obtained from the efficiency equations indicate that about 85% of the external ΔT (and consequently the heat flux) is applied across the device. The 15% loss is primarily due to the thermal interface resistance between the metalization and the MN header. According to some embodiments of the present invention, the thermal interface resistance can be reduced in the metal-to-dielectric interface by deep-annealing the metal into the dielectric bulk or by utilizing an AlN-diffused Al—Cu interface, as discussed above.

**[0081]** Calculated ZT values of the inverted couples utilized for demonstration of power conversion concepts of some embodiments of the present invention were about a ZT value of 1.1 at 300 K. The average ZT of the p-n couple of some embodiments of the present invention (e.g., the thermoelectric pair \(2a\) and \(2b\)) increases with temperature, consistent with the general trend of ZT shown in FIG. 3.

**[0082]** One p-n couple of some embodiments of the present invention was tested up to a ΔT of nearly 85 K, corresponding to an active device heat flux within the thermoelement of about 1800 W/cm\(^2\). For this tested p-n couple, the external heat flux was about 28 W/cm\(^2\) with a temperature rise of about 28 K at the heat-sink. Application of improved thermal management practices to operate even this test device with a ΔT of 150 K, even with the present ZT of ~1.5, will permit an efficiency of ~8.6% to be realized. Improvements in ZT values from 1.5 to ~2 may realize in some embodiments of the present invention efficiencies of ~11% for a ΔT of 150 K.

**[0083]** Accordingly, some embodiments of the present invention may include a system for thermoelectric power conversion. The system includes a thermoelectric pair of n-type and p-type thermoelements, a first header coupled to one side of the thermoelectric pair, a second header coupled to a second side of the thermoelectric pair, a thermal impedance increasing device disposed between the thermoelectric pair and one of the first and second headers, and a heat sink coupled to the second header which dissipates heat at a rate which maintains a temperature of the second header below a temperature of the first header. Further, a coupling member can be used to couple the first header to a heat source. The heat source can be a combustion source, a radioactive source, a solar-heated source, and an electrical power device. The coupling member in some embodiments of the present invention can be a thermally conducting member having a thermal conductance of at least Al and extending between said first header and said heat source. Alternatively, the coupling mem-
ber can be a steam pipe or a combustion exhaust pipe transporting heat flux by a convective medium such as, for example, steam or combustion gases.

[0084] FIG. 6A is a schematic illustration depicting a thermoelectric device module according to some embodiments of the present invention integrating a series of p-n couples on a single stage. Tests on p-n couple devices for open-circuit voltage (Voc), power (P), and power density (PD in W/cm²) are shown in FIG. 6D. Tests on an integrated 16 p-n couple devices show expected open-circuit voltage (Voc), power (P), and power density (PD in W/cm²). In particular, the open-circuit voltage has been observed to scale in the thermoelectric module to almost sixteen times that of a single-couple, for similar ΔT to the individual p-n couple, further supporting the HAF-LIOF concept. The power levels of 38 mW per couple, for a 600 μm×600 μm device and for a ΔT of about 107 K correspond to an electrical power density of as much as about -40.2 W/cm². The power level scales to 166 mWatts per couple for the 16-couple module for a ΔT of 77 K.

[0085] Both p-type and n-type thin-film superlattice thermoelements of some embodiments of the present invention have been stable. Exposures to temperatures of about -450 K and times of up to 60 hours have shown no marked deterioration in the device ZT of these elements, as shown in Table 3, below.

<table>
<thead>
<tr>
<th>Type</th>
<th>ZT as made</th>
<th>ZT after Tanneal</th>
<th>ZT after Tanneal</th>
<th>ZT after Tanneal</th>
<th>ZT after Tanneal</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td># 0 hrs.</td>
<td>~15 hrs.</td>
<td>~30 hrs.</td>
<td>~45 hrs.</td>
<td>~60 hrs.</td>
</tr>
<tr>
<td>P</td>
<td>1.7 ± 0.25</td>
<td>2.0 ± 0.25</td>
<td>2.25 ± 0.25</td>
<td>2.25 ± 0.25</td>
<td>1.95 ± 0.25</td>
</tr>
<tr>
<td>N</td>
<td>0.59 ± 0.1</td>
<td>0.68 ± 0.1</td>
<td>0.84 ± 0.15</td>
<td>0.71 ± 0.1</td>
<td>0.76 ± 0.15</td>
</tr>
</tbody>
</table>

[0086] Besides superlattices, the device fabrication methodologies and HAF-LIOF aspect of some embodiments of the present invention are applicable to some substrates from two non-superlattice material systems, GaSb and InAs, corresponding to the bandgaps of the n-SiGe/p-TAGS and n-PbTe/p-TAGS systems. Open-circuit voltage as a function of ΔT in a 100 element GaSb and InAs thin-substrate module of some embodiments of the present invention are capable of Voc values of ~4.5 Volts to ~3.5 Volts and are capable of generating AT in excess of 100 K, corresponding to active heat fluxes of ~300 W/cm², needed for achieving high electrical power densities.

Manufacure of the Thermoelectric Devices and Modules

[0087] Various methods are available for the manufacturing of the devices and the device components of some embodiments of the present invention. Given below for purposes of illustration are steps and methods involved in fabricating the individual p and n-type thermoelectric pairs of some embodiments of the present invention and are steps and methods for integration of the thermoelectric pairs into modules. The steps and method described below are illustrative and are not given to imply any limitations of some embodiments of the present invention.

[0088] The thermoelectric materials utilized as the p and n-type thermoelements of some embodiments of the present invention are typically overgrown films on commercial substrates, the overgrown films having a thickness of, for example, 5 to 20 μm. Substrates for the growth of, for example, the thin-film superlattices or other thin film thermoelectric structures, may have the same conductivity type as the overgrown films or may permit the overgrowth of opposite conductivity type films. The overgrown films can be metallized to provide a low-resistance contact, such as a low-resistance Peltier contact.

[0089] In one fabrication method of some embodiments of the present invention, fabrication of the thermoelectric devices of some embodiments of the present invention is facilitated by inverted-couple processing. Table 4 shown in FIG. 6C illustrates the inverted processing approach of some embodiments of the present invention. In inverted-couple processing, one leg of a p thermoelement and one leg of an n thermoelement are attached to a common electrical member adjoining the two elements. Fabricating the individual n-type and p-type thermoelements in each leg of the thermoelectric power conversion stages can occur in one example of some embodiments of the present invention by forming n-type and p-type films on separate substrates, and then attaching the individual n-type and p-type thermoelements to a common header.

[0090] Alternatively, films of a specific type can be formed on a common substrate and then selectively converting (e.g. by selective ion implantation) different regions of the formed thermoelectric material into n-type and p-type regions. For example, the thermoelements could be formed intrinsic (or specifically doped) and then type-converted to another (i.e., a p-type to n-type conversion or an n-type to p-type conversion) by for example impurity-diffusion. Type-conversion would then be performed at a convenient stage in the manufacturing process. Regardless of the specific details, a set of p and n-type materials having a pre-arranged pattern are attached to a common header like SiC, AlN, low-resistivity silicon, and silicon with a thin insulating layer.

[0091] In one fabrication method of some embodiments of the present invention, substrates including the individual n-type and p-type thermoelements are separated, for example, by scribing or laser dicing, into individual segments. The individual segments are then bonded onto a header such that alternating n-type and p-type conductivity materials exist between each adjacent thermoelement. The surfaces of the header that come in contact with the n- and p-type segments are preferably metallized prior to assembly to provide low-resistance electrical connection between adjacent n- and p-type segments where necessary to electrically interconnect adjacent thermoelements. Likewise, the surfaces of the individual n-type and p-type thermoelements that come in contact with the header are preferably metallized prior to assembly to provide the necessary low-resistance electrical connection to the n-type and p-type thermoelements, else a high electrical contact resistance can limit the efficiency of the thermoelectric stage and the resultant thermoelectric device.

[0092] Following bonding of n- and p-type segments, the substrates from each of the p- and n-segments are selectively
removed, for example, by using selective etchants. The thermoelements are then patterned using photolithographic patterning followed, for example, by etching, or by laser ablation, to produce a desired cross-sectional thermal conduction area for some embodiments of the present invention (i.e., to set the aspect ratio and ultimately determine the packing fraction). Low resistivity contact metallizations are then evaporated on an upper surface of the n- and p-type thermoelements. In this step, either the same metallization can be used for both of the n- and p-type section, or different metallizations can be used (i.e., separate evaporations), depending on the contact resistance requirements. Sheet resistances, or conductances as specified above, associated with the metallizations are designed not to restrict the performance of the thermoelectric devices:

[0093] A top, pre-patterned metallization header can, in some embodiments of the present invention, be attached to the metallized sections to function as the aforementioned heat pipe. Alternatively, the header itself prior to metallization can be patterned to provide the aforementioned heat pipe. The formed pair of thermoelements (i.e., the n-thermoelement and the p-thermoelement) including the attached header can then be flipped and bonded to a second header. The second header, referred to for the purpose of illustration as a bottom header, thermally connects the n-thermoelement to the p-thermoelement, but contains patterned electrical connections such that electrically the n-thermoelement and the p-thermoelement are individually connected, as shown in FIGS. 1A and 1B. The bottom header thus functions as an electrical member having, as shown in FIGS. 1A and 1B, a split electrical contact (i.e., an electrical contact only contacting individually the n-type and p-type thermoelements), while as a thermal member the bottom header functions as a continuous thermal contact. Regardless of the formation approach (i.e., direct deposition or bonding), thick metallizations and patterning can be used, according to some embodiments of some embodiments of the present invention, to form the noted bottom header and to provide the aforementioned split electrical contact. Direct attachment by deposition or bonding would permit a large number of patterned thermoelements each possessing the requisite thermal conduction area to be fabricated and electrically connected in series to provide either an output electrical contact for power conversion or for cooling. Subsequent stages of thermoelectric devices could then be added using similar procedures, or by attaching subsequent pre-fabricated stages, or by attaching selective members of subsequent stages.

[0094] One illustrative example of inverted couple processing is given below:

[0095] P-type and n-type superlattice thermoelectric films are deposited on GaAs substrates. The deposited superlattice films are patterned with Cr/Au/Ni/Au metallizations. The deposited superlattice films and/or the GaAs substrates are etched in preparation for dicing. Diced strips of the p-type and n-type superlattice films attached to the GaAs substrates are then bonded in an alternating conductivity type pattern to a header. The header includes an AIN substrate having Ti/Au metallization (annealed) and having a subsequent Cu/No/Au topmost metallization. A Sn preform bonds the diced strips to the AIN substrate (functioning as a first header). The GaAs substrate is then etch removed, and the Cr/Au/Ni/Au contacts are evaporated through shadow masks or evaporated and patterned to form electrical contacts to the superlattice thin films. Thick metal pads are then formed on the evaporated contacts to define, for example, a heat pipe structure. Dies containing the superlattice thin films and the attached AIN header are placed and bonded to a separate split metallized header (functioning as a second header) allowing for individual electrical connection to each of the n- and p-type thin film thermoelements.

[0096] By way of example, Table 5 depicts various bonding steps used to fabricate the three stage device shown in FIG. 2.

[0097] As depicted in Table 5 in stage 3 of the thermoelectric device (i.e., the uppermost header), a preferred heat spreader is AIN or Si. In this stage, a AgCu eutectic is used as a solder material for bonding the heat spreader to the metallization layers on the afore-mentioned N—SiGe/P—TAGS thermoelements. Metallization layers on the N—SiGe/P—TAGS thermoelement pair include silver having a typical diffusion barrier layer of W or Mo or Ni or similar refractory material to prevent diffusion of Ag into the N—SiGe and P—TAGS materials.

### Table 5

<table>
<thead>
<tr>
<th>BONDING STEP PROCESS</th>
<th>Heat Spreader</th>
<th>Solder Material</th>
<th>Interconnect Metallization and Resistivity at Mean Operating Temperature</th>
<th>Solder Diffusion Barriers</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 In Stage 3 of the Cascade: 1050 K</td>
<td>AIN or Si</td>
<td>AgCu (72/28)</td>
<td>Silver (ρ = 4.5 μΩ cm)</td>
<td>W (sputtered) Mo (E-beam)</td>
</tr>
<tr>
<td>2 In Stage 2 of the Cascade: 800 K</td>
<td>AIN or Si</td>
<td>AgAuGe (45/38/17)</td>
<td>Silver (ρ = 3.3 μΩ cm)</td>
<td>N/A</td>
</tr>
<tr>
<td>3 In Stage 1 of the Cascade: 505 K*</td>
<td>SiC</td>
<td>Sn</td>
<td>Copper (ρ = 2.3 μΩ cm)</td>
<td>Ni (E-beam or plated) N/A</td>
</tr>
<tr>
<td>4 Of Heat Source to Stage 3 at 975 K</td>
<td>N/A</td>
<td>AgCuP (15/80/5)</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>5 Of Stage 2 to Stage 3 (with Heat Source) at 738 K</td>
<td>N/A</td>
<td>AuIn (75/25)</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>6 Of Stage 1 to Stage 2 (with Stage 3 and Heat source) at 490 K</td>
<td>N/A</td>
<td>SnAu (90/10)</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>7 Of Heat sink to bottom of Stage 1 at 395 K</td>
<td>N/A</td>
<td>InSn (52/48)</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>
As depicted in Table 5, in stage 2 of the thermoelectric device, a preferred heat spreader is AlN. In this stage, a AgAuGe eutectic is used as a solder material for bonding the heat spreader to the metallization layers on the afore-mentioned N—PbTe/P-TAGS thermoelement pair. Metallization layers on the N—PbTe/P-TAGS thermoelement pair include silver having a typical diffusion barrier layers of Ni or W or Mo to prevent diffusion of Ag into the N—PbTe and P-TAGS materials.

As depicted in Table 5, in stage 3 of the thermoelectric device, a preferred heat spreader is SiC. In this stage, a Sn eutectic is used as a solder material for bonding the heat spreader to the metallization layers on the eutomer-mentioned n- and p-type Bi₂Te₃-superlattice-thin-film pair. Metallization layers on the n-type and p-type Bi₂Te₃-superlattice-thin-film pair include Cu having a diffusion barrier layer of Ni or a similar metal to prevent diffusion of Cu into the N-Bi₂Te₃, SL and/or P-type Bi₂Te₃, SL materials.

As depicted in Table 5, the uppermost stage (i.e., stage 3) can be bonded to the heat-source header (e.g., a Cu plate) using a AgCuP eutectic bond. Stages 2 and 3 can be eutectic bonded together using a AuAl eutectic. Stages 1 and 2 can be eutectic bonded together using a SnAu eutectic. Stage 1 can be bonded to the heat-sink header (e.g., an Al plate) using an InSn eutectic bond. Hence, in some embodiments of the present invention, successively-lower-melting point eutectics may bond the successive stages so that the previously-bonded stages are in tact. Such measures serve to match or reduce the mismatch in the coefficients of thermal expansion between the various stages as successive bonding can cause thermal stress.

An example of stacking of the various stages to obtain efficient thermal interfaces between each of the adjacent stacks by using eutectic metal bonding is described by R. Venkatasubramanian et al. in Appl. Phys. Lett., Vol. 60, 886 (1992), the entire contents of which are incorporated herein by reference.

Integration of Thermoelectric Devices and Modules to Semiconductor Chip Packages

A thermoelectric device according to some embodiments of the present invention can be attached to an integrated circuit die or wafer element (preferably to the backside) with or without an intervening layer of thermal grease or plastic adhesive. For direct attachment without intervening layers of thermal grease or plastic adhesive, a thin electrically insulating layer or a series of back-side p-n isolation junctions can be utilized to prevent electrical isolation of the integrated circuit on the die from the currents flowing in the thermoelectric devices. In this approach, the “top” header joining the thermoelectric device of some embodiments of the present invention to the integrated circuit die is made of thick metallizations which form the electrical contact and the heat pipe to the p-n thermoelements. Suitable thermoelectric materials deposition/attachment/formation, type conversion, and patterning form the p-n thermoelements and the heat pipe structures. Subsequent metallizations complete a “bottom” header and provide in some embodiments of the present invention a place for attachment to a heat sink device (e.g., an air-cooled plate or a heat-pipe).

FIG. 7A is a schematic depicting the bonding of a pre-fabricated thermoelectric device 72 to a semiconductor device chip 74. In this approach, bonding is used to bond the pre-fabricated thermoelectric devices to an integrated circuit die. As such, this approach separates the thermoelectric device fabrication steps from the semiconductor device chip.

In this approach, a number of bonding techniques (to be discussed below) can be used to join an upper header 75 of the pre-fabricated thermoelectric device 72 to the semiconductor device chip 74. Accordingly, in the attached structure, heat from power dissipating devices 76 in the semiconductor device chip 74 will be pumped through the thermoelements 73 and dissipated at a heat sink (not shown) attached to the lower header 77.

FIG. 7B is a schematic depicting the attachment of a thermoelectric device without a top header onto a semiconductor device chip according to some embodiments of the present invention. Specifically, FIG. 7B depicts the bonding of pair of thermoelements 73 to the semiconductor device chip 74. As shown in FIG. 7B, the bonding to the semiconductor device chip 74 is facilitated by the pre-deposition or growth of an electrically insulating layer 82 on the semiconductor device chip 74 (e.g., silicon dioxide formation on a Si device wafer). As shown in FIG. 7B, the semiconductor device chip 74 itself serves as a header spreading heat from power dissipating devices 76. Thus, in some embodiments of the present invention, the thermoelements are attached directly to the semiconductor device chip 74 without the utilization of a top header.

FIG. 7C is a schematic depicting the sequential formation of a thermoelectric device 72 on some embodiments of the present invention onto a semiconductor device chip 74. In this approach, the fabrication process of some embodiments of the present invention may utilize bonding at separate steps in the process to bond thermoelectric materials and/or superlattice layers to other layers of the thermoelectric device, and to provide a mechanism for direct attachment of the thermoelectric devices of some embodiments of the present invention to the semiconductor device chip 74.

In the simplified process depicted in FIG. 7C, at step (a), an electrically insulating layer 82 is formed on the semiconductor device chip 74. The layer 82 can be a thermal oxide grown on a Si device chip; the layer 82 can be a deposited oxide such as SiO₂ or Si₃N₄ deposited, for example, by sputtering or vapor deposition. At step (b), metallizations 83 (including interconnections between the thermoelements not shown for the sake of simplicity) are deposited and patterned in accordance with the layout of the thermoelectric devices 72 on the semiconductor device chip 74. The metallizations 83 can include, for example, materials and structures to form the heat pipe 5, described in FIG. 1. At step (c), pairs of thermoelements 73 are attached (deposited or bonded) to the metallizations 83. The pair of thermoelements 73 can include, for example, the features of the thermoelectric device 70 shown in FIG. 1. At step (d), a set of metallizations 85 are formed on thermoelements 73. At step (e), contact and annealing using the procedures detailed below complete the fabrication by joining a header 84 to the metallizations 85.

Accordingly, various approaches of some embodiments of the present invention may include:

(1) attaching a pre-fabricated thermoelectric module to a device wafer,
(2) building a thermoelectric device from the backside of a device wafer, or
(3) building a part of a thermoelectric device onto the backside of a device wafer (e.g., building heat pipes
onto the backside of a device wafer), and completing fabrication by attachment of remaining pre-fabricated components.

For attachment, several attachment methods can be used including: (1) soldering, (2) brazing, (3) friction bonding, and (4) insulator-insulator bonding similar to wafer bonding. Furthermore, in a preferred embodiment, a hybrid "reactive" bonding process is utilized in which insulator surfaces, having a thin reactive metal layer, are placed opposed to one another and then contacted and heated to react the metal layer with the insulating layers and thereby bond the opposed components together. Such a metal include, for example, Ti, W, Cr, Mo, etc., or alloys thereof. These metals readily oxidize and form in a preferred embodiment silicides which melt at temperatures of 300° C. or less. The hybrid reactive bonding process of some embodiments of the present invention relies on the reactivity of the thin metal layer with the respective insulators to achieve a bond. In some embodiments of the present invention, the metal layer is preferably thin (e.g., less than 500 Å) such that all of the reactive layer is consumed, or reacts with, the insulating layers. In hybrid reactive bonding, bonding is achieved when the surfaces are brought into contact and then heated such that the metal reacts with one or both insulating surfaces.

Furthermore, friction bonding according some embodiments of the present invention can be used to bond thermoelectric materials and/or superlattice layers to other layers on the thermoelectric device and provide a mechanism for direct attachment of the thermoelectric devices of some embodiments of the present invention to an integrated circuit die or wafer element. Friction bonding can be implemented with interposing reactive layers. In friction bonding, linear motion over a short distance using an ultrasonic transducer provides the friction necessary to produce heating at the surface that will produce the bond. Heating to a high fraction of the melting temperature and then using a friction bonding technique to produce local heating and thereby for instance melting or plastic deformation at the contact surfaces can produce a suitable bond. Heating from one direction and cooling from another side can be used to locally heat to a small area near the contact surfaces. Small amounts of material or thin sheets of material in a perform cut to die or strip size to match the thermoelectric component parts.

Materials in thin sheets or thin film form may be used, according to some embodiments of the present invention, to provide for a buffer that protects the thermoelectric superlattice materials during the friction bonding. Materials in thin sheets may reduce and/or avoid chemical damage to the top layers of the thermoelectric materials. The thin layer is selected to form a eutectic that allows friction bonding. In friction bonding, the surfaces of the materials to be bonded can be roughened if necessary to improve the friction and thus the efficacy of forming a friction bond.

Further, diffusion bonding or thermal annealing can be used to bond the thermoelectric devices to a semiconductor device chip.

Bonding can occur between a top header of a thermoelectric devices and a semiconductor device chip by any number of the processes described herein, and can utilize a bonding material to facilitate coupling of the semiconductor device chip to the semiconductor device chip. Regardless of approach, a thermally conductive and mechanically stable connection or bond is preferred between the top header and the semiconductor device chip. Bonding to the semiconductor device chip to the thermoelectric devices of some embodiments of the present invention can be accomplished in the following non-limiting examples by:

1. utilization of thermal adhesives or thermally conductive epoxy,
2. soldering,
3. diffusion bonding using electroplated or evaporated metal contacts,
4. utilization of anisotropic thermal adhesives,
5. utilization of thermoplastic conductive polymers, and
6. utilization of silicon to silicon molecular bonding (in the case where the cooling header of the thermoelectric device is made from silicon).

Heat flux from the semiconductor device chip can be dissipated from the thermoelectric devices of some embodiments of the present invention by a heat sink operating at a temperature above that of the semiconductor device chip. Moreover, once bonded, the attached thermoelectric devices of some embodiments of the present invention, when not cooling, can sense a heat flux from the chip and thus can provide active sensing of the device chip performance. A template of such thermoelectric devices can therefore, in some embodiments of the present invention, provide a mapping of device component utilization (i.e., those device components having higher utilizations will produce higher amounts of heat flux into the proximate thermoelectric devices).

Thus, as illustrated above, some embodiments of the present invention can utilize a number of approaches using bonding to facilitate thermal transfer by thermal conduction from one thermoelectric power conversion stage to another. Such techniques and other techniques known in the art can be used to appropriately bond the various stages together. These approaches, according to some embodiments of the present invention, realize high-quality thermal interfacing.

Another alternative approach according to some embodiments of the present invention for integrating the various thermoelectric conversion stages utilizes radiant thermal energy transfer using Purcell-enhancement cavity transmitter/receiver structures such as those described in the aforementioned U.S. Provisional Application No. 60/253,743, the entire contents of which are incorporated herein by reference, entitled "Spontaneous emission enhanced heat transport method and structures for cooling, sensing, and power generation" for heat transfer from one thermoelectric power conversion stage to another. In this approach, the radiant portion, if not the dominant process, plays a substantial role in managing thermal stress by providing less-rigidly-bonded interfaces. FIG. 9 is a schematic illustration in which radiant coupling is used between adjacent thermoelectric conversion stages.

As shown in FIG. 8 a heat source 14 is coupled via radiant coupling mechanism 216 to a thermoelectric stage 16. Stage 16 is in turn coupled via radiant coupling mechanism 217 to the thermoelectric stage 17. Stage 17 is in turn coupled via radiant coupling mechanism 218 to the thermoelectric stage 18. Electrical connections 220 provide connections to the thermoelements on each stage.

Further, some embodiments of the present invention can utilize Purcell enhancement from an enhanced density of radiative modes in small-scale structures (similar to enhanced electronic density of states in quantum-confined systems) for
enhanced spontaneous emission using patterned/um-size-range, appropriately-spaced, structures for specific temperatures, on the heat spreader. Thus, engineered micro-fins can also potentially enhance spontaneous radiative heat transport. These um-size geometries are achievable with photolithography and large-area wafers for a cost-effective implementation.

[0127] Spontaneous emission enhanced heat transport (SEEHT) may additionally enhance emission at infra-red wavelengths near 300 K. The incorporation of micron or sub-micron size Purcell cavities, will provide for the theoretical maximum radiative emission at peak wavelengths of 10 μm which will enhance heat transport by as much as a factor of 1000 at 300 K, leading to a radiative dissipative flux of $\Phi_{\text{SEEHT}}$ of 44 W/cm². Such micron size particles incorporated by impregnation or self-assembly, followed by overgrowth, permit the scope for radiative heat transfer mechanisms to be considerably enhanced. Such particles can further be incorporated in high-thermal conductivity heat spreader such as SiC, AlN, Si, diamond, etc. Enhancement of such intensities, even compared to highly-emissive (Ti) surfaces, showing both structure dependence and wavelength dependence, is shown in FIG. 9. Indeed, FIG. 9 is a plot of apparent emission intensity as a function of the surface temperature of different engineered structures according to some embodiments of the present invention. As such, in some embodiments of the present invention, a radiative coupling mechanism includes a thermally conductive layer having dispersed therein particles including one of metal, semimetal, and semiconductor particles to thereby enhance black body radiation from the thermally conductive layer and support radiative heat transfer across the interfaces of the thermoelectric device components without the necessity of physical bonding.

[0128] While not limited to the following theory, some embodiments of the present invention recognize that of enhanced emission with these Purcell cavity structures can be further enhanced realized if there is matching of “increased density of states” in emitters with “increased density of states” with receivers/absorbers, i.e., resonant thermal energy transfer. In addition to “resonant thermal energy transfer” by Purcell-cavity effects, other “proximity coupling of radiative infrared modes” can be exploited as well, in some embodiments of the present invention. Utilization of radiation coupling will, according to some embodiments of the present invention, reduce thermal stress, by removing (strong) physical interfacial contacts between various stages. Further, the mechanical alignment of the resonant structures may not be a significant issue, given that the typical size of the inverted couple headers are ~300 μm x 300 μm. Thermoelectric Modules

[0129] For automatic assembly of the modules described above a diec and pick-and-place tools (standard to the IC industry) can be used. A wafer diec and robotic pick-and-place tool, provide not only cost-effective but also reliable fabrication of both mini-modules and large-scale modules. The tool is used to dice p-n couple dies from a processed wafer and to assemble these inverted couple dies into a range of devices, from mini-modules to large-array of mini-modules. The diec and pick-and-place tools, described above can also be used according to some embodiments of the present invention to assemble thin-substrate (i.e., 100 μm to 250 μm thick) bulk modules as well as substrate die containing the afore-mentioned superlattice thin-film structures.

[0130] In some embodiments of the present invention, large-scale headers are used, on which a large array of mini-modules are assembled to produce large-scale modules and proportionally larger powers.

[0131] FIG. 10 is a schematic arrangement of a three stage or unit thermoelectric device of some embodiments of the present invention having a split-header on a lower stage 18 to provide thermal expansion relief. In other embodiments of the present invention, the lower-stage 18 of the multi-stage thermoelectric device can be nearly instantly converted to a heater stage for short periods of time, thus reducing and/or avoiding catastrophic device damage due to, for example, an interruption in coolant flow, and further enhancing reliability. As such, FIG. 10 represents a multi-stage thermoelectric device of some embodiments of the present invention in which electrical reconfiguration reduces and/or avoids catastrophic failures during coolant flow loss to the lower stage 18 and thus the risk of deterioration of the thermoelectric properties of the thermoelements at this stage (i.e., due to deterioration of the thermoelectric materials and/or contacts) is minimized.

[0132] An electrical configuration for permitting reduction and/or avoidance of a catastrophic failure is depicted in FIG. 11. FIG. 11 is an electrical diagram showing an exemplary configuration for operating a thermoelectric device according to some embodiments of the present invention in either a heat pump mode or a power conversion mode. As shown in FIG. 11, each stage of a thermoelectric device 102 is temperature monitored by temperature monitor block 104. Each stage is electrically controlled/sensed by a switch block 106 and a controller 108. In a power conversion mode, the controller 108 supplies power out from the thermoelectric device 102. The controller can include filters and de-ac converters to output ac power or can include dc-de power converters to output higher voltage dc power than directly available from the thermoelectric device 102. FIG. 12 depicts a cooling system 110 which for illustrative purposes depicts a heat exchanger 112 utilized to pump with pump 114 a fluid to a heat sink plate 116. A flow sensor 118 monitors the flow of coolant to the heat sink plate 116. A temperature of the lower stage and the output power from the lower stage is monitored by a power unit 120. In the event of coolant failure, the controller 108 can electrically reconfigure the thermoelectric device from a power conversion mode to a heat pump mode. As a result, heat will be pumped to the heat source upon this electrical reconfiguration permitting the temperature of the lower stage devices to at least momentarily reduce and/or avoid overheating and catastrophic destruction. Once the coolant failure is restored, or in the event of permanent failure of the cooling system 110, the thermoelectric device can continue in the “cooling” mode until the heat source is turned off, removed, or otherwise decoupled from the thermoelectric device 102. As such, catastrophic failures can be reduced and/or avoided.

[0133] Further, the controller 108 being connected to the separate stages can switch the stages from the above-noted power conversion mode and heat pump (i.e., a cooling mode) to a heat flux sensing mode. In a heat sensing mode, the current through the thermoelements are measured as an indicator of the heat flux through the thermoelements coming from a heat source. Such information can be used as a measure of the heat being dissipated from the heat source. The
controller can thus process a signal indicative of heat flux from the thermoelectric pair of n-type and p-type thermoelements.

[0134] Thus, the controller of some embodiments of the present invention connected electrically to the thermoelectric devices of some embodiments of the present invention can be configured to switch the thermoelectric devices between at least one of a cooling mode, a heat pump mode, a power conversion mode, and a heat flux sensing mode.

Electronics Application

[0135] Accordingly, integration of thermoelectric devices and thermoelectric device modules of some embodiments of the present invention to electronic devices such as semiconductor device chip packages can be accomplished through a plurality of mechanisms. Thermoelectric devices can be coupled to such devices for the purposes of “hot spot” cooling those parts of the device most susceptible to exceeding operational temperature limits.

[0136] Integrated semiconductor devices requiring hot spot cooling include, for example, microprocessors, graphic processors and other power dissipating devices fabricated in silicon, germanium, silicon-germanium, gallium arsenide, or any such semiconductor material. The integration can occur, for example, via recesses in the semiconductor chip and/or in the headers. In this approach, vertical and lateral vias or recesses are fabricated in the semiconductor chip and/or the heat spreader. The above-noted bonding techniques join the semiconductor chip to the heat spreader.

[0137] FIG. 12A is a schematic depicting a coupling structure for coupling a thermoelectric device of some embodiments of the present invention to a semiconductor device chip. Specifically, FIG. 12A depicts a thermoelectric device attached to a semiconductor device chip 74. The semiconductor device chip 74 includes the aforementioned power dissipating devices 76 in a region proximate to the recesses 78. Selective cooling occurs via the cooling of recesses 78 in the semiconductor device chip 74. The recesses 78 permit alignment of the thermoelectric devices 72 to the power dissipating devices 76.

[0138] Further, an electrically insulating interlayer 82 can be preferably interposed between the thermoelectric devices and the semiconductor material of the chip. As noted previously, the properties of the electrically insulating interlayer 82 are such to permit electrical isolation without impeding heat flux between the semiconductor device chip 74 and the thermoelectric devices. An electrically insulating material such as S10, can be suitable for use as the electrically insulating interlayer 82, although other insulating materials known in the art are likewise applicable. The electrically insulating interlayer 82 is at least applied to the semiconductor chip in regions where the thermoelectric devices are to be attached. Following application, metallized contacts 83 can be made on the electrically insulating interlayer 82 to provide electrical connections to the thermoelectric devices. Metallized contacts can be made using one or more of known metallization techniques such as, for example, but not limited to evaporation, electroplating, or sputtering. Following metallization, diffusion bonding, or thermal annealing can be used to bond the thermoelectric devices to the chip.

[0139] Bonding occurs between a top header 79 of the thermoelectric devices and the semiconductor device chip 74 by any number of the processes described above, and can utilize a bonding material 80 to facilitate coupling of the semiconductor device chip 74 to the semiconductor device chip 74. Regardless of approach, a thermally conductive and mechanically stable connection or bond is preferred between the top header 79 and the semiconductor device chip 74.

[0140] Heat flux from the semiconductor device chip 74 is dissipated from the thermoelectric devices 72 by a heat sink operating at a temperature above that of the semiconductor device chip 74. As such, heat flux from the power dissipating devices 76 is more efficiently dissipated to the outside environment due to the higher temperature differential existing between the temperature of the heat sink and the ambient than the temperature of the semiconductor device chip 74 and the ambient.

[0141] FIG. 12B is a schematic depicting another coupling structure for coupling a thermoelectric device to a semiconductor device chip. As shown in FIG. 8B, the thermoelectric devices 72 can be directly attached to the semiconductor device chip 74 without utilization of recesses 78. In this coupling structure, placement of the thermoelectric devices 72 on the semiconductor device chip 74 aligns the thermoelectric devices 72 opposite the power dissipating devices 76.

[0142] Thus, coupling of thermoelectric devices 72 to the semiconductor device chip 74 occurs with or without the utilization of recesses. FIG. 13 is a schematic depicting another coupling structure for coupling a thermoelectric device to a semiconductor device chip. As shown in FIG. 13, thermoelectric devices 72 are attached in recesses 78 existing in both the semiconductor device chip 74 and a heat spreader plate 90. The heat spreader plate 90 can utilize a bonding material 80 to couple the heat spreaders 84 to the heat spreader plate 90.

[0143] FIG. 14 is a schematic depicting another coupling structure for coupling thermoelectric devices to a semiconductor device chip. The coupling structure includes vias for electrical connections to the thermoelectric devices. Power requirements for the thermoelectric devices require that electrical leads to the thermoelectric devices be electrically insulated. As shown in FIG. 14, the electrical leads 92 can be integrated directly in a header (e.g., header plate 90) by vias 94, which either vertically or laterally provide electrically conductive channels. The vias 94 can be either etched or pre-fabricated such that the vias 94 run through the header plate 90. Insulating material 96 for the vias 94 can be any high temperature plastic or ceramic of sufficient dielectric quality which encapsulates metal (e.g., copper, gold or, any high electrically conductive metal). Vias in the header plate 90 can be created by laser ablation and can have electroplated metal deposited therein. This structure shown in FIG. 14 having insulated electrical leads facilitates independently power or sensing of individual ones of the thermoelectric devices. The header plate 90 would be made of materials that match the coefficient of thermal expansion of silicon (e.g., within a 5% match in terms of linear expansion coefficient).

[0144] FIG. 15 is a schematic depicting another coupling structure for coupling thermoelectric devices to a semiconductor device chip. The coupling structure includes vias for electrical connections to the thermoelectric devices and includes high thermal conductivity materials in the header plate 90. A combination of high thermal conductive materials 98 like highly oriented pyrolytic graphite, carbon foams, graphite foams can be used to enhance the rejection of heat from the hot side of the thermoelectric device. These materials can be used as a part or for the entirety of the heat spreader plate 90. Thermal conductivity of these materials can be live
times that of the thermal conductivity of copper. These materials would be extremely efficient in dissipating heat from the heat sink 84 of the thermoelectric devices 72. As illustrated in FIG. 15, lateral electrical connections 100 connect to the thermoelectric devices 72. The lateral electrical connections 100 like the electrical leads 92 are formed with electrically conductive materials and insulated from the heat sink plate 90.

[0145] Numerous modifications and variations of the present invention are possible in light of the above teachings. It is therefore understood that within the scope of the appended claims, embodiments of the invention may be practiced otherwise than as specifically described therein.

1. A thermoelectric device comprising:
at least one thermoelectric unit comprising, a plurality of thermoelectric pairs of n-type and p-type thermoelements, a first header coupled to one side of the thermoelectric pairs, a second header coupled to a second side of the thermoelectric pairs, and all of said plurality of thermoelectric pairs between the first and second headers defining a thermal conduction channel area through all of the plurality of thermoelectric pairs that is smaller than an area of at least one of the first header and the second header adjacent the plurality of thermoelectric pairs such that the thermal conduction channel area is a fraction of the area of said at least one of the first header and the second header adjacent the plurality of thermoelectric pairs, and wherein said fraction is less than 0.5%.

2-5. (canceled)

6. The device of claim 1, further comprising:
a thermal impedance increasing device disposed between the thermoelectric pair and one of said first and second headers and configured to set a thermal impedance across a gap between the first and second headers to be at least comparable to a thermal impedance across said thermoelectric pair.

7. The device of claim 6, wherein the thermal impedance increasing device comprises:
a heat pipe disposed between one of said first and second headers, coupled to said thermoelectric pair, and elongated in a transverse direction to space apart the first header from the second header.

8. The device of claim 7, wherein the heat pipe comprises:
a metal member disposed between said thermoelectric pair and one of said first and second headers, extending in said transverse direction, and having a width comparable to a width of the thermoelectric pair.

9. The device of claim 7, wherein said heat pipe is configured to separate said first header from said second header by a distance such that a thermal impedance across a gap between the first and second headers is at least comparable to a thermal impedance across the thermoelectric pair.

10. The device of claim 9, wherein said distance is at least 100 to 500 μm.

11. The device of claim 9, wherein said distance is at least 10 μm.

12. The device of claim 6, wherein the thermal impedance increasing device comprises:
an evacuated housing enclosing the thermoelectric pair and said one of the first and second headers.

13. The device of claim 12, wherein said housing comprises a vacuum level of no greater than 1 Torr.

14. The device of claim 6, wherein the thermal impedance increasing device comprises:
a housing enclosing the thermoelectric pair and said one of the first and second headers, said housing filled with a low thermal conductivity medium to reduce a thermal impedance across a gap between the first and second headers to be at least comparable to a thermal impedance across the thermoelectric pair.

15. The device of claim 14, wherein said low thermal conductivity medium comprises Ar gas.

16. The device of claim 1, wherein said thermoelectric pair, upon conduction of said heat through the thermoelements, produces an electrical potential.

17. The device of claim 1, wherein said thermoelectric pair, upon a current flow through the thermoelements, cools said first header.

18. The device of claim 1, further comprising:
electrical connections to said thermoelectric pair, having a resistance less than 1/10th of an Ohmic resistance of the thermoelectric pair.

19. The device of claim 18, wherein said electrical connections comprise metal connections.

20. (canceled)

21. The device of claim 1, wherein said thermoelectric pair comprises:
a thermoelectric material having a figure of merit of at least 1.

22. The device of claim 1, wherein said thermoelectric pair comprises:
a thermoelectric material having a figure of merit of at least 2.

23. The device of claim 1, wherein said thermoelectric pair comprises:
at least one of a superlattice and a quantum dot superlattice.

24. The device of claim 23, wherein said superlattice comprises:
at least one of a Bi₂Te₃/Sb₂Te₅ superlattice, a Si/Ge superlattice, and a PbTe/PbSe superlattice.

25. The device of claim 1, wherein at least one of said first header and second header comprises:
a thermally conducting member.

26. The device of claim 25, wherein the thermally conducting member comprises:
a thermally conducting member and an electrical insulation member formed on the thermally conducting member; and
a patterned conductor formed on the electrical insulation member and connecting to said thermoelectric pair.

27. The device of claim 26, wherein said electrically conducting member comprises at least one of Al, Cu, doped Si, and doped SiC.

28. The device of claim 26, further comprising:
plurals thermoelectric pairs connected in series by said patterned conductor.

29. The device of claim 25, wherein the thermally conducting member comprises:
an electrically insulating plate; and
a patterned conductor provided on the electrically insulating plate and connecting to said thermoelectric pair.

30. The device of claim 29, wherein said electrically insulating plate comprises at least one of AlN, SiC, Si, and diamond.
31. The device of claim 29, further comprising: plural thermoelectric pairs connected in series by the patterned conductor.

32. The device of claim 7, wherein the heat pipe has a thermal conduction channel area that is smaller than an area of said one of the first header and the second header.

33. The device of claim 7, wherein the heat pipe comprises a heat pipe having a temperature drop of less than 5 K for heat fluxes in a range about 25 W/cm².

34. The device of claim 7, wherein the heat pipe comprises a heat pipe coupled to said thermoelectric pair and said one of the first and second headers by a metal bond.

35. The device of claim 34, wherein the metal bond comprises at least one of a solder-bump bond, a friction bond, and a reactive-metal bond.

36. The device of claim 7, wherein the heat pipe comprises a radiative coupling mechanism coupling heat from the heat pipe to at least one of said first header, said thermoelectric pair, and said second header.

37. The device of claim 36, wherein the radiative coupling mechanism comprises a Purcell-enhancement cavity transmitter/receiver structure.

38. The device of claim 37, wherein the Purcell-enhancement cavity transmitter/receiver structure comprises: a thermally conductive layer including dispersed therein one of metal, semimetal, and semiconductor particles.

39. The device of claim 37, wherein the Purcell-enhancement cavity transmitter/receiver structure comprises: at least one of μm-size and sub-micron-size radiation fins configured to enhance spontaneous radiative heat transport.

40. The device of claim 1, further comprising: a controller configured to control a current through said thermoelectric pair such that said thermoelectric device operates in at least one of a cooling mode, a heat pump mode, a power conversion mode, and a heat flux sensing mode.

41. The device of claim 40, wherein said controller is configured in said heat flux sensing mode to measure said current through said thermoelectric pair.

42. The device of claim 1, wherein said second header comprises: a body having slits formed partially through the body.

43. The device of claim 1, wherein said second header comprises a material having a thermal conductivity higher than Cu.

44. The device of claim 1, wherein said first header comprises: an integrated circuit element; and a heat spreader disposed between said integrated circuit element and said thermoelectric pair.

45. The device of claim 1, wherein said at least one thermoelectric unit is configured to have a specific power greater than 1 W/gm.

46. The device of claim 1, wherein said at least one thermoelectric unit is configured to have a specific power in a range of 0.0001 W/gm to 0.01 W/gm.

47. The device of claim 46, wherein the first header is coupled to a heat source in a range of 30-40°C.

48. The device of claim 1, wherein said at least one thermoelectric unit is configured to produce a power density greater than 0.5 W/cm².

49. The device of claim 1, wherein said at least one thermoelectric unit is configured to produce a power density in a range from 0.0005-0.5 W/cm².

50. A thermoelectric device comprising: plural cascaded thermoelectric units, each unit including, a plurality of thermoelectric pairs of n-type and p-type thermoelements, a first header coupled to one side of the plurality of thermoelectric pairs, a second header coupled to a second side of the plurality of thermoelectric pairs, all of the plurality of thermoelectric pairs between the first and second headers defining a thermal conduction channel area smaller than an area of at least one of the first header and the second header and the thermal conduction channel area defining a packing fraction relative to an area of said at least one of the first header and the second header, wherein said packing fraction is less than 50%, wherein the plural cascaded thermoelectric units comprises first and second thermoelectric units thermally coupled in series between a heat source and a heat sink so that a temperature of a header between thermoelements of the first and second thermoelectric units is between a temperature of the heat source and a temperature of the heat sink during operation wherein a packing fraction in said at least one thermoelectric unit is less than 0.5%.

51. The device of claim 50, wherein the first thermoelectric unit comprises at least one upper thermoelectric unit coupled to the heat source; wherein the second thermoelectric unit comprises at least one lower thermoelectric unit coupled to the at least one upper thermoelectric unit; and wherein the heat sink is thermally coupled to the at least one lower thermoelectric unit and configured to dissipate heat from the at least one lower thermoelectric unit.

52.-54. (canceled)

55. The device of claim 51, wherein said thermoelectric pair in at least one of the at least one upper thermoelectric unit and the at least one lower thermoelectric unit comprises: at least one of Bi₂Te₃, Sb₂Te₃, SiGe, (AgSbTe₂)ₓ, (GeTe)₁₋ₓ, PbTe, PbSe, ZnTe, and skutterudites.

56. The device of claim 55, wherein the (AgSbTe₂)ₓ, (GeTe)₁₋ₓ comprises a GeTe mole fraction of 0.80 to 0.85.

57. The device of claim 51, wherein the at least one upper thermoelectric unit is configured to operate at temperatures from 670 K to 870 K.

58. The device of claim 51, wherein the at least one lower thermoelectric unit is configured to operate at temperatures from 470 K to 670 K.

59. The device of claim 51, wherein the at least one lower thermoelectric unit is configured to operate at temperatures from 300 K to 470 K.

60. (canceled)

61. The device of claim 51, wherein said plural cascaded thermoelectric units are configured to have a specific power in a range of 0.0001 W/gm to 0.01 W/gm.

62. The device of claim 61, wherein the first header is coupled to said heat source in a range of 30-40°C.

63. The device of claim 51, wherein said plural cascaded thermoelectric units are configured to produce a power density greater than 0.5 W/cm².

64. The device of claim 51, wherein said plural cascaded thermoelectric units are configured to produce a power density in a range of 0.005 W/cm² to 0.5 W/cm².

65.-67. (canceled)
68. A system for thermoelectric power conversion, comprising:
a plurality of thermoelectric pairs of n-type and p-type thermoelements;
a first header coupled to one side of the plurality of thermoelectric pairs;
a second header coupled to a second side of the plurality of thermoelectric pairs;
al so of said plurality of thermoelectric pairs between the first and second headers defining a thermal conduction channel area smaller than an area of at least one of the first header and the second header such that the thermal conduction channel area is a fraction of the area of said at least one of the first header and the second header, said fraction being less than 0.5%; and
a heat sink coupled to the second header and configured to dissipate heat at a rate which maintains a temperature of the second header below a temperature of the first header.
69.-72. (canceled)
73. The system of claim 68, further comprising:
a coupling member coupling the first header to a heat source.
74. The system of claim 73, wherein said coupling member comprises at least one of a steam pipe, a combustion exhaust pipe, and a thermally conducting member having a thermal conductance of at least 1 W/m K and extending from said first header to said heat source.
75. The system of claim 68, further comprising:
a thermal impedance increasing device disposed between the thermoelectric pair and one of said first and second headers.
76. The system of claim 68, further comprising:
plurals cascadable thermoelectric units, each comprising said first header, said thermoelectric pair, and said second header.
77. The system of claim 76, wherein one of said plural cascadable thermoelectric units comprises:
at least one upper thermoelectric unit coupled to a heat source;
at least one lower thermoelectric unit coupled to the at least one upper thermoelectric unit; and
a heat sink thermally coupled to the at least one lower thermoelectric unit and configured to dissipate heat from the at least one lower thermoelectric unit.
78. The system of claim 77, wherein said thermoelectric pair in at least one of the at least one upper thermoelectric unit and the at least one lower thermoelectric unit comprises:
at least one of Bi₂Te₃, Sb₂Te₃, Sb₂Ge, (AgSbTe₂)ₓ(GeTe)ₙ, PbTe, PbSe, ZnSb, and skutterudites.
79. The system of claim 78, wherein the (AgSbTe₂)ₓ(GeTe)ₙ comprises a GeTe mole fraction of ~0.80 to 0.85.
80. The system of claim 77, wherein said thermoelectric pair in at least one of the at least one upper thermoelectric unit and the at least one lower thermoelectric unit comprises:
at least one of a superlattice and a quantum dot superlattice.
81. The system of claim 80, wherein said superlattice comprises:
at least one of a superlattice of Si/Ge, PbTe/PbSe, ZnSb/CdSb, InAs/InSb, CdTe/HgCdTe, GaInAs/InGaAs, and GaAs.
82. The system of claim 77, wherein the at least one upper thermoelectric unit is configured to operate at temperatures from 670 K to 870 K.
83. The system of claim 77, wherein the at least one lower thermoelectric unit is configured to operate at temperatures from 470 K to 670 K.
84. The system of claim 77, wherein the at least one lower thermoelectric unit is configured to operate at temperatures from 300 K to 470 K.
85. The system of claim 76, wherein said plural cascadable thermoelectric units and said heat sink are configured to have a specific power greater than 1 W/gm.
86. The system of claim 76, wherein said plural cascadable thermoelectric units are configured to have a specific power in a range of 0.0001 W/gm to 0.01 W/gm.
87. The system of claim 86, wherein the first header is coupled to a heat source in a range of 30-40° C.
88. The system of claim 76, wherein said plural cascadable thermoelectric units and said heat sink are configured to produce a power density greater than 0.5 W/cm².
89. The system of claim 76, wherein said plural cascadable thermoelectric units are configured to produce a power density in a range of 0.0005 W/cm² to 0.5 W/cm².
90. The device of claim 50 wherein a packing fraction of all of the thermal elements of the first thermoelectric unit is different than a packing fraction of all of the thermal elements of the second thermoelectric unit.
91. The device of claim 50 wherein a packing fraction of all of the thermal elements of the first thermoelectric unit is greater than a packing fraction of all of the thermal elements of the second thermoelectric unit.
92. The device of claim 50 wherein a combined thermal conduction channel area of all of the thermal elements of the first thermoelectric unit is different than a combined thermal conduction channel area of all of the thermal elements of the second thermoelectric unit.
93. The device of claim 50 wherein a combined thermal conduction channel area of the first thermoelectric unit is greater than a combined thermal conduction channel area of all of the thermal elements of the second thermoelectric unit.

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