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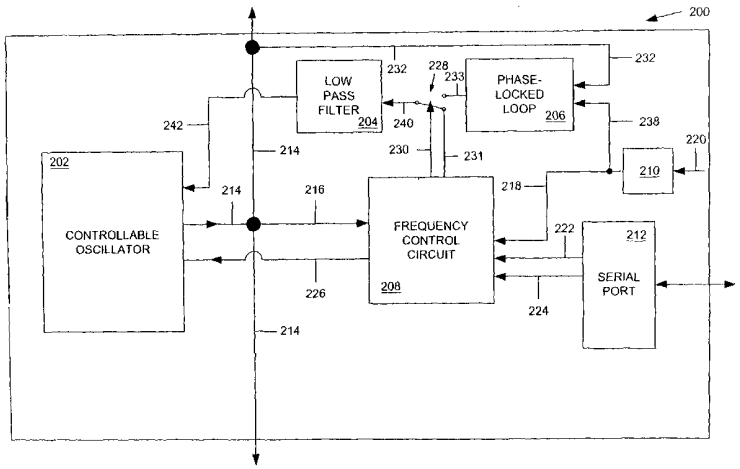
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(54) Title: SYSTEM FOR CONTROLLING THE FREQUENCY OF AN OSCILLATOR



(57) Abstract: Systems for controlling the frequency of the output signal of a controllable oscillator (202) in a frequency synthesizer (200) are provided. One such system comprises a controllable oscillator (202) and a frequency control circuit (208). The controllable oscillator (202) is configured to generate an output signal that has a predefined frequency. The controllable oscillator (202) is also configured with a plurality of operational states that are controlled by the frequency control circuit. Each operational state of the controllable oscillator (202) defines a distinct frequency for the output signal of the controllable oscillator (202). The frequency control circuit receives the output signal of the controllable oscillator and determines the distinct frequency for the output signal that best approximates the predefined frequency. The frequency control circuit may also provide a control signal to the controllable oscillator that is configured to change the controllable oscillator to the operational state corresponding to the distinct frequency that best approximates the predefined frequency.

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SYSTEM FOR CONTROLLING THE FREQUENCY OF AN OSCILLATOR

BACKGROUND OF THE INVENTION

1. Field of the Invention.

The invention is generally related to frequency synthesizers, and more particularly, is related to systems and methods for controlling the frequency and amplitude of an oscillator.

2. Related Art.

Frequency synthesizers are regularly employed in communication transceivers used in numerous types of communication systems and communication technologies, such as, radio frequency communication systems. Typically, such frequency synthesizers use a phase-locked loop to precisely control the frequency of the output signal of a voltage-controlled oscillator (VCO). The frequency synthesizer typically consists of a VCO, a low pass filter, and a phase-locked loop. The VCO generates an output signal having a particular frequency. A phase detector in the phase-locked loop receives the output signal and compares the output signal to a reference frequency. Based on the comparison of the output signal to the reference frequency, the phase-locked loop generates a control signal that is provided to the low pass filter and then to the VCO. The control signal is typically received by a variable capacitor, referred to as varactor, in the VCO. The control signal tunes the variable capacitor, thereby changing the frequency of the output signal of the VCO.

Generally, such frequency synthesizers are effective where the range of the frequency of the output signal is limited. However, in situations where the frequency of the output signal of the VCO needs to be varied over a broad frequency range, such frequency synthesizers are very problematic. For example, where frequency synthesizers are used in wireless broadband and wire-line broadband communication systems, or in multi-band devices and multi-mode devices, the limited tuning range of the varactors prevents effective tuning of the VCO and, therefore, effective channel selection. The limited tuning range of the varactors may also be problematic in situations where large fabrication process variations, temperature variations, or other variations require the output of the controllable oscillator to be varied over a broad frequency range. Additionally, varactors with a wide-tuning range are also problematic due to the fact that they are extremely sensitive to noise and interference on the control lines from the phase-locked loop. Furthermore, the non-linear characteristics of wide-tuning varactors are problematic in the design of the loop filter in the frequency synthesizer. Thus, there is a need in the industry to address these deficiencies and inadequacies.

SUMMARY

The invention provides a system for controlling the frequency of the output signal of a controllable oscillator in a frequency synthesizer. The invention provides a frequency synthesizer circuit having a controllable oscillator and a frequency control circuit. The controllable oscillator is configured to generate an output signal that has a predefined frequency. The controllable oscillator is also configured with a plurality of operational states that are controlled by the frequency control circuit. Each operational state of the controllable oscillator defines a distinct frequency for the output signal of the controllable oscillator. The frequency control circuit receives the output signal of the controllable oscillator and determines the distinct frequency for the output signal that best approximates the predefined frequency. The frequency control circuit may also provide a control signal to the controllable oscillator that is configured to change the

controllable oscillator to the operational state corresponding to the distinct frequency that best approximates the predefined frequency.

The invention also provides related methods of operation and computer readable media. Other systems, methods, features and advantages of the invention will be or will become apparent to one with skill in the art upon examination of the following figures and detailed description. It is intended that all such additional systems, methods, features and advantages be included within this description, be within the scope of the invention, and be protected by the accompanying claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The components in the figures are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention. In the figures, like reference numerals designate corresponding parts throughout the different views.

FIG. 1 illustrates a block diagram of a communication device in which the systems and methods of the present invention may be implemented.

FIG. 2 is a block diagram of one of a number of embodiments of the frequency synthesizer of FIG. 1.

FIG. 3 is a flow chart illustrating the architecture and operation of one of a number of embodiments of the frequency control circuit of FIG. 2 for controlling the frequency of the output signal of the controllable oscillator.

FIG. 4 is a block diagram of one of a number of embodiments of the controllable oscillator of FIG. 2 for implementing the plurality of operational states and corresponding distinct frequencies for the output signal, which are controlled by the frequency control circuit of FIG. 2

FIG. 5 is a block diagram of one of a number of embodiments of the frequency control circuit of FIG. 2 for controlling the frequency of the output signal of the controllable oscillator.

FIG. 6 is a flow chart illustrating the architecture and operation of the frequency control circuit of FIG. 5.

FIG. 7 is a binary state diagram of the binary state search module of FIGS. 5 and 6.

FIG. 8 is a block diagram of another of a number of embodiments of the frequency synthesizer of FIG. 1.

FIG. 9 is a flow chart illustrating the architecture and operation of one of a number of embodiments of the amplitude control circuit of FIG. 8 for maintaining the amplitude of the output signal of the controllable oscillator.

FIG. 10 is a block diagram of one of a number of embodiments of the controllable oscillator of FIG. 8 for implementing the plurality of operational states and corresponding distinct amplitudes for the output signal, which are controlled by the amplitude control circuit of FIG. 8.

FIG. 11 illustrates a block diagram of one of a number of embodiments of the amplitude control circuit of FIG. 8 for maintaining the amplitude of the output signal of the controllable oscillator of FIG. 8.

DETAILED DESCRIPTION

SYSTEM OVERVIEW

FIG. 1 illustrates a block diagram of a communication device 100 in which a frequency synthesizer 112 according to the systems and methods of the present invention may be implemented. Communication device 100 may be used for communication with any of a number of communication systems, such as, for example, wireless communication systems, fiber optic communication systems, any other known or future broadband communication system, or any other type of communication system. In situations where communication device 100 is a wireless device, communication device 100 may communicate with any of a number of wireless communication systems, which may be based on any of the following technologies: analog advanced mobile phone service (AMPS), global system for mobile communications (GSM), digital advanced mobile phone service (D-AMPS), Japanese mobile communication systems (MCS), Scandinavian nordic mobile telephone (system) (NMT), British total access communication system (TACS).

Furthermore, various modulation and access methodologies may be used, such as, for example, code division multiple access (CDMA), including CDMA2000, time division multiple access (TDMA), wideband CDMA (WCDMA), personal communication networks (PCN), Integrated Dispatch Enhanced Networks (iDEN), personal communications service (PCS), cellular digital packet data (CDPD), general packet radio service (GPRS), wireless access protocol (WAP) systems, specialized mobile radio (SMR), second generation (2G) systems, third generation (3G) systems, or similar predecessor or successor systems, or any other radio communication system supporting voice and/or data communications. Communication device 100 may also be a multi-band communication device capable of communicating with multiple wireless communication systems.

Communication device 100 comprises an antenna 102, a duplex filter 104, a low noise amplifier 106, a band pass filter 108, a receive mixer 110, a frequency synthesizer 112, a processor 114, a transmit mixer 116, a band pass filter 118, a power amplifier 120, a speaker 122, and a microphone 124. Examples of commercially available processors include, but are not limited to, an ARM processor such as an ARM 7 or ARM 9 processor, a ZSP Core supplied by LSI Logic or a Teak processor supplied by DSP Group. As known in the art, communication device 100 may include any of a number of other components. For example, communication device 100 may include a memory module, such as, random access memory (RAM), flash memory, non-volatile RAM (NVRAM), or any other known type of memory device. Communication device 100 may also include a user interface for performing a number of functions typically implemented with various types of communication devices, such as, for example, cellular telephones, personal digital assistants (PDAs), pagers, or any other desirable functionality.

In operation, communication device 100 receives and transmits broadband signals, such as, for example, radio frequency signals, from and to the communication system via antenna 102. In the receive direction, from the communication system to communication device 100, a broadband signal received by communication device 100 via antenna 102 is communicated to duplex filter 104. Duplex filter 104 receives

signals from the communication system and communicates them via connection 126 to amplifier 106. Amplifier 106 provides an amplified signal to band pass filter 108 via connection 128. Band pass filter 108 passes frequencies within the range of frequencies associated with the communication systems with which communication device 100 communicates to mixer 110 via connection 130. Frequencies outside this range are attenuated. Mixer 110 receives a signal from frequency synthesizer 112 via connection 132, mixes it with the signal received via connection 130, and provides a signal to processor 114 via connection 134. Processor 114 processes the signal received via connection 134 and, where the signal is an audio signal, may provide the resulting signal to speaker 122. In other embodiments where communication device 100 supports data communications, processor 114 may provide a data signal to a user interface, such as, for example, a liquid crystal display or other display device.

Although processor 114 is represented as a single element in FIG. 1, as known in the art, processor 114 may, for example, comprise a baseband processor, an integrated analog (IA) integrated circuit (IC), and a power management IC (PMIC). The baseband processor manages all communication and user interface functions. The baseband processor may be integrated on a single die and may be housed in a number of ways, such as, in a 128-pin thin quad flat pack (TQFP) or a 160-pin 12x12 mm chip array ball grid array (CABGA). The IAIC implements all signal conversion functions required by communication device 100. The IAIC may be a highly integrated mixed signal device that also manages all timing and interfacing between the baseband processor and the other components of communication device 100. IAIC may be housed in, for example, a 100-pin TQFP or a 100-pin 10x10 mm CABGA. The PMIC implements all power supply functions. The PMIC may also support subscriber identity modules (SIMs), and through the use programmable switching regulators, the PMIC may be independent of battery chemistry. The PMIC may be housed in, for example, a 48-pin TQFP.

In the transmit direction, from communication device 100 to the communication system, voice signals originating from microphone 124 are processed by processor 114 and provided to mixer 116 via connection 136. As described above,

communication device 100 may support data communication, in which case processor 114 processes the data signal and provides the resulting signal to mixer 116. Mixer 116 receives a signal from frequency synthesizer 112 via connection 138, mixes it with the signal received via connection 136 from processor 114, and provides a signal to band pass filter 118 via connection 140. Similar to band pass filter 108, filter 118 provides frequencies within the range of frequencies associated with the communication systems with which communication device 100 communicates to amplifier 120 via connection 142. Frequencies outside this range are attenuated. The amplified signal is provided to duplex filter 104 via connection 144, and then provided to the communication system via antenna 102.

FREQUENCY CONTROL CIRCUIT

FIG. 2 illustrates a block diagram of one of a number of embodiments of frequency synthesizer 112 of FIG. 1. Frequency synthesizer 112 may comprise a controllable oscillator 202, a low pass filter 204, a phase-locked loop 206, a frequency control circuit 208, an R-divider circuit 210, and a serial port 212.

Frequency synthesizer 112 may be implemented in hardware, software, firmware, or a combination thereof. In certain embodiments, frequency synthesizer 112 may be implemented in software or firmware that is stored in memory and that is executed by a processor or any other suitable instruction execution system. Where implemented in hardware, as in certain other embodiments, frequency synthesizer 112 may be implemented with any or a combination of the following technologies, which are all well known in the art: a discrete logic circuit(s) having logic gates for implementing logic functions upon data signals, an application specific integrated circuit (ASIC) having appropriate combinational logic gates, a programmable gate array(s) (PGA), a field programmable gate array (FPGA), *etc.*

Controllable oscillator 202 may be a voltage controlled oscillator (VCO). In alternative embodiments, controllable oscillator 202 may be any type of oscillator and need not be voltage controlled. As described in detail below, the important aspects of frequency synthesizer 112 are that controllable oscillator 202 is configured to have a

plurality of operational states in which each of the operational states correspond to a distinct frequency for the output signal of controllable oscillator 202 and that the operational state of controllable oscillator 202 is responsive to control signals received from phase-locked loop 206 and frequency control circuit 208.

Phase-locked loop 206 may be a typical phase-locked loop as known in the art, such as those described by Bezhad Razavi in "Monolothic Phase-Locked Loops and Clock Recovery Circuits," IEEE Press, 1996, which is hereby incorporated in its entirety by reference. For example, as described below, phase-locked loop 206 may comprise a phase detector and a plurality of charge pumps, or current sources.

In the operation of frequency synthesizer 112, controllable oscillator 202 generates an output signal on connection 214. As described above, the output signal of controllable oscillator 202 may be provided to mixer 110 via connection 132 and to mixer 116 via connection 138 (FIG. 1). The frequency of the output signal of controllable oscillator 202 may be controlled by frequency control circuit 208 and phase-locked loop 206. In certain embodiments of frequency synthesizer 112, the frequency of the output signal of controllable oscillator 202 is controlled first by frequency control circuit 208 and then by phase-locked loop 206.

As described above, controllable oscillator 202 may be configured to have a plurality of operational states in which each of the operational states corresponds to a distinct frequency for the output signal of the controllable oscillator. The frequency of the output signal of controllable oscillator 202 may be controlled by changing the operational state of controllable oscillator 202 and thereby changing the corresponding distinct frequency for the output signal.

FIG. 3 is a flow chart 300 illustrating the architecture and operation of one of a number of embodiments of frequency control circuit 208 of FIG. 2 for controlling the frequency of the output signal of controllable oscillator 202. At block 302, frequency control circuit 208 receives information associated with a predefined frequency, or reference frequency, for the output signal of controllable oscillator 202. The information associated with the predefined frequency may be received as a signal provided on connection 218 from R-divider circuit 210. R-divider circuit 210 may

generate the information associated with the predefined frequency for the output frequency of controllable oscillator 202 based on a system clock signal received on connection 220. In alternative embodiments, frequency control circuit 208 may also receive information associated with the predefined frequency from serial port 212 on connections 222 and 224.

At block 304, frequency control circuit 208 determines which of the plurality of distinct frequencies associated with the plurality of operational states of controllable oscillator 202 best approximates the predefined frequency. Frequency control circuit 208 receives the output signal of controllable oscillator 202 on connections 214 and 216. At block 306, frequency control circuit 208 generates a control signal configured to change the frequency of the output signal of controllable oscillator 202 to the operational state corresponding to the distinct frequency that best approximates the predefined frequency. Frequency control circuit 208 may provide the control signal to controllable oscillator 202 on connection 226. At block 308, in response to the control signal from frequency control circuit 208, controllable oscillator 202 may be changed to the operational state corresponding to the distinct frequency that best approximates the predefined frequency.

After the frequency of the output signal of controllable oscillator 202 has been changed to the operational state corresponding to the distinct frequency that best approximates the predefined frequency, the frequency of the output signal of controllable oscillator 202 may be further controlled by phase-locked loop 206. In this manner, frequency control circuit 208 may perform a less accurate approximation of the predefined frequency, but one which is much faster, for example, than phase-locked loop 206, over a wider range of frequencies. Then, phase-locked loop 206 may be used to perform a much more precise approximation of the predefined frequency.

Frequency control circuit 208 may enable phase-locked loop 206 to begin controlling the frequency of the output signal of controllable oscillator 202 by, for example, engaging switch 228 in response to a switch control signal supplied on connection 230. Switch 228 and the switch control signal may be configured so that

when phase-locked loop 206 controls controllable oscillator 202, switch 228 connects connection 233 and connection 240, and when frequency control circuit 208 controls controllable oscillator 202, switch 228 connects connection 240 and connection 231. Furthermore, when frequency control circuit 208 is engaged, a control signal may be provided to low pass filter 204 on connection 231. The control signal on connection 231 may be configured to disengage the controlling mechanism within controllable oscillator 202 that is engaged by phase-locked loop 206 while controlling the frequency of controllable oscillator 202. For example, where controllable oscillator 202 is voltage-controlled by phase-locked loop 206 through a variable capacitor, frequency control circuit 208 may be configured to provide a constant voltage on connection 231 in order keep the variable capacitor set to a constant value while frequency control circuit 208 is engaged.

When engaged by frequency control circuit 208, phase-locked loop 206 may control the frequency of the output signal of controllable oscillator 202 as known in the art and described by Bezhad Razavi in "Monolothic Phase-Locked Loops and Recovery Circuits." For example, phase-locked loop 206 receives the output signal of controllable oscillator 202 on connection 232 and the reference frequency on connection 238. Based on the output signal and the reference frequency, phase-locked loop 206 generates a control signal and provides the control signal to low pass filter 204 on connection 240. The filtered control signal is provided to controllable oscillator 202 on connection 242. In response to the control signal on connection 242, a variable capacitor (not shown in FIG. 2) in controllable oscillator 202 may be engaged. The control signal and the variable capacitor may be configured to control the frequency of the output signal of controllable oscillator 202 on connection 214.

It should be understood that there are numerous embodiments for frequency synthesizer 112. For example, the frequency of the output signal of controllable oscillator 202 may be controlled first by frequency control circuit 208 and then by phase-locked loop 206. However, in other embodiments of frequency synthesizer 112, the frequency of the output signal of controllable oscillator 202 may be controlled first by phase-locked loop 206 and then by frequency control circuit 208.

In still other embodiments of frequency synthesizer 112, the frequency of the output signal of controllable oscillator 202 may be controlled entirely by frequency control circuit 208.

FIG. 4 illustrates a block diagram of one of a number of embodiments of controllable oscillator 202 for implementing the plurality of operational states and corresponding distinct frequencies for the output signal, which are controlled by frequency control circuit 208. Controllable oscillator 202 may comprise an inductor 400, a variable capacitor 402, and switched capacitors 404, 406, and 408. Inductor 400, variable capacitor 402, and switched capacitors 404, 406, and 408 may be connected in parallel as shown in FIG. 4. However, as known by one of ordinary skill in the art, there are various other configurations for inductor 400, variable capacitor 402, and switched capacitors 404, 406, and 408. For example, inductor 400, variable capacitor 402, and switched capacitors 404, 406, and 408 may be connected in series or may be connected in any of a number of combinations of parallel and series connections. Furthermore, one of ordinary skill in the art should also know that there are numerous other ways of configuring controllable oscillator 202 in order to implement the plurality of operational states. As stated above, the important aspects of frequency synthesizer 112 are that controllable oscillator 202 is configured to have a plurality of operational states in which each of the operational states correspond to a distinct frequency for the output signal of controllable oscillator 202 and that the operational state of controllable oscillator 202 is responsive to control signals received from phase-locked loop 206 and frequency control circuit 208.

Switched capacitors 404, 406, and 408 receive the control signal from frequency control circuit 208 on connection 226. In response to the control signal from frequency control circuit 208, switched capacitors 404, 406, and 408 are engaged or disengaged in a predetermined manner corresponding to one of the operational states. In one of numerous embodiments of frequency synthesizer 112, the number of switched capacitors defines the number of operational states and corresponding frequencies for the output signal of controllable oscillator 202. For instance, if there are three switched capacitors, controllable oscillator 202 may have

eight ($2^3 = 8$) operational states. Because each of the switched capacitors may be engaged or disengaged, there are eight possible binary configurations for the switched capacitors, with each configuration producing a distinct frequency for the output signal of controllable oscillator 202. As shown in Equations 1 and 2, each distinct frequency for the output signal of controllable oscillator 202 may be defined as a function of the component values for inductor 400 (L), variable capacitor 402 (C_{var}), and switched capacitors 404 (C_0), 406 (C_1), and 408 (C_n) and binary weighting coefficients b_0, b_1 and b_n, where f_{co} is the frequency of the output signal of controllable oscillator 202:

$$f_{co} \alpha \frac{1}{\sqrt{LC}}$$

(Equation 1)

$$C = C_{var} + b_0 C_0 + b_1 C_1 + ... + b_n C_n$$

(Equation 2)

In Equation 2, switched capacitors 404, 406, and 408 are binary weighted. For example, in a 3-bit digital system, switched capacitors 404, 406, and 408 may be weighted as follows: $C_0 = C$, $C_1 = 2C$, and $C_n = 8C$.

The number of switched capacitors also defines the number of control lines required between frequency control circuit 208 and controllable oscillator 202. For example, if there are three switched capacitors to be engaged or disengaged, frequency control circuit 208 may use three control lines (one control line for each switched capacitor). For example, referring to FIGS. 3 and 4, at block 304, frequency circuit 208 may determine that for a 3-bit system the frequency of the output signal of controllable oscillator 202 best approximates the predefined frequency where switched capacitor 404 is engaged, switched capacitor 406 is disengaged, and switched capacitor 408 is engaged. Accordingly, at block 306, frequency control

circuit 208 may generate three control signals. A first control signal 410 corresponding to switched capacitor 404 may be configured to engage switched capacitor 404. A second control signal 412 corresponding to switched capacitor 406 may be configured to disengage switched capacitor 406. A third control signal 414 corresponding to switched capacitor 408 may be configured to engage switched capacitor 408. In response to these control signals, at block 308, switched capacitors 404, 406, and 408 are engaged, disengaged, and engaged, respectively. This configuration changes controllable oscillator 202 to the operational state corresponding to the distinct frequency that best approximates the predefined frequency.

In those embodiments where controllable oscillator 202 is also controlled by phase-locked loop 206, controllable oscillator 202 may be further controlled by varying the control signal applied to variable capacitor 402 on connection 242.

FIG. 5 illustrates a block diagram of one of a number of embodiments of frequency control circuit 208 for controlling the frequency of the output signal of controllable oscillator 202. Frequency control circuit 208 may comprise a program counter, or R-divider, 500, a frequency detector, or counter, 502, a digital decoder 504, a digital comparator 506, and a binary state search module 508.

FIG. 6 is a flow chart 600 illustrating the architecture and operation of frequency control circuit 208 of FIG. 5. At block 601, frequency control circuit 208 is enabled. At block 602, digital decoder 504 receives information associated with a predefined frequency for the output signal of controllable oscillator 202 on connections 222 and 224 from serial port 212 (FIG. 2). At block 604, frequency detector 502 determines a current frequency of the output signal of controllable oscillator 202, which corresponds to the current operational state of controllable oscillator 202. Frequency detector 502 receives a timing signal on connection 510 from program counter 500. Program counter 500 generates the timing signal based on the reference frequency received on connection 238 (FIG. 2). The timing signal may be used to clock the operation of frequency detector 502 and binary state search module 508. Frequency detector 502 receives the output signal of controllable

oscillator 202 on connection 214 (FIG. 2). In response to a clock pulse, frequency detector 502 generates a first digital word corresponding to the current frequency of the output signal.

At block 606, digital comparator 506 compares the first digital word to a second digital word received on connection 512 from digital decoder 504 and provides a control bit on connection 516 to binary state search module 508. For example, digital comparator 506 may be configured to generate a logic 1 for the control bit when the first digital word is higher than the second digital word and a logic 0 for the control bit when the second digital word is higher than the first digital word . Based on the control bit, the current operational state of controllable oscillator 202, and the timing signal received on connection 518, at block 608, binary state search module 508 selects a next operational state for controllable oscillator 202. As described in detail below, frequency control circuit 208 is configured so that the next operational state has a corresponding distinct frequency that better approximates the predefined frequency for the output signal of controllable oscillator 202. At block 610, binary state search module 508 generates a control signal configured to change controllable oscillator 202 to the selected next operational state. At block 612, controllable oscillator 202 is changed to the selected next operational state. At block 614, binary state search module 508 determines whether all of the operational states of controllable oscillator 202 have been searched. If all of the operational states have been searched, frequency control circuit 208 is disabled. If all of the operational states have not been searched, blocks 604, 606, 608, 610, 612, and 614 are repeated.

FIG. 7 is a tree state diagram of binary state search module 508 of FIG. 5. The binary tree comprises leaf nodes 700, intermediate nodes 702, and root node 704. Root node 704 represents the initial binary state that corresponds to the initial operational state of controllable oscillator 202 prior to the operation of frequency control circuit 208. Intermediate nodes 702 represent the set of intermediate binary states corresponding to the possible operational states that controllable oscillator 202 may occupy during the operation of frequency control circuit 208. Leaf nodes 700

designate the final binary states corresponding to the plurality of operational states of controllable oscillator 202.

As stated above, binary state search module 508 may use the binary tree to search the plurality of operational states of controllable oscillator 202 and determine which distinct frequency best approximates the predefined frequency. For instance, in the 3-bit system of FIG. 7, controllable oscillator 202 may be configured to have eight ($2^3 = 8$) operational states. Accordingly, the binary tree may also have eight leaf nodes 700. Before frequency control circuit 208 is enabled, binary state search module 508 is at root node 704, which represents the initial operational state (100 in the example of FIG. 7) of controllable oscillator 202. As described above, frequency control circuit 208 determines the current frequency of the output signal while controllable oscillator 202 is in the initial operational state (100 in the example of FIG. 7). Frequency control circuit 208 then compares the current frequency to the predefined frequency. Based on the comparison of the current frequency and the predefined frequency and in response to a clock pulse, binary state search module 508 selects one of the two intermediate nodes 702 linked to root node 704. The two intermediate nodes 702 linked to root node 704 represent the two next operational states (010, 110 in the example of FIG. 7) for controllable oscillator 202. Binary state search module 508 may be configured so that the two next operational states for root node 704 and intermediate nodes 702 are defined by the following equation, where M_{new} represents the next operational state and M represents the current operational state:

$$M_{new} = M \pm \frac{M}{2}$$

(Equation 3)

For example, in FIG. 7, the initial operational state may be represented in binary as 100, which corresponds to decimal 6. Based on Equation 3, the binary tree is configured so that the two next operational states are represented in binary as 010 and

110, which correspond to decimal 4 and 6, respectively. In this manner, in N clock pulses, binary state search module 508 may search through 2^N operational states to determine the operational state having the distinct frequency that best approximates the predefined frequency.

It should be understood by one of ordinary skill in the art that there are numerous ways of implementing the binary tree illustrated in FIG. 7. The particular value (binary or decimal) associated with each of the binary states in the binary tree may be configured in a number of ways for each embodiment. For example, in the exemplar binary tree of FIG. 7, the initial operational state is represented in binary as 100 and the two next operational states are represented in binary as 010 and 110. Binary state search module 508 may be configured to implement a binary tree having any values associated with each of the binary states in the binary tree.

After comparing the current frequency and the predefined frequency, binary state search module 508 selects the next operational state that has a distinct frequency that better approximates the predefined frequency. Frequency control circuit 208 then generates a control signal configured to change controllable oscillator 202 to the selected next operational state. After controllable oscillator 202 is changed to the selected next operational state, frequency control circuit 208 determines the frequency of the output signal of controllable oscillator 202 corresponding to the selected next operational state. This process is repeated for all states in the binary tree until binary state search module 508 selects a next operational state for controllable oscillator 202 corresponding to one of the leaf nodes 700. The leaf node 700 selected by binary state search module 508 represents the operational state having the distinct frequency that best approximates the predefined frequency.

AMPLITUDE CONTROL CIRCUIT

FIG. 8 illustrates a block diagram of another of a number of embodiments of the frequency synthesizer of FIG. 1. Frequency synthesizer 800 comprises a controllable oscillator 202, a low pass filter 204, a phase-locked loop 206, a frequency

control circuit 208, an R-divider circuit 210, a serial port 212, and an amplitude control circuit 802.

Frequency synthesizer 800 may be implemented in hardware, software, firmware, or a combination thereof. In certain embodiments, frequency synthesizer 800 may be implemented in software or firmware that is stored in memory and that is executed by a processor or any other suitable instruction execution system. Where implemented in hardware, as in certain other embodiments, frequency synthesizer 800 may be implemented with any or a combination of the following technologies, which are all well known in the art: a discrete logic circuit(s) having logic gates for implementing logic functions upon data signals, an application specific integrated circuit (ASIC) having appropriate combinational logic gates, a programmable gate array(s) (PGA), a field programmable gate array (FPGA), *etc.*

In general, frequency synthesizer 800 is configured and operates in a similar manner to frequency synthesizer 112 of FIG. 2. However, it should be understood by those of ordinary skill in the art that frequency synthesizer 800 need not include frequency control circuit 208. The important aspect of frequency synthesizer 800 is that amplitude control circuit 802 communicates with controllable oscillator 202, and as the frequency of the output signal of the controllable oscillator is controlled, such as, for example, by phase-locked loop 206 and/or frequency control circuit 208, amplitude control circuit 802 maintains the amplitude of the output signal.

Due to complex interactions between the amplitude and frequency of the output signal of controllable oscillator 202, it is desirable to maintain a constant amplitude for the output signal of controllable oscillator 202 over the entire frequency range. Therefore, as the frequency of the output signal of controllable oscillator 202 is changed, such as, for example, by phase-locked loop 206 and/or frequency control circuit 208, amplitude control circuit 802 may be enabled.

As described above with respect to FIG. 2, controllable oscillator 202 may be configured to have a plurality of operational states in which each of the operational states corresponds to a distinct frequency for the output signal of controllable oscillator 202. The frequency of the output signal of controllable oscillator 202 may

be controlled by changing the operational state of controllable oscillator 202 and thereby changing the corresponding distinct frequency for the output signal.

Where amplitude control circuit 802 is employed, controllable oscillator 202 may be further configured to have a plurality of operational states in which each of the operational states corresponds to a distinct amplitude for the output signal of controllable oscillator 202. The amplitude of the output signal of controllable oscillator 202 may be maintained throughout the frequency range by changing the operational state of controllable oscillator 202 and thereby changing the corresponding amplitude for the output signal.

FIG. 9 is a flow chart 900 illustrating the architecture and operation of one of a number of embodiments of amplitude control circuit 802 of FIG. 8. At block 901, amplitude control circuit 802 receives information associated with a predefined amplitude level for the output signal of controllable oscillator 202. The information may define a minimum amplitude level above which the amplitude of the output signal of controllable oscillator 202 should be maintained. The information may also be represented as an amplitude range in which the amplitude of the output signal should be maintained. The important aspect of amplitude control circuit 802 is that it receives information for maintaining or controlling the amplitude level of the output signal of controllable oscillator 202. The information associated with the predefined amplitude level may be received from serial port 212 or any other component not shown in FIG. 8. The information may even be contained in memory within amplitude control circuit 802. At block 902, amplitude control circuit 802 determines the amplitude of the output signal of controllable oscillator 202. At block 904, amplitude control circuit 802 compares the amplitude to the predefined amplitude level and determines whether the amplitude of the output signal needs to be changed. For example, if the amplitude of the output signal is less than the predefined amplitude level, amplitude control circuit 802 may determine which of the plurality of operational states has a distinct amplitude for the output signal that best approximates the predefined amplitude level. At block 906, amplitude control circuit 802 generates a control signal configured to change controllable oscillator 202 to the operational

state corresponding to the distinct amplitude that best approximates the predefined amplitude level. At block 908, in response to the control signal from amplitude control circuit 802, controllable oscillator 202 may be changed to the operational state corresponding to the distinct amplitude that best approximates the predefined amplitude level.

It should be understood by those of ordinary skill in the art that there are various embodiments of frequency synthesizer 800. For example, the important aspect is that amplitude control circuit 802 communicates with controllable oscillator 202, and as the frequency of the output signal of the controllable oscillator is controlled, such as, for example, by phase-locked loop 206 and/or frequency control circuit 208, amplitude control circuit 802 maintains the amplitude of the output signal in a predetermined manner. Therefore, in some embodiments of frequency synthesizer 800, amplitude control circuit 802 may operate in conjunction with frequency control circuit 208. For instance, every time frequency control circuit 208 changes the frequency of the output signal of controllable oscillator 202, amplitude control circuit 802 may be enabled to adjust the amplitude of the output signal. This interaction between frequency control circuit 208 and amplitude control circuit 802 may be controlled by timing signals communicated via connection 805 (FIG. 8). In other embodiments of frequency synthesizer 800, there may be no frequency control circuit 208, in which case amplitude control circuit 802 responds to frequency changes produced by phase-locked loop 206.

FIG. 10 illustrates a block diagram of one of a number of embodiments of a controllable oscillator 1002 for implementing the plurality of operational states and corresponding distinct amplitudes for the output signal, which are controlled by amplitude control circuit 802. Controllable oscillator 1002 may comprise a plurality of switched current sources 1000 connected in parallel. Switched current sources 1000 receive the control signal from amplitude control circuit 802 on connection 806. In response to the control signal, switched current sources 1000 are engaged or disengaged in a predetermined manner corresponding to one of the operational states of controllable oscillator 1002. In one of numerous embodiments of frequency

synthesizer 800, the number of switched current sources 1000 defines the number of operational states and corresponding amplitudes for the output signal of controllable oscillator 1002. For instance, if there are three switched current sources 1000, controllable oscillator 1002 may have eight ($2^3 = 8$) operational states. Because each of the switched current sources 1000 may be engaged or disengaged, there are eight possible configurations for the switched current sources 1000, with each configuration producing a distinct amplitude for the output signal of controllable oscillator 1002.

The number of switched current sources 1000 also defines the number of control lines required for amplitude control circuit 802 to control controllable oscillator 1002. For example, if there are three switched current sources 1000 to be engaged or disengaged, amplitude control circuit 802 may use three control (one control line for each switched current source 1000). Amplitude control circuit 802 controls the operational state of controllable oscillator 1002 in the same manner as described above with respect to frequency control circuit 208.

FIG. 11 illustrates a block diagram of one of a number of embodiments of amplitude control circuit 802 for maintaining the amplitude of the output signal of controllable oscillator 1002. Amplitude control circuit 802 may comprise peak detector 1100, low pass filter 1102, amplifier 1104, and binary state search module 1106.

In the operation of amplitude control circuit 802, peak detector 1100 receives the output signal of controllable oscillator 1002 on connection 804. Peak detector 1100 determines the amplitude of the output signal and provides the information on connection 1108 to low pass filter 1102 where the signal is filtered. The filtered signal is provided on connection 1110 to amplifier 1104. Amplifier 1104 compares the information associated with the amplitude of the output signal of controllable oscillator 202 to a reference voltage 1112 and provides a control bit on connection 1114 to binary state search module 1106. For example, amplifier 1104 may be configured to generate a logic 1 for the control bit when the amplitude of the output signal of controllable oscillator 202 is higher than the reference voltage and a logic 0 for the control bit when the reference voltage is higher than the amplitude of the

output signal. Where amplitude control circuit 802 operates in conjunction with frequency control circuit 208, amplifier 1104 may be connected to, and controlled by, frequency control signal 208 via connection 805. Referring again to FIG. 7, binary state search module 1106 functions the same way as described above with respect to binary state search module 508. Again, where amplitude control circuit 802 operates in conjunction with frequency control circuit 208, binary state search module 1106 may be connected to, and controlled by, frequency control signal 208 via connection 805.

Any process descriptions or blocks in FIGS. 3, 6, and 9 should be understood as representing modules, segments, or portions of code which include one or more executable instructions for implementing specific logical functions or steps in the process, and alternate implementations are included within the scope of the preferred embodiment of the present invention in which functions may be executed out of order from that shown or discussed, including substantially concurrently or in reverse order, depending on the functionality involved, as would be understood by those reasonably skilled in the art.

In addition, frequency synthesizers 112 and 800, frequency control circuit 208, and amplitude control circuit 802, which may comprise an ordered listing of executable instructions for implementing logical functions, can be embodied in any computer readable medium for use by or in connection with an instruction execution system, apparatus, or device, such as a computer-based system, processor-containing system, or other system that can fetch the instructions from the instruction execution system, apparatus, or device and execute the instructions. In the context of this document, a "computer readable medium" can be any means that can contain, store, communicate, propagate, or transport the program for use by or in connection with the instruction execution system, apparatus, or device. The computer readable medium can be, for example but not limited to, an electronic, magnetic, optical, electromagnetic, infrared, or semiconductor system, apparatus, device, or propagation medium. More specific examples (a nonexhaustive list) of the computer-readable medium would include the following: an electrical connection (electronic) having

one or more wires, a portable computer diskette (magnetic), a random access memory (RAM) (electronic), a read-only memory (ROM) (electronic), an erasable programmable read-only memory (EPROM or Flash memory) (electronic), an optical fiber (optical), and a portable compact disc read-only memory (CDROM) (optical). Note that the computer readable medium could even be paper or another suitable medium upon which the program is printed, as the program can be electronically captured, via for instance optical scanning of the paper or other medium, then compiled, interpreted or otherwise processed in a suitable manner if necessary, and then stored in a computer memory.

While various embodiments of the invention have been described, it will be apparent to those of ordinary skill in the art that many more embodiments and implementations are possible that are within the scope of this invention.

CLAIMS

What is claimed is:

1. A frequency synthesizer circuit, comprising:

a controllable oscillator configured to generate an output signal having a predefined frequency, the controllable oscillator having a plurality of operational states responsive to a plurality of control signals, each of the plurality of operational states defining a distinct frequency for the output signal of the controllable oscillator; and

a frequency control circuit in communication with the controllable oscillator, the frequency control circuit configured to determine the distinct frequency for the output signal that best approximates the predefined frequency and to provide the plurality of control signals, the plurality of control signals configured to change the controllable oscillator to the operational state corresponding to the distinct frequency that best approximates the predefined frequency.

2. The circuit of claim 1, wherein the frequency control circuit comprises:

a frequency detector configured to determine the frequency of the output signal;

a comparator configured to compare the frequency of the output signal to the predefined frequency; and

logic configured to determine which of the plurality of distinct frequencies for the output signal corresponding to the plurality of operational states best approximates the predefined frequency.

3. The circuit of claim 1, wherein the controllable oscillator comprises a plurality of parallel capacitors capable of being engaged by the plurality of control signals, the plurality of parallel capacitors defining the plurality of operational states of the controllable oscillator.

4. The circuit of claim 1, wherein the logic implements a binary search algorithm to determine which of the plurality of distinct frequencies for the output signal corresponding to the plurality of operational states best approximates the predefined frequency.

5. The circuit of claim 1, wherein the frequency control circuit comprises:

a program counter configured to generate a timing signal based on the predefined frequency, the timing signal having a plurality of clock pulses;

a frequency detector configured to receive the timing signal and, in response to each of the plurality of clock pulses, to generate a first digital word corresponding to the current frequency of the output signal of the oscillator;

a digital decoder configured to receive information, the information associated with the predefined frequency of the output signal of the oscillator, and to generate a second digital word corresponding to the predefined frequency;

a digital comparator configured to compare the first digital word to the second digital word; and

logic configured to receive the timing signal and, in response to each of the plurality of clock pulses, to generate the plurality of control signals based on the comparison of the first digital word to the second digital word.

6. A communication device for use in a communication system, comprising:

a transceiver configured to communicate with the communication system via a communication channel at a channel frequency; and

a frequency synthesizer configured to select the communication channel, the frequency synthesizer comprising:

a controllable oscillator configured to generate an output signal having a predefined frequency corresponding to the channel frequency, the controllable oscillator having a plurality of operational states responsive to a plurality of control signals, each of the plurality of operational states defining a distinct frequency for the output signal of the controllable oscillator; and

a frequency control circuit in communication with the controllable oscillator, the frequency control circuit configured to determine the distinct frequency for the output signal that best approximates the predefined frequency and to provide the plurality of control signals, the plurality of control signals configured to change the controllable oscillator to the operational state corresponding to the distinct frequency that best approximates the predefined frequency.

7. A method for controlling the frequency of an output signal of a controllable oscillator, the controllable oscillator having a plurality of operational states, each of the plurality of operational states defining a distinct frequency for the output signal of the controllable oscillator, the method comprising:

receiving information associated with a predefined frequency;

determining which of the plurality of distinct frequencies for the output signal of the controllable oscillator best approximates the predefined frequency; and

generating a control signal configured to change the controllable oscillator to the operational state corresponding to the distinct frequency that best approximates the predefined frequency.

8. The method of claim 7, wherein the determining which of the plurality of distinct frequencies for the output signal of the controllable oscillator best approximates the predefined frequency involves a binary search algorithm.

9. The method of claim 8, further comprising changing the controllable oscillator to the operational state corresponding to the distinct frequency that best approximates the predefined frequency.

10. The method of claim 9, wherein the changing the controllable oscillator to the operational state corresponding to the distinct frequency that best approximates the predefined frequency involves configuring a plurality of parallel capacitors in a predetermined manner.

11. A method for controlling the frequency of an output signal of a controllable oscillator, the controllable oscillator having a plurality of operational states, each of the plurality of operational states defining a distinct frequency for the output signal of the controllable oscillator, the method comprising:

receiving information associated with a predefined frequency;

determining a current frequency of the output signal of the controllable oscillator, the current frequency corresponding to a current operational state;

comparing the predefined frequency to the current frequency;

based on the comparing the predefined frequency to the current frequency, selecting one of two next operational states, the selected next operational state having a distinct frequency which better approximates the predefined frequency.

12. The method of claim 11, further comprising generating a control signal configured to change the controllable oscillator to the selected next operational state.

13. The method of claim 12, further comprising changing the controllable oscillator to the selected next operational state.

14. The method of claim 13, wherein the changing the controllable oscillator to the selected next operational state involves configuring a plurality of parallel capacitors in a predetermined manner.

15. The method of claim 13, further comprising repeating the determining the current frequency of the output signal of the controllable oscillator, the comparing the predefined frequency to the current frequency, the selecting one of two next operational states, the generating a control signal configured to change the controllable oscillator to the selected next operational state, and the changing the controllable oscillator to the selected next operational state.

16. A system for controlling the frequency of an output signal of a controllable oscillator, the controllable oscillator having a plurality of operational states, each of the plurality of operational states defining a distinct frequency for the output signal of the controllable oscillator, the system comprising:

means for receiving information associated with a predefined frequency;

means for determining which of the plurality of distinct frequencies for the output signal of the controllable oscillator best approximates the predefined frequency; and

means for generating a control signal configured to change the controllable oscillator to the operational state corresponding to the distinct frequency that best approximates the predefined frequency.

17. The system of claim 16, wherein the means for determining which of the plurality of distinct frequencies for the output signal of the controllable oscillator best approximates the predefined frequency involves a binary search algorithm.

18. The system of claim 17, further comprising means for changing the controllable oscillator to the operational state corresponding to the distinct frequency that best approximates the predefined frequency.

19. The system of claim 18, wherein the means for changing the controllable oscillator to the operational state corresponding to the distinct frequency that best approximates the predefined frequency comprises a plurality of parallel capacitors configured in a predetermined manner.

20. A system for controlling the frequency of an output signal of a controllable oscillator, the controllable oscillator having a plurality of operational states, each of the plurality of operational states defining a distinct frequency for the output signal of the controllable oscillator, the system comprising:

means for receiving information associated with a predefined frequency;

means for determining a current frequency of the output signal of the controllable oscillator, the current frequency corresponding to a current operational state;

means for comparing the predefined frequency to the current frequency;

means for selecting, based on the comparing the predefined frequency to the current frequency, one of two next operational states, the selected next operational state having a distinct frequency which better approximates the predefined frequency.

21. The system of claim 20, further comprising means for generating a control signal configured to change the controllable oscillator to the selected next operational state.

22. The system of claim 21, further comprising means for changing the controllable oscillator to the selected next operational state.

23. The system of claim 22, wherein the means for changing the controllable oscillator to the selected next operational state comprises a plurality of capacitors configured in a predetermined manner.

24. The system of claim 22, further configured to repeat the determining the current frequency of the output signal of the controllable oscillator, the comparing the predefined frequency to the current frequency, the selecting one of two next operational states, the generating a control signal configured to change the controllable oscillator to the selected next operational state, and the changing the controllable oscillator to the selected next operational state.

25. A computer readable medium for controlling the frequency of an output signal of a controllable oscillator, the controllable oscillator having a plurality of operational states, each of the plurality of operational states defining a distinct frequency for the output signal of the controllable oscillator, the computer readable medium comprising logic configured to receive information associated with a predefined frequency, to determine the distinct frequency for the output signal of the controllable oscillator that best approximates the predefined frequency, and to generate a control signal configured to change the controllable oscillator to the operational state corresponding to the distinct frequency that best approximates the predefined frequency.

26. The computer readable medium of claim 25, wherein the logic for determining the distinct frequency for the output signal of the controllable oscillator that best approximates the predefined frequency involves a binary search algorithm.

27. The computer readable medium of claim 26, wherein the logic is further configured to change the controllable oscillator to the operational state corresponding to the distinct frequency that best approximates the predefined frequency.

28. A computer readable medium for controlling the frequency of an output signal of a controllable oscillator, the controllable oscillator having a plurality of operational states, each of the plurality of operational states defining a distinct frequency for the output signal of the controllable oscillator, the computer readable medium comprising logic configured to receive information associated with a predefined frequency, to determine a current frequency of the output signal of the controllable oscillator, the current frequency corresponding to a current operational state, to compare the predefined frequency to the current frequency, and to select, based on the comparing the predefined frequency to the current frequency, one of two next operational states, the selected next operational state having a distinct frequency which better approximates the predefined frequency.

29. The computer readable medium of claim 28, wherein the logic is further configured to generate a control signal configured to change the controllable oscillator to the selected next operational state.

30. The computer readable medium of claim 29, wherein the logic is further configured to change the controllable oscillator to the selected next operational state.

31. The computer readable medium of claim 29, wherein the logic is further configured to repeat the determining the current frequency of the output signal of the controllable oscillator, the comparing the predefined frequency to the current frequency, the selecting one of two next operational states, the generating a control signal configured to change the controllable oscillator to the selected next operational state, and the changing the controllable oscillator to the selected next operational state.

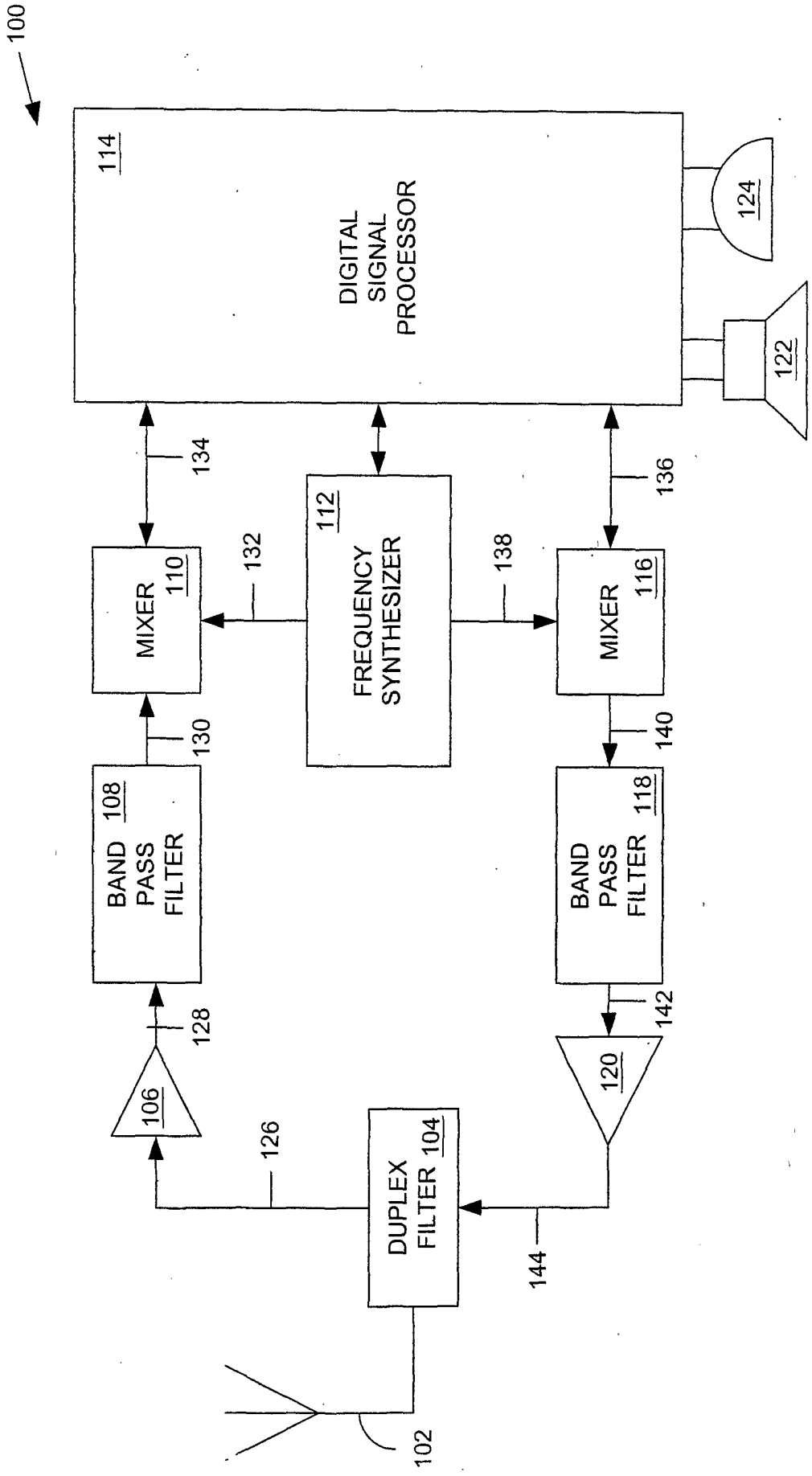

100
114
DIGITAL SIGNAL PROCESSOR
124
122
134
136
112
FREQUENCY SYNTHESIZER
132
138
MIXER 110
MIXER 116
130
140
BAND PASS FILTER 108
BAND PASS FILTER 118
128
142
106
120
126
DUPLEX FILTER 104
144
102

FIG. 1

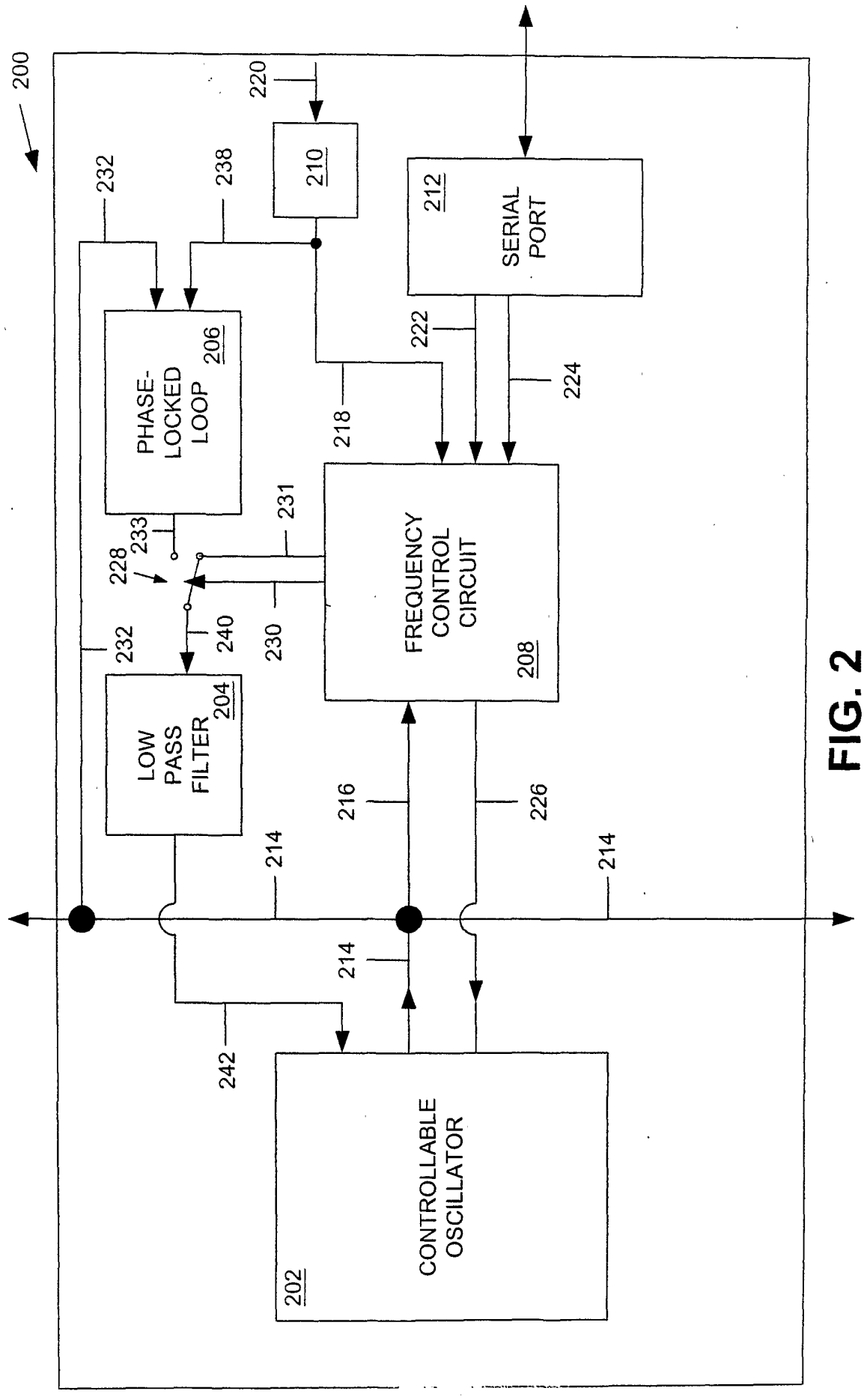

200
220
210
232
238
212
SERIAL PORT
PHASE-LOCKED LOOP 206
222
224
218
231
233
228
FREQUENCY CONTROL CIRCUIT 208
240
230
232
LOW PASS FILTER 204
216
226
214
214
214
242
CONTROLLABLE OSCILLATOR 202

FIG. 2

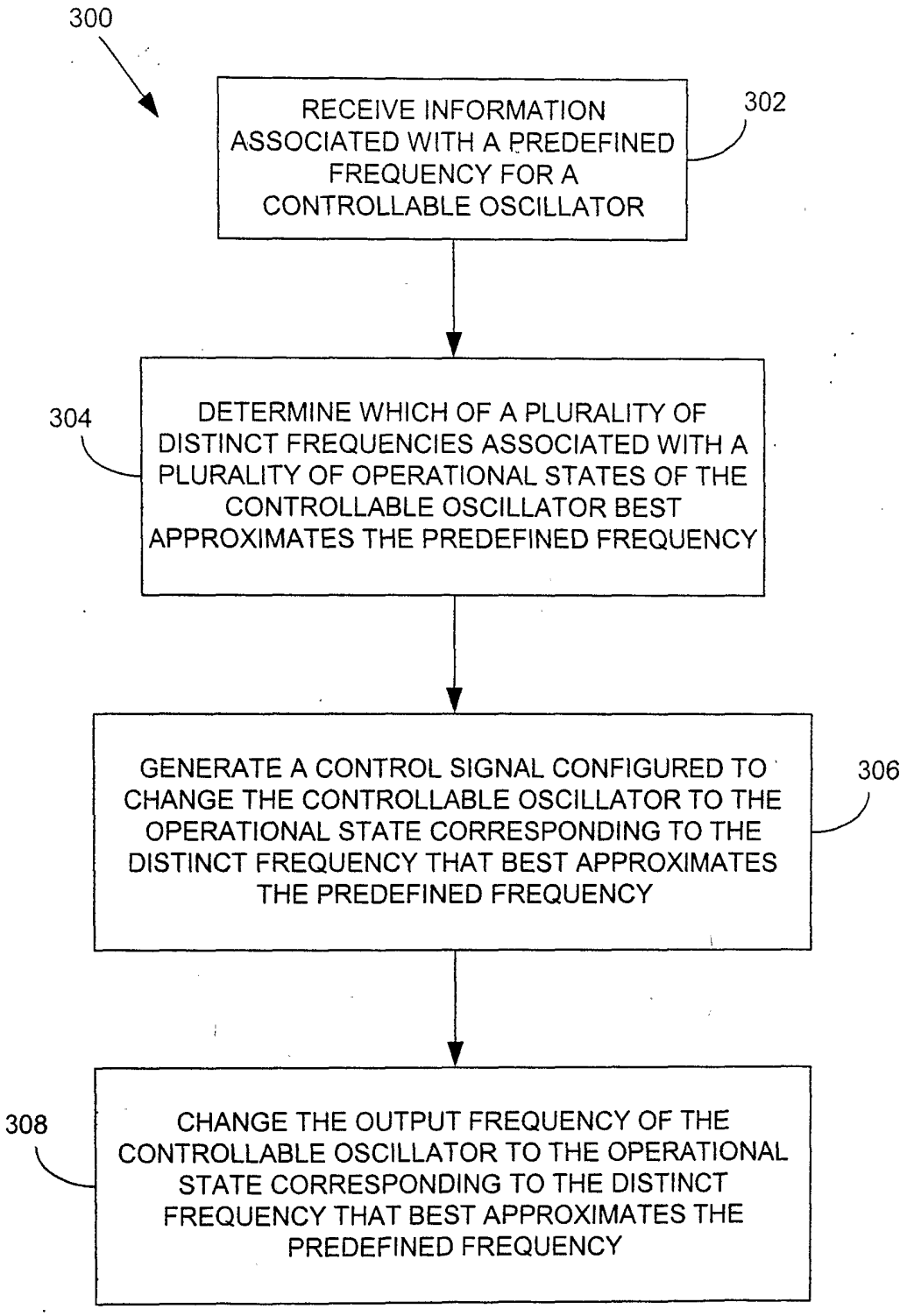

300
RECEIVE INFORMATION ASSOCIATED WITH A PREDEFINED FREQUENCY FOR A CONTROLLABLE OSCILLATOR
302
DETERMINE WHICH OF A PLURALITY OF DISTINCT FREQUENCIES ASSOCIATED WITH A PLURALITY OF OPERATIONAL STATES OF THE CONTROLLABLE OSCILLATOR BEST APPROXIMATES THE PREDEFINED FREQUENCY
304
GENERATE A CONTROL SIGNAL CONFIGURED TO CHANGE THE CONTROLLABLE OSCILLATOR TO THE OPERATIONAL STATE CORRESPONDING TO THE DISTINCT FREQUENCY THAT BEST APPROXIMATES THE PREDEFINED FREQUENCY
306
CHANGE THE OUTPUT FREQUENCY OF THE CONTROLLABLE OSCILLATOR TO THE OPERATIONAL STATE CORRESPONDING TO THE DISTINCT FREQUENCY THAT BEST APPROXIMATES THE PREDEFINED FREQUENCY
308

FIG. 3

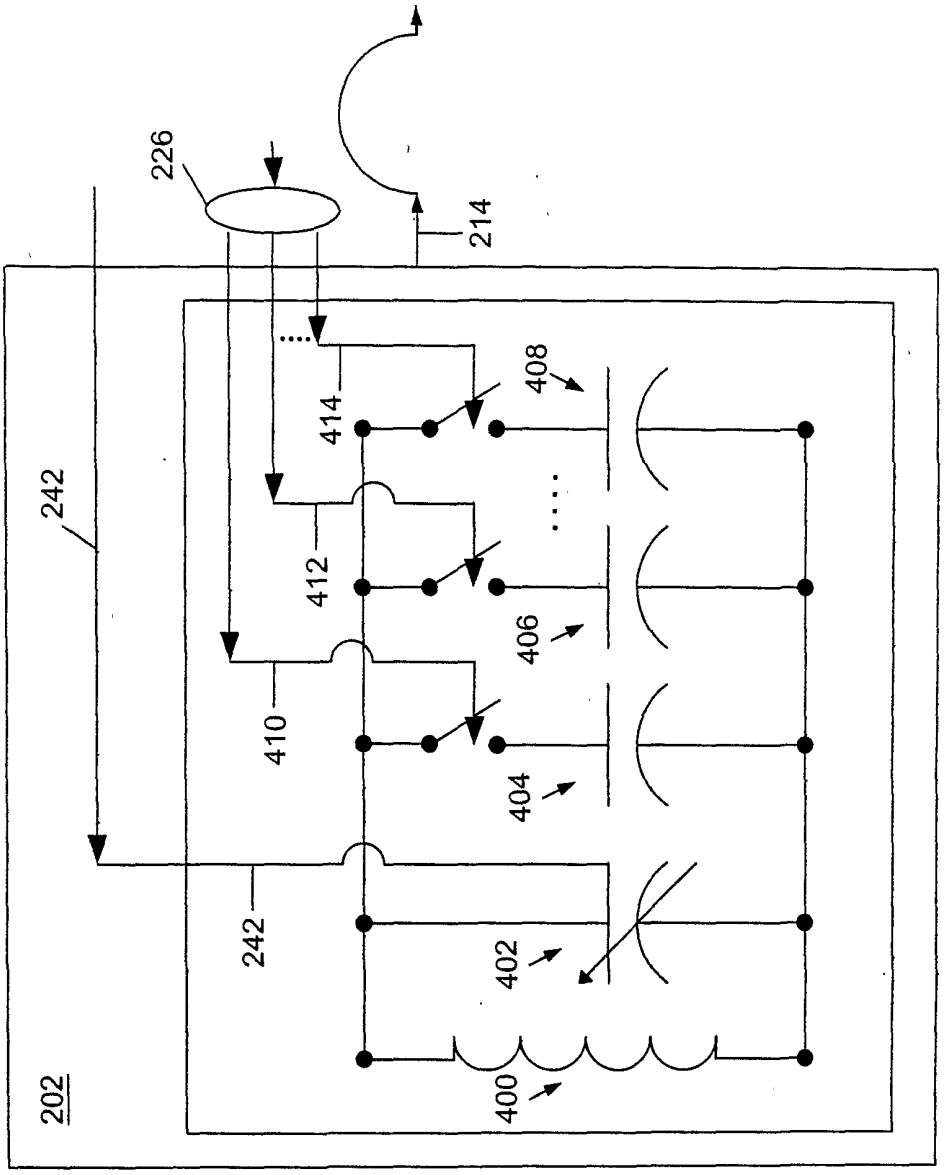


FIG. 4

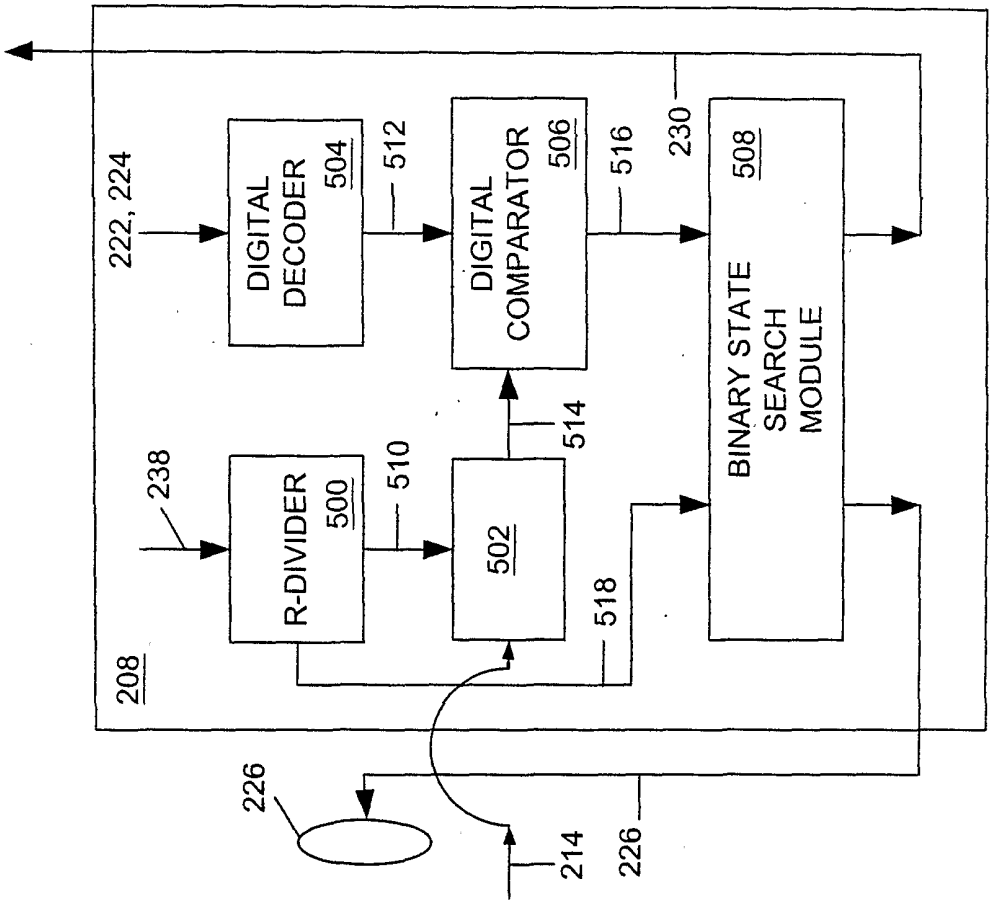

208
222, 224
DIGITAL DECODER 504
512
DIGITAL COMPARATOR 506
516
230
BINARY STATE SEARCH MODULE 508
238
R-DIVIDER 500
510
502
514
518
226
214
226

FIG. 5

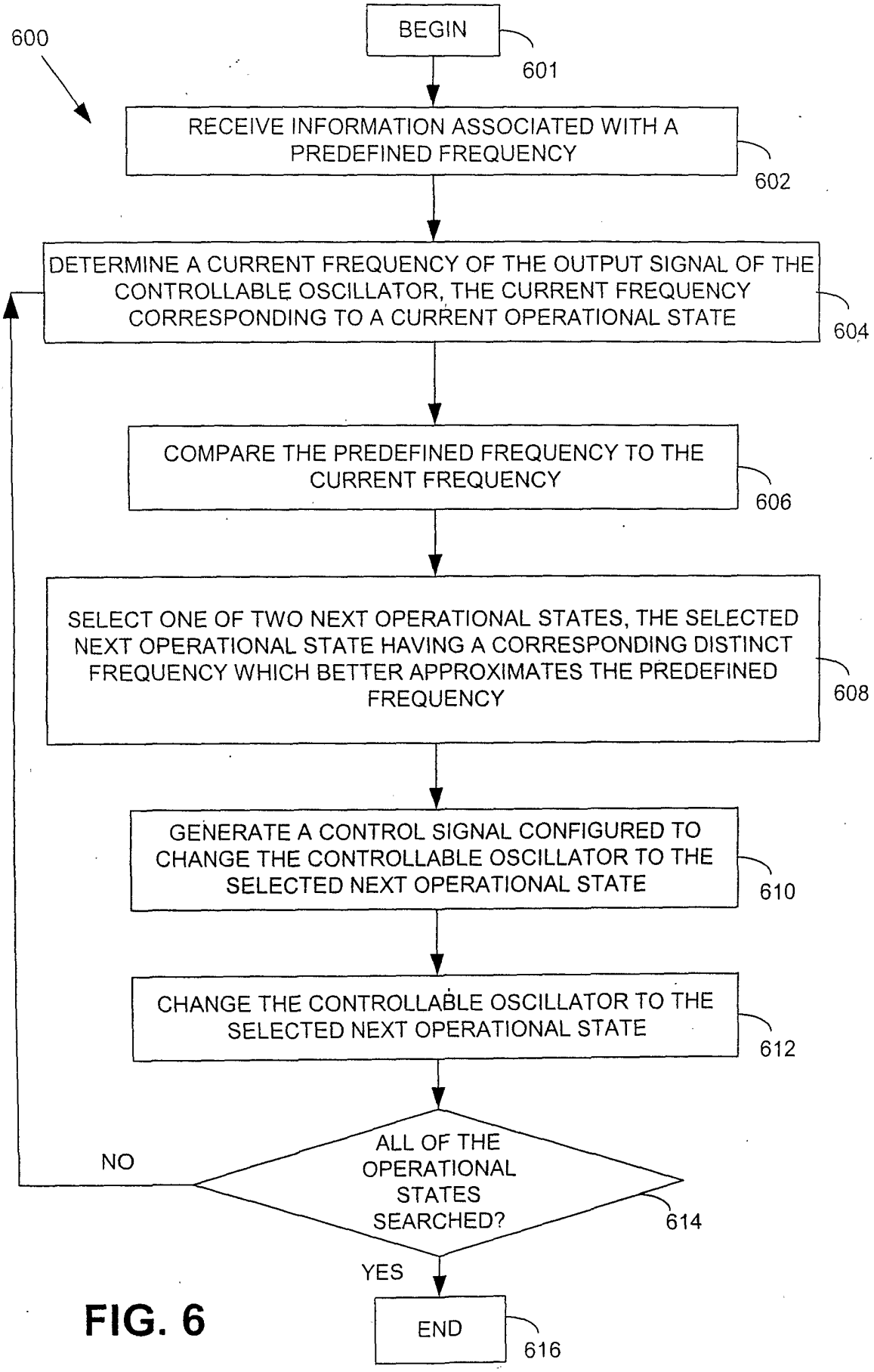

600
BEGIN
601
RECEIVE INFORMATION ASSOCIATED WITH A PREDEFINED FREQUENCY
602
DETERMINE A CURRENT FREQUENCY OF THE OUTPUT SIGNAL OF THE CONTROLLABLE OSCILLATOR, THE CURRENT FREQUENCY CORRESPONDING TO A CURRENT OPERATIONAL STATE
604
COMPARE THE PREDEFINED FREQUENCY TO THE CURRENT FREQUENCY
606
SELECT ONE OF TWO NEXT OPERATIONAL STATES, THE SELECTED NEXT OPERATIONAL STATE HAVING A CORRESPONDING DISTINCT FREQUENCY WHICH BETTER APPROXIMATES THE PREDEFINED FREQUENCY
608
GENERATE A CONTROL SIGNAL CONFIGURED TO CHANGE THE CONTROLLABLE OSCILLATOR TO THE SELECTED NEXT OPERATIONAL STATE
610
CHANGE THE CONTROLLABLE OSCILLATOR TO THE SELECTED NEXT OPERATIONAL STATE
612
ALL OF THE OPERATIONAL STATES SEARCHED?
614
NO
YES
END
616

FIG. 6

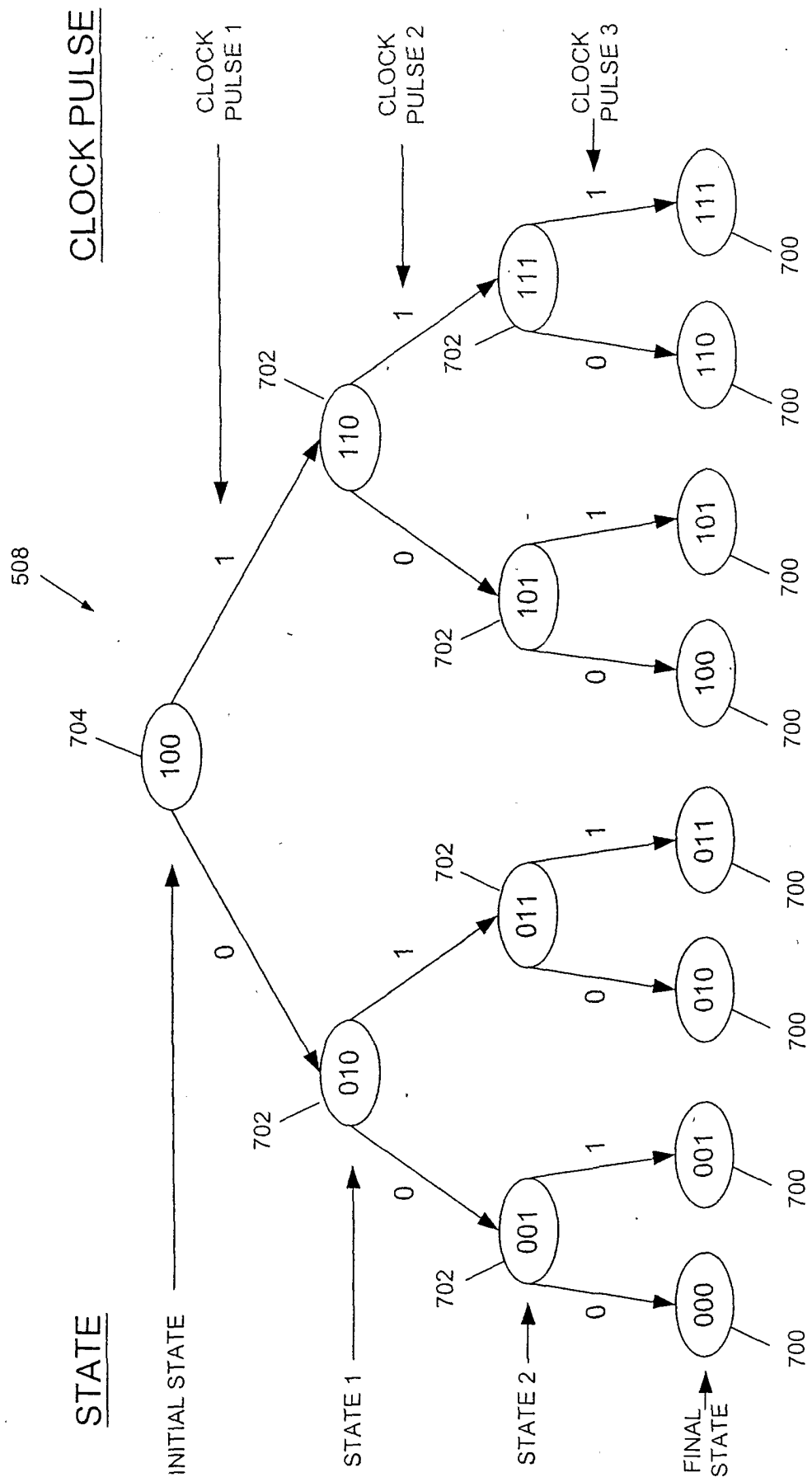

CLOCK PULSE
CLOCK PULSE 1
CLOCK PULSE 2
CLOCK PULSE 3
508
704
100
702
010
110
001
011
101
111
000
001
010
011
100
101
110
111
700
STATE
INITIAL STATE
STATE 1
STATE 2
FINAL STATE
0
1

FIG. 7

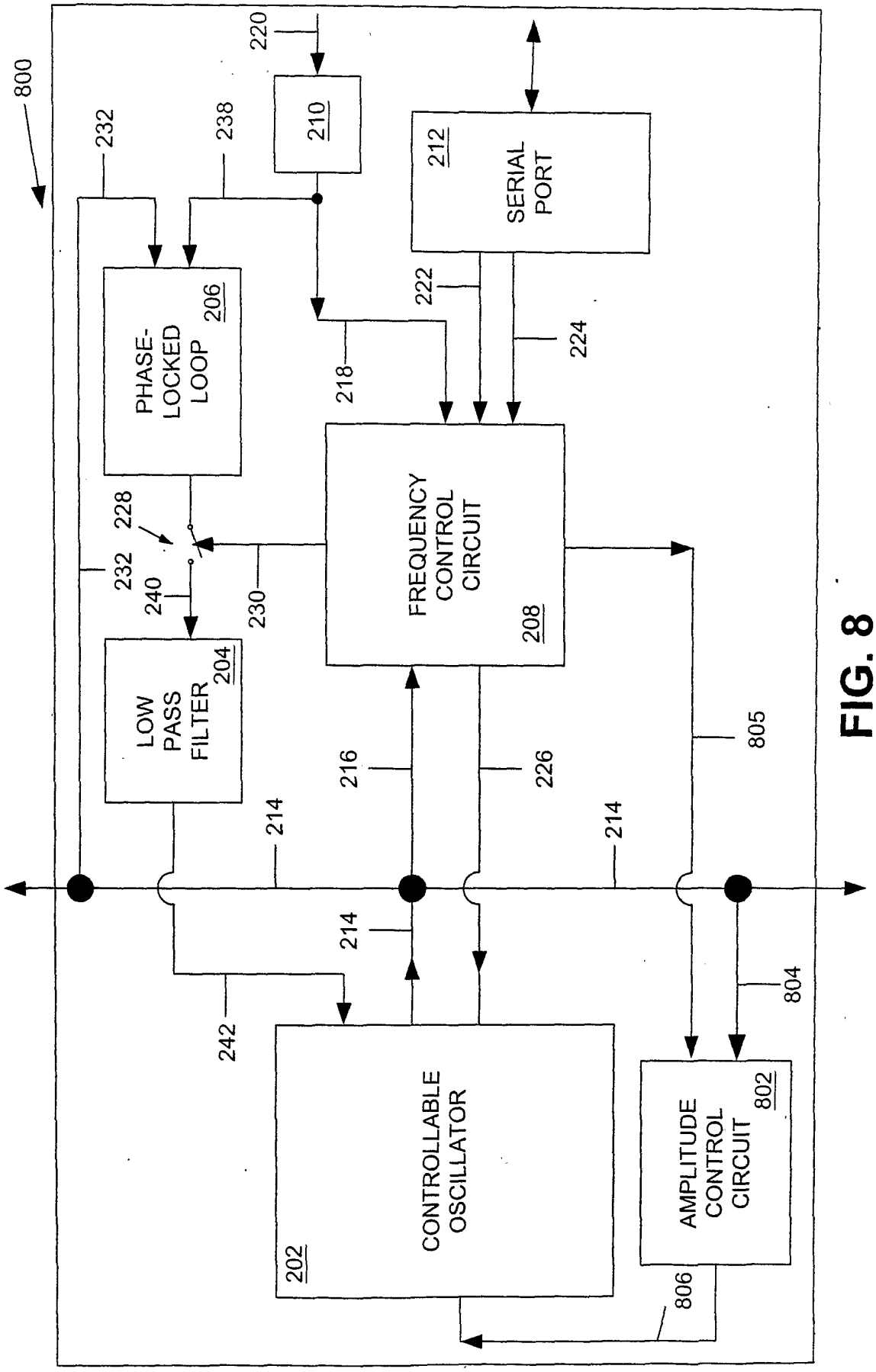

800
220
210
212
SERIAL PORT
232
238
PHASE-LOCKED LOOP 206
222
224
218
FREQUENCY CONTROL CIRCUIT 208
228
232
240
230
LOW PASS FILTER 204
216
226
805
214
214
214
804
242
CONTROLLABLE OSCILLATOR 202
AMPLITUDE CONTROL CIRCUIT 802
806

FIG. 8

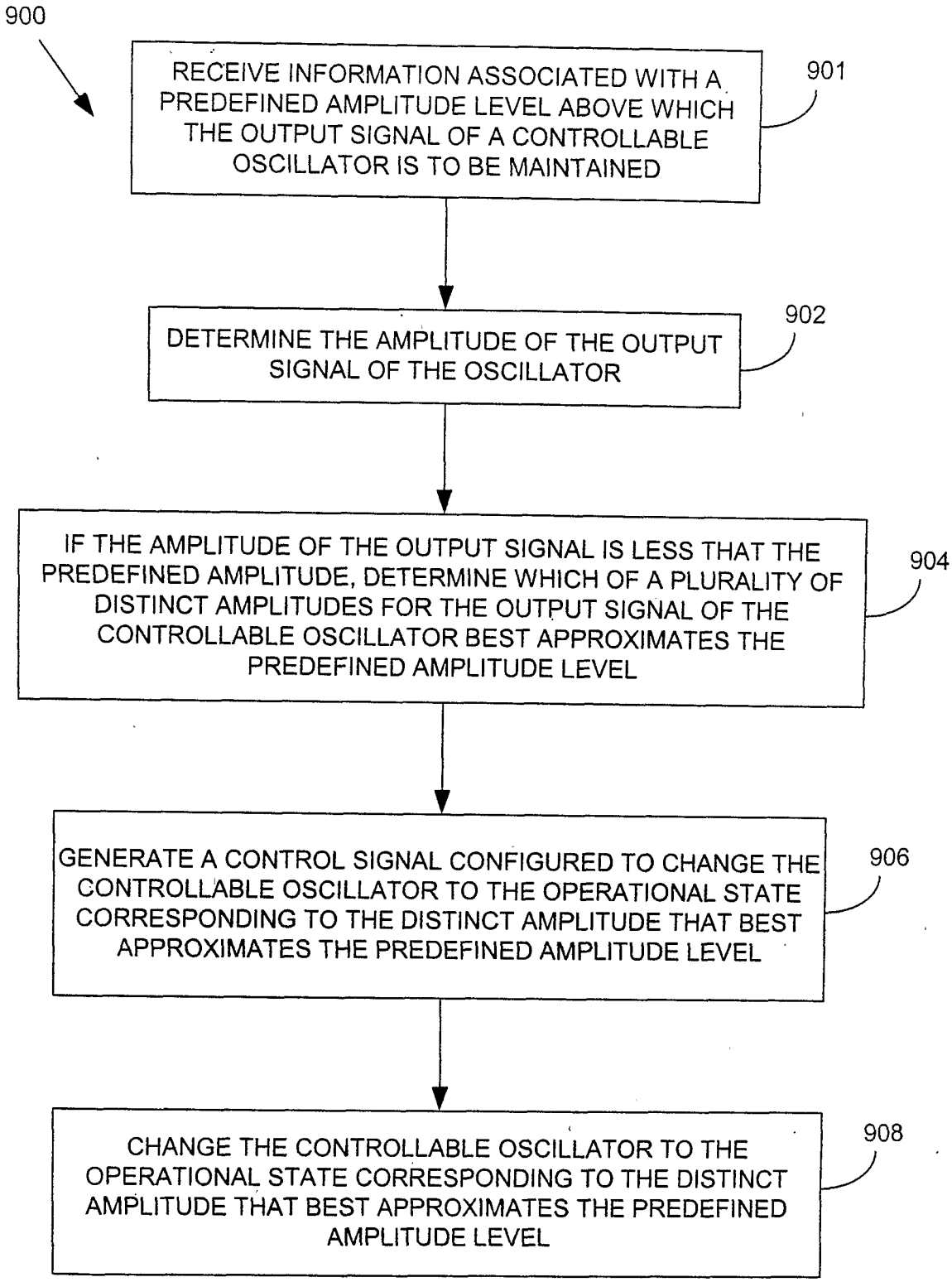

900
RECEIVE INFORMATION ASSOCIATED WITH A PREDEFINED AMPLITUDE LEVEL ABOVE WHICH THE OUTPUT SIGNAL OF A CONTROLLABLE OSCILLATOR IS TO BE MAINTAINED
901
DETERMINE THE AMPLITUDE OF THE OUTPUT SIGNAL OF THE OSCILLATOR
902
IF THE AMPLITUDE OF THE OUTPUT SIGNAL IS LESS THAT THE PREDEFINED AMPLITUDE, DETERMINE WHICH OF A PLURALITY OF DISTINCT AMPLITUDES FOR THE OUTPUT SIGNAL OF THE CONTROLLABLE OSCILLATOR BEST APPROXIMATES THE PREDEFINED AMPLITUDE LEVEL
904
GENERATE A CONTROL SIGNAL CONFIGURED TO CHANGE THE CONTROLLABLE OSCILLATOR TO THE OPERATIONAL STATE CORRESPONDING TO THE DISTINCT AMPLITUDE THAT BEST APPROXIMATES THE PREDEFINED AMPLITUDE LEVEL
906
CHANGE THE CONTROLLABLE OSCILLATOR TO THE OPERATIONAL STATE CORRESPONDING TO THE DISTINCT AMPLITUDE THAT BEST APPROXIMATES THE PREDEFINED AMPLITUDE LEVEL
908

FIG. 9

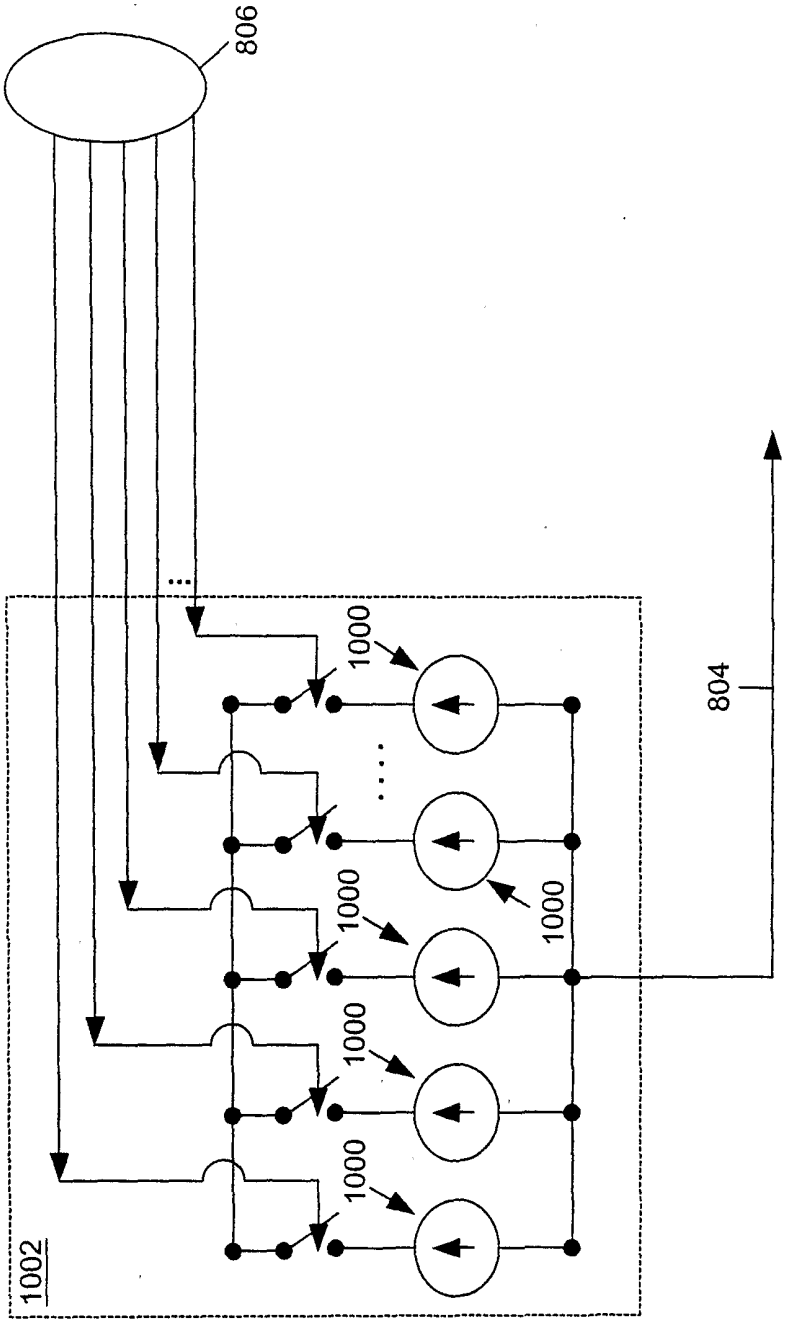


FIG. 10

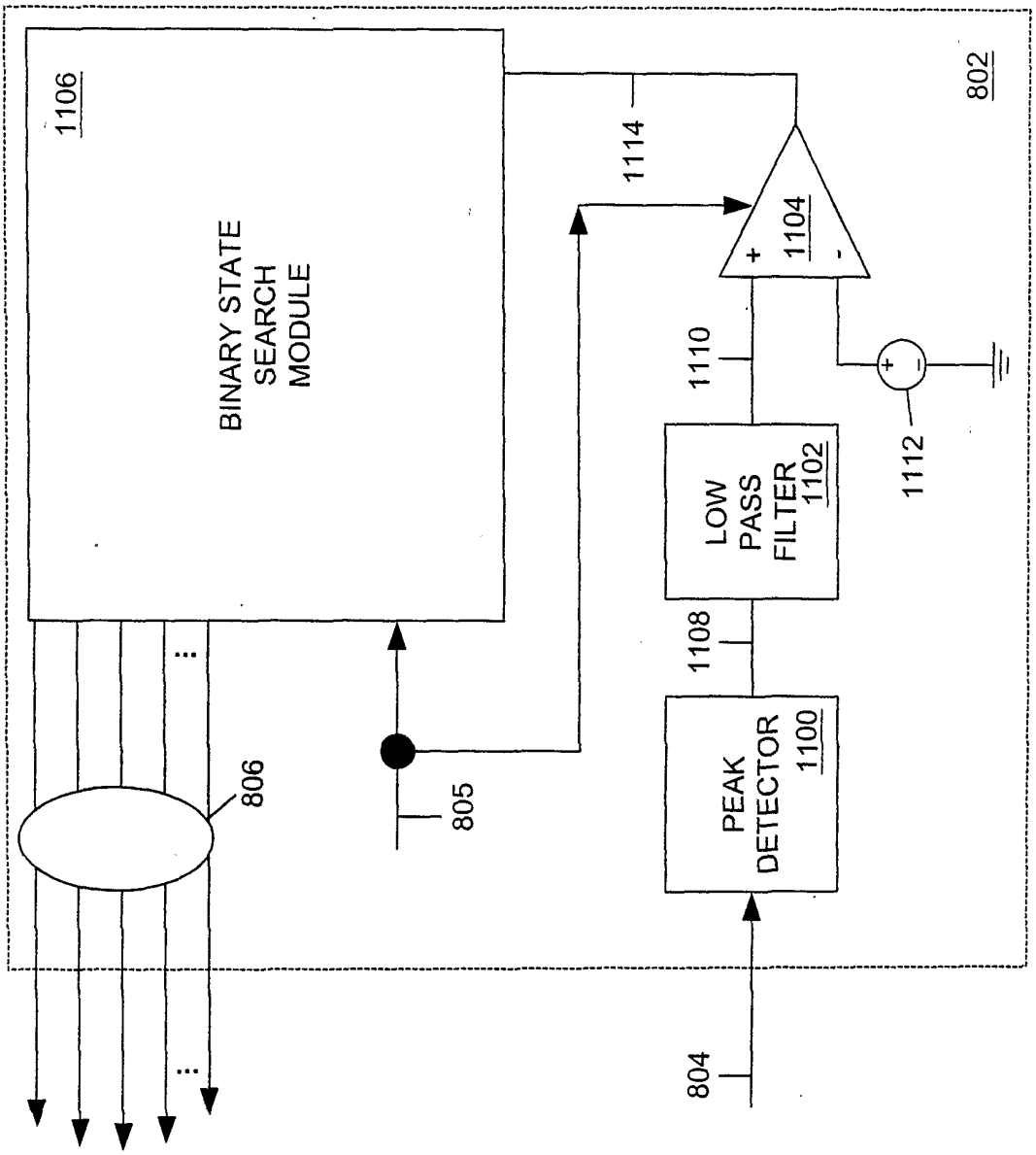

1106
BINARY STATE SEARCH MODULE
802
1114
1104
+
-
1110
LOW PASS FILTER 1102
1112
1108
PEAK DETECTOR 1100
804
805
806

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/09243

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :Please See Extra Sheet.
US CL :Please See Extra Sheet.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 375/376, 327, 344, 375, 294; 331/25; 327/147, 156; 445/165.1, 260, 325 .

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y,P	US 6,323,736 B2 (JANSSON) 27 November 2001, see entire document.	1-31
Y,P	US 6,317,027 B1 (WATKINS) 13 November 2001, see entire document.	1-31

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 07 MAY 2002	Date of mailing of the international search report 05 JUN 2002
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A. CLASSIFICATION OF SUBJECT MATTER:
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