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(54) Title: REVERSE LINK CORRELATION FILTER IN WIRELESS COMMUNICATION SYSTEMS

(57) Abstract: A single, common correlation filter (CF) core is provided in a wireless system using CDMA (code division multiple access). A plurality of channels with different data rates are provided in the wireless system. The channels provided in the wireless system include the access channel, the maintenance channel, and the traffic channel in which information (e.g., pilot or data symbols or both) is transmitted at the tier 1 (which is the basic despreading rate), tier 2 and tier 3 rates. The data rate for transmitting the information is programmable by an external programmable processor, e.g., a digital signal processor (DSP). A user-unique code, such as a PN (pseudo-random noise) code, is applied to the information being transmitted in the channels of the wireless system. Theinformation is modulated and transmitted in any one of the channels at any data rate. The transmitted information is correlated at the basic despreading rate (i.e., the tier 1 rate) in the correlation filter (CF) of the wireless system by time multiplexing delayed versions of the PN code (or orthogonal code, Walsh code) to the correlation filter core. The correlated information is then demultiplexed and demodulated. The demodulated information is summed at the proper integer multiple of the tier 1 rate to achieve the tier 2 and tier 3 rates. One or more signal components are selected (in terms of the received power, signal-to-noise ratio or multipath width) in a window or time period for optimal information recovery. The selecting step can also be implemented according to a pre-programmed time alignment. Furthermore, outputs from the demodulated information can be provided and combined for temporal diversity. Spatial diversity is achieved by providing a plurality of antennas, and a plurality of receivers at a location and providing a single, common correlation filter at each of the plurality of antennas of the receivers in the wireless system.

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REVERSE LINK CORRELATION FILTER IN WIRELESS COMMUNICATION SYSTEMS

RELATED APPLICATIONS

The present application claims priority to U.S. Provisional Patent Application Serial No. 60/184,364 entitled REVERSE LINK CORRELATION FILTER IN WIRELESS COMMUNICATION SYSTEMS filed on February 23, 2000. Copending U.S. Patent Application Serial No. 09/497,440 filed on February 3, 2000 and entitled PILOT SYMBOL ASSISTED MODULATION AND DEMODULATION IN WIRELESS COMMUNICATION SYSTEMS, is also a related application.

FIELD OF THE INVENTION

The present invention relates to a code division multiple access (CDMA) communication system and, more particularly to a receiver having a correlation filter in such a CDMA communication system.

DESCRIPTION OF THE RELATED ART

Code Division Multiple Access (CDMA) modulation, which is known in

the art, is a multi-user access transmission scheme in which signals from different users overlap both in frequency and in time. This is in contrast to Frequency Division Multiple Access (FDMA), also known in the art, in which user signals overlap in time, but are assigned unique frequencies, and Time Division Multiple Access (TDMA) in which user signals overlap in frequency, but are assigned unique time slots. CDMA signaling is frequently used in cellular communication systems between a base station (BS) within a cell and a plurality of mobile stations (MS) in the possession of users within the cell. The CDMA transmitted signal for each user that broadcast from the user's mobile station (MS) is spread over a wide bandwidth, which is greater than the initial user information bandwidth. Each user's signal is spread by a different spreading code to create a wideband spread. All of the spread wideband signals transmitted by the different users are received at the base station (BS) and form a composite received signal. The receiver at the base station (BS) distinguishes different users by using a local copy (or local reference) of the spreading code, which is available to both the mobile stations and the base station in the CDMA system. Such a process is called channelization. In an exemplary CDMA system according to the IS-95 standard and which is well known in the art, channelization in the reverse link, *i.e.*, when a mobile station (MS) is transmitting to a base station (BS) in the system, is accomplished using a wideband code called a pseudorandom noise (PN) code, also known in the art. The receiver at the base station (BS) sifts the desired signal from a particular user out of the composite signal by correlating, i.e., using a correlation filter (CF), on the composite signal with the original wideband code. All other signals having codes that do not match the code for the desired user code are rejected.

An exemplary CDMA wireless system includes a plurality of data channels, e.g., the access and traffic channels (and more channels depending on the design of the CDMA system). In the reverse link, the traffic channel is used to transmit user data and voice, as well as signaling messages. The access channel is used by the mobile station (MS), e.g., a cellular phone, to communicate control information with the base station (BS) in the wireless system when the MS does not have a traffic channel assigned. In particular, the MS uses the access channel to make call originations and to respond to pages and orders. These data channels in the CDMA system have different

functions and data rates. A receiver in the MS designed to accommodate data transmission in the different channels requires various types of correlation filter (CF) and digital signal processing (DSP) designs for different data rates. Such requirements contribute to the complexity and increase the cost of the receiver design.

There is, therefore, a general need in the art for a wireless system with a flexible, non-complex receiver design. A wireless system is particularly needed that provides a single correlation filter (CF) in the receiver which can be used in receiving data in all data channels. There is a further need for a receiver design with a correlation filter that serves all data channels and is also DSP programmable, which enhances system flexibility.

SUMMARY OF THE INVENTION

The invention relates to a reverse link receiver in wireless systems and a correlation filter thereof. A transmitter and a receiver are provided in the reverse link of a wireless system according to the invention. The receiver includes (1) a field programmable gate array (FPGA) which comprises a pseudorandom noise (PN) code generator, (2) a pilot post processor, (3) a data post processor (4) a correlation filter (CF), and (5) an external programmable processor such as a digital signal processor (DSP). The field programmable gate array (FPGA) and the correlation filter (CF), along with the digital signal processor (DSP), are included in the receiver to recover the original data transmitted by the transmitter. The correlation filter (CF) comprises a (correlating filter) CF core for processing data in the three channels, namely the access, maintenance and traffic channels. The external programmable processor is used to control and post-process the outputs of the field programmable gate array FPGA. A mode controller in the external programmable processor controls the channel selection (from the access, maintenance and traffic channels) and the channel symbol mode (data and/or pilot). The pilot post processor and data post processor in the FPGA, in conjunction with the external programmable processor, provide pilot symbol aided QPSK demodulation of up to 3 multipaths received at the receiver. QPSK modulation is a modulation technique that allows the transmission of two bits of information in each symbol period. QPSK modulation makes use of the quadrature component I in addition to the in-phase

component Q of a symbol in the frame being transmitted from the transmitter to the receiver. The I and Q components are typically viewed as the real and imaginary parts of a complex signal being transmitted in the channels of the CDMA system. In QPSK, the in-phase component, I, and the quadrature component, Q, can be combined without interfering with each other (i.e., they are orthogonal to each other) which doubles the bandwidth efficiency in comparison with simply transmitting one bit of information in a symbol period. Using time multiplexing, the CF core provides pilot symbol correlation at the three data or chip rates (tiers 1, 2 and 3). A chip is a unit of time which corresponds to the output interval of the PN spreading code. The chip time determines the bandwidth of the CDMA waveform and the chip time divided by the user symbol time determines the spreading factor of the system. For example, the sampling period for a chip in CDMA standard IS-95, known in the art, is $\frac{1}{1228800}$ seconds. The pilot post processing and data post processing in the FPGA, in conjunction with the data post processor and pilot post processor in the external programmable processor (such as a DSP), provide QPSK demodulation and recovery of the original data transmitted by the transmitter for all three channels, *i.e.*, the access, maintenance and traffic channels. The CF core according to the invention performs 8-chip (i.e., tier 1 rate or the basic despreading rate) complex correlation with 64 correlation lags while allowing no data loss as the 64 correlation lags are being processed, where a lag is a time instant for which the PN code (or orthogonal code, Walsh code) is held constant so that outputs can be generated. The basic despreading rate can also be 4 chips per symbol. This is advantageously achieved with a single time-multiplexed 8-chip correlator engine (i.e., CF core). The CF core, which is an 8-chip correlation engine, is time multiplexed to allow multiple 8-chip correlations to be performed with the same correlation engine. Furthermore, the invention advantageously provides the ability to generate integer multiples of the 8-chip correlation for larger correlation lengths, e.g., 32 chips (tier 2) or 128 chips (tier 3). The CF design according to the invention, in conjunction with the DSP, provides temporal diversity of the data signals by combining CF outputs. Spatial diversity is also achieved by providing a plurality of correlation filters in accordance with the CF design of the invention. Diversity is a technique employed to avoid or mitigate the negative effects of fading and interference. Diversity generally refers to the ability

of a communication system to receive data or information via several independently fading channels. In general, diversity enhances a receiver's ability to combine or select (or both) data signals arriving from these independently fading channels, thereby enabling (or facilitating) the extraction of data channels. A particular type of diversity is temporal or time diversity, where the same data signals transmitted in different multipaths and received at different time points at the receiver provide the diversity needed for combining or selecting the data signals. An exemplary diversity technique is maximum ratio combining, or MRC, known in the art. MRC provides sequences of weights in the multitude of data channels in the communication system. A sequence of distinct weights is assigned to segments of a data signal being transmitted. Copies of the data signal are produced for the antennas used in transmitting the data signal. This gives rise to temporal diversity at the receiver when copies of the data signal are received. With a single, common correlation filter design, the invention advantageously provides temporal diversity for all the data channels and modes without the necessity of using different correlation filters for different modes or channels. Temporal diversity is achieved by providing three outputs from the different multipaths and combining the three outputs into one, e.g., using MRC.

According to an embodiment of the method of the invention, a single, common correlation filter (CF) design is provided in a wireless system using CDMA. A plurality of channels with different data rates are provided in the wireless system. The channels provided in the wireless system include the access channel, the maintenance channel, and the traffic channel in which information (e.g., pilot or data symbols or both) is transmitted at the tier 1 (which is the basic despreading rate), tier 2 and tier 3 rates. The data rate for transmitting the information is programmable by the external programmable processor. A user-unique code, such as a PN code (or orthogonal code, Walsh code), is applied to the information being transmitted in the channels of the wireless system. The information is QPSK modulated and transmitted in any one of the channels and at any data rate. The transmitted information is correlated at the basic despreading rate (i.e., the tier 1 rate) using time multiplexing in the correlation filter (CF) of the wireless system. The basic despreading rate can be 4 or 8 chips per symbol. The correlated information is then demultiplexed and QPSK-demodulated. The demodulated

information is summed at the proper integer multiple of the tier 1 rate (the basic despreading rate) to achieve the tier 2 and tier 3 rates if needed. One or more signal components (in terms of the received power, signal-to-noise ratio or multipath width) are selected in a window or time period for optimal information recovery. The selecting step can also be implemented according to a preprogrammed time alignment. Furthermore, three outputs from the demodulated information can be provided and combined for temporal diversity. Spatial diversity is achieved by providing the single, common correlation filter design in a plurality of receivers in the wireless system. All the process steps according to the invention described herein are advantageously accomplished using a single, common correlation filter (CF) design, which eliminates the need for additional correlators or correlation filters for processing received information having multiple data rates.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features, aspects, and advantages of the invention will become more readily apparent with reference to the following detailed description of a presently preferred, but nonetheless illustrative, embodiment when read in conjunction with the accompanying drawings. In the accompanying drawings:

Figure 1 is a diagram generally illustrating a transmitter and a receiver in the reverse link in accordance with the invention;

Figure 2 is a diagram illustrating the structure of a frame of data/pilot symbols being transmitted in various channels in an embodiment according to the invention;

Figure 3 is a diagram illustrating a receiver with a field programmable gate array (FPGA) forming a correlation filter (CF) according to the invention;

Figure 4 is a diagram illustrating an exemplary field programmable gate array forming a correlation filter (CF) core for all channels in the wireless system according to the invention;

Figure 5 is a diagram illustrating an exemplary 8-chip correlation with a pseudorandom noise (PN) code according to the invention;

Figure 6 is a diagram illustrating the pilot post processing of all the channels in an embodiment of the wireless system according to the invention;

Figure 6A shows diagrams illustrating the gain coefficient setting of an accumulating filtering random access memory (AFRAM) and a magnitude accumulating filtering random access memory (MAFRAM) for three different data rates in an embodiment according to the invention;

Figure 6B is a diagram illustrating the basic structure of an embodiment of the AFRAM and MAFRAM according to the invention;

Figure 7 is a diagram illustrating the multipath search processing of multipath response peaks according to the invention;

Figure 7A is a flow diagram illustrating an embodiment of the method of the multipath search processing of multipath response peaks according to the invention;

Figure 8 is a diagram illustrating the data post processing in the channels of the wireless system according to the invention; and

Figure 9 is a flow diagram illustrating an embodiment of the method of QPSK modulation according to the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Turning to Figure 1, a transmitter 10 and a receiver 20 communicate over the reverse link in an exemplary wireless system according to the invention. In Figure 1, transmitter 10, Tx 1, is a part of a mobile station (MS) or mobile cellular phone communicating with receiver 20, Rx 2, which is part of a base station (BS). Digital information at a basic data rate is coded or spread to a transmit data rate (or chip rate) at transmitter 10. A user-unique digital code (the signature or spreading sequence) is applied to the digital information being transmitted, which increases the bandwidth. The application of the digital code, such as a pseudorandom noise (PN) code, typically involves multiplication or logical XOR (exclusive-or) operations on the digital information being transmitted with the PN code (or orthogonal code, Walsh code). The resulting transmitted data sequences or chips are then QPSK modulated at transmitter 10 to generate an output signal. The output signal is added to other similarly processed output signals for multi-channel transmission to the receiver 20 over a communications

medium. The output signals of multiple users advantageously share a single transmission communications frequency, with the multiple signals appearing to be located on top of each other in both the frequency domain and the time domain. Because the applied digital codes are orthogonal and user unique, each output signal transmitted over the shared communications frequency is similarly unique, and can be distinguished from each other through the application of proper processing techniques at receiver 20.

The receiver 20, comprises a correlation filter CF 3 formed by a field programmable gate array FPGA 5 and a digital signal processor DSP 4. In receiver 20, the received signals are QPSK-demodulated and the appropriate digital code for the user of interest is applied to (i.e., multiplied with) the signal to despread and remove the coding from the desired transmitted signal, and to return it to the basic data rate. Where the digital code (i.e., PN code, orthogonal code, or Walsh code) is applied to other transmitted and received signals, there is no despreading as the signals maintain their chip rate.

This despreading operation effectively comprises a correlation process comparing the received signal with the appropriate digital code. In accordance with QPSK, the transmitted data sequences or chips include an in-phase component (I) and a quadrature phase component (Q), which are the real and imaginary parts of a complex signal. The despreading operation performed by receiver 20 correlates the I and Q components of the received complex signal to the appropriate digital code or signature sequence. This is accomplished using a single correlation filter design (e.g., CF 3) for all data rates in the channels of the wireless system.

In a preferred embodiment of the invention, the exemplary wireless system provides an access channel 11, a maintenance channel 12, and a traffic channel 13 in the reverse link. The correlation filter CF 3 is DSP programmable (*i.e.*, controlled by DSP 4) and can be configured to perform the digital signal processing needed in receiving data from any of the three channels 11, 12 and 13 and at all user data rates. After processing in the correlation filter CF 3 and digital signal processor 4, the original data from the transmitter 10, is recovered. The system and the various embodiments according to the invention are described in further detail below.

Figure 2 illustrates the structure of a frame of data/pilot symbols being

transmitted in the access, maintenance and traffic channels in an embodiment according to the invention. In this particular embodiment, the access channel (e.g., access channel 11 of Figure 1) is used by the receiver 20 to communicate with the transmitter 10 when no traffic channel is assigned. The access channel provides a user with a shared data channel for requesting access to the CDMA system. The maintenance channel (e.g., maintenance channel 12 of Figure 1) maintains the timing of the transmitter and the receiver in the reverse link using a plurality of pilot symbols. No data symbols are transmitted in the maintenance channel. The maintenance channel provides a user with the ability to maintain synchronization with the CDMA system during periods of inactivity. User data and signaling messages (*i.e.*, pilot symbols) from the transmitter are transmitted to the receiver Rx 2 in the traffic channel (e.g., traffic channel 13 of Figure 1).

The wireless system according to the invention provides three tiers of data rates, *i.e.*, tier 1 (which is the basic despreading rate), tier 2 and tier 3, for use by the channels (access channel 11, maintenance channel 12, and traffic channel 13). At tier 1, the transmitter transmits 8 chips per symbol to the receiver. At tier 2, the transmitter transmits 32 chips per symbol to the receiver in the reverse link. At tier 3, the transmitter transmits 128 chips per symbol in the reverse link of the exemplary wireless system according to the invention. Transmitting data in the access, maintenance and traffic channels is described in further detail below.

When transmitting a frame of data and/or pilot symbols in the reverse link using the access channel, the frame comprises a preamble, succeeded by data, another preamble, and data (Figure 2). The frame is modulated using QPSK (quadrature phase shift keying), which is known in the art, and channelized (spread) using a unique digital code, such as a pseudorandom noise (PN) code, also known in the art.

When transmitting the modulated frame in the access channel, three access modes of operation for the access channel are provided, namely, the preamble mode, the pilot mode, and the data mode. A PN epoch marks the end of one frame and the beginning of another frame. A preamble of a frame in the access channel comprises a plurality of pilot symbols transmitted at the tier 2 rate (*i.e.*, 32 chips per symbol in the frame). In the preamble mode, pilot symbols only and no data symbols are transmitted.

Data, which succeed the preamble in the frame being transmitted in the access channel, comprise a plurality of data symbols and pilot symbols interleaved at the tier 2 rate (*i.e.*, 32 chips per symbol). A mode controller in DSP 4 controls the mode of operation of the access channel and switches between the preamble, pilot and data modes.

When transmitting a frame in the maintenance channel, the frame includes information for multiple users denoted P1, P2, P3, ..., P128, and no data which is time division multiplexed (TDM) with two pilot symbols per user. The data rate is Tier 3 with 128 chips per symbol (Figure 2). Only one mode of operation is provided in the maintenance channel, namely, the pilot mode.

When transmitting a frame in the reverse link of the traffic channel, two transmission modes are provided, namely, the pilot mode and the data mode. A frame comprises pilot and data symbols, where the pilot symbols are placed at periodic intervals between the data symbols. The data and pilot symbols may be transmitted at any data rate; transmission at tier 1 rate (*i.e.*, 8 chips per symbol), tier 2 rate (32 chips per symbol) and tier 3 (128 chips per symbol). The data symbols are transmitted at the same rate as that of the pilot symbols. Similarly, a mode controller in DSP 4 controls the mode of operation of the traffic channel and switches between the pilot mode and the data mode.

Figure 3 is a diagram illustrating a receiver with field programmable gate array (FPGA 5) and controlled by a digital signal processor (DSP) 4 according to the invention. The FPGA 5 comprises an FPGA pilot post processor 33, an FPGA data post processor 35, pseudorandom noise (PN) code generator 46, and a correlation filter CF 3 having a CF core 31. The field programmable gate array FPGA 5 with the correlation filter CF 3, and the digital signal processor DSP 4 are included in the receiver 20 to recover the original data transmitted by the transmitter 10. The CF core 31 is used for despreading received data in the three channels (access, maintenance and traffic) 11, 12 and 13. The digital signal processor DSP 4 is used to control and post-process the outputs of the field programmable gate array FPGA 5.

DSP 4 includes a mode controller 41 which indicates the channel selection (from the access, maintenance and traffic channels) for transmitting data and/or pilot symbols. DSP 4 also includes a pilot DSP post processor 34 and a DSP data post processor 36 which provide pilot symbol-aided QPSK demodulation of the multipaths

received at the receiver 20. Pilot symbol aided demodulation is described in the copending U.S. Patent Application Serial No. 09/497,440 entitled PILOT SYMBOL ASSISTED MODULATION AND DEMODULATION IN WIRELESS COMMUNICATION SYSTEMS, which is incorporated herein by reference.

Figure 4 is a diagram that illustrates an exemplary field programmable gate array (FPGA) 5 with a correlation filter (CF) core 31 for all channels in the wireless system according to the invention. The CF core according to the invention performs 8-chip complex correlation with 64 correlation lags, while allowing no data loss as the 64 correlation lags are being processed. A correlation lag is a time instant for which the PN code (or orthogonal code, Walsh code) is held constant, so that the received data in the receiver 20 is correlated based on the PN code (or orthogonal code, Walsh code) and corresponding outputs therefor are generated. Correlation lags are computed independent of the channel type and data rate. This is advantageously achieved with a single time-multiplexed 8-chip correlator engine (i.e., CF core 31) which allows multiple 8-chip correlations to be performed with the same correlation engine. Furthermore, the invention advantageously provides the ability to generate integer multiples of the 8-chip correlation (e.g., 32 or 128 chips) for larger correlation lengths. The operation of the CF core according to the invention is described in further detail below.

As seen in Figure 4, the field programmable gate array 5 includes a correlation filter CF 3 with a CF core 31, a PN (pseudorandom noise) code generator 46 with correlator pattern buffers 401 through 408, a multiplexer (MUX) 44, a window processor 43, a demultiplexer (DEMUX) 45, and symbol processors 411 through 418. CF core 31 (which is explained in more detail with reference to Figure 5) is a correlation engine which is a single 8-chip correlation module that provides despreading for all channels (*i.e.*, access, maintenance and traffic channels 11, 12 and 13). CF core 31 is the basic correlation engine which can be used to obtain any x-chip correlation, x being the factor of 8, of the QPSK-modulated frame of data and/or pilot symbols received from the transmitter 10.

PN code generator 46 in the receiver 20 (Rx 2) generates the local PN reference of the PN code (or orthogonal code, Walsh code) used by the transmitter 10 (Tx 1). PN code generator 46 is DSP programmable and controlled by DSP 4 (Figure 3) to

generate the proper PN code phase. The PN code (or orthogonal code, Walsh code) phase used by each user is established during transmitter-receiver connection setup and remains fixed for the duration of that user's call, i.e., during that connection time to the wireless system.

The PN code phases from the PN code generator 46 are applied to respective correlator patterns 401 through 408. The outputs or the correlator patterns are selectively e.g., sequentially, processed in CF core 31 via the MUX 44. The length of each correlator pattern is 8 chips. In particular, the MUX 44 loads 8 chips of PN reference data of the PN code (or orthogonal code, Walsh code) from one of the correlator patterns into a buffer so that the PN reference can be used by the time multiplexed CF core 31 at the proper time. The 8 chips of the PN code (from respective correlator patterns 401 through 408) are held in the buffer for a period of 64 chips and are used to despread the received data from the transmitter 10. CF core 31 generates a correlation value for each shift of the received waveform from MUX 44 as it passes the PN reference. The time multiplexed CF core 31 allows the generation of multiple correlation lags with a single correlation engine.

Assuming that the modulated frame received from the transmitter 10 is oversampled four times the normal sampling rate set for the system, 256 correlation lags are provided in the 64-chip period. Furthermore, time multiplexing allows a single 8-chip correlator engine (e.g., CF core 31) to provide multiple correlation lags with no loss of data. This process is repeated for the next 8 chips of the PN code (or orthogonal code, Walsh code).

The correlation core 31 performs a complex correlation. That is, each of the CF core 31 outputs one of four real correlation values. The correlation values are the results of an 8-chip complex correlation which is broken into four real 8-chip correlations in the correlation engine. The result of the four real correlations represents four real multiplications in a complex multiplication, as follows:

$$(a+jb)*(c+jd) = ac - bd + jbc + jad \qquad \text{(Eq. 1)}$$

where ac = II, bd = QQ, bc = QI and ad = IQ.

The 8-chip complex correlation corresponds to the smallest despreading factor used in the wireless system according to the invention, which is 8 chips for a tier

1 rate (the basic despreading rate). All other data rates in the wireless system are multiples of 8 and can therefore be generated by summing multiple 8-chip correlation outputs. If the number of correlation lags is to be greater than 8 chips (i.e., the PN code (or orthogonal code, Walsh code) is being held constant for more than 8 chips), the next 8-chip time period will have passed and the correlation on the following data will not be properly calculated. As a result, more than one pattern is needed and the number of correlators will be a function of the number of correlation lags needed.

Figure 5 is a timing diagram illustrating an exemplary time multiplexed, 8-chip complex correlation with a pseudorandom noise (PN) code according to the invention. Since the number of correlation lags in the wireless system according to the invention is established at 64 chips, there is provided a methodology for performing correlations in parallel with time shifting to properly correlate the next 56 chips. As a result, 8-chip time multiplexed correlations are staggered in time by 8 chips. That is, for every 8 chips a new correlation begins while the preceding correlation is still being performed. Therefore, if the correlation output of the 8-chip complex correlation in CF core 31 is to have 64 correlation lags, eight different 8-chip correlator patterns (e.g., 401 through 408 of Figure 4) are processed, each spaced by 8 chips so that no data is missed, as shown in Figure 5. Each of the eight phases of the correlator pattern (e.g., Corr Phase 1 through 8) is shifted by 8 chips, which is shown by the load notation of LD in Figure 5. Once the 8 chips of the PN code (e.g., from PN code generator 46) have been loaded, each phase of the correlator pattern produces 64 chips of correlation lag for that set of 8 PN chips in a store operation denoted ST in Figure 5. To avoid missing the next 56 chips of data, seven other phases of the correlator pattern are set up with the next 56 chips of the PN code and 64 chips of correlation lag calculated for the 8 chips of the PN code. During each correlator phase (e.g., Corr Phase 1 through 8), CF core 31 generates correlation lags for a tier 1 symbol. Each phase of the 64 correlation lags of valid data is shifted in time, as noted in Figure 5, e.g., Phase 1 Data Potentially Valid, Phase 2 Data Potentially Valid. The 8-chip time multiplexed correlation engine (e.g., CF core 31) produces the 4 real components of a complex correlation for a tier 1 symbol, each having 64 chips of correlation lag. The time multiplexing cycle for CF core 31 is 8 symbols in length, where 8 symbols of tier 1 data are produced per cycle.

The window processor 43 of Figure 4, the demultiplexer (DEMUX) 45, and the symbol processors 411 through 418 together demodulate the received data from the transmitter 10 using QPSK demodulation. An exemplary QPSK demodulation is described herein and in the copending U.S. Patent Application Serial No. 09/497,440 filed on February 3, 2000 and entitled PILOT SYMBOL ASSISTED MODULATION AND DEMODULATION IN WIRELESS COMMUNICATION SYSTEMS. The window processor 43, performs a phase de-rotation of the received signal with a channel estimate from the pilot post-processing (Figure 3). In particular, the window processor 43 performs complex multiplication of the correlation values corresponding to each tier 1 symbol from the CF core, and outputs the pilot post processor signal which estimates the channel.

The DEMUX 45 takes the output of the time multiplexed CF core 31 and window processor 43 and produces 64 chips of correlation lag for each tier 1 symbol and routes them to their corresponding symbol processors (411 through 418). There are eight symbol processors (411 through 418), one for each tier 1 symbol that is produced by CF core 31 during the eight phases of the 8-chip complex correlation. The symbol processors (411 through 418) are programmed by DSP 4 to select the proper multipaths from the output of the window processor 43. The symbol processors take the DSP programmable number of correlation lags associated with up to three multipaths, and sum the correlation lags to form three outputs (Figures 3 and 4). The outputs from the symbol processors are always at the tier 1 rate (the basic despreading rate) from which the DSP 4 can accumulate the outputs to achieve the tier 2 and tier 3 rates. In addition, for the tier 2 rate (32 chips), four outputs from the symbol processors at the tier 1 rate (which is the basic despreading rate) are summed. For the tier 3 rate (128 chips), sixteen outputs from the symbol processors at the tier 1 rate are summed.

Figure 6 is a diagram illustrating the pilot post processing of any channel of the wireless system according to the invention, namely the access channel, traffic channel and maintenance channel. In each of the three channel types, a portion of the information being transmitted includes pilot symbols. A pilot symbol is a known constant value which the receiver 20 uses to estimate the channel conditions for each received multipath. As the mode controller 41 of DSP 4 (Figure 3) indicates pilot

processing in the access, traffic or maintenance channel, pilot post processor 33 in FPGA 5 of the receiver 20 (Rx 2) starts the processing of the pilot symbols transmitted in the channel. Two accumulating filtering random access memories (AFRAM) 61 and 63 (shown in Figure 6) having a one-pole infinite impulse response (IIR) filter are provided in pilot post processing 33 for integration of the pilot symbols being transmitted in the channel. Based on the pilot symbols and the IIR filtering thereof, an estimate of the channel is obtained for completing pilot symbol aided QPSK demodulation. Each AFRAM contains 64 correlation lags of IIR-filtered pilot symbols at 4 samples/chip. This allows receiver 20 to have 64 chips of delay-spread range for searching the received multipaths at a resolution of ¼ of a chip time.

AFRAM 61 (and similarly, AFRAM 63) can act as a one-pole IIR filter with coefficients α and β. An IIR filter, known in the art, is a digital filter that linearly processes sampled data in a recursive manner. That is, an IIR filter samples continuous-time data signals with a fixed periodicity and linearly manipulates and transforms the samples. The one-pole IIR filter has two coefficients, α and β, which controls the function of the AFRAM. The coefficients (α and β) are DSP programmable and controlled by DSP 4. Based on the selection of coefficients, the AFRAM (61 or 63) can serve three functions, namely storage (or more particularly, random access memory or RAM), accumulation, and filtering. As a RAM, the AFRAM stores 256 correlation lags of data for a tier 1 pilot symbol. As an accumulator, the AFRAM accumulates correlation data over multiple tier 1 pilot symbols to generate tier 2 or tier 3 data. As a filter, the AFRAM is a one-pole IIR filter that filters data at the tier 1, 2 or 3 data rates for pilot symbol estimation in the presence of noise and interference in the channel. When the β coefficient of the IIR filter equals zero, there is no recursive feedback in the IIR filter, *i.e.*, no filtering, and AFRAM 61 (and similarly AFRAM 63) acts as a sample RAM (Figure 6) for storing the inputs from summer 621 (or summer 623 for AFRAM 63). If the β coefficient equals one, AFRAM 61 (and similarly AFRAM 63) acts as a simple accumulator for accumulating the inputs from summer 621 (or summer 623 for AFRAM 63). If the β coefficient is between zero and one, then AFRAM 61 (and similarly AFRAM 63) acts as a filter. In effect, by controlling the coefficients (e.g., through DSP 4) the AFRAM 61 (and similarly AFRAM 63) can act as a simple RAM for storing data,

an accumulator for accumulating data inputs, or a filter for filtering data signals. This allows the system to process data inputs at any of the tier 1, tier 2 and tier 3 rates, and to integrate the pilot symbols over a time period specified by DSP 4, *i.e.*, multiple-tier pilot symbols at tier 1, tier 2 or tier 3.

Figure 6 also contains a MAFRAM 65, which is a magnitude accumulating filtering random access memory (MAFRAM 65). MAFRAM 65 also includes a one-pole IIR filter containing 64 correlation lags of IIR-filtered pilot symbols. Similar to AFRAM 61 and AFRAM 63, MAFRAM 65 has coefficients α and β and functions as a memory, accumulator and filter. The coefficient are DSP programmable and controlled by DSP 4. MAFRAM 65 serves the three functions similar to the AFRAM (61 or 63) but on the magnitude squared data from the AFRAM. As a RAM, MAFRAM 65 stores 256 correlation lags of data for 1 pilot symbol.

As an example in Figure 6, in the maintenance channel the pilot symbols are transmitted at the tier 3 rate only. The TDM maintenance channel comprises two pilot symbols, with 128 chips per symbol. The four real correlation outputs, the in-phase and quadrature phase components (I and Q) of the each user's two pilot symbols are stored, accumulated and filtered by AFRAM 61 and AFRAM 63, respectively. The four real correlation outputs are denoted IrxIref, QrxIref, IrxQref and QrxQref. AFRAM 61 and AFRAM 63 respectively process the two I and Q of two symbols (with 128 chips per symbol) at the tier 3 rate. In particular, since the pilot symbols are transmitted in the maintenance channel at a rate larger than the tier 1 rate (which is the basic despreading rate), AFRAM 61 (and similarly AFRAM 63) accumulates the pilot symbols with filtering. The accumulation is performed by setting the β coefficient of AFRAM 61 (and similarly AFRAM 63) to one. The filtering is accomplished by setting the α and β coefficient of AFRAM 61 (and similarly AFRAM 63) to a value between zero and one. Once the frame is processed, AFRAM 61 (and similarly AFRAM 63) overwrites the old data and stores/accumulates the pilot symbols of the next user being transmitted in the maintenance channel.

After processing in AFRAM 61 and 63, the filtered I and Q (denoted Pcos and Psin, respectively) are squared at squarers 625 and 627, respectively. The squared AFRAM-filtered I and Q components are summed at summer 629, and forwarded to

MAFRAM 65 whose output is the post processing signal.

Figure 6A illustrates the α and β coefficient settings of MAFRAM 65, AFRAM 61 and 63 for the tier 1, 2 and 3 data rates. The pilot symbols (denoted P in the Data Type row) are shown alongside the data symbols (denoted D) with corresponding AFRAM and MAFRAM coefficient settings. The α and β coefficient settings illustratively demonstrate the use of the AFRAMs as a RAM, accumulator and filter, and the MAFRAM as a RAM only.

Figure 6B is a lower level diagram illustrating an embodiment of the AFRAM or MAFRAM according to the invention, e.g., AFRAM 61, 63 or MAFRAM 65 of Figure 6, which is a basic IIR filter. Information is input into a multiplier 631 where it is multiplied with the α coefficient. RAM 635 is a random access memory that stores 256 elements of information. The stored information from RAM 635 is multiplied with the β coefficient at a multiplier 637. The data multiplied with the gain coefficients α and β are summed at summer 633 and then forwarded to RAM 635 for storage and output.

Referring back to Figure 6, AFRAM 61, AFRAM 63, MAFRAM 65, together with the time-multiplexed correlation engine (e.g., CF core 31), provide the ability to search for pilot symbols over a 64-chip window. The pilot symbol search is a DSP programmable process for searching the one or more signal components (in terms of the received power, signal-to-noise ratio or the multipath width) in the received multipath power profile stored in the MAFRAM. The searching can also be implemented according to a preprogrammed time alignment. The AFRAM-filtered I and Q values are squared and summed for multipath search processing 67 for selecting one or more signal components (in terms of the received power, signal-to-noise ratio or multipath width), as described herein and in Figures 7 and 7A. The selecting step can also be implemented according to a preprogrammed time alignment. Pilot post processor 34 of DSP 4 determines which multipaths are useful for maximum ratio combining to achieve diversity, which is described in further detail below. DSP 4 then forwards the best multipaths to the symbol processors 411 through 418 (Figure 4) in data post processing circuit 35 (Figure 3) for pilot symbol aided QPSK demodulation and recovery of the data symbols.

Figure 7 is a diagram illustrating the search processing of the multipath power profile according to the invention. Three peaks 1, 2 and 3 are selected from the 64-chip search window for demodulation. The one or more signal components (in terms of the received power, signal-to-noise ratio or the multipath width) are selected by processing a succession of passes through the MAFRAM data. The selecting step can also be implemented according to a preprogrammed time alignment. The selection process allows DSP 4 to identify the multipath responses for use in demodulation and recovery of the data symbols. In such a selection process, the strongest peak (or most desired signal component) in the multipath response of the demodulated waveform for the data received from the transmitter is selected and a window (in terms of time or a time period) is assigned thereto. The multipath response is examined again, barring the window for the strongest peak (peak 1 (or most desired signal component)), and the second strongest peak (or second most desired signal component) is selected and a window is assigned thereto. The multipath response is examined once more, barring the windows for the strongest peak (peak 1 (or most desired signal component)) and the second strongest peak (peak 2 (or second most desired signal component)), and the third strongest peak (peak 3 (or third most desired signal component)) is selected and a window is assigned thereto. The same process steps can be repeated until the Nth most desired signal component is selected. Upon completion of the selection process, the three peaks 1, 2, 3 (and/or through N) are supplied to digital signal processing DSP 4.

Figure 7A is a flow diagram illustrating an embodiment the multipath search processing of the multipath response peaks according to the invention. The summed squares of AFRAM-filtered I and Q are stored in MAFRAM 65 (Figure 6). The information stored in MAFRAM 65 is used for the multipath search processing in a 64-chip window as shown in Figure 7. In step 71 of Figure 7A, the strongest peak (or most desired signal component) in terms of the received power of the multipath response is stored as index 1 and its magnitude stored as max_power 1. In step 72, a blank-out region 1 is set. The blank-out region is ignored for the next examination of the multipath response. In particular, the blank-out region is defined by a lower limit 1 and an upper limit 1, as follows:

$$\text{lower limit 1} = \text{index 1} - \text{window} \qquad \text{(Eq. 2)}$$

upper limit 1 = index 1 + window (Eq. 3)

where window denotes the length of the multipath response which should not be searched on the next pass. In step 73, the strongest peak (or most desired signal component) in the multipath response is selected by examining the multipath response, while ignoring the blank-out region 1. In effect, the second strongest peak (or second most desired signal component) in the entire multipath response is selected, which is stored as index 2 and its magnitude stored as max_power 2. In step 74, another blank-out region 2 is set with a lower limit 2 and an upper limit 2, as follows:

lower limit 2 = index 2 - window (Eq. 4)

upper limit 2 = index 2 + window (Eq. 5)

In step 75, the strongest peak (or most desired signal component) in terms of the received power (or signal-to-noise ratio, multipath width) in the multipath response is selected by examining the multipath response while ignoring the blank-out regions 1 and 2. The selecting step can also be implemented according to a preprogrammed time alignment. In effect, the third strongest peak (or third most desired signal component) in the entire multipath response is selected, which is stored as index 3 and its magnitude is stored as max_power 3. In step 76, an additional blank-out region 3 is set with a lower limit 3 and an upper limit 3, as follows:

lower limit 3 = index 3 - window (Eq. 6)

upper limit 3 = index 3 + window (Eq. 7)

In step 77, the noise power of the multipath response is stored. The noise power is the sum of all the remaining power in the multipath response. In particular, the nosie power is obtained by summing all power elements of the multipath response in the window, while ignoring blank-out regions 1, 2 and 3. The noise power is then reported to DSP 4.

The strongest peaks (or most desired signal component) in terms of the received power (or signal-to-noise ratio, multipath width) in the multipath response and the noise power information in MAFRAM 65 are available to DSP 4 after each pilot symbol is processed. With such information, pilot post processor 34 of DSP 4 determines which multipaths are useful for maximum ratio combining to achieve diversity, which is described in further detail below. DSP 4 then forwards the best

multipaths to the symbol processors 411 through 418 (Figure 4) in data post processor 35 (Figure 3) for pilot symbol aided QPSK demodulation and recovery of the data symbols.

Figure 8 is a diagram illustrating the data post processing in the channels of the wireless system according to the invention and, more particularly, the data post processing in the access channel and the traffic channel. In the data mode of the access channel or the traffic channel, data symbols are then processed at the tier 1 data rate which is the basic despreading rate. The basic despreading rate can be 4 or 8 chips per symbol. No data symbols are transmitted in the maintenance channel.

As the mode controller 41 of DSP 4 (Figure 3) indicates the data mode in the access channel, data symbols are processed at the tier 1 rate. The four PN referenced correlation values, namely IrxIref, QrxIref, QrxQref and IrxQref are respectively input into window processor 43 (Figure 8 and Figure 4) comprising multipliers 811, 812, 813 and 814. Window processor 43 performs a complex de-rotation or multiplication of the received correlation values IrxIref, QrxIref, QrxQref and IrxQref with pilot symbol estimates from AFRAM 61, 63, and pilot post processor 33. IrxIref and QrxQref are multiplied with the AFRAM-filtered in-phase component I (e.g., output Pcos 81 from AFRAM 61) and QrxIref and IrxQref are multiplied with the AFRAM-filtered quadrature phase component Q (e.g., output Psin 83 from AFRAM 63). After de-rotation or multiplication of the components, the results are input at window select units 801, 802, 803 and 804, respectively, for the multipath selection based on the pilot search processing in a 64-chip window as described herein and in Figures 7 and 7A. This pilot symbol aided demodulation process produces QPSK outputs which are rotated to a QPSK signal constellation. The gate array with the window processor receives the output of the correlation filter core and produces a phase-compensated output using a complex multiplier for all correlation lags for each 8-chip symbol.

Due to the time multiplexed structure of the correlation core, the 64 chips of correlation values associated with each tier 1 data symbol are not in the proper order and require time demultiplexing to yield appropriately ordered data symbols. Upon completion of the window selection at circuits 801, 802, 803 and 804, the four real correlations are combined into I and Q at summers 821 and 823 and demultiplexed at

DEMUX 45.

After demultiplexing, DEMUX 45 outputs the 64 chips of correlation lag for each tier 1 data symbol to the corresponding symbol processors in circuits 831 and 833. There are eight symbol processors (411 through 418 in circuits 831, 833), one for each tier 1 data symbol produced by CF core 31 during the eight phases of the 8-chip correlation process, described herein and in Figures 4 and 5. The symbol processors (411 through 418) of one unit 833 take the DSP programmable number of correlation lags associated with up to three multipaths and sum the correlation lags to form three outputs. The low index (lower limits 1, 2 and/or 3) and high index (upper limits 1, 2 and/or 3) for all three multipaths determine which correlation lags are used in forming the three outputs. DSP 4 performs further integration of the tier 1 data symbols to provide tier 2 and tier 3 data symbols. This is accomplished by summing four tier 1 data symbols to yield one tier 2 data symbol, and summing sixteen tier 1 data symbols to yield one tier 3 data symbol. DSP 4 then uses the three outputs for combining into a single output for signal diversity.

Referring again to Figure 8, DSP 4 further provides post processing of the data symbols (in data post processor 36) for normalizing the outputs of the symbol processors by taking the square root of the absolute value to yield voltage signals. This normalization is needed because complex de-rotation or multiplication has been performed based on the received power (or signal-to-noise ratio, multipath width) of the pilot symbols in units of signal power. In order to produce proper diversity combining according to maximum ratio combining (MRC) of the three outputs, normalization is required for yielding voltage signals. The absolute values (representing the magnitudes of the received power) are taken at circuits 841 and 843. Then the square root of the signals from absolute value circuits 841, 843 are generated in square root circuits steps 851 and 853. Next, output of the square root circuits 851, 853 is scaled at divider 861 and divider 863, respectively. Using MRC as described herein, the three outputs are then combined in summing circuits 871 and 873 to obtain one output for each of the I and Q components.

Another type of diversity is spatial diversity, where multiple antenna are provided in the transmitter or receiver for transmitting the same data signals which

provide the diversity needed for combining or selecting the data signals. Spatial diversity is achieved by providing the same correlation filter design according to the invention in each antenna receiver in the wireless system.

Figure 9 is a flow diagram that illustrates an embodiment of the method according to the invention. This method is carried out in a wireless CDMA system using a single, common correlation filter (CF). The system has a plurality of channels with different data rates and they include the access channel, the maintenance channel, and the traffic channel in which information (e.g., pilot or data symbols or both) is transmitted at the tier 1, tier 2 and tier 3 rates, as described herein in conjunction with Figure 2. The data rate for transmitting the information is programmable by digital signal processing (DSP). To begin the method a user-unique code, such as a PN code (or orthogonal code, Walsh code), is applied to the information being transmitted in the channels of the wireless system (step 93). In step 94, the information is QPSK modulated and transmitted in any one of the channels. The transmitted information is correlated at the basic despreading rate (i.e., the tier 1 rate) using time multiplexing in the correlation filter (CF) of the wireless system (step 95). The basic despreading rate can be 4 or 8 chips per symbol. The correlated information is then demultiplexed (step 96) and QPSK-demodulated (step 97). The demodulated information is summed (step 98) at the proper integer multiple of the tier 1 rate to achieve the tier 2 and tier 3 rates, as described herein in conjunction with Figure 4. The one or more signal components (in terms of the received power, signal-to-noise ratio or the multipath width) of the multipath response of the information are selected in a window or time period for optimal information recovery, as described herein in conjunction with Figures 7 and 7A. The selecting step can also be implemented according to a preprogrammed time alignment. Furthermore, in step 99 three outputs from the demodulated information can be provided and combined for temporal diversity, as described herein in conjunction with Figure 8. All the process steps according to the invention described herein are advantageously accomplished using a single, common correlation filter (CF) which eliminates the need for additional correlators or correlation filters for processing received information having multiple data rates.

Although the invention has been particularly shown and described in detail

with reference to the preferred embodiments thereof, the embodiments are not intended to be exhaustive or to limit the invention to the precise forms disclosed herein. It will be understood by those skilled in the art that many modifications in form and detail may be made without departing from the spirit and scope of the invention. Similarly, any process steps described herein may be interchangeable with other steps to achieve substantially the same result. All such modifications are intended to be encompassed within the scope of the invention, which is defined by the following claims and their equivalents.

WE CLAIM:

1. In a code division multiple access (CDMA) communications system having a plurality of channels with different data rates, a method comprising the steps of:

applying a user-unique code to information being transmitted in the channels;

modulating the information;

correlating the transmitted information at a basic despreading rate using time multiplexing in a single correlation filter;

demultiplexing the correlated information;

demodulating the correlated information; and

summing the demodulated information at a rate greater than or equal to the basic despreading rate to obtain information at other data rates of the different data rates.

2. The method of claim 1 wherein the user-unique code is pseudorandom noise (PN) code.

3. The method of claim 1 wherein the user-unique code is orthogonal code.

4. The method of claim 1 wherein the user-unique code is Walsh code.

5. The method of claim 1 wherein the modulating and demodulating steps are performed using QPSK (quadrature phase shift keying).

6. The method of claim 1 wherein the information in any one of the channels consists of pilot symbols and data symbols interleaved in a specified and known order.

7. The method of claim 1 further comprising the step of:

after the summing step, selecting one or more signal components in terms of received power based on a channel estimate from pilot symbols inserted into a waveform of the transmitted information.

8. The method of claim 1 further comprising the step of:

after the summing step, selecting one or more signal components in terms of signal-to-noise ratio based on a channel estimate from pilot symbols inserted into a waveform of the transmitted information.

9. The method of claim 1 further comprising the step of:

after the summing step, selecting one or more signal components in terms of multipath width based on a channel estimate from pilot symbols inserted into a waveform of the transmitted information.

10. The method of claim 1 further comprising the step of:

after the summing step, selecting one or more signal components according to a preprogrammed time alignment.

11. The method of claim 1 in which temporal diversity is provided by causing the demodulated step to provide two or more outputs of demodulated information and combining the outputs into one output.

12. The method of claim 11 wherein the outputs are combined into one output using maximum ratio combining (MRC).

13. The method of claim 1 wherein the channels comprise of an access channel, a maintenance channel, and a traffic channel.

14. The method of claim 1 wherein the basic despreading rate is 8 chips per symbol.

15. The method of claim 1 wherein the basic despreading rate is 4 chips per symbol.

16. The method of claim 1 wherein any one of the steps of the applying, correlating, demodulating and summing steps is programmable by an external programmable processor.

17. The method of claim 1 wherein any one of the steps of the applying, modulating, transmitting, correlating, demodulating and summing steps is performed in a traffic channel.

18. The method of claim 1 wherein any one of the steps of the applying, modulating, transmitting, correlating, demodulating and summing steps is performed in an access channel.

19. The method of claim 1 wherein any one of the steps of the applying, modulating, transmitting, correlating, demodulating and summing steps is performed in a maintenance channel.

20. The method of claim 1 in which spatial diversity is provided by providing multiple antennas, multiple receivers at a location and providing the same, single correlation filter at each of the plurality of receivers of the system.

21. The method of claim 1 further comprising the steps of:

(a) after the summing step, selecting a most desired signal component in terms of received power of a multipath response in a time period;

(b) storing a magnitude of the most desired signal component;

(c) setting a first blank-out region of the most desired signal component defined by a first upper limit and a first lower limit;

(d) selecting a second most desired signal component of the multipath

response in the time period by ignoring the first blank-out region;

(e) setting a second blank-out region of the second most desired signal component defined by a second upper limit and a second lower limit; and

repeating steps (a), (b), (c), (d) and (e) until the Nth most desired signal component is selected.

22. The method of claim 21 wherein the selecting in steps (a) and (d) are performed in terms of signal-to-noise ratio based on a channel estimate from pilot symbols inserted into a waveform of the transmitted information.

23. The method of claim 21 wherein the selecting in steps (a) and (d) are performed in terms of multipath width based on a channel estimate from pilot symbols inserted into a waveform of the transmitted information.

24. The method of claim 21 wherein the selecting in steps (a) and (d) are performed according to a preprogrammed time alignment.

25. The method of claim 21 further comprising the steps of:

setting 1 through N blank-out regions respectively defined by 1 through N upper limits and 1 through N lower limits; and

summing all power elements of the multipath response in the time period for noise power estimation, while ignoring all of the blank-out regions.

26. The method of claim 21 wherein the lower and upper limits of each signal component are programmed by an external programmable processor.

27. A code division multiple access (CDMA) communications system having a plurality of channels with different data rates, the system comprising:

a transmitter applying a user-unique code to data and pilot signal information being transmitted in the channels and modulating the information; and

a receiver comprising a gate array and an external programmable

processor,

the gate array further comprising (a) a code generator generating the user unique code, (b) a correlation filter having a single, common correlation filter core operable with all of the channels with different data rates, said correlation filter core correlating the transmitted information at a basic despreading rate, (c) a multiplexer for directing to the correlation filter, on a time multiplexed basis, delayed phase versions of the user-unique code, (d) a gate array data post processor for receiving the output of the correlation filter and demodulating it to recover the transmitted data signals, (e) and a gate array pilot post processor for receiving the output of the correlation filter and processing it to recover pilot signals, and

the external programmable processor further comprising (a) a mode controller connected to the code generator, correlation filter, multiplexer, data post processor and pilot post processor for controlling channel selection in the system, (b) an external programmable data post processor for receiving and processing signals from the gate array data post processor and the external programmable data post processor, and (c) an external programmable pilot post processor for receiving and processing signals from the gate array pilot post processor, said external programmable data and pilot post processors summing the demodulated information at a multiple of the basic despreading rate to obtain information at other data rates of the different data rates.

28. The system of claim 27 wherein the user-unique code is pseudorandom noise (PN) code.

29. The system of claim 27 wherein the user-unique code is an orthogonal code.

30. The system of claim 27 wherein the user-unique code is a Walsh code.

31. The system of claim 27 wherein the information in any one of the

channels consists of pilot symbols and data symbols interleaved in a specified and known order.

32. The system of claim 27 wherein one or more desired signal components in terms of received power are selected at the external programmable processor for data processing.

33. The system of claim 27 wherein temporal diversity is achieved by providing two or more outputs as demodulated information from the correlation filter and combining the outputs into one output in the external programmable data and pilot post processors by use of maximum ratio combining (MRC).

34. The system of claim 27 wherein the channels consist of an access channel, a maintenance channel, and a traffic channel.

35. The system of claim 27 wherein the basic despreading rate is 8 chips per symbol.

36. The system of claim 27 wherein the basic despreading rate is 4 chips per symbol.

37. The system of claim 27 wherein the correlation filter (CF) core is programmable by the mode controller of the external programmable processor.

38. The system of claim 27 wherein the correlation of the transmitted information is programmable by the external programmable processor.

39. The system of claim 27 wherein spatial diversity is achieved by providing multiple antennas, multiple receivers at a location and providing the same, single common correlation filter at each of the plurality of antennas of the receivers in the system.

40. In a code division multiple access (CDMA) communications system having a plurality of channels including an access channel, a maintenance channel and a traffic channel with different data rates, the system comprising:

a transmitter applying a user-unique code to pilot symbol and data symbol information and modulating the information; and

a receiver comprising a gate array and an external programmable processor,

the gate array further comprising (a) a code generator generating the user unique code, (b) a correlation filter having a single, common correlation filter core operable with all of the channels with different data rates, said correlation filter core correlating the information at a basic despreading rate, (c) a multiplexer for directing to the correlation filter, on a time multiplexed basis, delayed phase versions of the user-unique code, (d) a gate array data post processor for receiving the output of the correlation filter and demodulating it to recover the transmitted data signals, (e) and a gate array pilot post processor for receiving the output of the correlation filter and processing it to recover pilot signals, and

the digital signal processor further comprising (a) a mode controller connected to the code generator, correlation filter, multiplexer, data post processor and pilot post processor for controlling channel selection in the system, (b) an external programmable data post processor for receiving and processing signals from the gate array data post processor and the external programmable data post processor, and (c) an external programmable pilot post processor for receiving and processing signals from the gate array pilot post processor, said external programmable data and pilot post processors summing the demodulated information at a multiple of the basic despreading rate to obtain information at other data rates of the different data rates; and wherein

said correlation filter core correlates the pilot and data symbols at the basic despreading rate using time multiplexing in said received signal;

said gate array demodulates and recovers the data symbols according to the correlated pilot symbols; and

said external programmable processor sums the demodulated information at a rate greater than or equal to the basic despreading rate to obtain desired data symbols.

41. The system of claim 40, said gate array further comprising a time multiplexer for directing user unique codes to the correlation filter core and a time demultiplexer for receiving the output of the correlation filter core.

42. The system of claim 40 wherein said correlation filter core is an 8-chip complex correlation engine which produces the basic despreading rate of 8 chips per symbol.

43. The system of claim 40 wherein said correlation filter core is a 4-chip complex correlation engine which produces the basic despreading rate of 4 chips per symbol.

44. The system of claim 43, said gate array further comprising a window processor receiving the output of the correlation filter core and producing a phase-compensated output using a complex multiplier for all correlation lags for each 4-chip symbol.

45. The system of claim 42, said gate array further comprising a window processor receiving the output of the correlation filter core and producing a phase-compensated output using a complex multiplier for all correlation lags for each 8-chip symbol.

46. The system of claim 40 wherein said gate array pilot post processor further comprises two accumulating filter random access memories (AFRAMs) having an infinite impulse response (IIR) filter, the AFRAMs functionally serving as memory, accumulator and filter and wherein the filter coefficients of the AFRAMs are programmable by the external programmable processor.

47. The system of claim 40 wherein said gate array pilot post processor further comprises a magnitude accumulating filter random access memory (MAFRAM) serving as a memory, accumulator and a filter for magnitude squared data from the accumulating filter random access memories (AFRAMs), and wherein the IIR filter coefficients of the MAFRAM are programmable by the external programmable processor.

48. The system of claim 40, said gate array pilot post processing further comprising multipath search processing which is programmable by the external programmable processor, wherein the multipath search process searches for the one or more signal components in terms of received power in a time period.

49. The system of claim 40, said gate array pilot post processing further comprising multipath search processing which is programmable by the external programmable processor, wherein the multipath search process searches for the one or more signal components in terms of signal-to-noise ratio in a time period.

50. The system of claim 40, said gate array pilot post processing further comprising multipath search processing which is programmable by the external programmable processor, wherein the multipath search process searches for the one or more signal components in terms of multipath width in a time period.

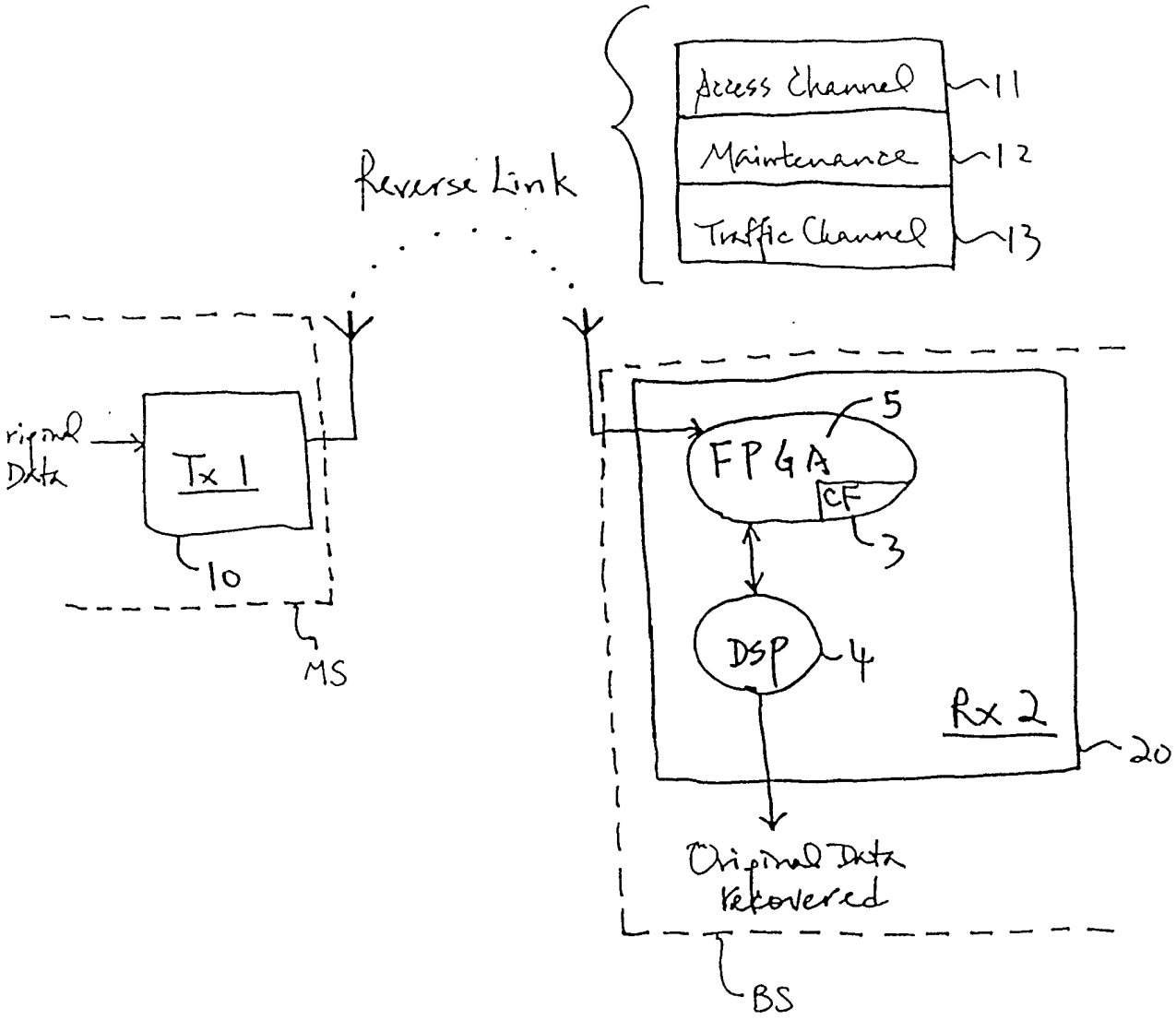
51. The system of claim 40, said gate array pilot post processing further comprising multipath search processing which is programmable by the external programmable processor, wherein the multipath search process searches for the one or more signal components according to a preprogrammed time alignment.

52. The system of claim 48 wherein said external programmable data post processor uses maximum ratio combining (MRC) to achieve temporal diversity according to the two or more signal components found by the multipath search processing of said gate array.

53. The system of claim 40 wherein spatial diversity is achieved by providing a plurality of antennas, and a plurality of receivers at a location and providing the same, single correlation filter design at each of the plurality of antennas of the receivers of the system.

54. The system of claim 45, said gate array data post processor further comprises symbol processors summing programmable sections of correlation delay and forming two or more outputs, wherein said external programmable processor combines the outputs into one output to achieve temporal diversity.

FIGURE 1


Access Channel
11
Maintenance
12
Traffic Channel
13
Reverse Link
Original Data
Tx 1
10
MS
5
FPGA
CF
3
DSP
4
Rx 2
20
Original Data Recovered
BS

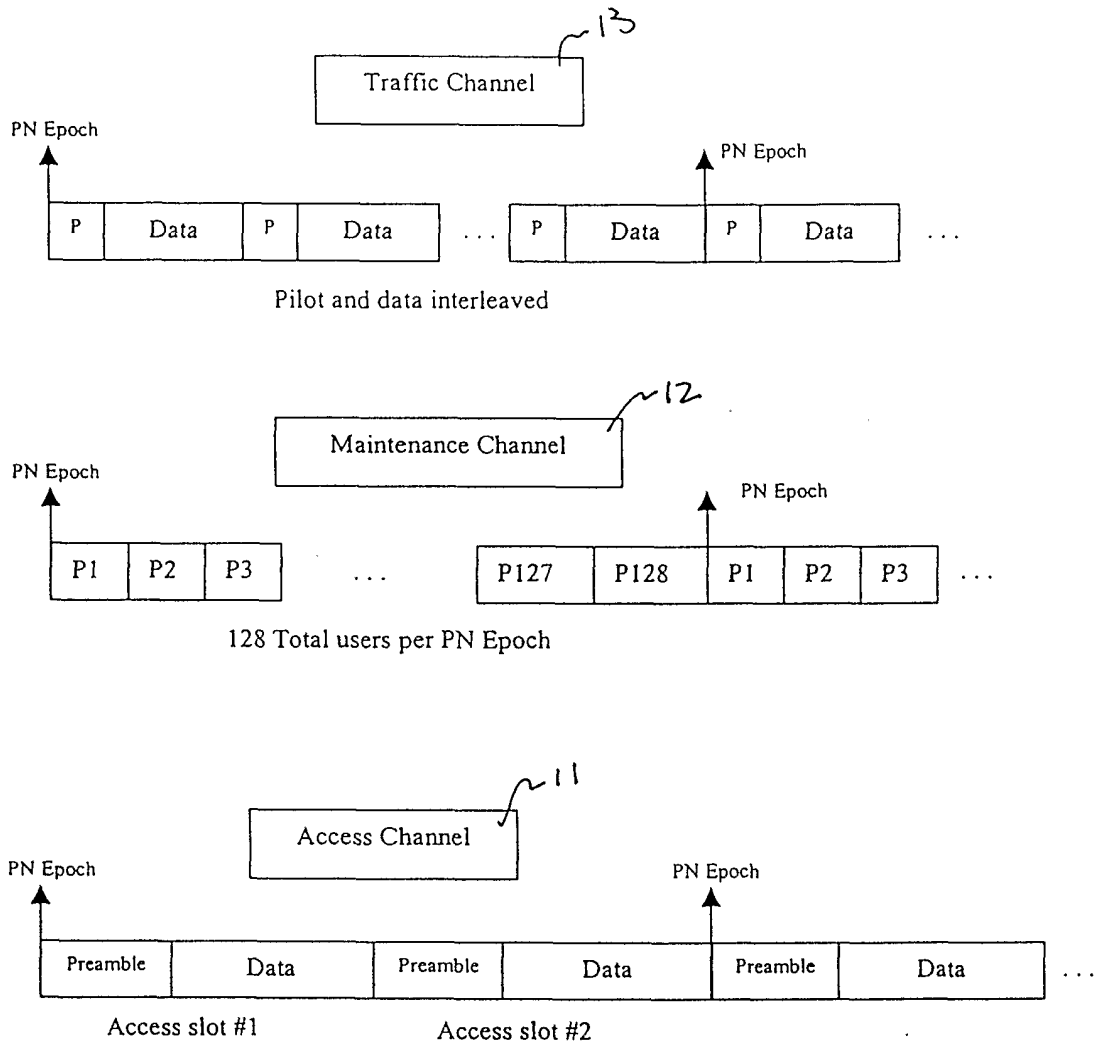

13
Traffic Channel
PN Epoch
PN Epoch
P
Data
P
Data
P
Data
P
Data
Pilot and data interleaved
12
Maintenance Channel
PN Epoch
PN Epoch
P1
P2
P3
P127
P128
P1
P2
P3
128 Total users per PN Epoch
11
Access Channel
PN Epoch
PN Epoch
Preamble
Data
Preamble
Data
Preamble
Data
Access slot #1
Access slot #2

Figure 2

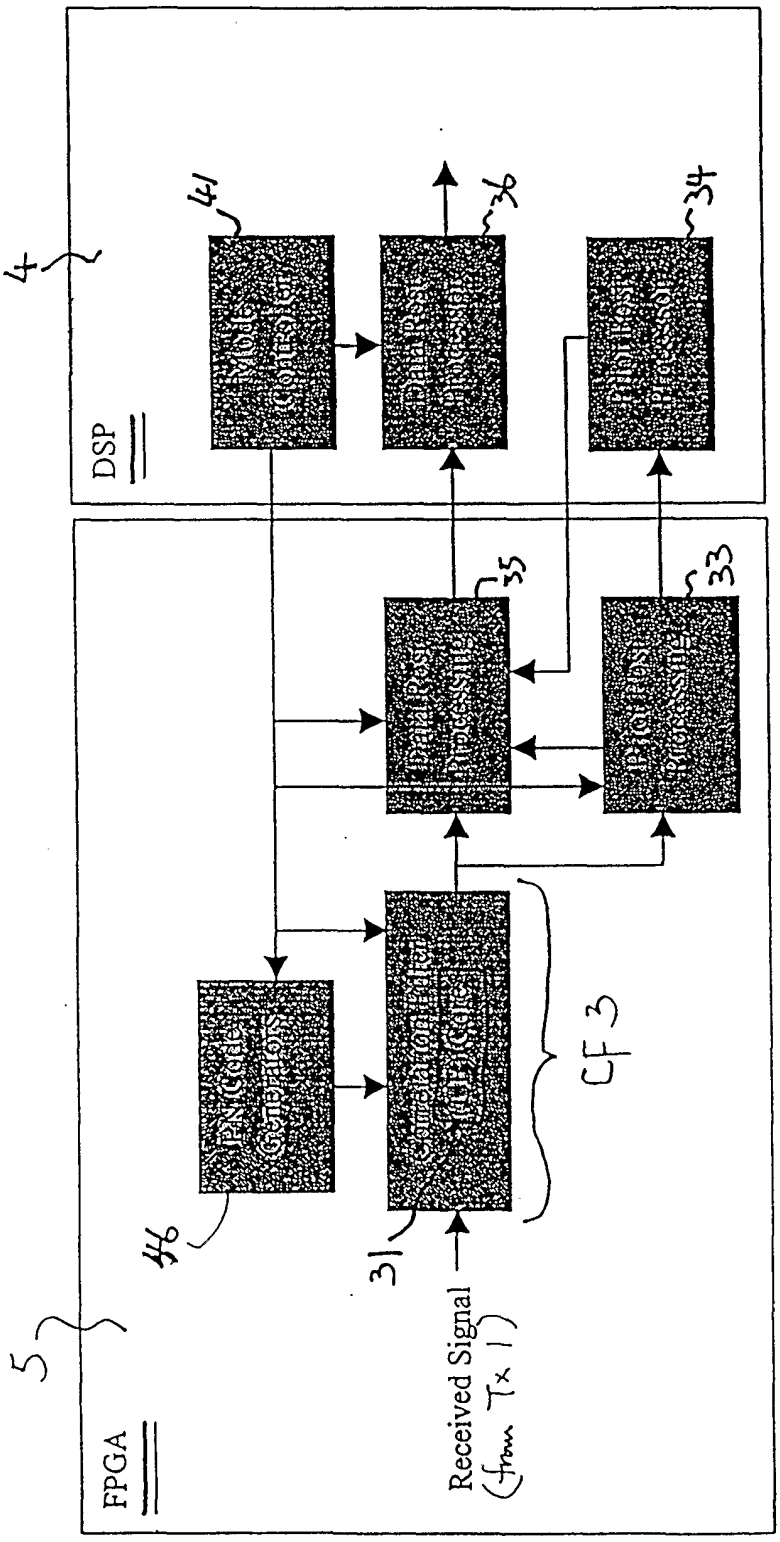


FIGURE 3

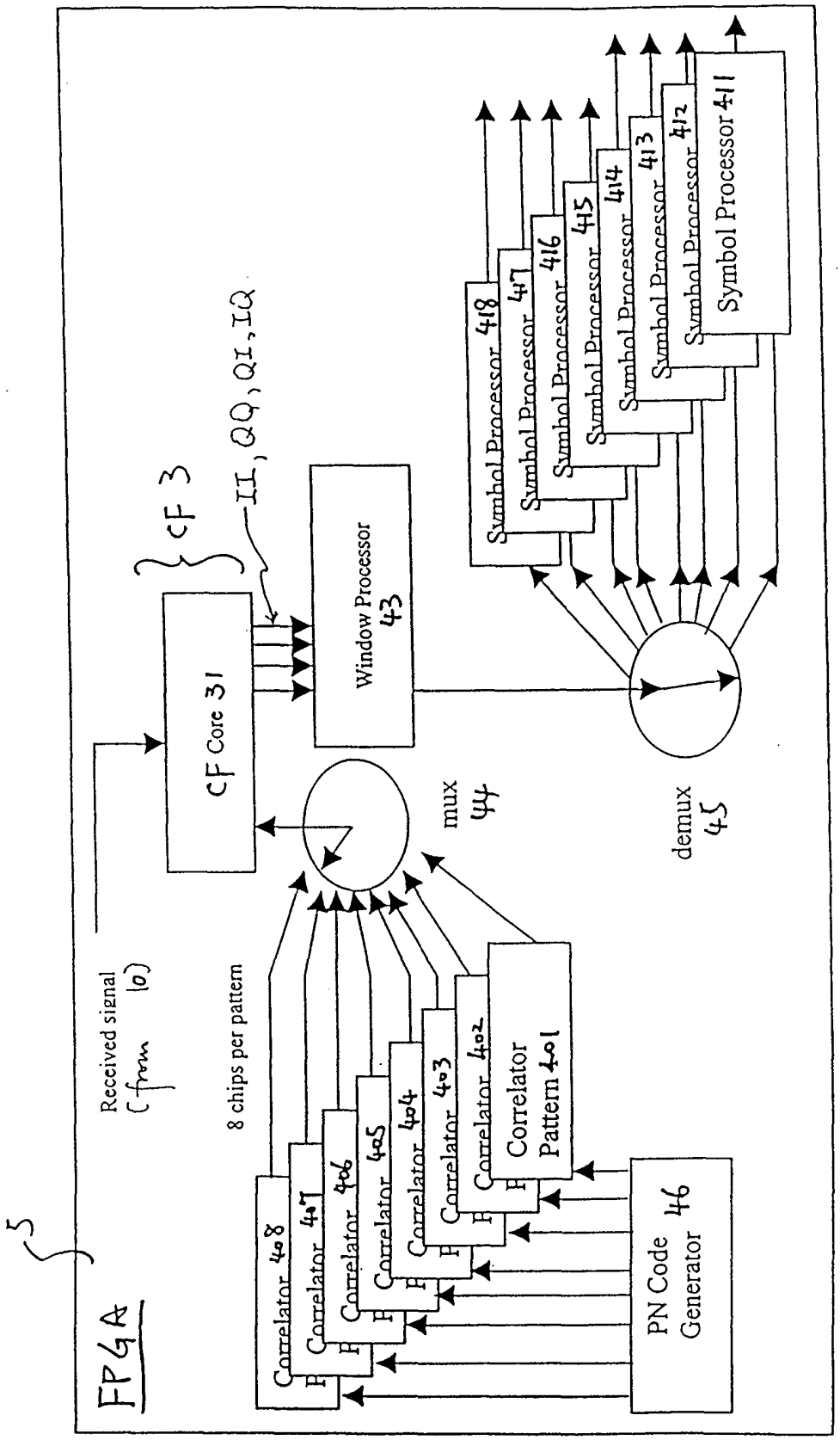

FPGA
5
Received signal (from 10)
8 chips per pattern
CF Core 31
CF 3
I, Q, QI, IQ
Window Processor 43
mux 44
demux 45
Correlator 408
Correlator 407
Correlator 406
Correlator 405
Correlator 404
Correlator 403
Correlator 402
Correlator Pattern 401
PN Code Generator 46
Symbol Processor 418
Symbol Processor 417
Symbol Processor 416
Symbol Processor 415
Symbol Processor 414
Symbol Processor 413
Symbol Processor 412
Symbol Processor 411

FIGURE 4

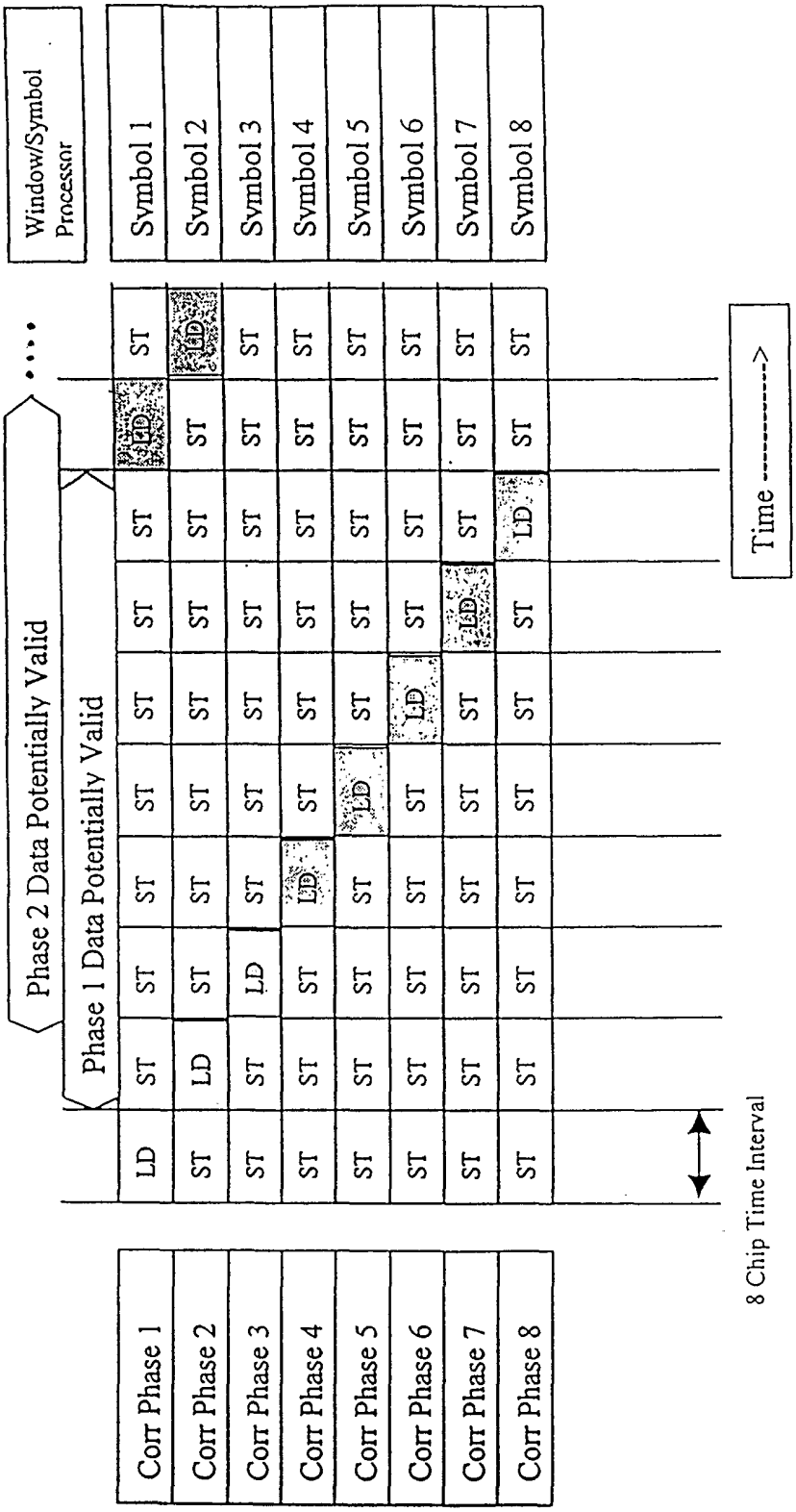

Window/Symbol Processor
Symbol 1
Symbol 2
Symbol 3
Symbol 4
Symbol 5
Symbol 6
Symbol 7
Symbol 8
Phase 2 Data Potentially Valid
Phase 1 Data Potentially Valid
Corr Phase 1
Corr Phase 2
Corr Phase 3
Corr Phase 4
Corr Phase 5
Corr Phase 6
Corr Phase 7
Corr Phase 8
8 Chip Time Interval
Time --------->

FIGURE 5

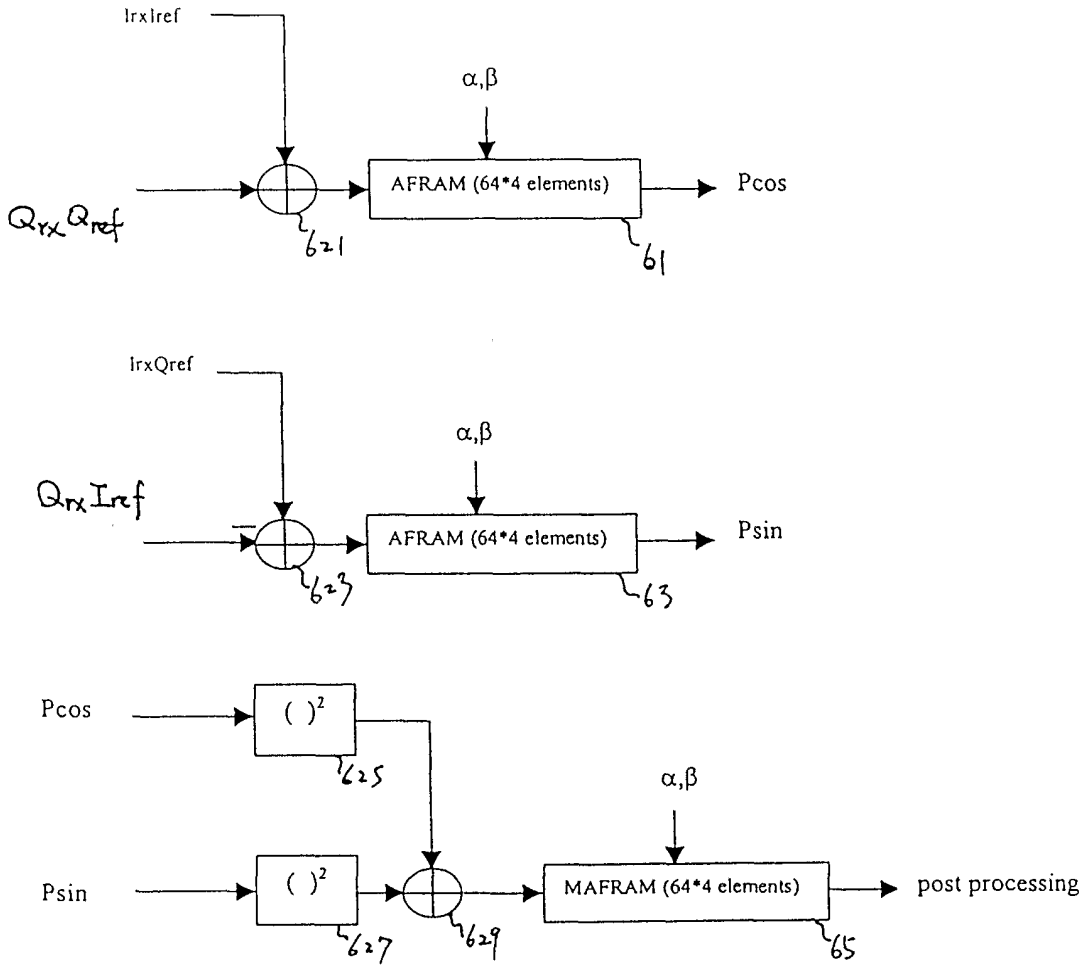

IrxIref
α,β
AFRAM (64*4 elements)
Pcos
Qrx Qref
621
61
IrxQref
α,β
Qrx Iref
AFRAM (64*4 elements)
Psin
623
63
Pcos
( )²
625
α,β
Psin
( )²
MAFRAM (64*4 elements)
post processing
627
629
65

Figure 6

Tier 1 symbol #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Data Type	P	D	D	D	D	D	D	D	P	D	D	D	D	D	D	D
AFRAM α	α	0	0	0	0	0	0	0	α	0	0	0	0	0	0	0
AFRAM β	β	1	1	1	1	1	1	1	β	1	1	1	1	1	1	1
MAFRAM α	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
MAFRAM β	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Tier 1 Pilot and Data Pattern with Corresponding AFRAM and MAFRAM Filter settings.

Tier 1 symbol #	1	2	3	4	5	6	7	8	62	63	64	65	66	67	68	69
Data Type	P	P	P	P	D	D	D	D	D	D	P	P	P	P	D	D
AFRAM α	α	α	α	α	0	0	0	0	0	0	α	α	α	α	0	0
AFRAM β	β	1	1	1	1	1	1	1	1	1	β	1	1	1	1	1
MAFRAM α	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
MAFRAM β	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Tier 2 Pilot and Data Pattern with Corresponding AFRAM and MAFRAM Filter settings.

Tier 1 symbol #	1	2	3	14	15	16	17	255	256	257	258	271	272	273
Data Type	P	P	P	P	P	P	D	D	P	P	P	P	P	D
AFRAM α	α	α	α	α	α	α	0	0	α	α	α	α	α	0
AFRAM β	β	1	1	1	1	1	1	1	β	1	1	1	1	1
MAFRAM α	1	1	1	1	1	1	1	1	1	1	1	1	1	1
MAFRAM β	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Tier 3 Pilot and Data Pattern with Corresponding AFRAM and MAFRAM Filter settings.

FIGURE 6A

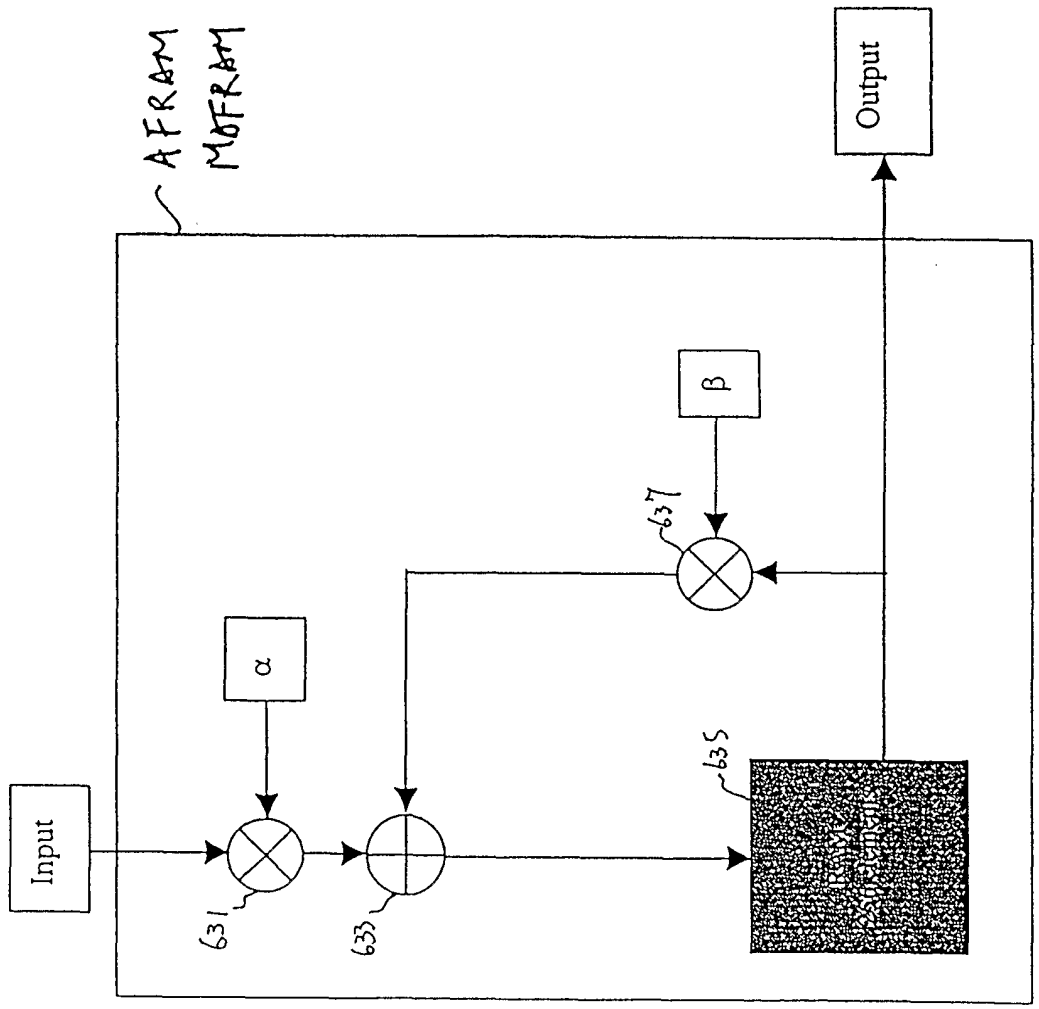


FIGURE 6B

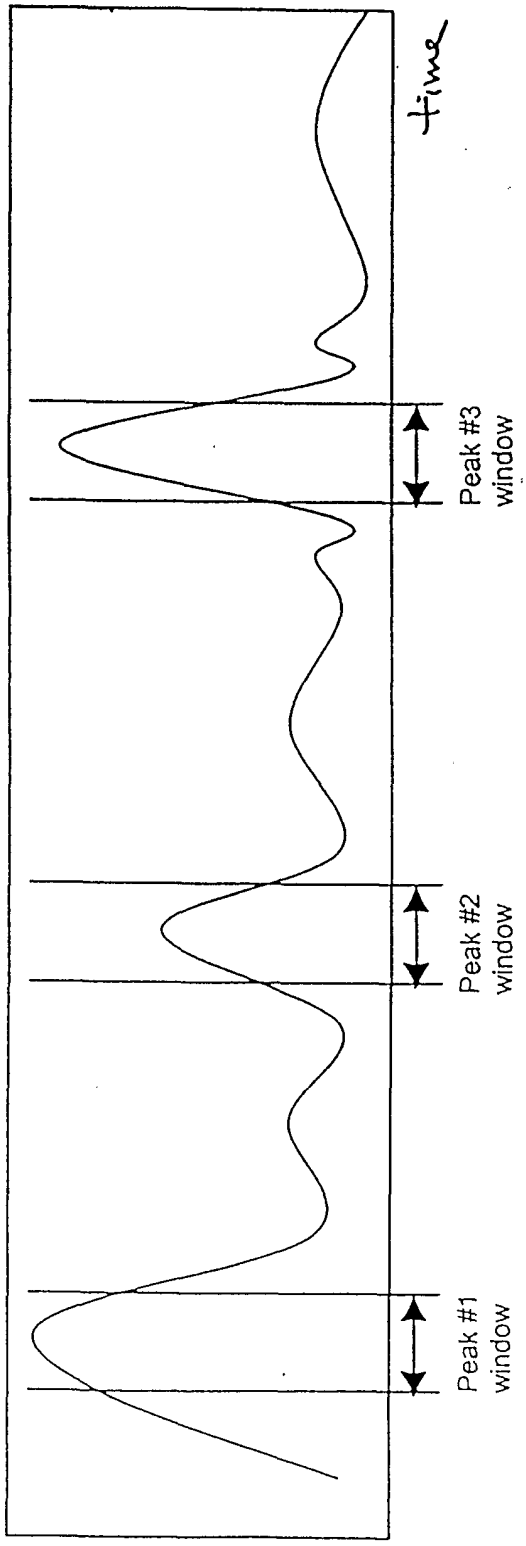
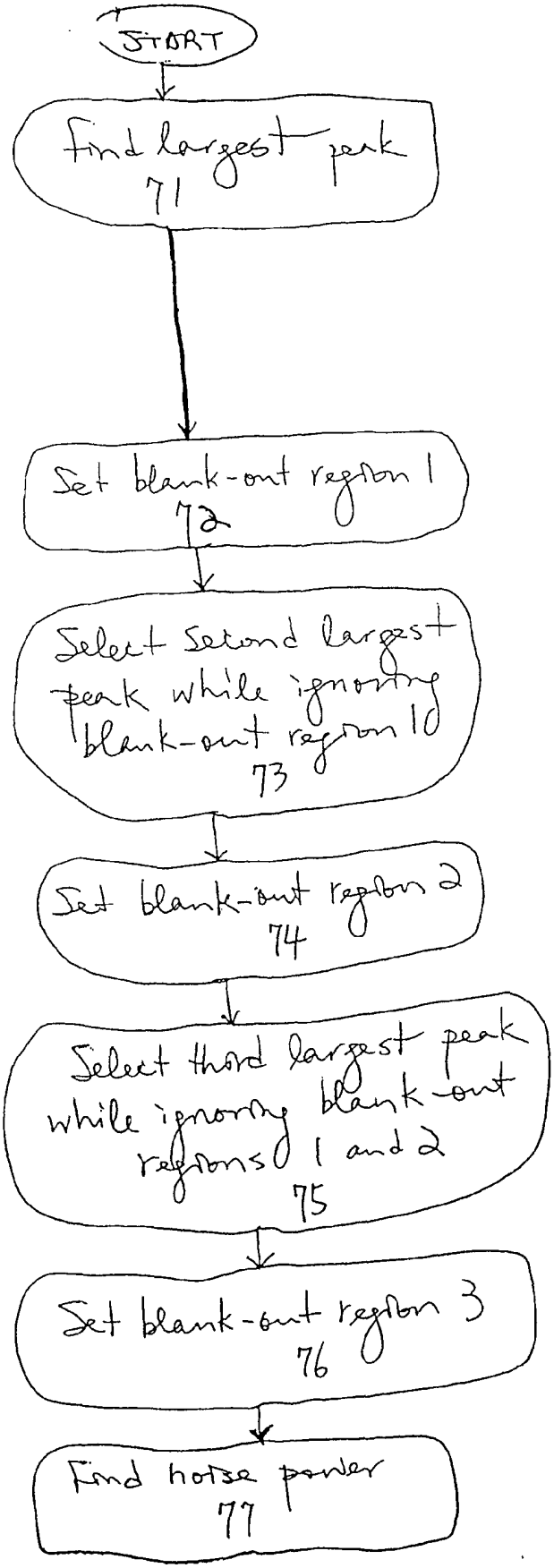

Multipaths
(Amplitude)
time
Peak #1
window
Peak #2
window
Peak #3
window

FIGURE 7

FIGURE 7A


START
Find largest peak
71
Set blank-out region 1
72
Select second largest peak while ignoring blank-out region 1
73
Set blank-out region 2
74
Select third largest peak while ignoring blank-out regions 1 and 2
75
Set blank-out region 3
76
Find horse power
77

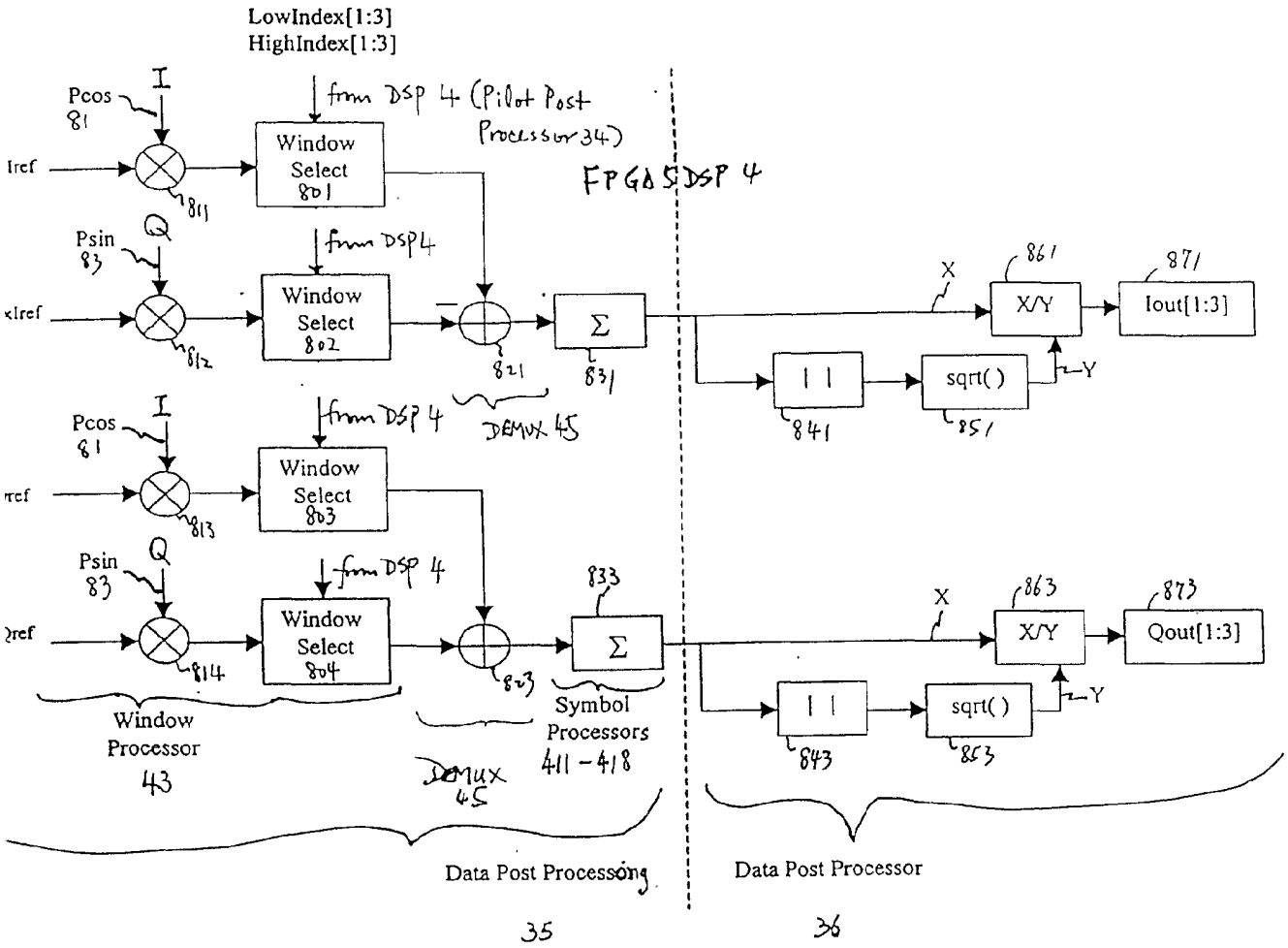
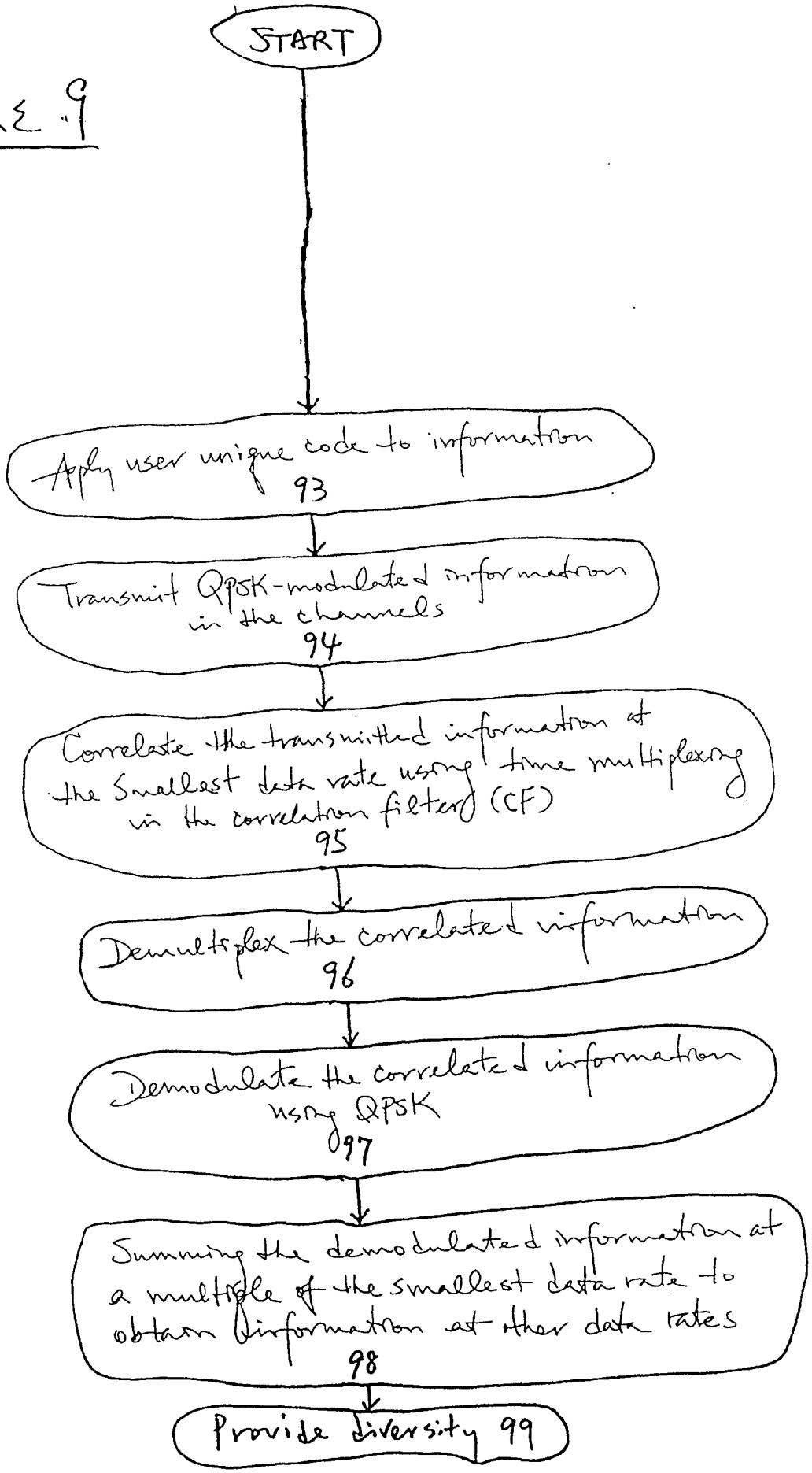

LowIndex[1:3]
HighIndex[1:3]
Pcos
81
I
Iref
811
Window Select 801
from DSP 4 (Pilot Post Processor 34)
FPGA'S DSP 4
Psin
83
Q
xIref
812
Window Select 802
from DSP4
821
Σ
831
DEMUX 45
861
X
X/Y
871
Iout[1:3]
| |
841
sqrt( )
851
Y
Pcos
81
I
rref
813
Window Select 803
from DSP 4
Psin
83
Q
)ref
814
Window Select 804
from DSP 4
823
833
Σ
Symbol Processors 411 - 418
Window Processor 43
DEMUX 45
863
X/Y
873
Qout[1:3]
| |
843
sqrt( )
853
Data Post Processing
Data Post Processor
35
36

FIGURE 8

FIGURE 9


START
Apply user unique code to information
93
Transmit QPSK-modulated information in the channels
94
Correlate the transmitted information at the smallest data rate using time multiplexing in the correlation filters (CF)
95
Demultiplex the correlated information
96
Demodulate the correlated information using QPSK
97
Summing the demodulated information at a multiple of the smallest data rate to obtain information at other data rates
98
Provide diversity 99