# United States Patent

[11] 3,594,778


[72] Inventors **Vernon R. Herald**
**Chicago;**
**Paul M. Kolesar, Chicago; Robert A. Payne, Des Plaines, all of, Ill.**



[21] Appl. No. **626,459**
[22] Filed **Mar. 28, 1967**
[45] Patented **July 20, 1971**



[73] Assignee **Stewart-Warner Corporation**
**Chicago, Ill.**


[54] **DISPLAY SYSTEM**
**20 Claims, 24 Drawing Figs.**


[52] **U.S. Cl.** ..... **340/337,** 340/324, 340/334
[51] **Int. Cl.** ..... **G09f 9/34**
[50] **Field of Search** ..... 340/324, 334, 337, 336, 339, 324.1, 347 DD, 174, 154, 152



[56] **References Cited**

UNITED STATES PATENTS

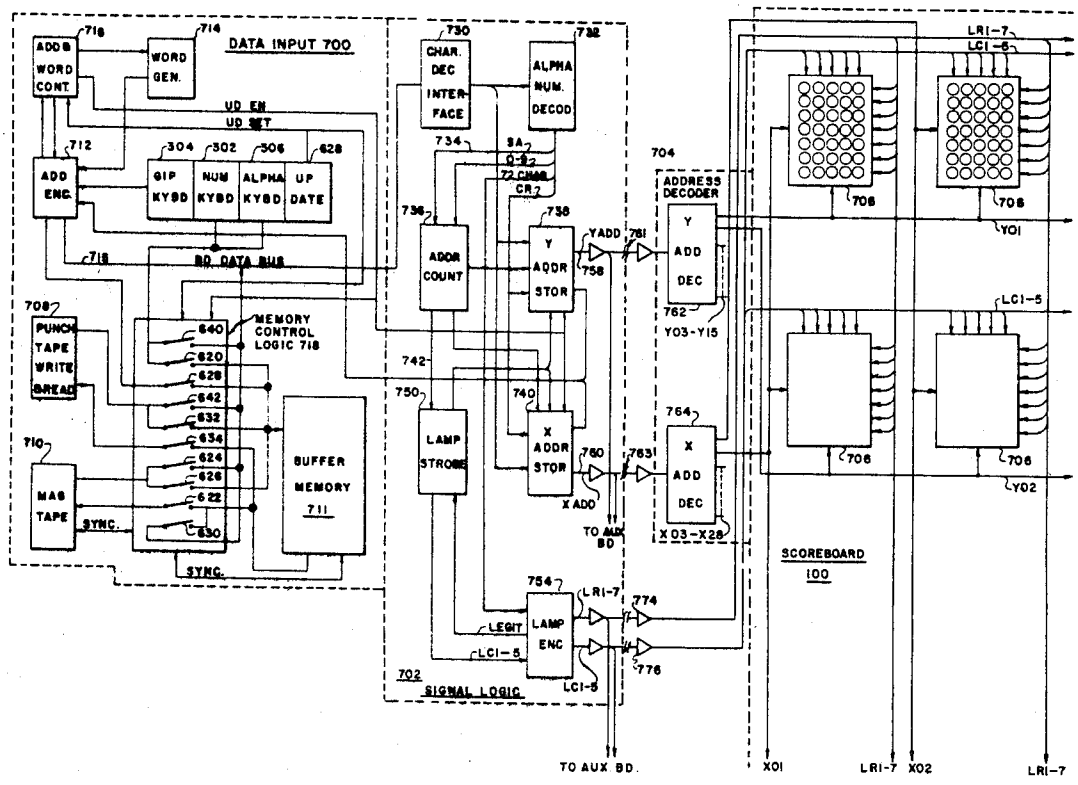
| | | | |
|---|---|---|---|
| 1,054,336 | 2/1913 | Brown | 340/339 |
| 2,911,622 | 11/1959 | Ayres et al. | 340/174 |
| 3,225,342 | 12/1965 | Clark | 340/324 |
| 3,273,140 | 9/1966 | Foster et al. | 340/334 |
| 2,181,682 | 11/1939 | Scheidegger | 340/154 |
| 3,462,739 | 8/1969 | Scantlin | 340/152 |



*Primary Examiner*—John W. Caldwell
*Assistant Examiner*—Marshall M. Curtis
*Attorneys*—Augustus G. Douvas, William J. Newman and Norton Lesser



**ABSTRACT:** Control System for a data display system such as a scoreboard, message board or the like wherein display indicators having location addresses, on the board, are addressed and actuated through a logic system which first receives and stores address data pertaining to a particular indicator, receives display character data, and automatically reads out the address data to the board for enabling the desired indicator followed by the display character data to actuate it to display the desired character. A buffer memory is provided for controlling the input to the logic system from a variety of input devices including console keyboard, punch tape typewriter and reader as well as magnetic memory storage devices. Circuits are provided in conjunction with the buffer for updating particular message data existing in the buffer as required by changes in the game or other information.

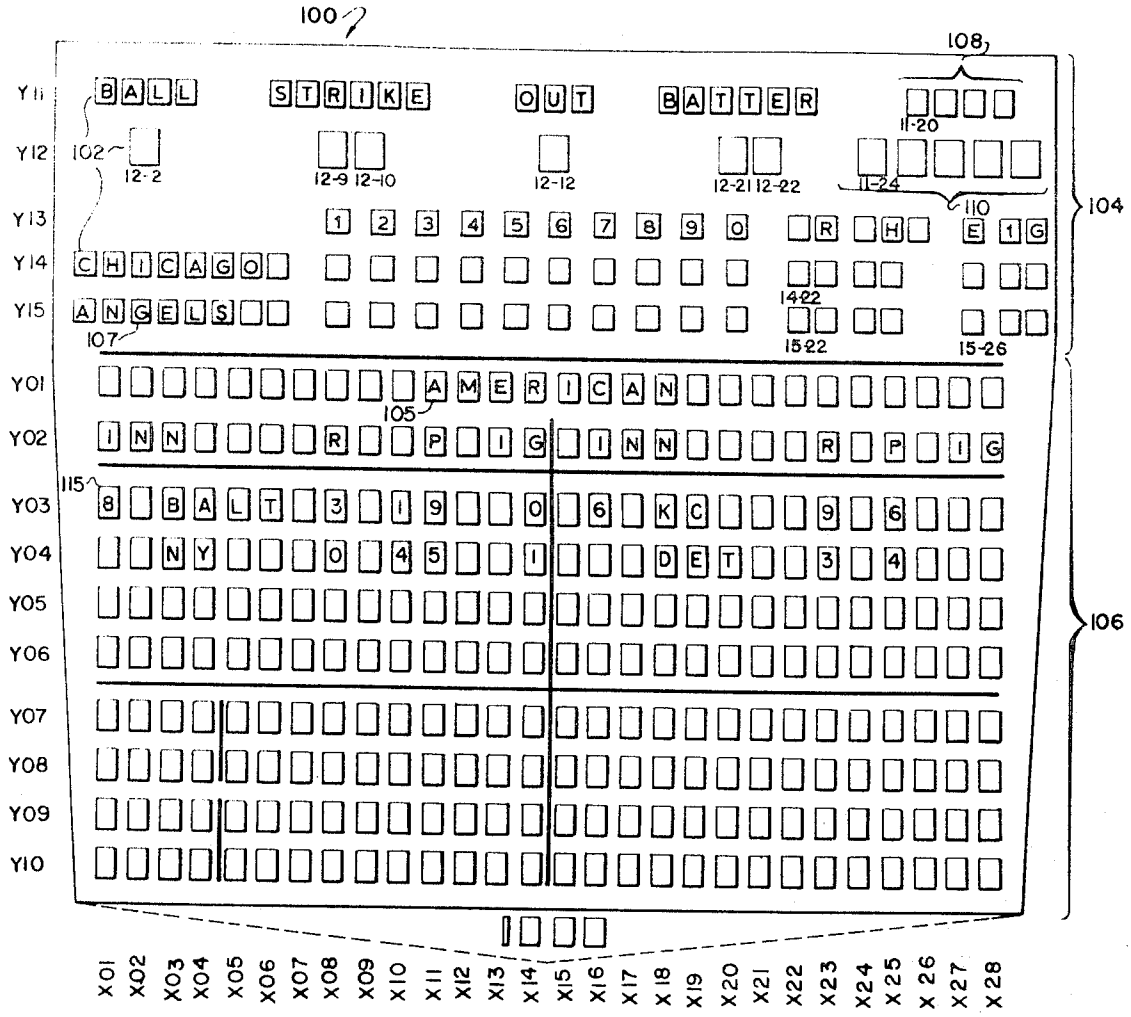



FIG. 1.

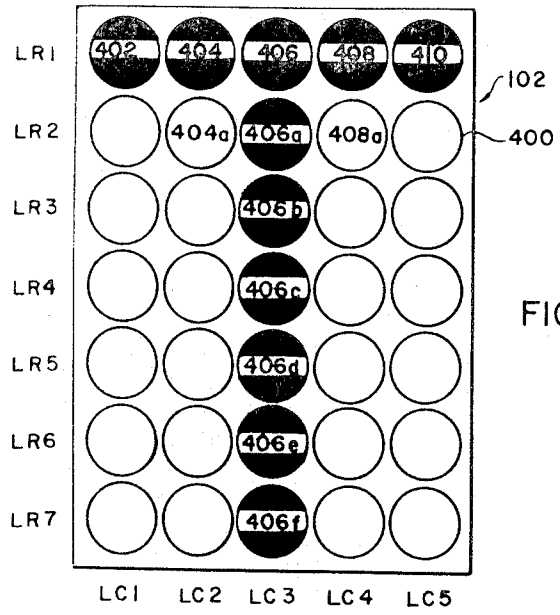



FIG. 4.

INVENTORS
VERNON R. HERALD
PAUL M. KOLESAR
ROBERT A. PAYNE

By

Attorney

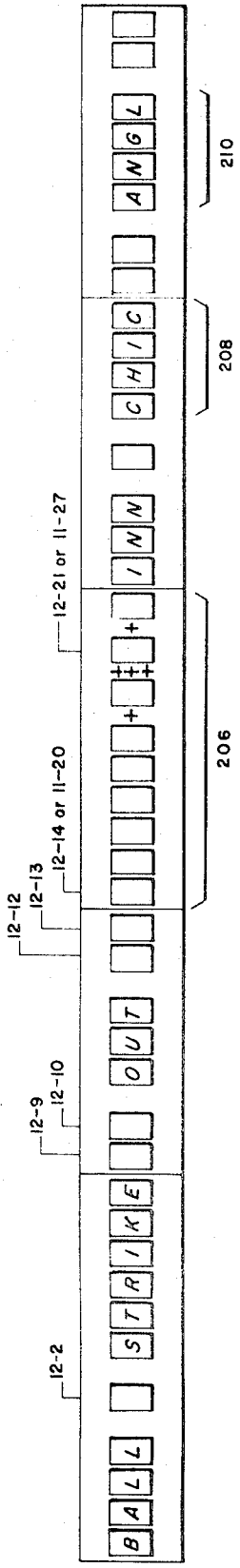



FIG. 2.

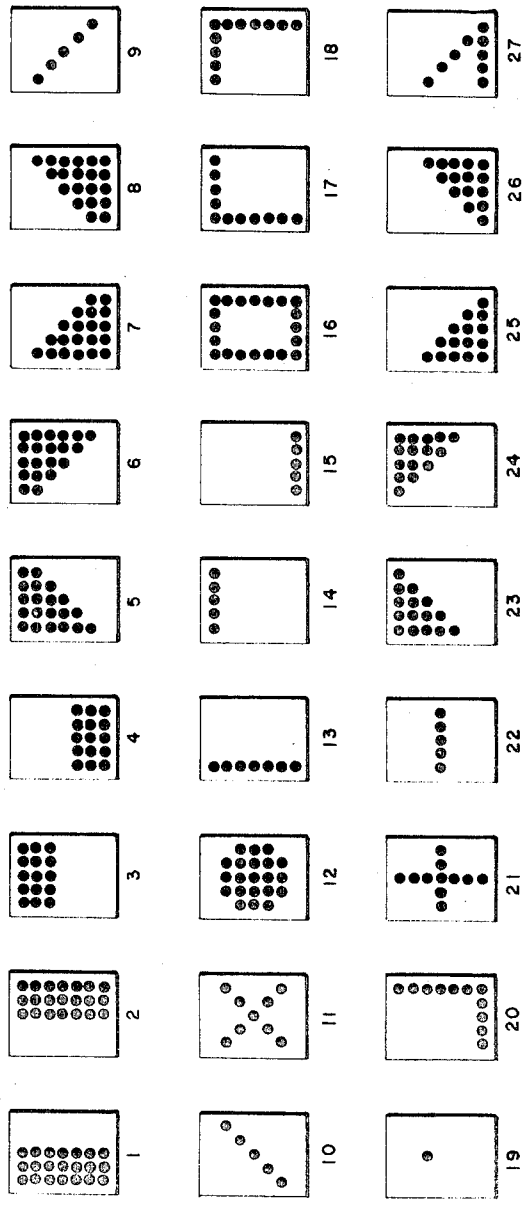



FIG. 5A.

INVENTORS
VERNON R. HERALD
PAUL M. KOLESAR
ROBERT A. PAYNE

By

Attorney

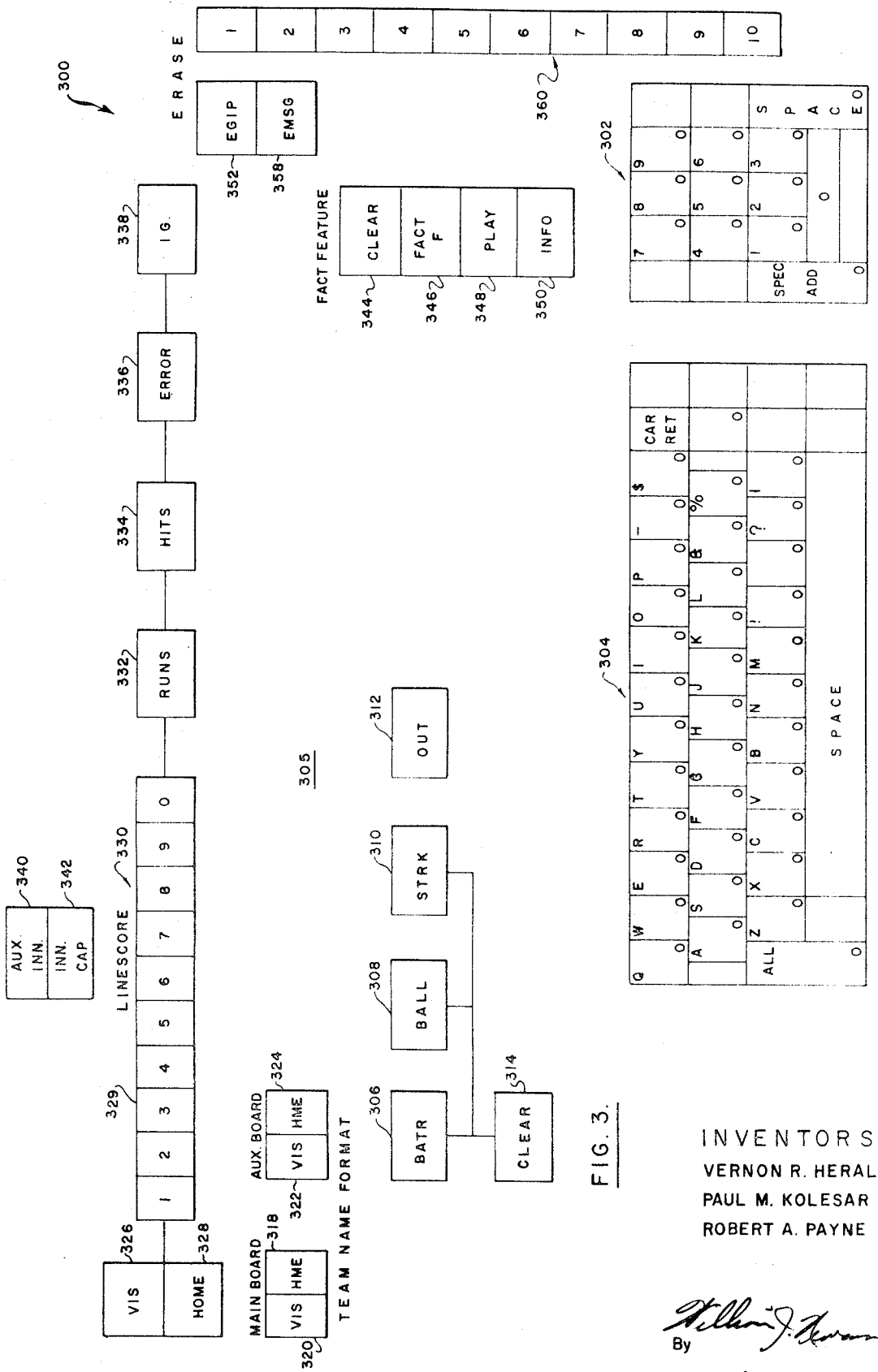



FIG. 3.

INVENTORS
VERNON R. HERALD
PAUL M. KOLESAR
ROBERT A. PAYNE

By

Attorney

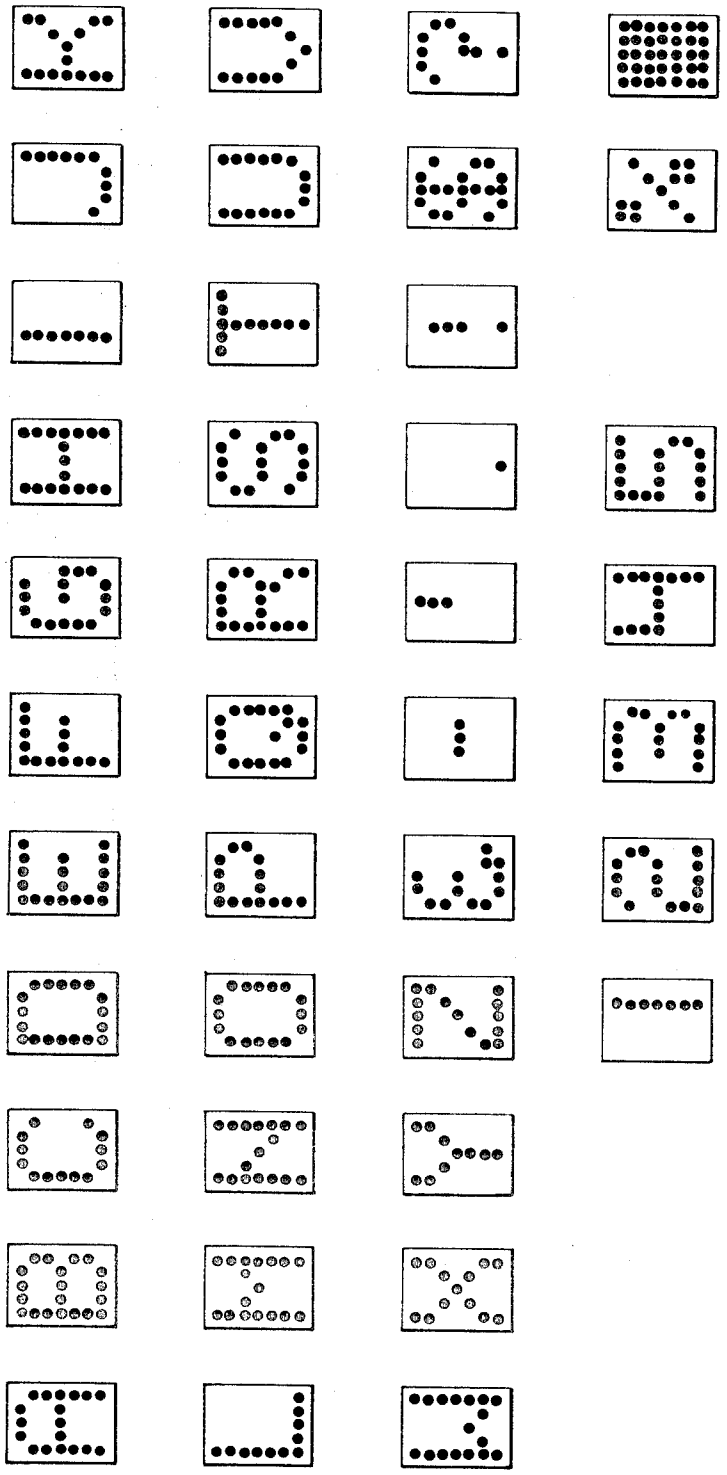


FIG. 5.

INVENTORS
VERNON R. HERAL
PAUL M. KOLESAR
ROBERT A. PAYNE

By

Attorney

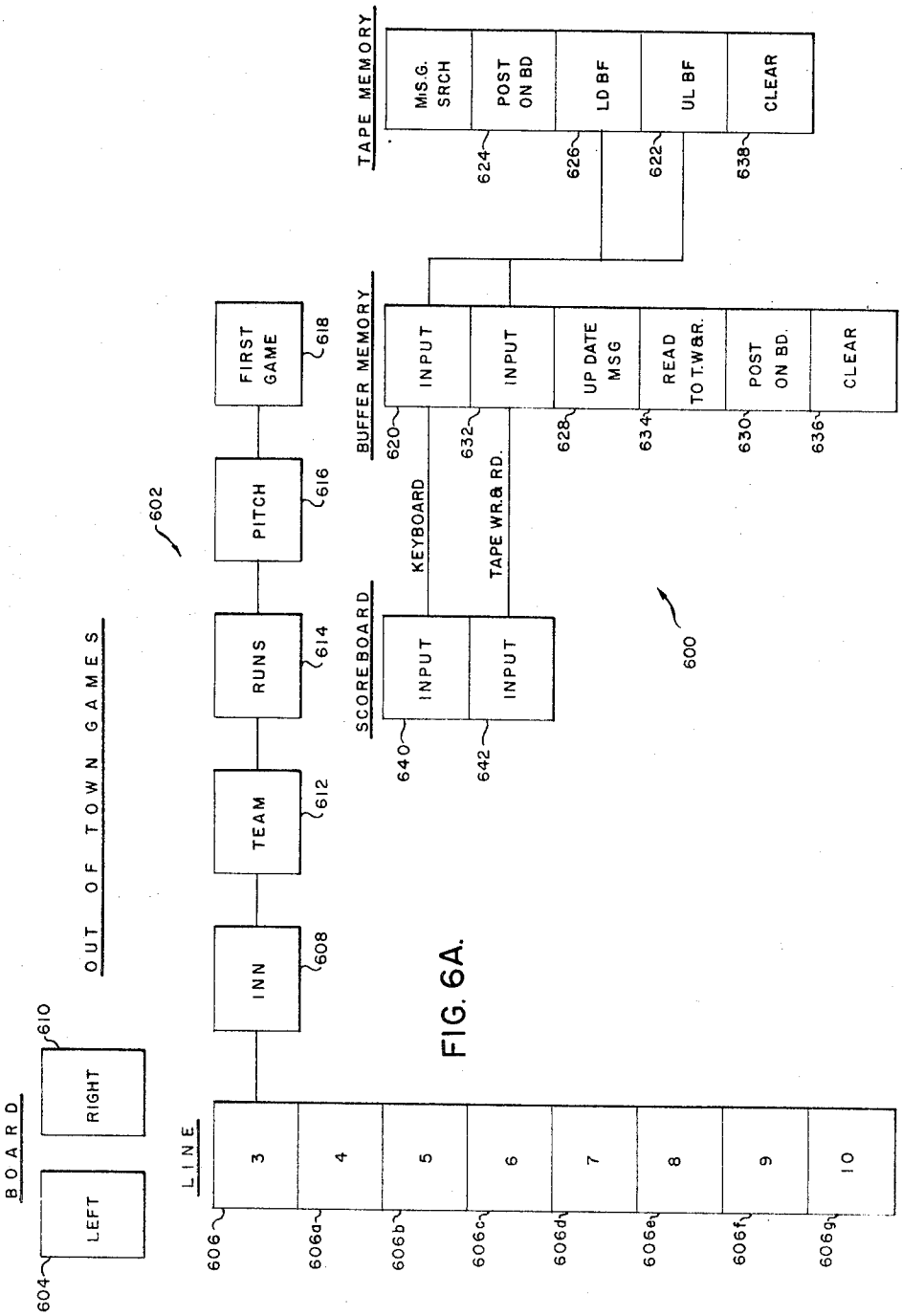



FIG. 6A.

FIG. 6.

INVENTORS
VERNON R. HERALD
PAUL M. KOLESAR
ROBERT A. PAYNE

By William J. Kenyon
Attorney

PATENTED JUL 20 1971

3,594,778

SHEET 06 OF 21

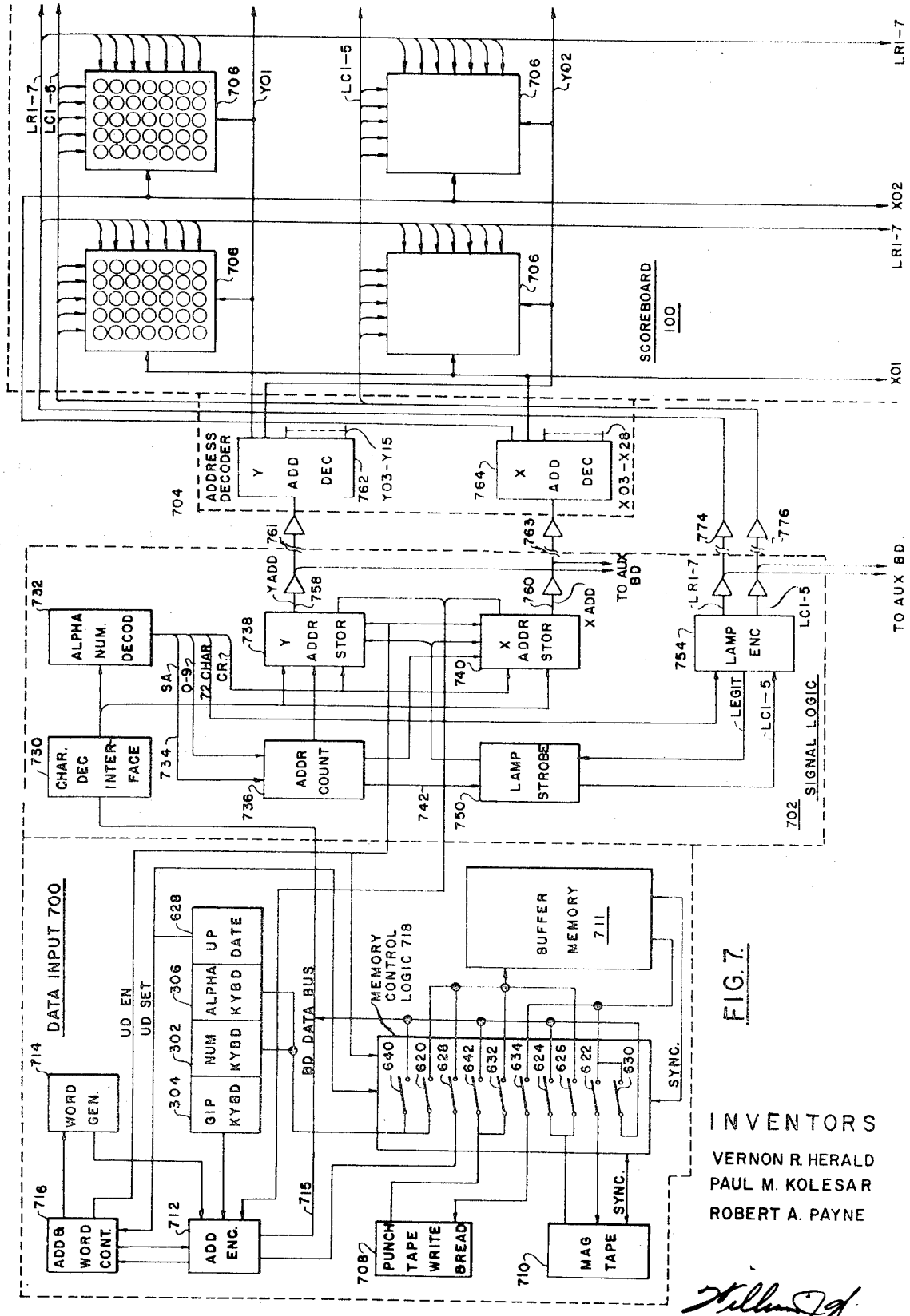



FIG. 7.

INVENTORS
VERNON R. HERALD
PAUL M. KOLESAR
ROBERT A. PAYNE

By

Attorney

# MODIFIED ASCII CODE

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | COLUMN / ROW | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 0 | 0 | 0 | 0 | | | SPACE | 0 | | P | ALL | ALL |
| | | | 0 | 0 | 0 | 1 | 1 | | | ! | 1 | A | Q | SC1 | SC16 |
| | | | 0 | 0 | 1 | 0 | 2 | | | | 2 | B | R | SC2 | SC17 |
| | | | 0 | 0 | 1 | 1 | 3 | | | # | 3 | C | S | SC3 | SC18 |
| | | | 0 | 1 | 0 | 0 | 4 | | | $ | 4 | D | T | SC4 | SC19 |
| | | | 0 | 1 | 0 | 1 | 5 | | | % | 5 | E | U | SC5 | SC20 |
| | | | 0 | 1 | 1 | 0 | 6 | | | & | 6 | F | V | SC6 | SC21 |
| | | | 0 | 1 | 1 | 1 | 7 | | ETB | ' | 7 | G | W | SC7 | SC22 |
| | | | 1 | 0 | 0 | 0 | 8 | | | | 8 | 4 | X | SC8 | SC23 |
| | | | 1 | 0 | 0 | 1 | 9 | | | ) | 9 | I | Y | SC9 | SC24 |
| | | | 1 | 0 | 1 | 0 | 10 | | | *SA | | J | Z | SC10 | SC25 |
| | | | 1 | 0 | 1 | 1 | 11 | | | + | | K | | SC11 | SC26 |
| | | | 1 | 1 | 0 | 0 | 12 | | | BLANK MESS, | | L | | SC12 | SC27 |
| | | | 1 | 1 | 0 | 1 | 13 | CR | | - | | M | | SC13 | |
| | | | 1 | 1 | 1 | 0 | 14 | | | . | | N | | SC14 | |
| | | | 1 | 1 | 1 | 1 | 15 | | | / | ? | O | | SC15 | |

FIG. 9.

INVENTORS
VERNON R. HERALD
PAUL M. KOLESAR
ROBERT A PAYNE

By

Attorney

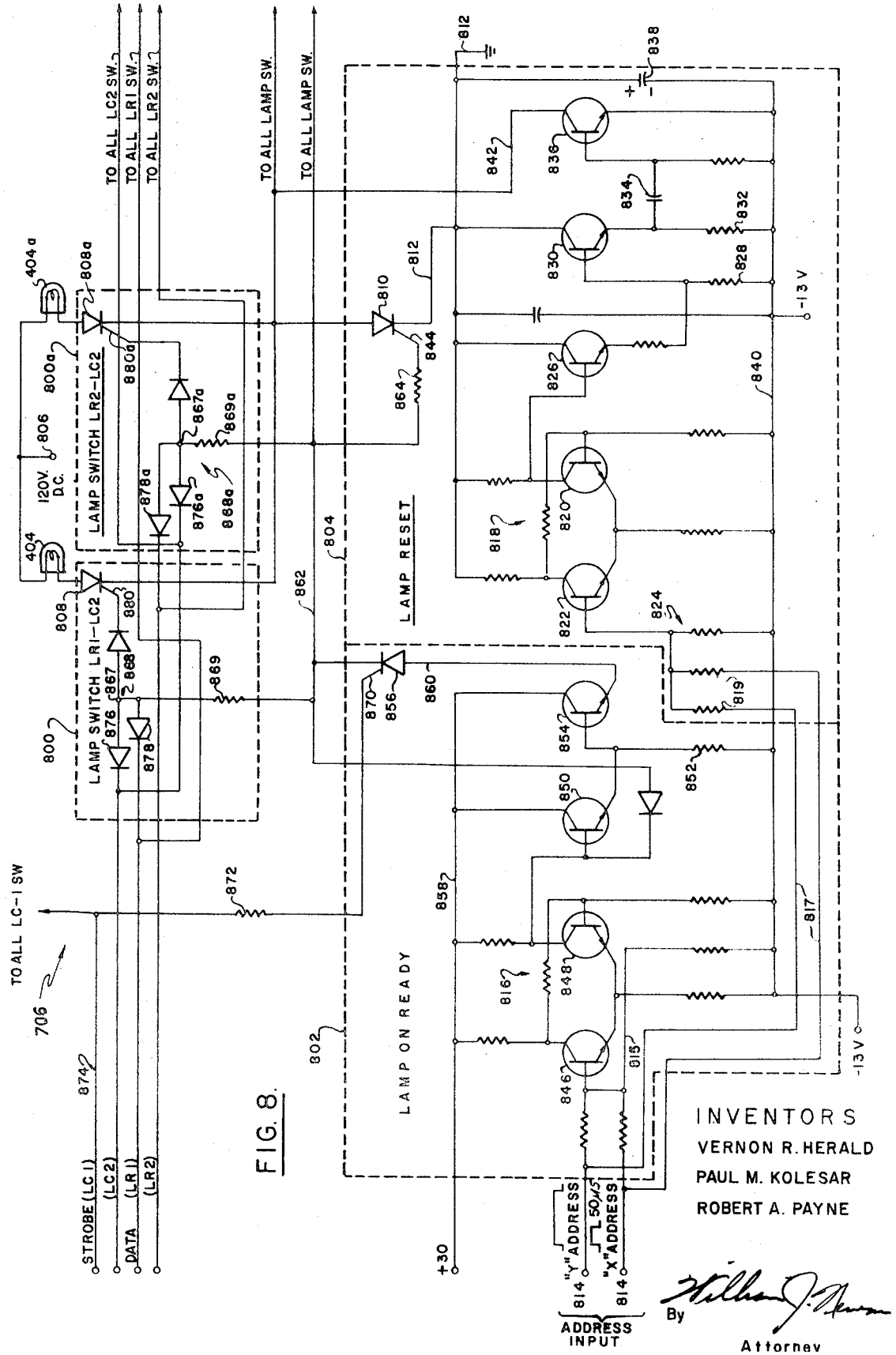



FIG. 8.

INVENTORS
VERNON R. HERALD
PAUL M. KOLESAR
ROBERT A. PAYNE

By

Attorney

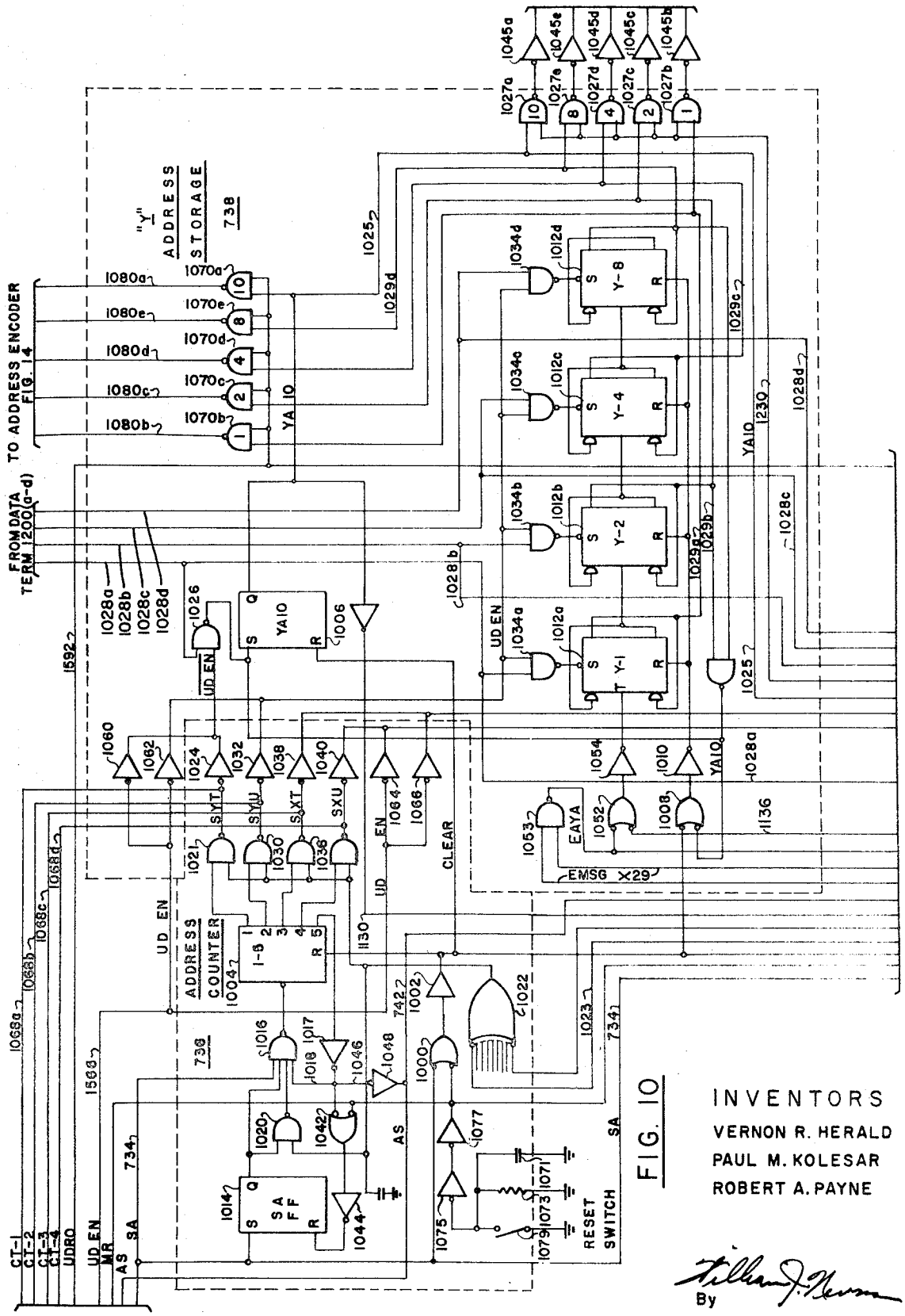



FIG. 10

INVENTORS
VERNON R. HERALD
PAUL M. KOLESAR
ROBERT A. PAYNE

By

Attorney

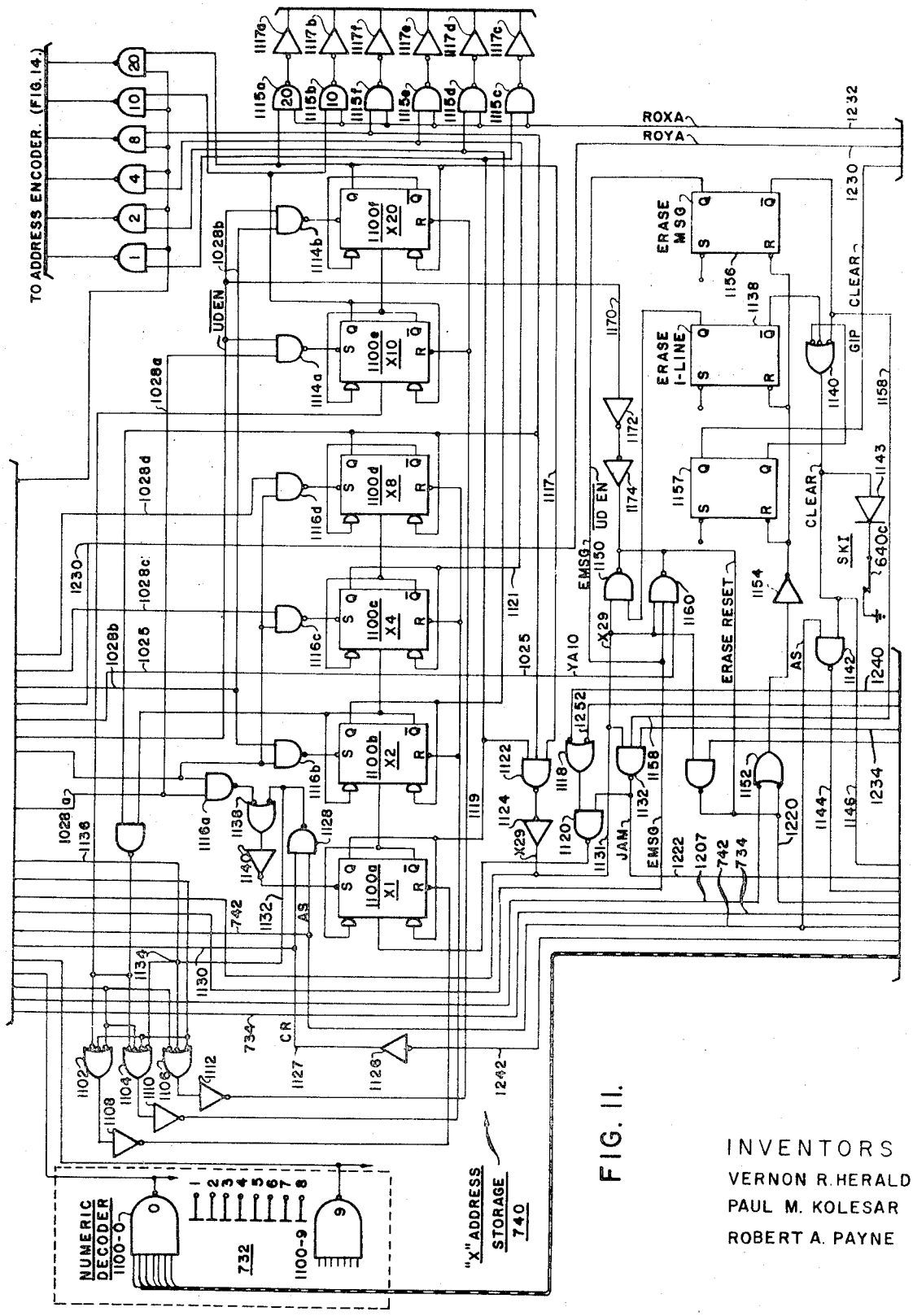
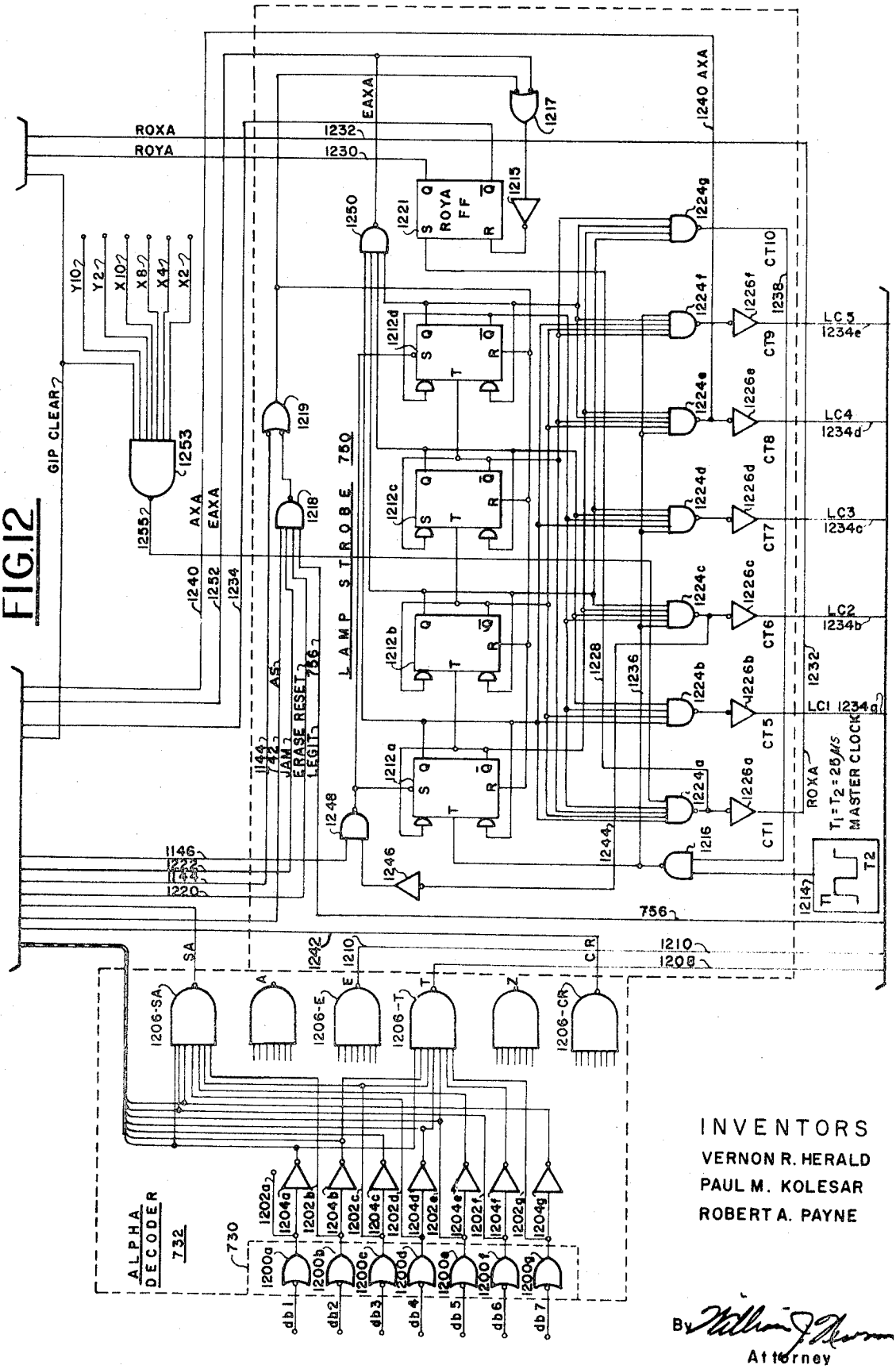



FIG. 11.

INVENTORS
VERNON R. HERALD
PAUL M. KOLESAR
ROBERT A. PAYNE

By William J. Thomson
Attorney

FIG. 12




INVENTORS
VERNON R. HERALD
PAUL M. KOLESAR
ROBERT A. PAYNE

By William J. Keenan
Attorney

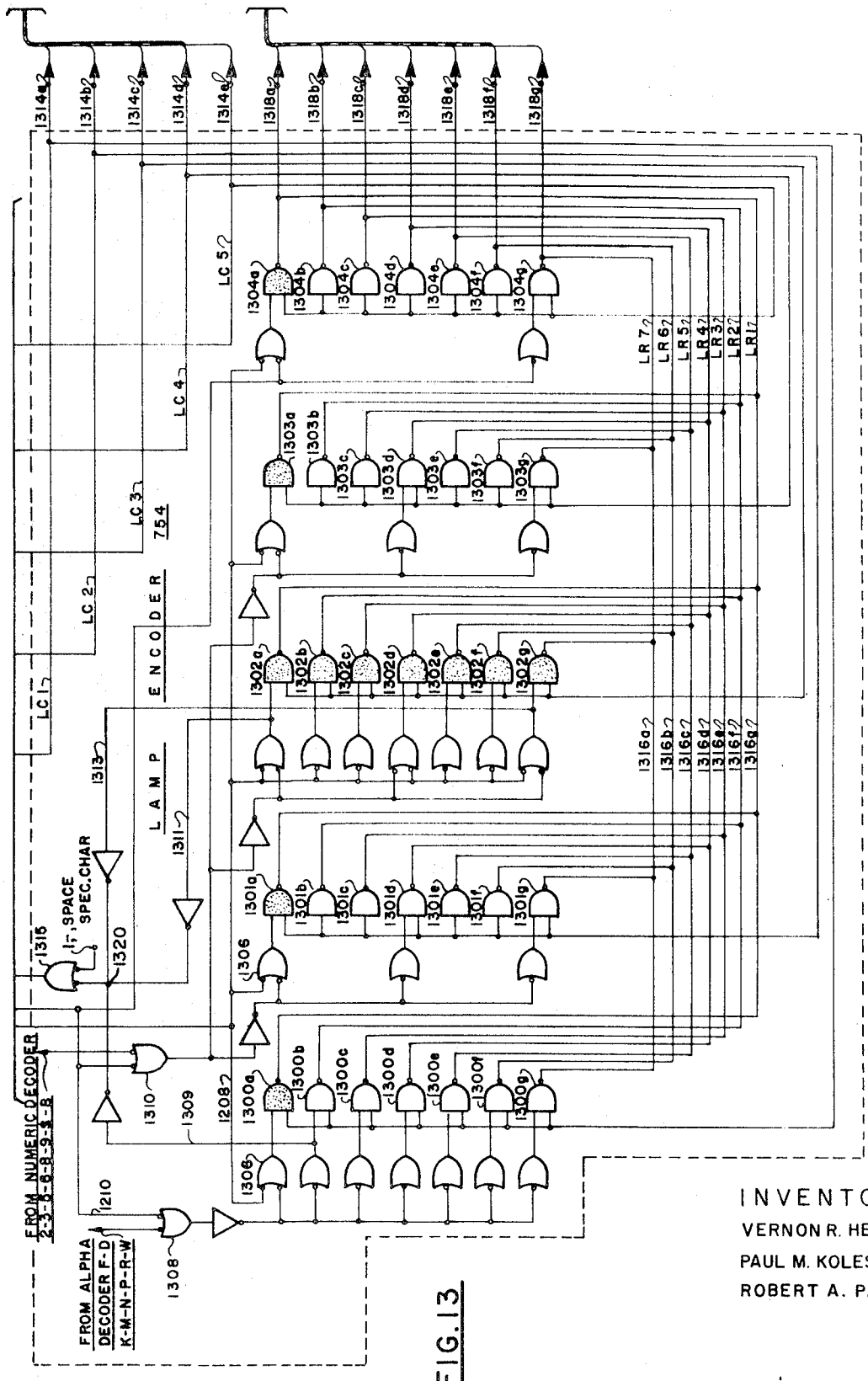
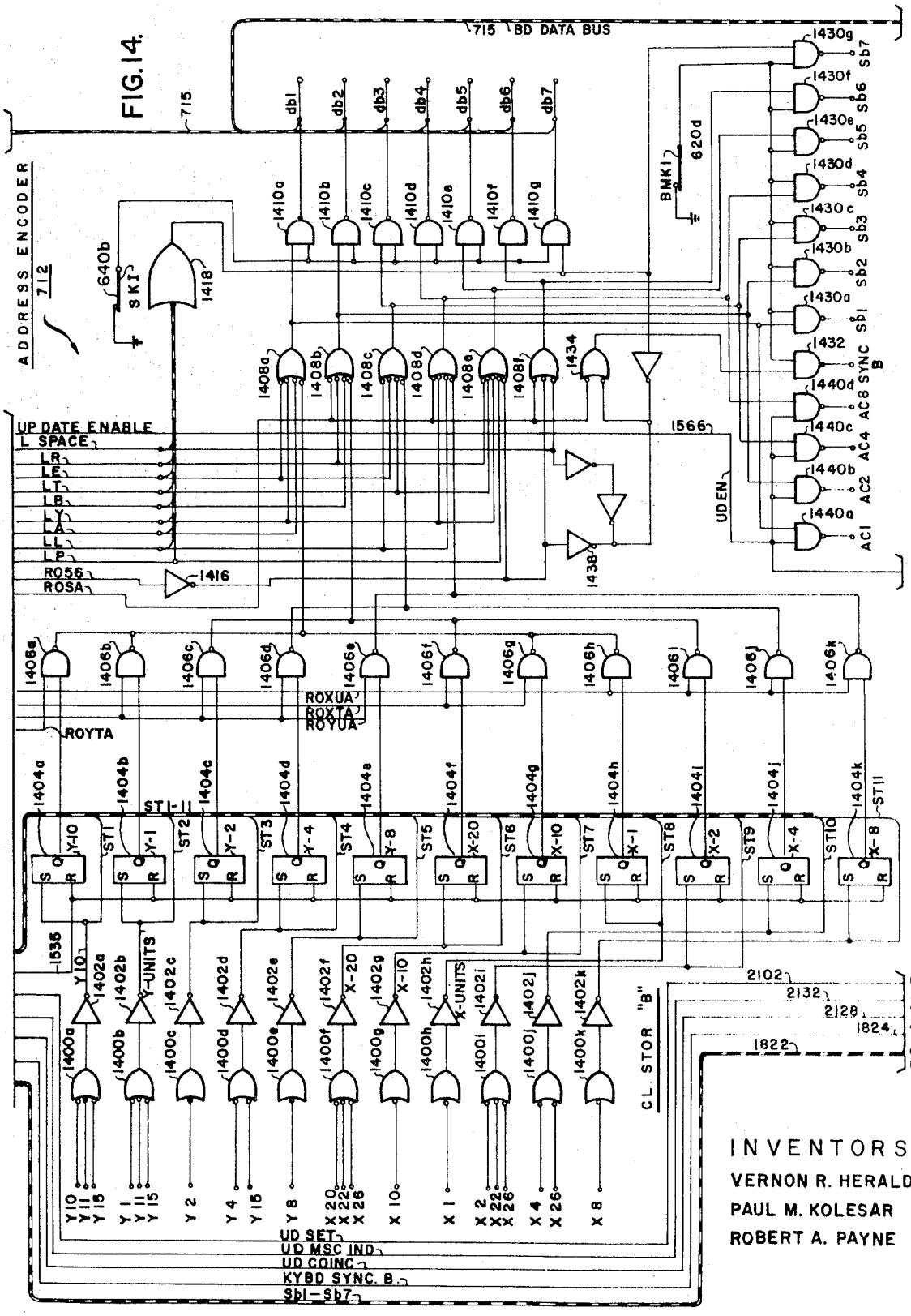



FIG. 13

INVENTORS
VERNON R. HERALD
PAUL M. KOLESAR
ROBERT A. PAYNE

By William J. Thomas
Attorney

FIG. 14.




INVENTORS
VERNON R. HERALD
PAUL M. KOLESAR
ROBERT A. PAYNE

By
Attorney

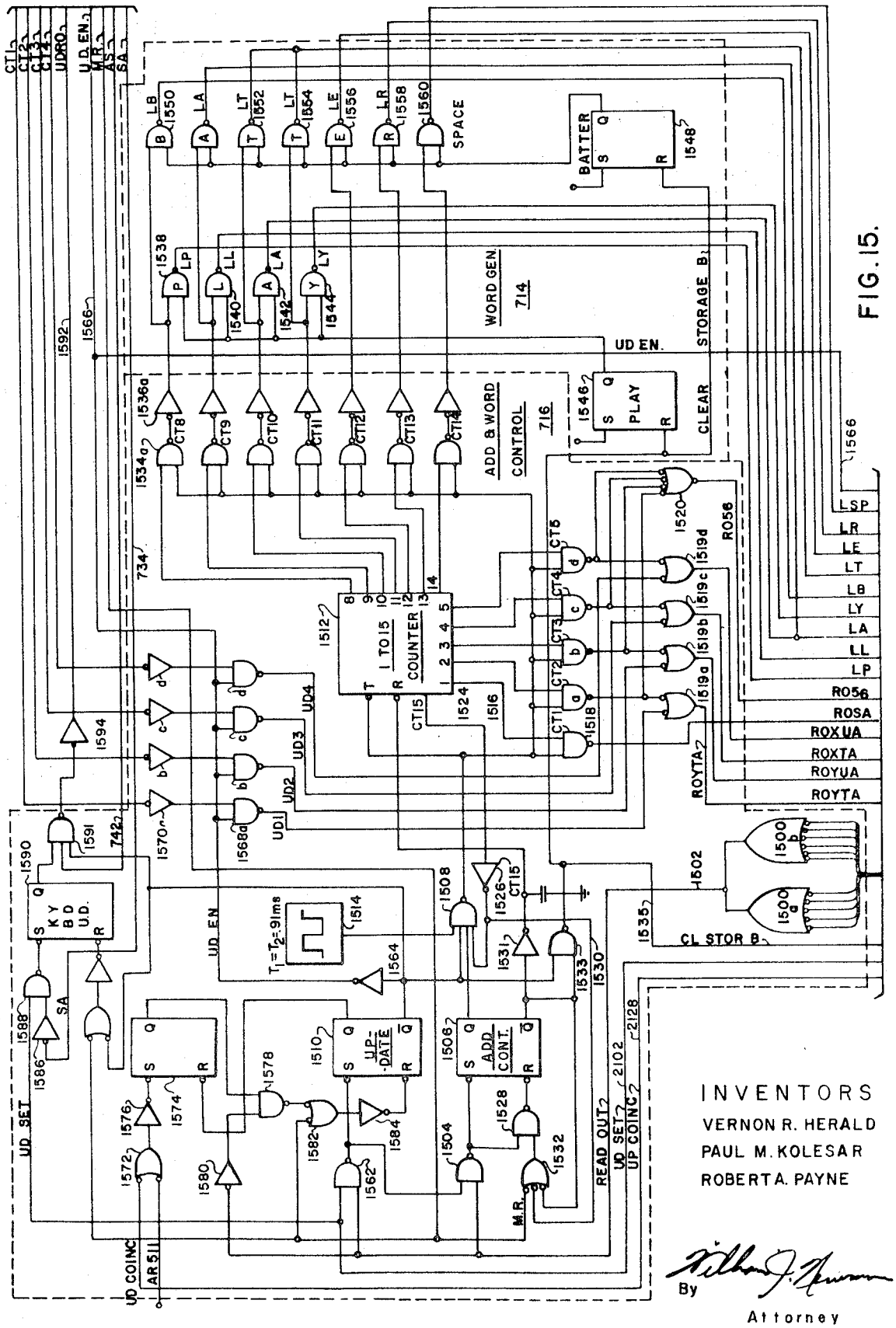
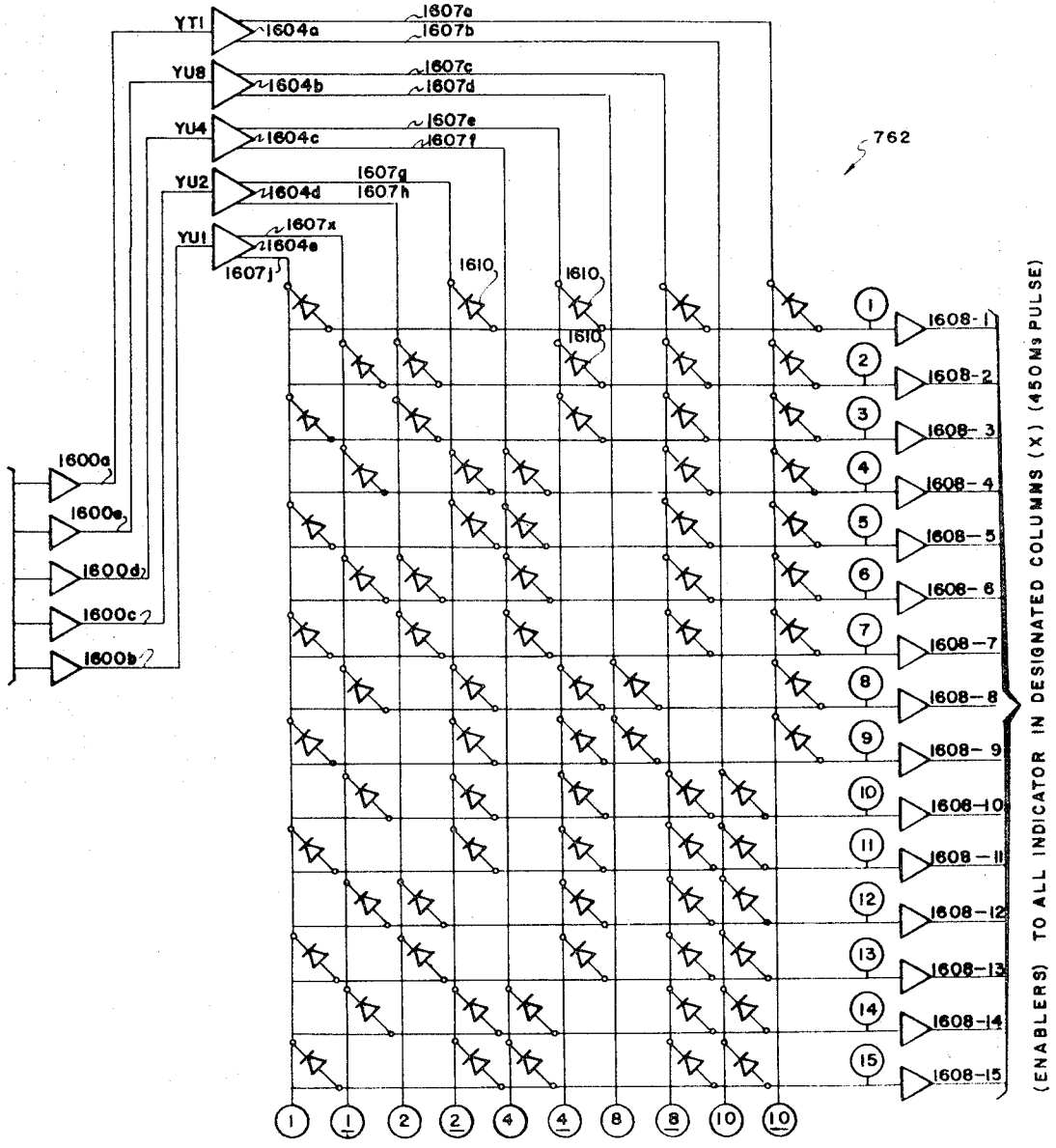



FIG. 15.

INVENTORS
VERNON R. HERALD
PAUL M. KOLESAR
ROBERT A. PAYNE

By

Attorney



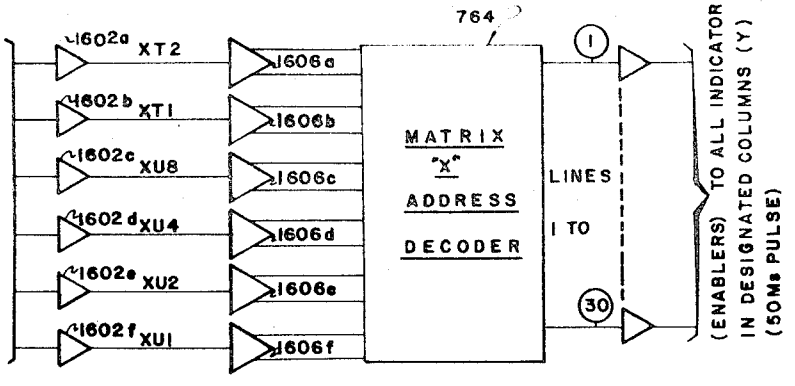




FIG. 16.

INVENTORS
VERNON R. HERALD
PAUL M. KOLESAR
ROBERT A. PAYNE

By William J. Thomas
Attorney

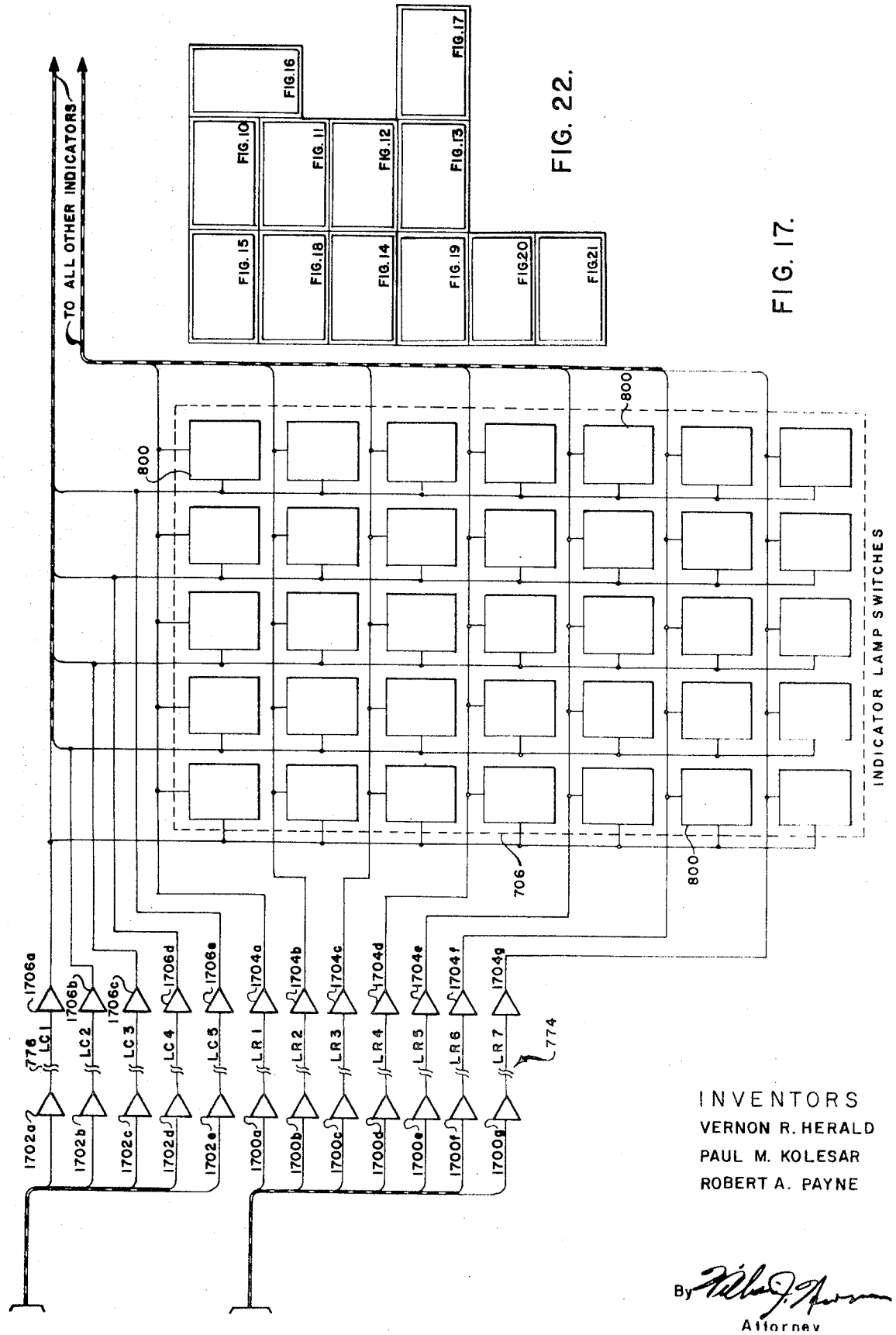
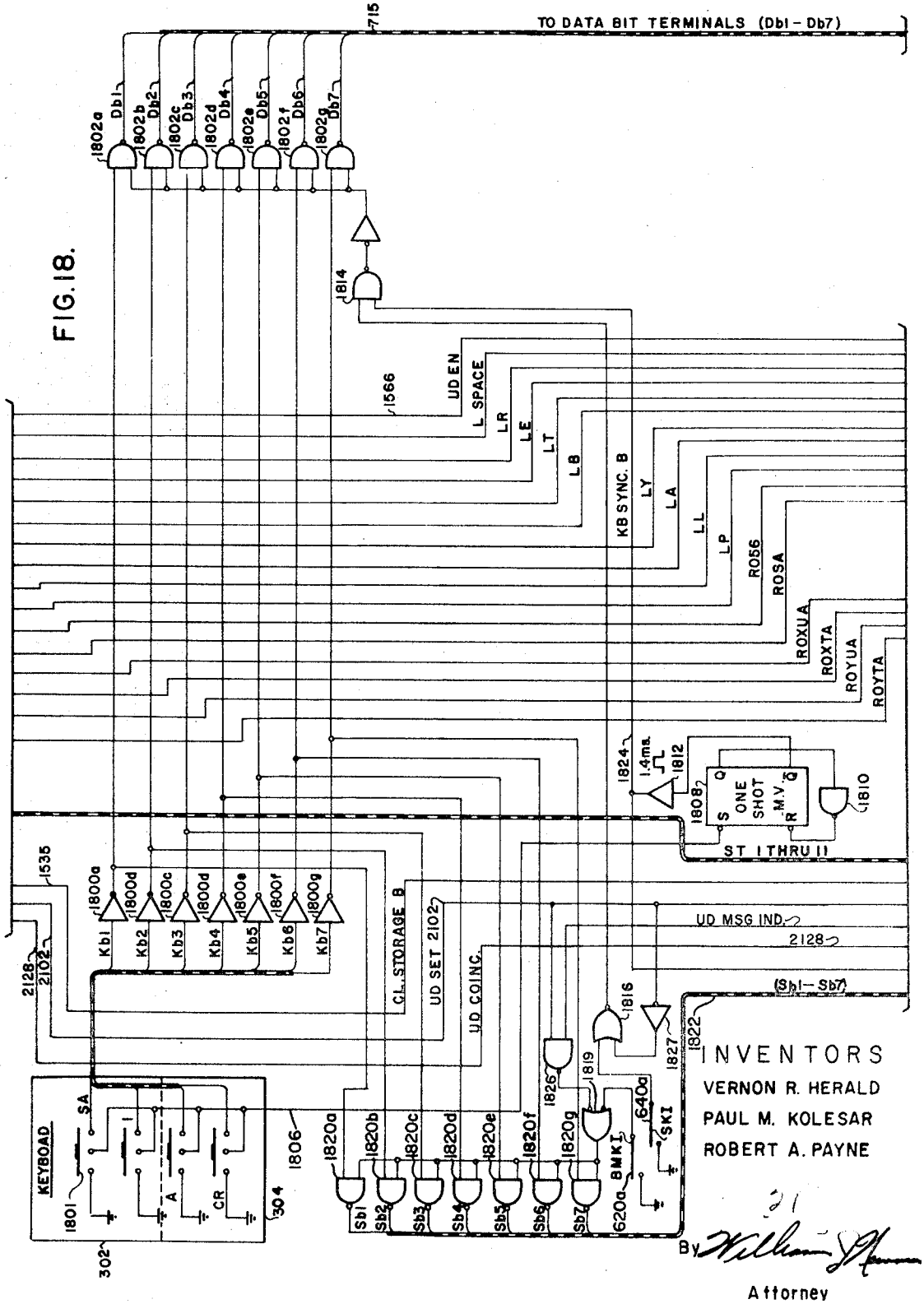



FIG. 17.

INVENTORS
VERNON R. HERALD
PAUL M. KOLESAR
ROBERT A. PAYNE

By
Attorney

FIG. 18.




INVENTORS
VERNON R. HERALD
PAUL M. KOLESAR
ROBERT A. PAYNE

By William J. Kenyon
Attorney

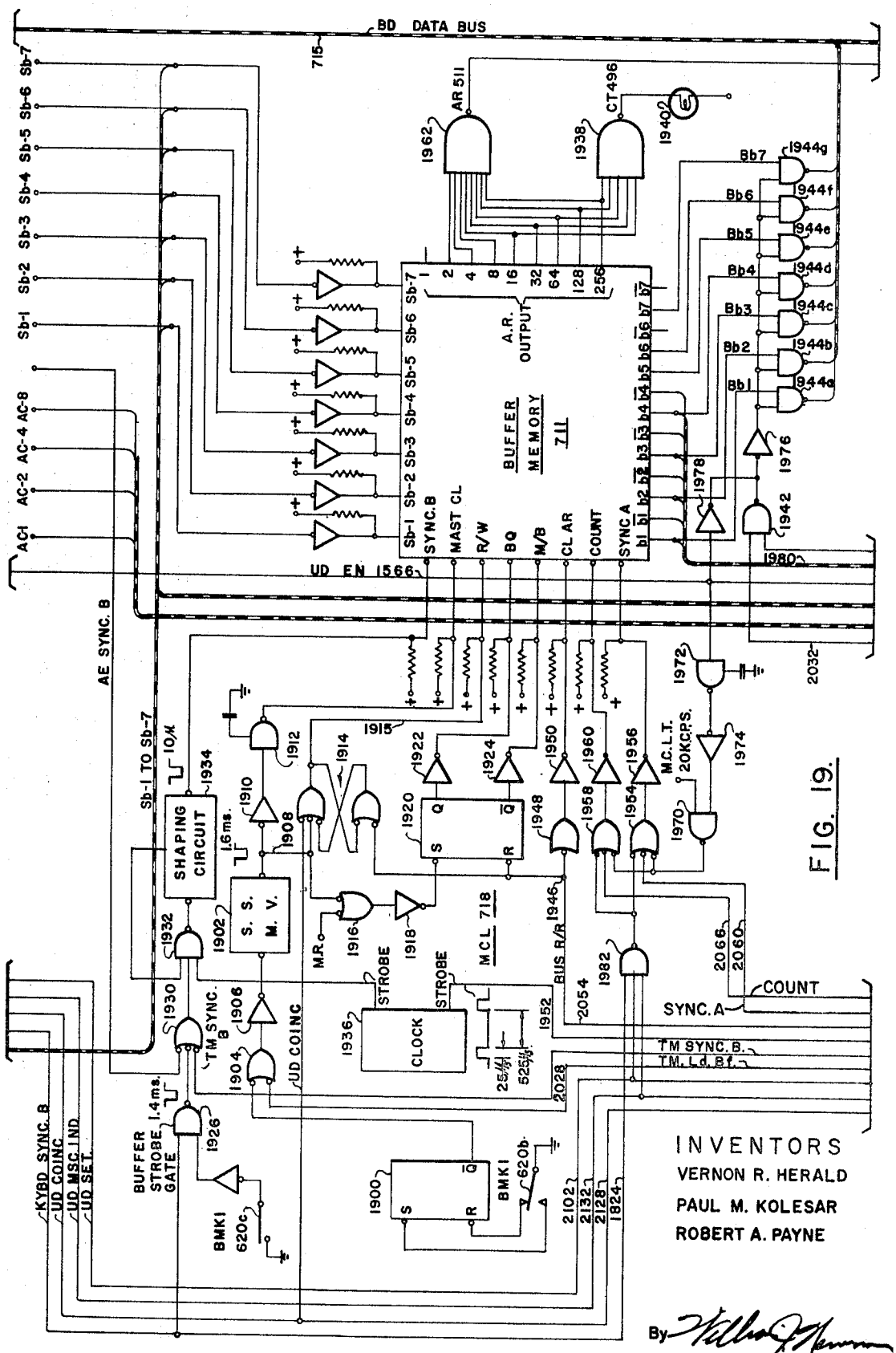



FIG. 19.

INVENTORS
VERNON R. HERALD
PAUL M. KOLESAR
ROBERT A. PAYNE

By
Attorney

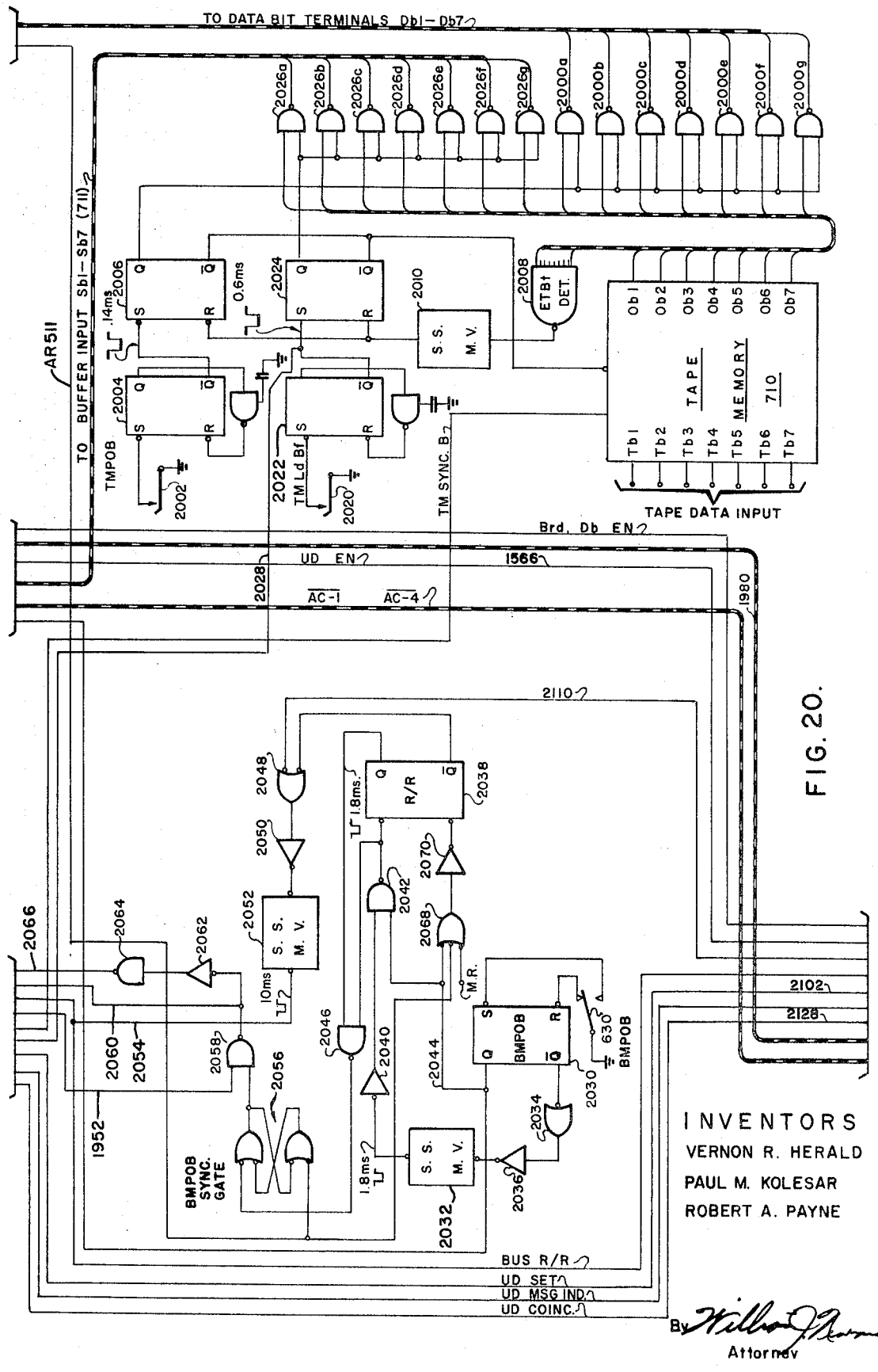



FIG. 20.

INVENTORS
VERNON R. HERALD
PAUL M. KOLESAR
ROBERT A. PAYNE

By William J. Thomas
Attorney

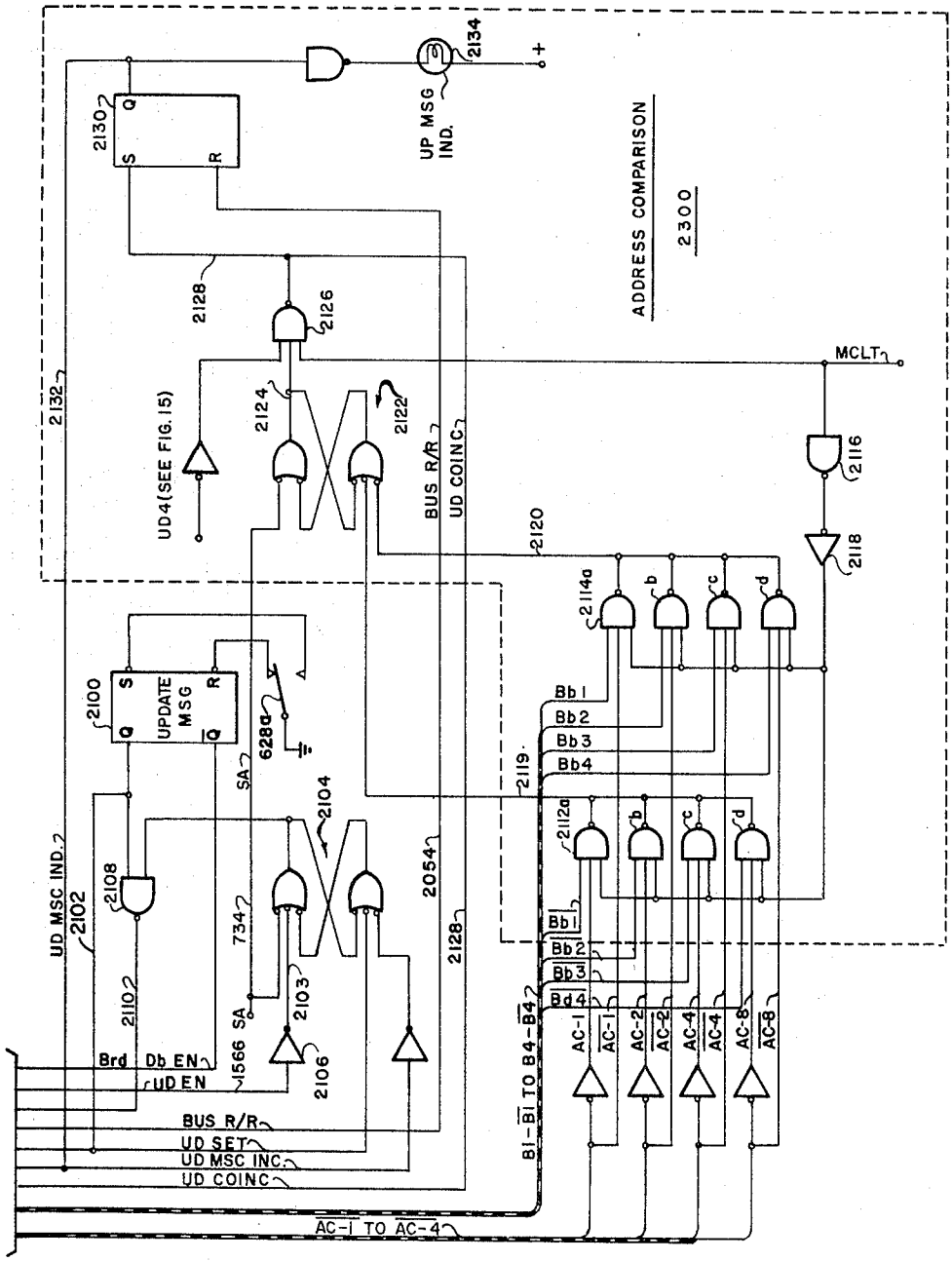



FIG. 21.

INVENTORS
VERNON R. HERALD
PAUL M. KOLESAR
ROBERT A. PAYNE

By William J. Kenyon
Attorney

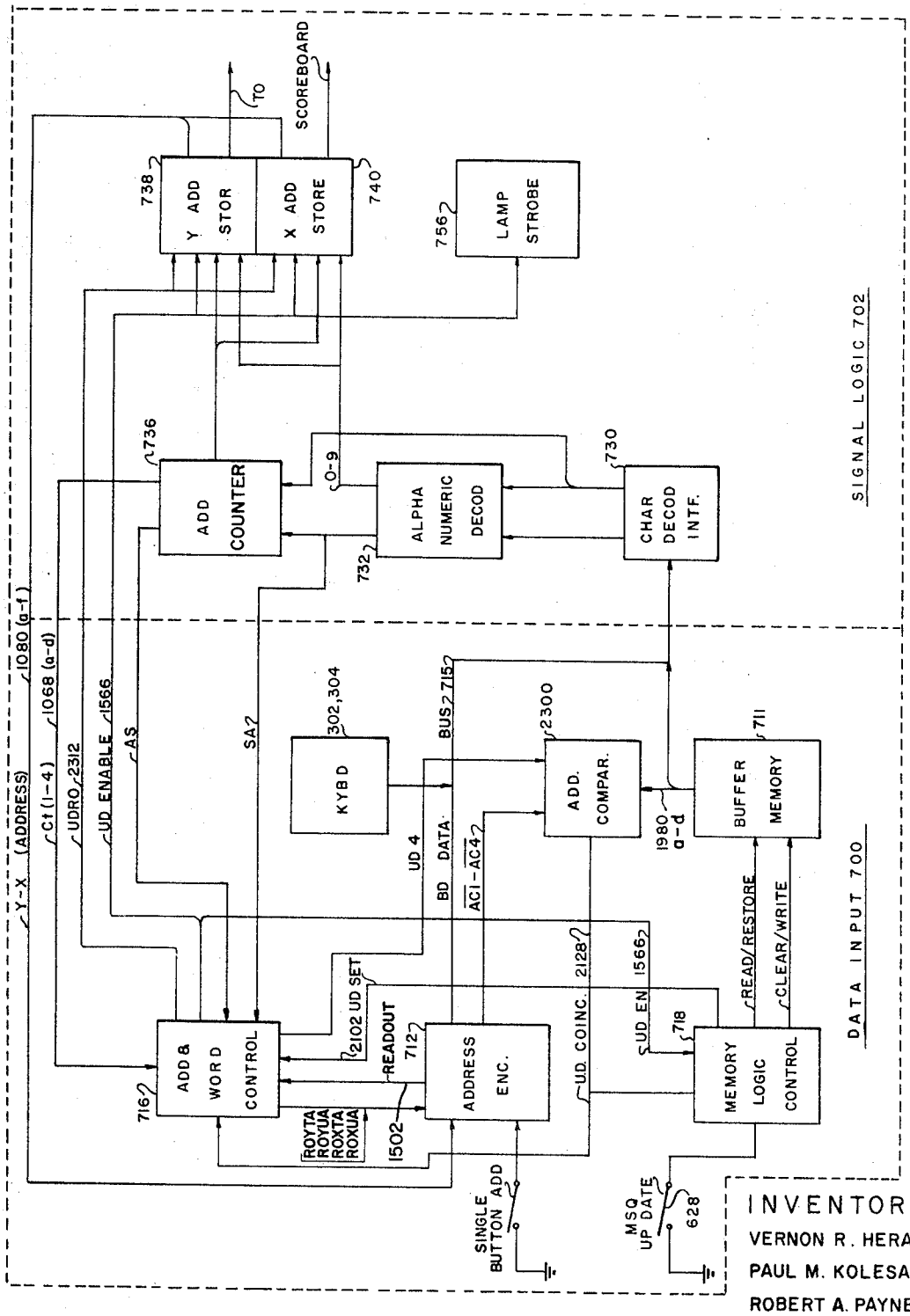



FIG. 23.

INVENTORS
VERNON R. HERALD
PAUL M. KOLESAR
ROBERT A. PAYNE

By William J. Kenyon
Attorney

# DISPLAY SYSTEM

## BACKGROUND OF INVENTION

The system herein described and claimed is a digital controlled, all electronic, semiconductor system having highly flexible input and display output capabilities operable at very high speeds. It is capable of addressing and reading in display data to any location on the display board without having to switch through a number of other locations and without disturbing the data at any other location. That is, any display device or indicator at the display board may be reached and caused to display a desired character merely by inserting the proper address data followed by the desired character data. The address data enables the desired indicator at the desired location on the board and the display data triggers that indicator to operate in accordance with the desired character. Any other desired display device or indicator may then be addressed and triggered, or, in the case of message information display, the next sequenced indicator may be automatically addressed to display the desired character. Hence, the system has full flexibility to provide an almost unlimited array of visual arrangements.

The system has the capability of being served by a variety of different types of input devices. Through the use of a sequentially operated buffer memory and unique control circuits therefor, information may be read in at any speed from a typewriter-type keyboard, a punch tape reader, magnetic tape or drum storage etc., and read out to the display board at a uniform fast rate.

In addition provisions are made for the convenient change of any data in a message to be displayed on the board. For example, during a baseball game it is desirable to display up-to-date information regarding ballgames being played by other baseball team such as the inning of play, score, battery, and first game score if a doubleheader is being played. Since one or more segments of this information changes frequently during the course of a game, it is desirable to change only the required information segments without having to reprogram the whole message each time the message is displayed.

The present system provides apparatus for updating display data previously read into the buffer memory including means for encoding the address data of the display device to be changed and means for comparing the encoded address with the address data in each data segment in the buffer memory to locate the data segment to be updated. Means including the keyboard are also included to erase the display data in the data segment and enter the updating display data.

It is therefore an object of this invention to provide a new display system for informational message display.

It is also an object of this invention to provide a display system having flexible data input means including a variety of different data input devices.

Another object of this invention is to provide a display system having facilities to update selected portions of stored messages.

Further, it is an object of this invention to provide a display system including a buffer memory input which controls the speed of data input to the message board controls from a variety of input devices and forms a part of the apparatus for updating previously programmed message data.

Other objects and features will become apparent with a further reading of this specification making special reference to the accompanying drawings in which:

FIG. **1** is an elevation view of a display board of the type to be used in an athletic stadium for the display of game statistics and message information;

FIG. **2** is an elevation view of an auxiliary scoreboard;

FIG. **3** is a plan view of a portion of the operator control console for operating the scoreboards of FIGS. **1** and **2**;

FIG. **4** is an elevation view of an indicator of the type used in the scoreboards of FIGS. **1** and **2**;

FIG. **5** depicts alpha-numeric and punctuation characters of the type which may be displayed on the indicator of FIG. **4**;



FIG. **5***a* depicts special characters which may be displayed on the indicator of FIG. **4** for shaping pictures and/or designs on the message portion of the scoreboard of FIG. **1**;

FIGS. **6** and **6***a* are plan views of other portions of the operator console for operating the scoreboards;

FIG. **7** is a block diagram of the display control system of this invention;

FIG. **8** is a schematic diagram of a control circuit for each individual indicator;

FIG. **9** is a table of modified ASCII coded representations for the display characters shown in FIGS. **5** and **5***a*; and

FIGS. **10** through **21** are schematic diagrams of the control system to be arranged in the manner shown in FIG. **22**;

FIG. **23** is a block diagram of the circuits utilized in performing the update function.

Although the features of this invention pertain to any type of display system, they will be herein described with reference to a scoreboard system which embodies all of the claimed features. The scoreboard hereinafter described is essentially of the type now being used in the Anaheim Stadium at Anaheim, Calif. In the description to follow, the reference numbers used will be coded by means of the 100's and 1000's digits to the particular figure in which the component or element first appears and that component or element will retain that number in any subsequent figure in which it appears. Thus, an element with the number 246 would be found in FIG. **2** whereas an element with number 1216 would be found in FIG. **12**. Conductors extending between one or more figures will be numbered in accordance with the first figure to which they are referenced in the description.

## GENERAL DESCRIPTION OF SCOREBOARD AND CONSOLE (FIGS. 1, 2 & 3)

The scoreboard display portion of the system comprises a main scoreboard **100** (FIG. **1**) made up of a plurality of display devices or indicators **102** which may register alpha-numeric characters or other designs if desired as will be described hereinafter. If the main board is located in the park so that certain portions of the spectators cannot view it, one or more auxiliary scoreboards **200** (FIG. **2**) may be located at appropriate locations. The auxiliary scoreboard **200** is also made up of display indicators **102** of essentially the same type utilized in the main board. The main scoreboard **100** is divided into two basic sections, namely, the game in progress section **104** and the message portion **106**, while the auxiliary scoreboard **200** is devoted strictly to the game in progress information.

As shown in FIG. **1** the scoreboard display panel is arranged in rows (**Y01** through **Y15**) and columns (**X01** through **X28**) of indicators for the purpose of exact addressing of any desired indicator. Thus, any indicator on the display panel **100** may be referred to by stating its address in terms of its Y number and its X number. In the system described the first row of the message section **106** is designated **Y01** and the message portion continues through row **Y10** while the game in progress portion includes rows **Y11** through **Y15**. Thus, the indicator **105**, upon which the letter A in the word AMERICAN is portrayed, has the location address **Y01–X11**, whereas the indicator **107** displaying the letter G in the word ANGELS is located by the address **Y15–X03**. In the system described each Y and X address number must consist of two digits to satisfy the system logic as will be seen later. Hence, address numbers under 10 must be preceded by a zero, e.g. 01, 02 etc.

Any indicator on the board except certain fixed caption indicators in the game in progress section **104** may be reached to display a desired character by reading into the control system the proper address for that indicator. This is accomplished, for example, by the use of the numeric keyboard **302**, forming a part of the operators console **300** shown in FIG. **3**. Thus, indicator **105** may be reached to display the letter A by first punching the key marked SPEC. ADD. (Special Address) followed by the number 01 for the Y address, which is in turn

followed by the number 11 for the X address. The subsequent actuation of the A key in the typewriterlike alpha keyboard **304** will then cause the latter A to be displayed on addressed indicator **105**. The following indicators are then automatically sequentially addressed so that the operator needs merely to punch the alpha keys M, E, R, I, C, A and N to display the whole word AMERICAN.

If the message is longer than the row, then further message display is impeded until the carriage return key **305** is actuated to cause the automatic addressing of the first indicator in the next row. The message may then be continued until the last indicator in the last row of the message section (Y10–X28) is reached. Further automatic advancing of the address is then prevented because the next numbered indicator row Y11 is in the game in progress section **104**. Thus, the indicators in the Game in Progress Section cannot be inadvertently affected, when writing in a message on the Message Section **106**.

As previously mentioned, the game in progress section **104** of the main scoreboard **100** as well as the auxiliary scoreboard **200** are devoted to information pertaining to the particular game being played. The top two rows of indicator Y11 and Y12 are used for the display of play by play information while the next three rows Y13 through Y15 are used for the inning by inning or line score information as well as the game totals. This section of the board is controlled by the upper portion **305** of the operators console shown in FIG. 3. The indicators in the top row Y11 displaying the words BALL, STRIKE, OUT and BATTER are fixed caption indicators which are actuated by a power switch directly connected to those indicators and are not controlled by the control logic of the system hereinafter described. These indicators might also be arranged to display fixed captions for football games in which case the words DOWN, TO GO, QTR, and BALL ON will be displayed. The indicators in row Y13 displaying the captions R, H, E and 1G are also fixed caption indicators not controllable by the control logic.

To display the desired play by play information the operator manipulates the proper button **306**, **308**, **310** or **312** which automatically addresses the related numeric indicators immediately below the appropriate fixed captions. The numeric information is then read in by means of the numeric keyboard **302**. Thus, the present batter's number is displayed by first operating key **306** which automatically addresses numeric indicator Y12–X21 followed by the player's number inserted from the keyboard **302**. Each ball and strike of the batter is registered by operation of buttons **308** and **310**, followed by the insertion of the numeric data from keyboard **302**. When the next batter comes to bat the previous batter's number and the balls and strikes may be erased by operation of the CLEAR button **314**.

The ball, strike and out data is displayed on the auxiliary scoreboard **200** simultaneously with its display on the main board **100**. The numeric indicators immediately following the fixed captions on the auxiliary board **200** are designated by the same addresses as the corresponding numeric indicators on the main board so that they may be controlled together. Thus, the indicator immediately after the fixed caption indicators spelling BALL on the auxiliary board **200** has the same address, Y12–XO2, as the indicator immediately under the fixed caption indicators spelling BALL on the main board **100**.

The group of indicators **206** are used for displaying various information including the present batter's number. However, since these indicators are used for other information, fixed caption indicators cannot be used and the word BATTER is automatically displayed by means of the control logic. Therefore, when the operator actuates button **306** on the console, the control logic automatically generates the word BATTER and causes it to be displayed on the first six indicators of the group **206**. The insertion of the batter's number automatically causes its display on the last two indicators of the group **206** on the auxiliary board. The addresses for the auxiliary board indicators of group **206** and the word is generated in a manner which will be hereinafter described with respect to the control logic system.

The line score information of rows Y13 through Y15 of the main board is also controlled by means of single button addressing in a manner similar to the play by play information of lines Y11 and Y12. For example the word ANGELS is written onto indicators Y15–X01 through Y15–X06 on the main board **100** by use of the home team button **318** in the team name format portion of the console **300** which automatically addresses indicator Y15–X01. This is followed by the insertion from the alpha character buttons on keyboard **304**, the letters spelling out the name ANGELS. The visiting team name format button **320** is used for the single button addressing of indicator Y14–X01 for writing in the name of the visiting team. Separate auxiliary board team name format buttons **322** and **324** are provided because the names are to be abbreviated in indicator groups **208** and **210** on the auxiliary board **200**. However, if the same number of indicators were provided as in the main scoreboard, the names could be written in simultaneously on the two boards by giving them both the same address.

It is to be noted that the single button means of addressing is in addition to the multibutton addressing previously described for writing in the word AMERICAN, and this capability extends throughout all of the scoreboard so as to give double access to any indicators therein.

The line score statistics may be inserted in rows Y14 and Y15 for the visitor and home teams, respectively by actuation of the appropriate team buttons **326**, **328** followed by the appropriate inning button from inning button group **330** or one of the buttons **332**, **334**, **336** or **338**, which ever is required for the information to be displayed. This addresses the proper indicator in the line score portion of the board and the subsequent input of a numerical character from keyboard **302** will cause the proper display. Thus, to indicate an ANGELS run in the third inning, the operator will press the home team button **328** followed by the third inning button **329** of the line score inning group **330**, followed by the numeric character 1 button on numeric keyboard **302**.

The auxiliary board only displays the total runs of each team on the indicators immediately following the team name groups **208** and **210** and are addressed simultaneously with the runs indicators Y14–X22 and Y15–X22 when the respective team buttons **326**, **328** and the runs button **332** are actuated. A subsequent insertion of the numeric data from keyboard **302** will cause the data to be displayed simultaneously on the two boards. The inning number is entered into the auxiliary board following the fixed caption indicators displaying INN by operation of the AUX INN button **340**, followed by the appropriate number from keyboard **302**. The INN CAP button **342** is used for displaying the inning captions 1 through 0 in row Y13 of the main board **100**.

The fact feature controls on the console, including buttons **344**, **346**, **348** and **350**, are used for displaying pertinent facts about a particular play in the nine indicators in rows Y11 and Y12 at the upper right-hand corner of the main board **100** and in the group of indicators **206** on the auxiliary board **200**. The FACT F. button **346** is a one button address selector for the group of four indicators **108** in row Y11 and is used for writing any desired two, three or four-letter word thereon. It also addresses the first four indicators in the group **206** on auxiliary board **200**. Thus, if it is desired to display the rule book number pertaining to a particular play, the operator presses the FACT F. button **346** and writes in the word RULE from the alpha keyboard **304**. The INFO button **350** is then pressed which addresses the first indicator in group **110** and the rule book number is entered into the indicators **110** from the numeric keyboard **302**. This information is also displayed on the auxiliary board group **206**.

The play button **348** automatically displays the word PLAY on the indicators of group **108** of the main board and also on the first four indicators of the group **206** on the auxiliary

board. The indicator group 110 and the last five indicators of group 206 are then automatically addressed for insertion of the desired information. Thus, if the shortstop commits an error, the operator would press the play button 348 to display the word PLAY on the proper indicators and immediately enter the display data E6 from the keyboards 304, 302 to designate an error by the shortstop.

The erase function buttons 352, 358 and 360 perform the obvious function of extinguishing the bulbs in particular indicators on the scoreboards. The EGIP button 352, which stands for Erase Game In Progress, serves to erase all of the information displayed in the section 104 of the main scoreboard as well as the information on the auxiliary scoreboard, except for the fixed caption indicators. The EMSG button 358 provides for the erasure of all the information in the 10 rows forming the message section 106 of the message board. The group of button 360 provide for the erasure of a selected row in the message portion 106 of the scoreboard and that row is erased merely be depressing the particular button corresponding to the row desired to the erased.

FIGS. 6 and 6*a* show additional console buttons for controlling the input and flow of data in the display system. The group of buttons 600 control the flow of data between the keyboards, the scoreboard, the buffer memory and the tape memory in a manner which will be described in detail in the description of the circuit diagrams of FIGS. 10 through 21.

The group of buttons 602 are single button address types which aid in displaying the out-of-town game format in the message portion 106 of the scoreboard as shown in FIG. 1. The word AMERICAN is written into row Y01 in the manner previously described and the inning captions are inserted in row Y02 in a similar manner. The actual data pertaining to the out-of-town games is easily inserted in lines Y03 to Y10 by means of single button addressing in the following manner. The Baltimore-New York game is first programmed by actuating the left button 604, the line 3 button 606 and the inning button 608. The actuation of these three will develop the address Y03–X01 for selecting indicator 115 at which the number 8 for the 8th inning is to be displayed. Actuation of the right button 610 along with the line 3 button 606 and inning button 608 will cause the automatic selection of indicator Y03–X16 for the game displayed on the right-hand side of the format. The digit 6 for display on indicator Y03—X16 is inserted by means of the numeric keyboard 302 as previously described. Likewise, the team name, number of runs, pitcher's number and first game score information is inserted by means of the buttons 612, 614, 616 and 618, respectively, with the proper row being selected by the line buttons 606, 606*g*. The proper side of the board is selected by means of the left and right buttons 604, 610 and the display data is written in by the alpha and numeric keyboards 302, 304.

It is not desirable to maintain the out-of-town information displayed on the message portion 106 of the scoreboard constantly throughout the game because of the need to display courtesy notes, advertising, crowd handling instructions, songs, etc. at different times during the game. Therefore, provisions are made for maintaining the out-of-town information in a storage memory from which it may be read out and displayed on the board whenever desired. To accomplish this the data is read into a buffer memory (to be described later) instead of going directly to the display board. From the buffer it may be written out to the board or into a permanent storage device such as a magnetic tape memory (also to be described later) or a punch tape typewriter.

To program and store the out-of-town game format the buffer memory keyboard input (BMKI) button 620 is actuated before writing in the out-of-town game information with the group of buttons 602 and keys 302, 304. After the data has been inserted into the buffer memory, it is transferred into the magnetic tape memory by depressing the tape memory unload buffer button 622. The message is then permanently stored on the magnetic tape for use at any time. Messages are stored at particular address locations on the tape and retrieved for subsequent use in any well-known manner which does not form a part of this invention. If desired, the stored data may be posted directly onto the message portion of the scoreboard from the tape by depressing the tape memory post on board button 624 after selecting the desired message on the tape by any well-known means. Otherwise the information may be read from the tape into the buffer for subsequent readout to the board by use of the tape memory load-to-buffer switch 626.

The out-of-town game information of course changes during the course of the afternoon or evening, and it is therefore desirable to provide means for updating the information where required without having to reprogram the whole message. This can be accomplished in the present system by reading the message stored on tape back into the buffer memory through the actuation of the tape memory load-to-buffer switch 626 and correcting the information while the message is in the buffer memory.

The address of the indicator to be updated is read into the system logic either by one of the single addressing buttons or by the numerical keyboard 302 after which the update message button 628 is actuated to cause the inserted address to be sequentially compared with each of the addresses stored in the message buffer memory. When the address is found, a light (not shown) in the data message button 628 goes on indicating that address has been found and the update data may be read in from the proper keyboard 302, 304. The updated message in the buffer then may be transferred directly to the scoreboard by actuation of the buffer memory post-on-board (BMPOB) switch 630 and/or returned to the tape memory by means of the tape memory unload buffer switch 622.

The button 632 provides for the input of data from a punched tape typewriter and reader to the buffer memory while the button 634 enables reading of the buffer memory data back to the tape typewriter and reader in order to check the data contents of the buffer. The buffer memory clear button 636 is merely a mechanical interlock with the other buffer memory switches and enables the operator to release any of the other buffer memory switches after the function has been performed. The tape memory clear switch 636 performs the same function for the tape memory function buttons.

The button 640 provides for the direct reading to the scoreboard from the buttons and keys on the console 300, while the button 642 provides for the direct reading to the scoreboard from the tape typewriter and reader.

The manner in which the manipulation of the various buttons in the group 600 perform their indicated functions will be described in later sections of the specification relating to the control logic of the system.

## DISPLAY CHARACTERS (FIGS. 4 and 5)

The display devices or indicators 102 utilized in the display system herein described are individual modules, each comprising a matrix of 35 lamps 400 arranged in seven rows (LR–1 through LR–7) and five columns (LC–1 through LC–5) as indicated in FIG. 4. The different characters are formed by illumination of the lamps in the desired pattern. FIG. 5 shows the standard alpha, numeric and punctuation displays as they would be formed on a 35-lamp matrix.

A large variety of other display characters may also be formed by the lamp matrix indicators 102 which can be used in forming pictures, designs or animated displays on the message portion 106 of the scoreboard. FIG. 5*a* shows a number of different display characters which may be programmed for use in this manner.

It is to be understood that other indicator configurations might be utilized without departing from the teachings of this invention. For example, the lamps 400 need not necessarily be arranged in 5×7 matrices, but may be arranged in any convenient manner with any number of lamps. Also, it may be desireable to use other visually observable elements than lamps depending upon the use of the board. Whereas light bulbs mounted in a board having a black surface is preferred

for out door display systems where a wide range of ambient light conditions call for the use of transmitted light, indoor locations may call for other visually observable elements. For example, if the board is located in a constant high illumination ambient area, it may be desireable to utilize reflective members such as white painted discs or the like instead of lamps **400**.

In additions, for certain aspects of this invention it may be desirable to use other types of visual displays than the matrix-type indicators. Some message board applications might call for alpha-numeric wheels or belts or any of the other well-known types of alpha-numeric character displays and where applicable the use of such are contemplated.

## GENERAL DESCRIPTION OF CONTROL SYSTEM (FIG. 7)

The control system as shown in the block diagram of FIG. **7** comprises data input means **700** and signal logic means **702**, as well as the address decoder means **704** and the indicator circuits **706** (one for each indicator **102**).

The data input means **700** which is controllable by the operator, provides data in the form of a modified ASCII digital code such as shown in the table of FIG. **9** to the signal logic **702** which then transforms it into appropriate signals for transmission over cables to the scoreboards. There the signals enable the desired indicators and actuate the appropriate lamps in the selected indicators to display any of the characters in FIGS. **5** and **5***a*. The address data is generated in the data input **700** in binary coded decimal form utilizing the ASCII code while the display data is in ordinary binary form using the ASCII code. The data is presented to the signal logic by the alpha-numeric keyboards **304**, **302** previously mentioned, by punch tape typewriter and reader **708**, and by storage devices such as a magnetic tape memory **710** and buffer memory **711**. Also, address and display data for certain words (e.g. BATTER or PLAY) can be automatically encoded into the modified ASCII code for serial transmission to the signal logic **702** by means of the address and word control circuit **716**, address encoder **712** and word generator **714** in a manner to be described in more detail hereinafter.

The flow of data between the various input devices **302**, **304**, **306**, **708**, **710**, **711** and **712**, as well as the flow of data through the board data bus **715** to the signal logic, is controlled by a memory control logic circuit **718**. The memory control logic **718** performs the functions of the buttons in console group **600** (FIG. **6**) as indicated by the corresponding reference numbers of the switches shown in the memory control logic box **718** in FIG. **7**. The showing of these function buttons as switches in FIG. **7** is symbolic only and the circuits for performing the various functions will be discussed in detail with respect to the detailed schematic drawings of FIGS. **10** through **21**.

The signal logic **702** provides the control function by which the proper indicators on the scoreboard **100** are addressed and actuated to display the desired character in accordance with the address and character display data received from the data input **700**. The seven bit ASCII code signals are received from the data input **700** by the character decoder interface **730** in the signal logic. The alpha-numeric decoder **732** then transforms the ASCII code signals into a single conductor signal on one of the 72 output conductors, each of which is representative of one of the display characters in FIGS. **5** and **5***a* or on a special instruction conductor such as the Special Address or Carriage Return.

As previously described, address data is always immediately preceded by a special address character which indicates to the signal logic that the immediately following two digits represent the Y, or row address, while the third and fourth digits indicate the column, or X address. The alpha-numeric decode **732** recognizes the special address character and sends a signal over conductor **734** to start the operation of the address digit counter **736**. The four address digits for the Y and X addresses are then received and stored in their respective address storage circuits **738** and **740** respectively. After the four address digits have been stored, the address counter **736** sends a signal over conductor **742** to the lamp strobe circuit **750** which enables the read out of the character display data when it is received in the lamp encoder circuit **754**.

The character display data is received by the character decoder interface **730** and the alpha-numeric decoder **732** which furnishes a signal pulse on one of the 72 lines to the lamp encoder **754**. If the lamp encoder **754** recognizes it as a legitimate character display signal which is able to be displayed by an indicator lamp matrix, a Legit signal is provided over line **756** to the lamp strober **750**.

The receipt of the Address Stored signal and the Legit signal cause the lamp strober **750** to operate to read the address data from the Y and X address storage circuits **738**, **740**, in parallel fashion over their respective multiline conductors **758**, **760** and cables **761**, **763** to the Y and X address decoders **762**, **764** at the scoreboards **100** and **200**.

The parallel received signals at the Y and X address decoders **762** and **764** are transformed into a simultaneous single signal on one of the 15 output lines of the Y address decoder and one of the 28 output lines of the X address decoder. Each of the 15 lines of the Y address decoder is connected to a respective row of indicators **Y01** through **Y15** whereas each of the 28 output lines of the X address decoder **764** is connected to a respective column of indicators **X01** through **X28**. Thus, each indicator **102** is connected to one line from the Y address decoder **762** and one line from the X address decoder **764** and when the particular indicator receives simultaneous signals from both it is enabled to receive the immediately following character display data to actuate its lamps **400** in accordance with the character to be displayed.

Immediately after the Y and X address data has been read out of the storage devices **738**, **740** the lamp strobe **750** signals the lamp encoder **754** to transmit signals in accordance with the character display data over its output data conductors **768** and strobe conductors **770** through the respective cables **772**, **774** to the particular preaddressed indicator circuit **706** at the scoreboard.

The lamp encoder data output and cable **774** are 7-line conductors each of which is connected to enable a respective row of lamps in the 5×7 lamp matrix indicators. The strobe output and cable **776** are 5-line conductors each of which is connected to enable a respective column of lamps in the 5×7 lamp matrix indicators. The five strobe conductors transmit five consecutive pulse signals, one on each line, which are delivered successively to the five lamp columns in sequential order from the left-hand column to the right-hand column of each lamp matrix indicator. The simultaneous receipt of lamp data signals over one or more of the seven data lines connected to the rows of indicator lamps in coincidence with the lamp column strobe signals causes the appropriate lamps in each column to be actuated in accordance with the particular character to be displayed.

Referring back to FIG. **4** for a more precise description of the lamp data and strobe signal operation of the indicator lamps **400**, it will be noted that each of the rows of lamps are marked respectively **LR1** through **LR7** whereas each of the columns are marked **LC1** through **LC5**. Each of the lamps in rows **LR1** through **LR7** connected to be enabled by a signal on the corresponding one of the seven data lines from the lamp encoder **754** while the five columns of LAMPS LC1 through LC5 are connected to be actuated by lamps pulse on a respective one of the five strobe lines from the lamp encoder **754**. Thus, to form the letter T as shown on the indicator **102** in FIG. **4**, the first pulse **LC1** on the first of the five strobe lines from the lamp encoder will correspond with a simultaneous signal on the first data line which corresponds to the lamp row or **LR1** row of indicator lamps. Thus, lamp **402** is lit with the first strobe pulse. The second strobe pulse on the second strobe line of the 5-line strobe output of lamp encoder **754** is

received simultaneously at the indicator 102 with another LR1 signal on the first lamp data line of the 7-line data output from the lamp encoder. Thus, lamp 404 is lit on the second or LC2 pulse. The LC3 strobe pulse on the third of the five strobe lines from the lamp encoder is received simultaneously with pulses on each one of the seven lamp data lines from the lamp encoder so that all seven of the lamps 406 through 406*f* are lit on the third or LC3 strobe pulse. Likewise, lamps 408 and 410 are lit on strobe pulses LC4 and LC5, respectively, to complete the letter T on the lamp indicator 102. Means are provided in the indicator circuit 706 for each indicator 102 for maintaining the actuated lamps lit until a reset signal is received by the indicator circuit 706 to turn out all energized lamps in a manner to be hereinafter described.

## INDICATOR CIRCUIT (FIG. 8)

Reference is now made to FIG. 8 showing in schematic form an indicator circuit 706 which is used to control the lamps in each indicator 102 for the display of a desired character. The indicator circuit 706 includes 35 lamp switch circuits such as 800 and 800*a*, one for each lamp in the 5×7 matrix in the indicator. As will be seen switches 800 and 800*a* control lamps 404, 404*a* in matrix positions LR1–LC2 and LR2–LC2 respectively. There is also a lamp on-ready circuit 802 for preparing the circuit responsive to the receipt of the indicator address data corresponding to the particular indicator, and a lamp reset circuit 804 for turning off any previously lit lamps in the indicator responsive to the receipt of the particular indicator address data.

The energizing circuit for each of the lamps in the indicator extends from a 120 volt DC source 806 through the respective lamps 404, 404*a* and lamp switch silicon controlled rectifiers 808, 808*a* in the respective lamp switch circuits 800, 800*a*. The cathodes of all the lamp switch SCR's 808, 808*a* are connected together and to the anode of a reset SCR 810 in the lamp reset circuit 804, the cathode of which is connected to ground at 812. Thus, any lamp 400, 400*a* may be energized through the actuation of its respective lamp switch SCR 808, 808*a* and the reset SCR 810. All of the lamps may be extinguished or reset by the cutoff of reset SCR 810 in a manner to be hereinafter described.

The Y and X address data is received at terminals 814 in the form of simultaneously appearing positive going pulses. The X address pulse is 50 microseconds long and the Y address pulse is substantially longer being governed by the speed of data input as will become apparent hereinafter.

The Y and X address pulses are ANDed at the input 815 to a Schmidt monostable multivibrator circuit 816 in the lamp on-ready circuit 802 and, by means of conductors 817 and resistors 819, at the input 824 to another Schmidt monostable multivibrator circuit 818 in the lamp reset circuit 804. The Schmidt circuit 818 in the lamp reset circuit 804 has a short hysteresis curve so that its duty cycle is governed by the short X address data signal. Transistor 820 is normally conducting but transistor 822 goes into conduction upon receipt of the Y and X address signals at the input circuit 824 to the base of transistor 822. The conduction of transistor 822 causes 820 to cut off, and the positive pulse at the collector thereof is fed to the base of emitter follower transistor 826. The positive pulse across emitter resistor 828 pulses emitter follower transistor 830 into conduction, and the positive pulse across its emitter resistor 832 is transmitted through capacitor 834 to the base of transistor 836. The emitter-collector circuit of transistor 836 thus provides an effective shunt across reset SCR 810 from the grounded cathode 812 of the reset SCR 810 through capacitor 838, negative 13-volt conductor 840, the emitter-collector circuit of transistor 836, and conductor 842 to the anode of SCR 810. Thus, conduction of transistor 836 places −13 volts from the charged capacitor 838 directly across the reset SCR 810 to cut it off and open the energizing circuits to any previously lit lamps 400, 400*a*. After the 50 microsecond X address pulse the Schmidt circuit 818 restores to normal cutting off transistor 836 to remove the shunt from across the reset SCR 810. The reset SCR 810 will of course not conduct again until a positive signal is received on its gate 844.

The lamp on-ready circuit 802 operates responsive to the receipt of the Y and X address pulses to prepare the lamp switch circuits 800 and also to reactivate reset SCR 810 in the following manner. The two address signals are ANDed at the input 815 of the Schmidt multivibrator circuit 816 which in contrast to the Schmidt circuit 818 in the lamp reset circuit 804 has a long duty cycle of at least 450 microseconds. Thus, it will not follow the 50 microsecond X address pulse as does the lamp reset multivibrator 818. The normally off transistor 846 is triggered into conduction by the ANDed address pulses causing transistor 848 to cut off. The positive going signal at the collector of transistor 848 triggers emitter follower transistor 850 into conduction and the positive pulse across its emitter resistor 852 appears at the base of transistor 854. Positive 30 volts is thus placed on the anode of a triggering SCR 856 from the +30 volt conductor 858 through the collector to emitter circuit of transistor 854 and conductor 860. The cathode of SCR 856 is connected through conductor 862 and resistor 864 to the gate 844 of reset SCR 810 so that when SCR 856 goes into conduction it triggers the reset SCR into conduction. The gate 870 of SCR 856 is connected through resistor 872 to the first indicator lamp strobe signal (LC1) line 874 so that it is triggered into conduction at the initiation of data character input signals to the indicator after the indicator has been addressed.

The triggering SCR 856 also functions to enable each of the 35 lamp switch circuits 800 in the indicator. It does so by placing a positive signal to the respective gate circuits 868, 868*a* in each of the lamp switch circuits 800, 800*a* through resistors 869, 869*a* when it goes into conduction. The positive signal from the triggering SCR 856 to the lamp SCR gate circuits does not throw these SCRs into conduction unless and until positive signals are simultaneously received on the cathodes of both diodes 876, 878, 876*a*, 878*a* in each lamp switch circuit 800, 800*a*.

As will be seen in the later description of the lamp encoder circuit 754 the strobe signals and data signals provided therefrom to the scoreboard indicator circuits 706 are normally at negative potential and rise to positive potential to signify character display data. Thus if the character display data requires that lamp 404 be lit as in the letter T shown in FIG. 4, the diodes 876, 878 will receive simultaneous positive signals from the LR1 and LC2 inputs. Junction 867 goes high and the triggering SCR 856 supplies positive current to the gate 880 of the lamp switch SCR 806 causing it to conduct and complete the circuit for the lamp 404. The letter T does not call for lamp 404*a* to be lit so that while an LC2 signal will be received at diode 876*a* in the LR2–LC2 lamp switch circuit 800*a*, negative voltage remains at diode 878*a* and no current is delivered to the SCR gate 880*a*.

Once a lamp switch SCR 808 is triggered into conduction it remains conducting to keep the lamp lit until a subsequent receipt of address data indicates the selection again of that particular indicator which causes reset SCR 810 to be cut off in the manner previously described and in turn the lamp switch SCR's including SCR 808.

## ADDRESS-CHARACTER SIGNAL LOGIC (FIGS. 10—22)

### Address Data Storage

This section describes the basic address and character data handling circuits of the signal logic 702 between the data input 700 and the scoreboard 100. This discussion will be best understood with reference to FIGS. 10 through 21 arranged in the format indicated in FIG. 22.

All of the address and character display data from the data input 700 is received at the data bus terminals *db*1 through *db*7 (FIG. 12) at the character decoder interface 730 from the data bus 715. The various code producing devices in the Data

Input **700** deliver signals to the terminals *db***1** through *db***7** such that a low or ground signal represents the presence of a data bit and a high represents its absence. The signal at the output of each of the NOR gates **1200***a* through *g* in the character decoder interface therefore represents the data bits **1** through **7** of the modified ASCII code shown in the chart of FIG. **9**. The code is thus presented to the alpha-numeric decoder **732** in the form of high and low signals corresponding, respectively, to the 1's and 0's in the table of FIG. **9**.

Conductors **1202***a* through *g* provide a straight pass through of the data bit **1** through **7** signals and negators **1204***a* through *g* provide the inverse of the data bit **1** through **7** signals, each of which is connected to appropriate NAND gates **1206** (FIG. **12**) and **1100** (FIG. **11**) in the alpha-numeric decoder **732** corresponding to a particular alpha, numeric, punctuation, or special characters or a special instruction (Special Address or Carriage Return). The alpha decoder NAND gates **1206** shown in FIG. **12**, and the numeric decoder NAND gates **1100**, shown in FIG. **11**, are all essentially the same (thus only representative gates are shown), and all of the gates are connected to the character decoder interface **730** so that each will present an output pulse when the ASCII code for its particular character is received. As an example, the alpha character T is represented by the modified ASCII code (FIG. **9**) 0010101, and the corresponding high and low signals will be presented at the outputs of NOR gates **1200***a* through **1200***g* of the character decoder interface **730**. It will be noted that the T NAND gate **1206**–T receives the negated data bit **1** signal, the negated data bit **2** signal, the straight data bit **3** signal, the negated data bit **4** signal, straight through data bit **4** signal, the negated data bit **6** signal and the straight data bit **7** signal. Thus, it will respond to the character T data, and not to any other data. The special address (SA) NAND gate **1206**–SA, carriage return (CR) NAND gate **1206**–CR, and the numeric decoder NAND gates **1100**–**0** through **9** (FIG. **11**) operate in the same manner to provide single conductor outputs responsive to the respective 7-bit data character input.

As previously described every time it is desired to insert address data into the system to seek a desired indicator, the numerical data pertaining to the Y and X coordinates must be preceded by the special address character (SA). This may be performed by the operator punching the special address button on the numeric keyboard **302** at the console **300** which initiates the code 0101010 at the input to the alpha-numeric decoder **732**. Seven high inputs are presented to the SA NAND gate **1206**–SA to produce a low on the special address conductor **734**.

The SA signal readies the Y and X address storage circuits **738** (FIG. **10**) and **740** (FIG. **11**) for storage of the Y and X address data by presenting a low or ground pulse signal to NOR gate **1000** (FIG. **10**) in the address counter circuit **736**. The high at the output of NOR gate **1000** is inverted by negator **1002**, and the resulting ground on the CLEAR conductors resets a five-count address digit counter **1004** and the Y tens digit storage flip-flop **1006**. The y tens storage device **1006** is a set-reset type flip-flop which performs a storage function by flipping to its Q state (high voltage at Q output) responsive to a ground pulse at its set S input and remains in that state until a ground pulse is applied to its reset R input.

The clear signal is NOR'd at gate **1008** and inverted at **1010**, so that a ground reset signal is also applied to the reset terminals of the four Y units digit storage flip-flops **1012***a* through **1012***d*. These flip-flops are each of the conventional triggered type which is reset to its $\overline{Q}$ state by a ground signal at its reset R terminal and set to its Q state by a ground signal at the set S terminal. Also the circuit may be flipped between its Q and $\overline{Q}$ states responsive to low signals at the trigger input T provided ground does not appear at the R or S inputs.

In addition the clear signal feeds to the X address storage circuit **740** (FIG. **11**) where it similarly resets the X tens and units flip-flops **1100***a* through **1100***f* through NOR gates **1102**, **1104**, **1106** and negators **1108**, **1110** and **1112**. Thus, pressing the SA button resets all of the X and Y storage flip-flops as well as the 5-count address digit counter **1004**.

In addition, the SA ground signal also sets the set-reset type flip-flop **1014** in the address counter circuit **736**, the set or Q output of which goes high responsive to the low SA signal at the set input. The high Q output of flip-flop **1014** is applied to NAND gate **1016** which also has three other inputs as follows: a normally high input on conductor **1018** at the output of negator **1017** which goes low at count 5 of the address digit counter **1004**; a high output from NAND gate **1020** which goes low when a numeral button is pushed as will be hereinafter described; and the SA signal on conductor **734** which is low until the special address button is released. To facilitate this explanation it will be assumed that the keyboard buttons actuate grounding switches directly connected to the data bus terminals *db***1**—*db***7**. The actual keyboard circuits will be described in detail later. Therefore, when the special address button is released all four inputs to the NAND gate **1016** go high and a ground output is applied to the counter **1004**.

The address digit counter **1004** actually counts the number of digits in the address data inserted into the Y and X storages and prepares the logic for receipt of character display data upon completion of the address data input. The counter **1004** is a conventional type made up of three set-reset type flip-flops (not shown) and provides a high signal successively on the output lines **1** through **5** responsive to the first five successive low pulses at its input following its reset. Thus, the first low at the address digit counter input caused by the cessation of the SA signal provides a high pulse to NAND gate **1021** connected to the count 1 output of the counter, and it remains there until the operator punches the first numerical key at keyboard **302** representing the tens digit of the Y address to be stored.

As an example, assume that the desired address is Y09—X25. After punching the SA button the numeral button "0" is pressed to produce seven high inputs to the zero NAND gate **1100**–**0**. The low output on the zero line **1023** from the gate **1100**–**0** is applied to one of the inputs of NOR gate **1022** which acts as a numerical input detector. It is connected to the outputs of each of the numeric NAND gates **1100**–**0** through **1100**–**9** to produce a high signal at its output responsive to the input of any number. The high output from the numeral detector NOR gate **1022** is NANDed with the count **1** signal of the counter **1004** at gate **1021** to cause a set Y tens storage signal through negator **1024** to NAND gate **1026**. The outer input to NAND gate **1026** is through conductor **1028***a* which is connected (not shown) to the output of NOR gate **1200***a*in the character decoder interface. The conductors **1028***a* through **1028***d* carry signals according to the first four bits of the ASCII code with the respective binary weights 1, 2, 4 and 8. These conductors thus provide the address data input to the storage circuits **738** and **740** as will be further shown. Therefore, if the Y address is any one of the numbers 10 to 15 a coincidence will appear at the output of NAND gate **1026** and provide a ground signal to the set terminal of the Y tens storage flip-flop **1006**. The Y tens flip-flop would flip to its Q state placing a high voltage on the YA **10** line **1025** to the Y**10** read out NAND gate **1027***a* signifying tens digits in the Y address. Since the Y address in out example was 09 no pulse appears on **1028***a* and the Y tens storage flip-flop **1006** is not set

When the operator released the zero keyboard button at the console the input to NAND gate **1020** from the numeral detector NOR gate **1022** goes low to provide a high to the counter input NAND gate **1016**. Since the special address conductor is high, the set output of the special address flip-flop **1014** is still high, and the count **5** conductor **1018** is high, the gate **1016** is satisfied and produces a ground signal to the counter **1004**. The counter then advances to its count **2** state to send an enabling signal to NAND gate **1030** in readiment for storage of the Y units digit.

The operator next presses the keyboard button "9" and the alpha-numeric decoder **732** sends a low signal which is NOR'd in gate **1022** causing gate **1020** to inhibit the counter input gate **1016**. The high output of gate **1022** is NANDed at gate **1030** with the count **2** output signal of counter **1004** and the low therefrom is inverted by negator **1032**. The high at the

output of negator **1032** is applied to the Y units bits NAND gates **1034***a* through *d* which have their other inputs connected to separate ones of the *b*1 through *b*4 data bit lines **1028***a* through *d*. Since the units digit of the Y address is the numeral 9, highs will appear on the *b*1 and *b*4 bit lines **1028***a* and **1028***d* to NAND gates **1034***a* and **1034***d* and the ground pulses therefrom will set the Y unit flip-flop **1012***a* (having binary weight 1) and flip-flop **1012***d* (having binary weight 8). The Q outputs of Y units storage flip-flops **1012***a* through **1012***d* are connected via conductors **1029***a* through **1029***d* to the binary weighted readout NAND gates **1027***b* through **1027***e*, respectively. For the number 9 in the example address Y09—X25 NAND gates **1027***b* and **1027***e* will have high inputs at one of their inputs. A readout signal will later appear at the second input as will be hereinafter described. It is to be noted that the bit 5 through bit 7 data channels are not used for storing the address number because, as may be seen, in the code chart of FIG. 9 they are not required to distinguish the numerals 0 through 9.

When the operator releases the 9 keyboard button, the counter input gate **1016** delivers a low to the counter **1004** to step it to its count 3 condition enabling the set X tens digit NAND gate **1036**. The operator presses the keyboard button for the number two representing the tens digit of the X address **25** causing numeral detector NOR gate **1022** to open the set X tens digit NAND gate **1036**. The high from negator **1038** is presented to the NAND gates **1114***a*, **1114***b* at the set inputs to the X tens digits storage flip-flops **1100***e*, **1100***f* in the X storage circuit **740** (FIG. **11**). Since the number **2** has been pressed a high appears on the conductor **1028***b* (FIG. **10**) to the NAND gate **1114***b*, thus setting the **X20** storage flip-flop **1100***f*. A high signal is thus delivered to one input of the **X20** read out NAND gate **1115***a* over conductor **1117**. If the X address had been a number 10 through 19 the bit **1** conductor **1028***a* would have carried a high to satisfy the NAND gate **1114***a* and set the **X10** flip-flop **1100***e*. Likewise, if the X address had been between 1 and 9 neither the **X10** nor the **X20** flip-flops would have been set.

Release of the keyboard numeral **2** button by the operator advances the counter **1004** to its step count **4** condition to prepare for storage of the X address units digit in the X units digit flip-flops **1100***a* through **1100***d*. Depression by the operator of the digit 5 for the units digit of the example X address **25** produces high outputs on the binary weight 1 line **1028***a* and the binary weight 4 line **1028***c*. These are each NANDed with the set X unit signal at NAND gates **1116***a* and **1116***c* to set the X1 and X4 flip-flops **1100***a*, **1100***c* and send high signals to the first inputs of X units read out NAND gates **1115***c* and **1115***e* via lines **1119** and **1121**.

Release of the numeral **5** keyboard button steps the counter **1004** to its count **5** condition which closes the counter input gate **1016** by placing a ground on the conductor **1018**. The address digit counter is thus inhibited from further pulsing until it receives a subsequent reset signal. The count **5** output of the counter also causes the SA flip-flop **1014** to be reset by means of NOR gate **1042** and negator **1044**.

The count **5** output of the counter **1004** also produces the addressed stored signal (AS) at the output of negator **1048** which is fed by the negator **1017**. The addressed stored (AS) signal is transmitted via conductor **742** to the lamp strober **750** (FIG. **12**) indicating that the full address has been stored. The signal logic is thus set to receive the character display data for actuating the desired lamps in the addressed indicator.

### Display Character Lamp Encoding

To display the desired character after addressing the proper indicator, the operator presses one of the alpha or numeric buttons on the respective keyboards **302**, **304** which causes the proper signals to appear at the data bit **1** through data bit **7** terminals at the character decoder interface **730**. The alphanumeric decoder **732** produces a single line output from the proper NAND gate in the series **1206** or **1100** in the manner previously described, and the single line output signal is presented to the lamp encoder **754** shown in detail in FIG. **13**.

The lamp encoder **754** comprises a matrix of 35 NAND gates **1300***a* through *g*, **1301***a* through *g*, **1302***a* through *g*, **1303***a* through *g*, and **1304***a* through *g*. The matrix corresponds to the 5×7 matrix of lamps **400** in the indicators **102** so that each NAND gate is associated with a particular lamp position in the indicator matrix. The NAND gates in the column marked **1300** correspond to the lamps in column LC—1 of the indicator and similarly the column **1301** corresponds to the column LC–2 etc. Likewise, the NAND gates in the a row correspond to the lamps in lamp row LR—1 of the indicator matrix, those in row *b* correspond to lamp row LR–2, etc.

To describe the detailed operation of the lamp encoder **754** it will be assumed that the alpha character T is desired to be displayed on the previously addressed indicator Y09—X25. The code table of FIG. 9 shows that the code for the letter T is 0010101 and this code will open the gate **1206** T to produce a low signal on conductor **1208**.

The signal on the "T" conductor **1208** is applied through appropriate NOR gates **1306** to NAND gate **1300***a* in the first column of gates, to NAND gate **1301***a* in the second column, to gates **1302***a* through g in the third column, to gate **1303***a* in the fourth column, and to gate **1304***a* in the fifth column which as may be seen by the shading of these NAND gates forms a letter T. The high signals at the first inputs to the selected NAND gates remain as long as the data signal from the data input lasts. During this time the address data is strobed out of the address data storages followed by the strobing of the display data from the encoder NAND gates, one column at a time in a manner described in the nest section of this specification.

In a similar manner any other of the display characters may be encoded by the lamp encoder **754**. For example, if the letter "E" is selected, the signal from the output of the E NAND gate **1206**–E in the alpha numeric decoder **732** is delivered to the appropriate NAND gates **1300**i a through *g* in the first column, gates **1301***a*, *d* and *g* in the second column, gates **1302***a*, *d* and *g* in the third column, gates **1303***a*, *d* and *g* in the fourth column and gates **1304***a* and *g* in the fifth column.

The number of input NOR gates **1306** to the lamp encoder NAND gates may be materially reduced by combining inputs to various gates which are common to a number of different display characters. For example, each of the letters E, F, D, K, M, N, P, R and W as well as the all-lamps-lit character and a number of the other special characters shown in **5***a* call for all of the lamps in the first column LC–1 to be lit. Thus, the output lines from the decoder NAND gates for all of these characters are NOR'd at gate **1308** to produce a single line for signalling the first column of NAND gates **1300***a* through *g* for all of these display characters. Likewise, the characters 2, 3, 5, 6, 8, 9 and $ as well as the alpha characters B and E all have common thereto the LR1, LR4 and LR7 lamps in columns LC2, LC3 and LC4. Nor gate **1310** provides for these common displays. Other lamp groups may also be so combined to limit the number of input NOR gates **1306** which may be calculated from an analysis of the display characters.

If display character data has been encoded by the circuit **754** in the manner set forth a signal is generated to start the readout of the address and character display data to the scoreboard. If one of the display characters is encoded, a legit signal is sent to the lamp strober **750** which controls the read out of the address and display character data. The legit signal is derived from the inputs of certain NAND gates making up the matrix in the lamp encoder **754**. NAND gate **1300***b*, which corresponds to the second lamp from the top in the first column of lamps (LC1—LR2), is actuated whenever any of the alpha-numeric characters is selected except I, J, T, Z, -, ', ., !, 1, 3, 7 and various special characters shown in FIG. **5***a*. Thus, a high signal on conductor **1309** from the input to

NAND gate **1300***b* will indicate a legitimate character display when any but the above listed characters are encoded by the lamp encoder NAND gate matrix. It may be seen that the characters I, J, T, Z, ', 1, !, 3 and 7 all have either the top lamp (LR1) or bottom lamp (LR7) in the third column (LC3) of lamps lit and therefore conductors **1311** and **1313** connected respectively to the inputs of NAND gates **1302***a* and **1302***g*, will carry signals indicating the legitimate display of any of those characters. The inverted signals from the lines are joined with the inverted signal from conductor **1309** at junction **1320** and are NOR'd with signals generated by the selection of the remaining characters (1, -, space) **not having a previously discussed legitimate signal, at NOR gate** 1315.

The high-going legit signal at the output of NOR gate **1315** is applied to the lamp strober enabling gate **1218** via conductor **756**.

Address and Display Character Readout

The lamp strober circuit **750** (FIG. 12) performs the function of a master timer for controlling the readout of the address data to the scoreboard as well as the readout and display of the character data. It comprises a 15 count counter made up of four conventional triggered flip-flops **1212***a* through *d* pulsed by a master oscillator **1214** which constantly produces 25 microsecond pulses at its output to NAND gate **1216**. The other input to gate **1216** is connected to the normally high count 10 output of the counter so that the trigger input to the first flip-flop **1212***a* receives clock pulses from multivibrator **1214** only until count 10 is reached.

The lamp strober counter is inhibited from counting, however, until the storage of the address data and the encoding of the display character data because of the inhibit gate **1218**. The normally high output of gate **1218** is inverted by NOR gate **1219** presenting ground reset and inhibit voltage to the reset terminals of the counter flip-flops. The ground voltage also serves to reset the readout Y address (ROYA) flip-flop **1221** through the double inversion of NOR gate **1217** and negator **1219**.

The lamp strober inhibiting NAND gate **1218** is satisfied by the completion of storage of the address as indicated by the address stored AS signal on conductor **742**, and the encoding of a legitimate display character in the lamp encoder as indicated by the legit signal on conductor **756**. The erase reset input from line **1220** to gate **1218** is normally positive and remains so except for an occurrence during the message board erase function as will be hereinafter described. The jam conductor input is also high as long as the last indicator X28 in a particular row has not been previously addressed as will be discussed in detail later.

Thus, upon the receipt of the legit signal the gate **1218** releases the inhibit from the counter flip-flop reset terminals and the trigger input to the first flip-flop **1212***a* is pulsed by the multivibrator clock **1214** through the NAND gate **1216** to start the timing function.

Count **1** of the lamp strober timer is utilized to initiate the readout of the Y and X address data from the respective storage circuits to the scoreboard. Count **1** is initiated by the first 25 microsecond multivibrator pulse after the inhibit is released and appears as a 50 microsecond long ground pulse at the output of the count 1 NAND gate **1224***a* and as a high pulse at the output of negator **1226***a*. The ground pulse from gate **1224***a* is applied over conductor **1228** to the set input of the readout Y address (ROYA) flip-flop **1221** which puts a high at its Q output. The high signal from the Q output of the ROYA flip-flop is applied over the ROYA conductor **1230** to the Y address output NAND gates **1027***a* through *e* where it is NANDed with the binary code address signals from the Y storage flip-flops **1012***a* through *d*, **1006** in accordance with the Y address of the desired indicator to read out the address data through amplifying negator circuits **1045***a* through *e* and over the cables to the scoreboards. The ROYA signal remains as long as the legit signal appears at the counter inhibit gate **1218** and when it terminates the ROYA flip-flop is reset through NOR gate **1219**, NOR gate **1217** and negator **1215** as previously discussed.

The 50 microsecond high going count 1 signal at the output of negator **1226***a* is the readout X address (ROYA) signal and provides a high over conductor **1232** to the X address readout NAND gates **1115***a* through *f* where it is NANDed with the X address storage data from the X address storage flip-flops **1100***a* through **1100***e* and read out through amplifying negator circuits **1117***a* through *f* and over the cable to the scoreboards.

Counter outputs 2 through 4 of the lamp strober counter are unused. At count 5 the strobe LC1 pulse for reading out the first column of display character data is derived at NAND gate **1224***b* which therefore appears as a 50 microsecond high pulse on line **1234***a* at the output of negator **1226***b*. At count 6 the strobe LC2 pulse for column 2 information is derived on line **1234***b*. Likewise the LC3, LC4 and LC5 pulses are derived, respectively, from the count 7, count 8 and count 9 outputs on the lines **1234***c* to **1234***e*. However, whereas, the LC1 signal pulse is a 50 microsecond pulse, the LC2 through LC5 pulses are 25 microsecond pulses because of the connection via conductor **1236** from the output of the timer clock output NAND gate **1216** to the fifth input of the NAND gates **1224***c*—**1224***f*.

The LC1 through LC5 pulses are directed to respective columns of lamp encoder NAND gates **1300** through **1304**, as well as to the LC1 through LC5 output terminals **1314***a* through *e* to the cable leading to the scoreboard. Thus, each of the LC1 through 5 strobe pulses is NANDed with the appropriate display character data encoded signals appearing at the NAND gates in the lamp encoder matrix to provide LR1 through LR7 signals on the 7-lamp row output conductors **1316***a* through *g* and lamp row data terminals **1318***a* through *e* to the cable leading to the scoreboard. Thus, the strobe signals comprising the single pulses in sequential time relationship from LC1 through LC5 appear at terminals **1314***a* through *e*, and simultaneous with each LC pulse the data pulses corresponding to the required lamps to be lit for forming the desired display character sequentially appear at the lamp row 1 through 7 terminals **1318***a* through **1318***g*.

The address and character display data having all been read out to the scoreboard, the lamp strober counter advances to count **10** which develops a ground pulse over conductor **1238** to the clock timer output gate **1216**. Further clock pulses are inhibited from being transmitted to the lamp strober counter flip-flops and the counter stops. Reset of the counter occurs when the legit signal to inhibit gate **1218** disappears to place ground at the reset terminals of the flip-flops **1212***a*—*d* and **1221**.

The lamp strober **750** also causes the X address storage **740** to advance its stored number to the next succeeding X20, X8 number thus causing the automatic addressing of the next succeeding scoreboard indicator **102** without the operator having to insert the address data. It will be seen that at count **8** of the lamp strobe counter, a ground signal appears on the advance X address (AXA) conductor **1240** from the output of count 8 NAND gate **1224***e*. The signal is inverted at NOR gate **1118** to present a high input to NAND gate **1120**. The jam signal at the other input to NAND gate **1120** is also high except when X29 designating the end of a row is addressed, so the output of the gate **1120** goes low to provide a trigger pulse to the X1 flip-flop **1100***a* in the X address storage circuit **740**. The trigger pulse advances the count registered therein by one digit in a well-known manner to raise the address one number. The Y address storage circuit **738** maintains the Y address date previously stored so that data is now stored in the address storage circuits indicative of the next succeeding indicator in the desired row.

When the last indicator in a row has been addressed and the character display data pertaining thereto has been transmitted, it is desirable to stop the automatic advancing of the X address until the next row indicators is addressed. A jam signal

is therefore generated which prevents further data input until a carriage return signal is received by the logic which automatically causes the storage circuit 738 and 740 to register the address of the first indicator in the next row.

The X address designating the end of the row (No. 29, or one more than the number of indicators) is detected by NAND gate 1122 which is fed by the Q outputs of the X20,X8 and X1 flip-flops of the X address storage. When all three are high indicating the X address number 29 the gate 1122 opens to provide a high signal on the X29 conductor 1131 through negator 1124 to the jam NAND gate 1132. Conductor 1158 at the second input of NAND gate 1132 from the erase function circuits to be hereinafter discussed, is normally high, as is conductor 1234 to the third input from the $\overline{Q}$ output of the ROYA flip-flop 1221. This $\overline{ROYA}$ signal prevents jamming until after read out to the scoreboard of the data pertaining to the 28th indicator in the row.

As previously discussed the output of the jamming NAND gate 1132 forms an input to the lamp strober inhibit gate 1218 over conductor 1222. When the jam signal goes low indicating the end of the row, the gate 1218 is closed placing a low signal on the reset terminals of the lamp strober counter flip-flops preventing any further strobe cycling until the signal on the jam line 1222 again goes high.

The low jam signal from the jam NAND gate 1132 is also sent to NAND gate 1120 closing that gate to prevent any further advancing of the X address in the X address storage.

The signal logic stays in the jammed condition until a carriage return (CR) signal is received. The ASCII code for the carriage return arriving at the character decoder interface 730 is detected by the carriage return alpha decoder NAND gate 1206CR sending a low signal on conductor 1242 and inverted to a high by negator 1126 connected to the input of a NAND gate 1128 in the X address storage.

The other input to the gate 1128 is the address stored (AS) signal on conductor 742 derived from the count 5 output of the 5-count counter 1004 in the address counter circuit 736. It will be recalled that the counter 1004 remains in the count 5 condition until reset. The ASCR signal from the output of gate 1128 triggers the Y address storage to advance to the next number via conductor 1132, junction 1134, conductor 1136, NOR gate 1052 and negator 1054 to the trigger input of the Y1 flip-flop 1012*a* of Y address storage circuit. The ASCR signal appearing at junction 1134 also resets the X address storage to the number 1 to indicate the first indicator in the next row by causing low signals to the reset terminals of the binary weighted 2, 4 and 8 flip-flops 1100*b*, *c* and *d*, as well as X10, X20 flip-flops 1100*e* and *f*, through the NOR gates 1104, 1106 and negators 1110, 1112, respectively. The binary weighted 1 flip-flop 1100*a* is set to its 1 condition by the ASCR signal through NOR gate 1138 and negator 1140 whose output is connected to the set terminal of the flip-flop 1100*a*.

The shift of the X address storage from the X29 address to the X1 address causes the X29 detector NAND gate 1122 to close, removing the high from the first input of the jam NAND gate 1132, and hence restoring the high on the jam signal line 1222 to the lamp strober inhibit gate 1218.

It is also desirable to jam the further readin of data after the last row Y10 of the message board has been actuated to prevent message information from interfering with the ball-game information in the upper portion 104 of the scoreboard (rows 11 through 15). If the Y address stored in the Y address storage circuit is 10 or higher, ground appears on the YA $\overline{10}$ conductor 1130 due to the set condition of the YA 10 storage flip-flop 1006 in the Y address storage circuit 738. Thus, the carriage return CR signal does not reach the ASCR gate 1128 if the Y address is ten or greater preventing the advance of the Y address, and the jam signal continues until the logic is subsequently reset.

Master Reset

It is desirable that the X and Y address storage, the counter and the SA flip-flops be reset to zero when the equipment power is first turned on. This is effected by capacitor 1071 and resistor 1073 connected to the input of negator 1075. The negator 1075, being the type that ordinarily has a momentary high input when power is on, has a ground signal at its input when the power is initially turned on due to the action of capacitor 1071. Thus, a momentary ground appears at the output of negator 1077 (needed for loading purposes) and feeds through NOR gate 1000 and negator 1002 to reset the address counter 1004 and the Y and X address storage flip-flops in the same manner as the SA signal, as previously described. The output of negator 1077 is also directed to NOR gate 1042 which through negator 1044 provides a ground reset pulse to the SA flip-flop 1014.

A switch 1079 between the input of negator 1075 and ground is also provided for resetting the address storage address counter and SA flip-flops without having to previously turn off the power or generate an SA character signal. The reset switch thus enables reset of the address storage circuits when necessary for service procedures.

## SCOREBOARD ADDRESS DECODING AND CHARACTER DATE DISTRIBUTION

The previous discussion has shown how the address and character data signals are generated for transmission to the scoreboards. THe five Y address signals YT1, YU1, YU2, YU4, and YU8 as well as the six X address signals XT1, XT2, XU1, XU4 and XU8 are all amplified by line drivers 1600*a* through *e* and 1602*a* through *f*, respectively (FIG. 16), after being transmitted over the respective cables to the scoreboard. The signals are again amplified by matrix drivers 1604*a* through *e* and 1606*a* through *f* which, besides amplifying the signals, also provide the real and the inverse of each of the signals. The real and inverse signals from the matrix drivers 1604*a* through *e* and 1606*a* through *f* form the inputs to the Y and X address decoder circuits 762 and 764 which are essentially diode matrices of the standard type. Since the X address decoder matrix is the same as the Y address decoder matrix except for the number of addresses that must be handled, only the Y matrix is shown in detail.

The diode matrix address decoder 762 converts the binary coded decimal address signals at its input into a signal line signal on one of its 15 output conductors 1608–1 through 1608–15 to the respective rows of indicators. As is well known an output line, 1608–1 through 1608–15, passes a positive signal when a high going signal is received on each of the real and inverse conductors 1607*a* through *j* connected thereto by the diodes 1610. As an example, suppose the indicator being addressed is in the row 15. High signals will appear on the real 10's line 1607*b*, the real 4 line 1607*f* and the real 1's line 1607*j*, as well as on the $\overline{8}$ line 1607*c* and the $\overline{2}$ line 1607*g*. All other conductors will have low signals thereon. It will be noted that the row 15 output conductor 1608–15 has diodes connected therefrom to each of the lines 1607*b*, 1607*c*, 1607*f*, 1607*g* and 1607*j* so that the simultaneously received high signals will be passed therethrough to the output line 1608–15. No other output conductor 1608–1 through 1608–14 will pass a signal because one or more of the diodes connected to those lines would have their cathodes connected to low signal conductors and thus shunt any high going signals on the other conductors connected thereto.

Each of the outputs 1608–1 through 1608–15 is connected to all of the indicators in the row designated by that Y address. Likewise, the outputs from the X address matrix 764, which operates in the precise manner described for the Y matrix, are each connected to all of the indicators in the column of indicators designated by the respective X address. These Y and X address signals are those appearing at terminals 814 shown in the lamp indicator circuit diagram (FIG. 8). Their simultaneous receipt extinguish all previously lit lamps and reset the circuit for the immediately following character display data.

The character display data is transmitted from lamp encoder output terminals 1318*a* through *g*, 1314*a* through *e* over the cables 774 and 776 after being amplified by line driver amplifiers 1700*a* through *g* for the lamp row data signals and line driver amplifiers 1702*a* through *e* for the lamp column strobe signals. At the scoreboard the signals are again amplified by the character data lamp row drivers 1704*a* through *g* and the lamp column strobe signal line drivers 1706*a* through *e*. The seven lamp row drivers 1704*a* through *g* have their outputs connected to the seven rows of lamp switches 800 in every indicator circuit 706 on the scoreboards. Likewise the lamp column drivers 1706*a* through *e* have their outputs connected to the respective columns of lamp switches in every indicator circuit 706 on the scoreboard. The signals from the lamp row and lamp column drivers from the LR data signals and the LC strobe signals to the indicator circuits 706 shown in FIG. 8 and cause the display of the desired character on the indicator having the immediately preceding address transmitted from the signal logic to the scoreboard.

## DATA INPUT

### Keyboard Generation of Address and Character Data (FIG. 18)

The keyboards 302, 304 are shown schematically in FIG. 18 to show how the ASCII code signals are generated and transmitted to the data bus terminals *db1—db7* in FIG. 12. Depressing any one of the keys 1801 at the keyboards provides ground to the inputs of one or more of the negators 1800*a* through *g* with resulting enabling high voltages at the first input of the respective data NAND gates 1802*a* through 1802*g*. The input signals to these NAND gates correspond to the 1's and 0's representing the particular ASCII code notation shown in the chart of FIG. 9 for the selected character to be read into the signal logic.

Depressing any one of the keys 1801 also places ground on conductor 1806 leading to the set input of flip-flop 1808. The flip-flop has its Q output connected through an inverting NAND gate 1810 to its reset input so that it acts as a one shot multivibrator in a well-known manner. Thus the $\overline{Q}$ output produces a low going pulse having a duration of about 1.4 millisecond. This pulse is inverted at negator 1812 and NANDed at gate 1814 with a high from the output of NOR gate 1816. The input of gate 1816 is in receipt of ground voltage through the Scoreboard Keyboard Input (SKI) switch contacts 640*a*. As previously indicated this switch is actuated whenever it is desired to reach the scoreboard directly from the console keyboards and buttons at the console 300.

The gate 1814 serves as a strobe gate providing a high synchronizing pulse signal to the second input of the previously enabled ones of date gates 1802*a* through *g*. Thus simultaneous low signals appear at the output of the data gates which are transmitted to the *db1—db7* terminals (FIG. 12) via the 7 conductor board data bus 715.

It will be recalled that the explanation of the signal logic assumed the direct connection of the keyboard keys to the data bus terminals to facilitate that explanation. The present description indicates that the console keys produce 1.4 millisecond, synchronized pulses instead which, although not absolutely necessary, do a better job of controlling the signal logic and eliminating the effects of any contact bounce at the keyboard.

### Single Button Addressing

The previous sections described the operation of the signal logic assuming that all of the address data and the character display data is generated by the operator manipulation of the keyboards 302, 304 in the console 300. For game in progress information to be displayed in the section 104 of the scoreboard, the data indicators associated with the fixed captions such as BALL, STRIKE, OUT, LINE SCORE, etc. may be automatically selected by the button on the console 300 having the caption name associated therewith as previously described. The words "batter" or "play" may also be generated and displayed by pressing the appropriate buttons. These functions are performed by the address encoder 712, shown in detail in FIG. 14, as well as the word generator 714 and address and word control 716, shown in detail in FIG. 15.

As an example of the operation of single button addressing, assume it is desired to address the indicator which displays the total errors of the home team as the game progresses. The indicator address where this information is to be displayed is Y15—X26 as indicated on the scoreboard of FIG. 1. Depressing home button 328 and error button 336 produces ground signals on the Y15 and X26 input conductors, respectively, to the appropriate gates of the series of input NOR gates 1400*a* through 1400*k*. Thus the three ground Y15 inputs to the respective NOR gates 1400*a*, 1400*b* and 1400*d* provide set pulses through the respective ones of inverters 1402*a—k*to the appropriately weighted Y address encoder flip-flops 1404*a* through *e* to store the number 15 in binary coded decimal notation. The X26 grounded inputs cause setting pulses through the respective NOR gates and negators to the appropriately weighted X address encoder flip-flops 1404*f* through *k* to store the X address number 26 in binary coded decimal notation. Thus, to register the address Y15–X26 flip-flops 1404*a*, *b*, *d*, *f*, *i*and *j* will be set to provide high inputs to the address storage NAND gates 1406*a*, 1406*b*, 1406*d*, 1406*f*, 1406*i* and 1406*j*.

The stored address is then converted to ASCII code as it is serially read out from the storage NAND gates 1406 one digit at a time for presentation to the data bit terminals in the character encoder interface 730. To read the address data out of the address storage NAND gates 1406*a—k*, properly sequenced pulses are received at the first inputs to the gates 1406*a* through *k*. The pulses are preceded by a readout special address signal (ROSA) followed by the four digit readout pulses—readout Y tens address (ROYTA), readout Y units address (ROYUA), readout X tens address (ROXTA), readout X units address (ROXUA). This will be recognized as the same order that the operator keys in the Y and X address data as explained previously.

The readout signals are generated in the address and word control circuit 714, shown in FIG. 15, responsive to the storage of the one button address data. It will be noted that the outputs of the negators 1402*a* through 1402*k* leading to the set terminals of the Y and X storage flip-flops 1404*a* through *k* each connect to one of the lines indicated ST1 through ST11 which lead to the NOR gates 1500*a*, 1500*b* (FIG. 15) in the address and word control 716. NOR gate 1500*a* is associated with the Y storage flip-flops 1404*a—e*and NOR gate 1500*b* is associated with X storage flip-flops, 1404*f—k*, so that if both X and Y data is presented the coincident highs at the output of the NOR gates 1500*a* and 1500*b* are sent over conductor 1502 to the input of NAND gate 1504. The other input to NAND gate 1504 is always high except for the message update function which will be described later.

The low output from NAND gate 1504 sets the address control set-reset type flip-flop 1506 to its high Q output state. This high prepares the address and word control timer enabling gate 1508 at its third input. The second input to NAND gate 1508 is already high by means of the message update flip-flop 1510 which remains in its high $\overline{Q}$ output state during the operation of the system in the manner herein described. The fourth input to gate 1508 is also high because of the low count 15 output of the address and word control counter 1512 which had been previously reset to its zero state at the end of its last cycle of operation as will become apparent hereinafter. The gate 1508 is thus enabled to pass 0.91 millisecond pulses from the multivibrator timing clock 1514 to the trigger input of the 15-**count counter** 1512.

The counter 1512 begins to count producing a 1.82 millisecond pulse at its first output on conductor 1516 to the count 1 NAND gate 1518. There it is NANDed with a 0.91 millisecond pulse from gate 1508 to produce a 0.91 millisecond ground on the ROSA (Read Out Special Address) con-

ductor. The ROSA signal generated by the clock count 1 is delivered to the ASCII code bit encoder formed by the NOR gates 1408*a* through *f* and NAND gates 1410*a* through *g* in the address encoder 712 (FIG. 14). Specifically the ground ROSA pulse is fed to NOR gates 1408*b*, 1408*d* and 1408*f* with the high outputs therefrom being delivered to the NAND gates 1410*b*, 1410*d* and 1410*f*. The data inputs to the gates 1410*a* through 1410*g* are NANDed with a high signal from the direct to scoreboard (SKI) switch contacts 640*b* which is actuated by the operator if the encoded information is to go directly to the scoreboard for display. The resulting low outputs from the NAND gates 1410*b*, *d* and *f* along with the normally existing high outputs of gates 1410*a*, *c*, *e* and *g* represent the inverted ASCII code for the special address character presented to the character decoder interface 730 as previously explained.

Returning to the readout signals from the address and word control, the count 2 signal from NAND gate 1518*a* establishes the readout Y tens address on conductor ROYTA through NOR gate 1519*a* which leads to the NAND gate 1406*a* (FIG. 14) at the output of the Y tens flip-flop 1404*a*. Since our example address (15—26) caused the Y10 flip-flop 1404*a* to be set, the NAND gate 1406*a* is satisfied and its output is transmitted though the first encoder NOR gate 1408*a* to the first encoder NAND gate 1410*a*.

It will be noted from the ASCII code table in FIG. 9 that for the numeric character 1 as well as all other numeric characters the data bits 5 and 6 must also be present which indicate that NAND gates 1410*e* and 1410*f* must be satisfied when ever address date is being generated. Therefore, simplified circuitry is utilized to provide high signals to these gates for each of the four readout address signals which appear at counts 2 through 5 from the address and word control counter 1512. Each of the count signals 2 through 5 from the counter circuit are fed to a NOR gate 1520 (FIG. 15), the output of which is termed the readout five and six bits (RO5+6). The RO5+6 signal is fed to the address encoder circuit 712, inverted by negator 1416 and fed to encoder NOR gates 1408*e* and *f*. These gates produce the high signals to the 5 and 6 bit NAND gates 1410*e*, 1410*f* as required for each of the numeric character ASCII code notations. The ASCII code 1000110 for the numeral 1 representing the Y tens digit therefore appears at the input to NAND gates 1410*a* through *g* during count 2 from the Address and Word Control and consequently readout to the Y address storage 738 in the signal logic.

The count 3, count 4 and count 5 signals from the address and word control counter 1512 actuate, respectively, the readout Y units address (ROYUA), readout X tens address (ROXTA) and readout X units address (ROXUA), the numeric date for each digit being encoded by the NOR gates 1408*a* through *f* and NAND gates 1410*a* through *g* and sent to the respective storage circuits in the signal logic. The circuits may be readily traced out to show how the ASCII code bits are generated for each of the remaining digits of the example address 15—26.

The home team errors indicator Y15–X26 having been single button addressed with the information stored in the Y and X storage circuits 738 and 740, the signal logic only awaits the operator's input of the desired character display date indicating the number of errors. When the operator presses the proper number button at the console 300, the character is encoded in the lamp encoder 754, and if it is a legitimate signal, the lamp strober 750 is caused to readout the address and character display data over the cables to the scoreboard.

It may be seen that only the first five counts of the 15-count address and word control counter 1512 are utilized for single button addressing. The counter continues to cycle through the rest of its counts, however, until count 15 is reached which places a high on conductor 1524. The high is inverted by negator 1526 to close the gate 1508 between the multivibrator clock 1514 and the trigger input to the counter 1512. The flip-flop 1506 is reset to its $\overline{Q}$ state, and the counter 1512 is reset to its zero condition when the operator releases the one button address button at the console. Release of the button removes all of the ST signals from the inputs to NOR gates 1500*a* and 1500*b* which in turn removes the high from the second input of NAND gate 1504. The resulting high is applied to the input of NAND gate 1528 which receives a high at its other input when the counter reaches count 15 from the output of negator 1526, conductor 1530 and NOR gate 1532. The low signal from gate 1528 applied to the reset terminal of flip-flop 1506 resets it to its high $\overline{Q}$ condition for its next operation. The high $\overline{Q}$ signal from flip-flop 1506 is inverted at negator 1531, the low signal resetting counter 1512 to its zero state. The high $\overline{Q}$ signal from flip-flop 1506 is also NANDed at 1533 with the normally high signal from the update flip-flop 1510 and the resulting low provides a Clear Storage B signal on conductor 1535 to reset the Address Encoder flip-flops 1404*a*—*1404k*.

## Word Generation

As previously described, during the progress of a baseball game it is desirable to display the word PLAY in the group of indicators marked 108 on the scoreboard 100 (FIG. 1) and on the first four indicators of the group marked 206 of the auxiliary board shown in FIG. 2. Since these indicators are used for the display of other information also, means are provided in the control system for automatically writing the word "PLAY" on these indicators. The first indicator in each of these groups has been given the address Y11–X20.

The scoreboard operator causes the word PLAY to be displayed on the two boards by depressing the PLAY button 348 in the fact feature portion of the console 300 (FIG. 3). The operation of the PLAY button first generates the address data for selecting the first indicator 11—20 in the display groups 108, 206. The address data is generated in the same manner as previously described for one button addressing. That is, ground signals appear on all of the Y11 and X20 input lines to the NOR gates 1400*a*, *b* and *f* to set the appropriate flip-flops 1404*a*, *b and f*. High inputs are thus provided to the NAND gates 1406*a*, *b and f* to await the readout signals from the address and word counter as previously described.

It will be recalled that the readout signals are initiated by the appearance of one or more signals on the ST1 through 5 conductors and one or more signals on the ST6 through 11 conductors which through the input circuitry previously described begins the operation of the address and word control counter 1512.

The counter 1512 being triggered produces the count 1 through count 5 pulses to readout the special address character and each of the digits forming the Y and X address to the signal logic 702 in the manner described in the previous section of the specification describing single button addressing.

The counter continues, count 6 and 7 not being used, and count 8 begins the readout of the character display data for displaying the word PLAY. Count 8 from the output of NAND gate 1534*a* and negator 1536*a* is applied to the P NAND gate 1538. The other input to the P gate 1538, as well as the second inputs to the L gate 1540, A gate 1542 and Y gate 1544 are previously set to a high from the PLAY generator flip-flop 1546 which has its set input connected directly to the PLAY button 348 on the console.

A low signal, therefore, appears on the P conductor LP responsive to count 8 which is transmitted to the encoder circuit in FIG. 14 where the encoder NOR gates 1408*a* through *f* and NAND gates 1410*a* through *g* convert it to ASCII type 7-bit code signals. It will be noted that the LP line is connected to the NOR gate 1408*e* which feeds a high to the first input of NAND gate 1410*e* . Also the LP line is connected to NOR gate 1418 which places a high at the second input to NAND gate 1410*g*. The high inputs to gates 1410*e* and 1410*g* which represent date bits 5 and 7, along with the low inputs to the NAND gates 1410*a* through 1410*d* and 1410*f* which represent data bits 1 through 4 and 6 are indicative of the ASCII code for the letter P as shown in the table of FIG. 9. The outputs of the gates 1410*a* through *g* are fed to the character decoder in-

terface 730 and applied to the alpha-numeric decoder 732 which signals the lamp encoder and lamp strober to encode the letter P and read out the address and character display data to the scoreboard in the manner described previously. The address in the X address storage 740 is automatically advanced to the next indicator address in the row (Y11–X21) and the system is ready for the display of the next character L in the word "Play."

The letter L is generated at count 9 of the address and word control counter 1512 which causes a ground signal to be produced on the LL line to the inputs of the appropriate NOR gates 1408*a* through 1408*f*. Tracing of the circuits will shown that the gates 1408*a* through *f* and 1410*a* through *g* will develop the proper signals for the ASCII code representation of the letter L to the signal logic circuits. The letter A is generated at count 10 of the address and word control counter 1512 and the last letter Y is generated at count 11 in a similar manner, counts 12 through 14 not being used for generation of the word PLAY.

After display of the letter Y in the word PLAY the X address storage is again automatically advanced to the next number. The address now stored is 11—24. It wild be noted that the first indicator in the group 110 (FIG. 1) for the display of the particular play information has the address Y11—X24 so that automatic address advance feature causes the first indicator in group 110 to be automatically addressed at the end of the readout of the word PLAY. Count 15 then resets the address counter 1506 which then causes the Clear Storage B signal to reset the PLAY flip-flop 1546 as well as the address encoder flip-flops 1404*a*—*k*.

The display of the Word BATTER on the group of indicators 206 on the auxiliary board 200 is performed in substantially the same manner with the proper address being encoded in the address encoder circuit 712 and the word BATTER being generated in the word generator circuit 714. The selection of the button 306 on the console marked BATR causes the automatic encoding of the proper address for the first indicator in the group 206 on the auxiliary board during the first 5 counts of the address and word control counter 1512 and also sets the batter flip-flop 1548 to enable the word generating NAND gates 1550 through 1560. Counts 8 through 13 of the counter 1512 successively trigger each of the NAND gates 1550 through 1558 to cause the encoding of each of the letters in the word BATTER by the encoding gates 1408*a* through *f* and 1410*a* through *g*. On count 14 the space character is generated from NAND gate 1560. After the word and space character has been automatically generated and displayed onto the board, the first indicator (V12–X21) for registering the batter data is automatically addressed. It will be noted in FIGS. 1 and 2 that the first indicator directly under the word BATTER on the main board 100 and the eighth indicator of the group 206 on the auxiliary board both have the same address so that both boards are addressed for display of the batter data after the word BATTER has been generated and displayed on the auxiliary board.

## Erase Function

As will be recalled the erase function is used to clear display data off of desired indicators. During the erase function the signal logic is caused to automatically generate sequential address signals pertaining to the particular section of the board it is desired to erase. As described in the detailed explanation of the indicator circuits, addressing of an indicator automatically causes it to be extinguished in preparation for the receipt of character display data. Thus, an indicator need merely be addressed to erase previous data on display.

Assuming the operator wishes to erase one line of the message section 106 of the scoreboard, he selects the button from the group 360 on the console 300 for the line he desires. This button produces the address of the first indicator in the selected line, the one button address being produced by the address encoder 712 (FIG. 14) in the manner previously described, and this address is stored in the Y and X address storage circuits 738, 740.

The button also has a contact which feeds a ground to the set terminal of the erase 1 line flip-flop 1138 (FIG. 11) in the signal logic. The $\overline{Q}$ output of flip-flop 1138 goes to ground which is inverted to a positive clear signal on conductor 1146 by NOR gate 1140. The positive clear signal is transmitted to NAND gate 1142 provided the direct to scoreboard switch is closed putting positive potential through S.K.I. switch contacts 640*c* to the cathode of diode 1143. The S.K.I. (direct to scoreboard) switch contacts 640*c* and diode 1143 are used to insure that the erasure function takes place only if the circuits are connected to erase the data on the scoreboard. The positive clear signal is NANDed with the address stored (AS) signal by NAND gate 1142, the ground output therefrom on conductor 1144 being inverted by NOR gate 1219 to provide a positive enabling signal to the reset terminals of the lamp strober counter flip-flops 1212*a*—*1212d*. The ground trigger pulses from the multivibrator clock 1214 and NAND gate 1216 actuate the lamp strober counter to begin its count. Count 1 occurs normally to read out the Y and X address to the boards which causes any lamps which are previously lit on the addressed indicator to be extinguished in the manner discussed earlier. Count 5 produces the strobe LC1 pulse.

No further strobing to the scoreboard indicators is required so that at count 6 of the counter the following occurs. The negative count 6 pulse from the output of NAND gate 1224*c* on conductor 1244 is inverted to a positive pulse by negator 1246 and NANDed at gate 1248 with the positive clear pulse on the conductor 1146 leading from the output of the NOR gate 1140 (FIG. 11). The ground at the output of NAND gate 1248 is applied to the set terminals of counter flip-flops 1212*a* and 1212*d* to set them to their high Q states. Since flip-flops 1212*b* and 1212*c* already are in their high Q states at count 6 the effect is to instantaneously change the count to 15 bypassing count stages 7 through 14. Therefore, strobes LC2 through LC5 pulses are not produced and count 10 is also bypassed which otherwise would close the gate 1216 between the multivibrator clock 1214 and the trigger input to stop the count. The four high Q outputs of the lamp strober counter flip-flops 1212*a* through 1212*d* are NANDed by gate 1250 to produce a ground signal to reset the readout Y address flip-flop 1221 and also to automatically advance the X address (EAXA) via conductor 1252 and NOR gate 1118 (FIG. 11) to NAND gate 1120. As long as the jam NAND gate 1132 has a high output indicating that the last indicator in the row has not been reached, gate 1120 sends a ground pulse to the trigger input of X address storage flip-flop 1100*a* to advance the X address stored number up one count, signifying the next indicator.

The next pulse from clock 1214 to the lamp strober counter then restarts it from count zero again counting through to count 6 and converting to count 15 to extinguish the next indicator and automatically address the following indicator. This occurs repeatedly until number 29 at the end of the row has been addressed, at which time NAND gate 1122 is satisfied to provide a high signal from the output negator 1124 to the input of the jam NAND gate 1132 via conductor 1131. The low output from jam gate 1132 closes gate 1120 preventing the further advance of the X address storage.

The number 29 signal is also applied to NAND gate 1150 which in addition receives a high signal from the Q output of the erase 1 line flip-flop 1138, and the resulting ground erase reset signal causes the reset of the erase 1 line flip-flop 1138 through NOR gate 1152 and negator 1154. When the erase 1 line flip-flop 1138 resets, it $\overline{Q}$ output goes high producing a low to NAND gate 1142 and hence a high on conductor 1144 to NOR gate 1219 in the lamp strober. At the same time the low erase reset signal on conductor 1220 from NAND gate 1150 (FIG. 11) insures that the lamp strober inhibit gate 1218 is closed to provide a high at the other input of NOR gate 1219. The ground output signal therefrom thus resets the lamp strober flip-flops to zero and the signal logic is reset to receive succeeding data from its various inputs.

If the operator wishes to erase all 10 message lines of the message section **106** of the scoreboard, he selects the EMSG erase button **358** on the console **300**. This button automatically produces the address of the first indicator in line 1 of the scoreboard (**Y01—X01**) which is automatically read in to the X and Y address storage circuits. Also, the one button feeds a ground to the set terminal of the erase message flip-flop **1156**. The low going $\overline{Q}$ output thereof initiates the counter in the lamp strober **750** and erase of the first line occurs just as described for the erase of 1 line. However, at address **Y01–X29**, no jam signal is desired because the next row must be automatically addressed and erased. THe jam NAND gate **1132** which controls NAND gate **1120** and the advance X address ground pulses to the X address storage is not actuated because of the low at the second input of gate **1132** on conductor **1158** connected to the $\overline{Q}$ output of the erase message flip-flop **1156**. That is, during the erase message function the second input to the jam NAND gate **1132** is maintained low to keep gate **1120** open for the passage of the erase advance X address (EAXA) pulses to the X address storage from the lamp strober counter through NOR gate **1118**.

The address in the Y address storage **738** is automatically advanced to the next row of indicators when the last indicator in the previous row has been erased by means of NAND gate **1053** which feeds the trigger input to the first Y address storage flip-flop **1012*a*** through NOR gate **1052** and negator **1054**. The NAND gate **1053** is satisfied by the Erase Message Signal (EMSG) from the high Q output of the erase message flip-flop **1156**, and the X number **29** signal (**X29**) indicating the end of the row. The low pulse output from gate **1053** thereby causes the advance of the Y address in the Y address storage flip-flops. The output of NAND gate **1053** also provides inputs to gates **1102**, **1104** and **1106** which are used to reset the X address flip-flops to count O.

The lamp strober counter continues to cycle until the address **Y10—X29** is reached. This condition is detected by NAND gate **1160** which has inputs connected to the Q output of the YA10 flip-flop **1006** (**YA10**), the **X29** line, and the high Q output of the erase message flip-flop **1156** (EMSG). The concurrence of these signals produces a ground erase reset signal on the erase reset line **1220** to the lamp strober inhibit gate **1218** to stop and reset the lamp strobe counter. The erase reset signal also causes the reset of the erase message flip-flop **1156**, and the reset of the remaining signal logic circuits as hereinbefore described.

The erase game in progress button (EGIP) **352** is used to erase all of the indicators in the section **104** of the scoreboard as previously described. Depressing the EGIP button causes the automatic address encoding for the first indicator of the game in progress section **104**. THe button also sets another erase flip-flop (not shown) and causes the automatic addressing and hence erasing from that address on through the last indicator **X15—Y28** on the board in essentially the same manner as described for the erasure of the message portion of the board.

The clear button **314** for erasing the batter number and the number of balls and strikes operates in essentially the same manner as any one of erase 1 line buttons **360** previously described except for the fact that we do not want to erase the number of outs on indicator **Y12–X12**. Thus, we want to erase by the operation of button **314**, indicator **Y12–X02**, **Y12–X09**, **Y12–X10**, skipping indicator **Y12–X12** and erasing indicators **Y12–X21**, **Y12–X22**. depressing the clear button **314** automatically addresses the first indicator in row **Y12** and sets flip-flop **1157** to begin the automatic erasure of the indicator therein. It will be noted, however, that the high Q output of flip-flop **1157** is also delivered to gate **1253** (FIG. **12**) in the lamp strober where it is NANDed with the Q outputs of the **Y10** flip-flop **1006**, **Y2** flip-flop **1012*b***, **X10** flip-flop **1100*e*** and the **X2** flip-flop **1100*b***. Also NANDed therewith are the $\overline{Q}$ outputs of the **X8** flip-flop **1100*d*** and **X4** flip-flop **1100c**. It will be noted that the gate **1253** is satisfied by highs at all of its inputs when the address **X12—X-12** appears in the X and Y storages to provide a low at conductor **1255** leading to the input of the count 1 NAND gate **1224*a***. This prevents readout of the X and Y addresses at that point to prevent the indicator **Y12–X12** from being addressed and hence erased. The erase function continues, however, until the end of row 12 is completed at which time the jam signal occurs and the erase reset signal resets flip-flop **1157**.

Any one indicator at any address location on the scoreboards may be erased by the operator merely by use of the console keyboards **302**, **304**. He may select the address of the desired indicator by depressing first the special address button, then the four numbers indicating the Y and X address and followed by operation of the spacebar on the alpha character keyboard **304**, the spacebar providing a high at the input to NOR gate **1315** and therefore a legit signal to initiate the lamp strober causing all indicator lights to be extinguished. Succeeding indicators may then be extinguished merely by continuous releasing and depressing of the spacebar which causes the automatic address advance and turn out of the indicator lamps.

## AUXILIARY INPUTS

### Magnetic Tape Memory

A magnetic tape may be programmed in the same manner as the punched tape to cause the display of messages on the board. It may also be used for rapidly displaying succeeding character displays to give animated cartoon effects, flashing messages and many others of an unlimited variety.

When desired to post the prerecorded tape message directly on the message board, the magnetic tape memory **710** (FIG. **20**) reads the address and character date from its output terminals O*b* 1 through O*b* 7 to the signal logic input terminals O*b* db1 through db7 via NAND gates **2000*a*** through *g* and the board data bus **715**. The gates **20000*a*—*g*** are enabled by means of the Tape Memory Post on Board (TMPOB) switch **2002** operable by button **624** on the control **602** which momentarily sets flip-flop **2004**. The momentary low at its $\overline{Q}$ output causes flip-flop **2006** to be set with the high Q output enabling the gates **2000** *a* through *g*. The low $\overline{Q}$ output is used to signal the tape memory to start running in the read out mode. The address and character data is thus fed to the signal logic **702** to display the message on the board.

When the desires message has been completed the tape memory reads out a special End of Tape Block (ETB) coded signal which is detected by NAND gate detector **2008**. The low output thereof triggers a single shot multivibrator **2010** which delivers a reset pulse to flip-flop **2006**.

Provisions are also made for transferring data between the tape memory and the buffer memory in the manner and for the purposes to be discussed hereinafter.

### Buffer Memory

The buffer memory is a temporary storage device which facilitates the transfer of data from the various input devices to the scoreboard. It provides a means for writing data into and out of the magnetic tape storage memory and is also used in the message updating function as will be described. The buffer memory used in the constructed embodiment at Anaheim, Calif. is a magnetic core storage device of a well-known type and is described in the "Technical Manual for the RVS Magnetic Core Memory" published Mar. 1, 1964 by Computer Products Div., Ampex Corp. P.O. Box 329, Culver City, Calif. The buffer includes a 512 word capacity data register which is used in the sequential, or first date in—first date out, mode and an address register which is used sequentially as a counter.

The buffer memory **711** is capable of operating in a number of different modes dependent upon the particular function for which it is being utilized. These modes of operation will be discussed in the description of the circuit operation for each of the functions described.

Buffer Memory Keyboard Input (BMKI)

The buffer memory keyboard input function enables the operator to write a desired message into the buffer memory and hold it there before posting it on the board. The scoreboard operator may write his desired message into the buffer memory at a random speed, and subsequently post the message on the scoreboard in a quarter of a second or less dependent upon the length of the message. The buffer memory keyboard input function is initiated by depressing the BMKI button **620** on the console portion **600** which closes contacts **620***a* (FIG. **18**), contacts **620***b* and contacts **620***c* (FIG. **19**).

The BMKI switch contact **620***b* sets flip-flop **1900**, the low going $\overline{Q}$ output of which drives a single shot multivibrator **1902** through the NOR gate **1904** and negator **1906**. The output of the single shot multivibrator **1902** is a 1.6 millisecond pulse which drives the load bus **1908**. The 1.6 millisecond pulse is transmitted through negator **1910** and NAND gate **1912** to the master clear terminal of the buffer memory which clears the date and address registers therein.

The negative pulse on the load bus **1908** also sets the read/write flip-flop **1914**. The high signal is delivered therefrom on conductor **1915** to the R/NW terminal of the buffer memory which conditions the memory for a write function. In addition, the negative pulse on the load bus **1908** is applied through NOR gate **1916** and negator **1918** to the set terminal of flip-flop **1920**. The low signal at the BQ input of the buffer from the Q output and of flip-flop **1920** through negator **1922** places the buffer in its sequential operation mode. This permits each data word subsequently fed thereto, to be stored at sequential addresses within the memory. Since the master clear was also triggered, the first data word will thus be inserted at the first address.

The memory/buffer terminal M/B of the buffer receives a high signal resulting from the low $\overline{Q}$ output of flip-flop **1920** and negator **1924**. This places the memory in its buffer mode to eliminate the automatic clearing of data at each address before new data is received. The buffer memory **711** is now ready to receive the address and character data from the keyboard inputs **302**, **304**.

The BMKI switch contacts **620***a* (FIG. **18**) provided an enabling signal through NOR gate **1819** to the NAND gates **1820***a* through **1820***g* connecting the keyboard date lines from the output of negators **1800***a* through **1800** *g* to the S*b* **1**—S*b* **7** multiline conductor **1822**. Conductor **1822** leads to the buffer memory date input terminals S*b***1**—S*b***7** (FIG. **19**).

The buffer and its circuits are now ready for input data from the keyboards **302**, **304**, which is initiated by a 1.4 millisecond synchronizing pulse which is developed by the one shot multivibrator **1808** on the keyboard sync *b* conductor responsive to each alpha or numeric key actuation in the manner previously described for posting information on the scoreboard directly from the keyboards. The keyboard sync b pulse is transmitted via conductor **1824** to the buffer strobe gate **1926** (FIG. **19**) which was enabled by the BMKI contacts **620***c*. The 1.4 millisecond keyboard sync B pulse is therefore transmitted through strobe gate **1926** and NOR gate **1930** to the NAND gate input input **1932** of the pulse shaping circuit **1934**. The keyboard sync B signal is NANDed with a 2 kc. pulse signal from clock **1936** with the resulting signal output from the shaping circuit **1934** being a 10 microsecond low going pulse, The NAND gate **1932** and shaping circuit **1934** operate in a familiar manner to provide the 10 microsecond pulse regardless of the length of the various sync B pulses which are fed through the NOR gate **1930**. The sync B pulse to the buffer causes the simultaneous read in of the data word bits at the data inputs S*b*—S*b***7** and advances the address register to the next sequential position for receipt of the next data word in the buffer.

The operator may load the buffer up to **496** words or characters at which time the count **496** NAND gate **1938** will be satisfied by the appropriate weighted AR outputs. The buffer full lamp **1940** lights indicating to the operator that he has only 14 more characters to load into the buffer memory before destroying previously loaded information at the first buffer addresses.

The buffer memory may also be filled utilizing the single button addressing keys such as found in the out-of-town games portion **602** of the console. It is desirable to maintain the out-of-town format data in storage during a ballgame so that it may be displayed on the message board at any desired time. Thus, the data for the out-of-town format is read into the buffer memory by means of the single button address keys and the console keyboard buttons after which it is transferred to the magnetic tape.

Single button addressing operates in the same manner as previously described for single button addressing direct to the scoreboard utilizing the address and word control **716** (FIG. **15**) as well as the address encoder circuit **712** in FIG.**14**. However, the address data is prevented from reaching the signal logic because the NAND gates **1410***a* through *g* are disabled in view of the ground at their inputs through the nonactuated S.K.I. switch contacts **604***b*. Instead gates **1430***a* through *g* (FIG. **14**) which lead to the inputs S*b* **1**—S*b* **7** of the buffer memory **711** are enabled by the BMKI switch contacts **620***d*. The sync B pulses required for writing data into the buffer from the address encoder are generated at the output of NAND gate **1432** by means of the ROSA and RO**56** pulses from the address and word control **716**. That is, a sync B pulse is generated when the special address character is generated and for each of the four address digits generated. The low going ROSA signal is NOR'd in gate **1434** passed through NAND gate **1432** enabled by the BMKI switch contacts **620***d*. Likewise, the low going RO**56** signal is negated by inverter **1416** and again by negator **1438** to present a low signal to the other input of NOR gate **1434**, the high output of which is fed to gate **1432** to provide sync B pulses. As previously indicated the RO**56** signal is indicative of each address digit because the 5 and 6 bits of the 7-bit ASCII code are present in each of the numerals 0 through 9. After the automatic insertion of the address data into the buffer memory from the single button address key, the character display data is then inserted directly from the keyboards **302** or **304** through the gates **1820***a*—*g*. The next single button addressing key may then be actuated to read in subsequent data.

The punched tape typewriter and reader **708** writes information into the buffer memory in a quite similar manner to that just described for the console keyboard input. Thus, the circuits are not shown in the schematic diagram of FIG. **10** through **21**.

Loading the Buffer From The Tape Memory (TM L*d* BF)

This function is used to temporarily store a message in the buffer from the magnetic tape memory **710** for posting on the board, and for preparing for the update of a message which as been stored on the tape. The function is initiated by means of the TM load buffer switch **2020** (FIG. **20**) operated by button **626** at the console **602** which sets flip-flop **2022**. The low going $\overline{Q}$ output in turn sets flip-flop **2024** which through its high going Q output enables the buffer input NAND gates **2026***a* through **2026***g*. The data from the tape memory **710** may thus be read from its output terminals O*b* **1** through **0***b* **7** to the buffer input S*b***1** through S*b***7**.

The low going $\overline{Q}$ output signal of flip-flop **2022** is also applied via conductor **2028** to the input of NOR gate **1904** (FIG. **19**) the output of which through negator **1906** actuates the single shot multivibrator **1902** to provide the 1.6 millisecond low going pulse on the load bus 1908. The buffer 711 is thus prepared for the load operation in the same manner as it was set for the keyboard input function.

The buffer memory **711** is thus prepared to receive the data from the tape memory **710** and its operation is properly synchronized with the input data by means of the tape memory sync B pulses generated by the tape memory and

transmitted via the TM sync *b* line to the NOR gate 1930 (FIG. 19). The TM sync B pulses from the tape memory are approximately 30 microseconds duration; however, the gate 1932 and shaping circuit 1934 convert them to the 10 microsecond sync B pulses.

## Posting The Buffer To The Scoreboard (BMPOB)

The contents of the buffer memory 711 are causes to be read out to the signal logic 702, and hence, to the scoreboard by actuation of the BMPOB switch 630 (FIG. 20) which sets the BMPOB flip-flop 2030. The high signal at the Q output thereof is applied through conductor 2032 to NAND gate 1942 (FIG. 19) where it is gated with a normally high signal from the update function circuits as will be hereinafter described. The low at the output of gate 1942 is inverted to provide high enabling signals to the buffer data output gates 1944*a* through *g* in preparation of the transmission of the buffer data therethrough and over the board data bus 715 to the date input terminals *db*1 through *db*7 (FIG. 12 of the signal logic)

The low $\overline{Q}$ output of BMPOB flip-flop 2030 is NOR'd at gate 2034 and inverted by negator 2036 to trigger a single shot multivibrator 2038 which produces a 1.8 millisecond low going pulse at its output. This is inverted by negator 2040 and NANDed at gate 2042 with a high signal on conductor 2044 from the high Q output of flip-flop 2030. THe 1.8 millisecond low going pulse through gate 2042 sets the flip-flop 2038 and inhibits a gate 2046 for its duration, the other input thereof being connected to the high Q output of the flip-flop 2038.

During the period of the 1.8 millisecond pulse the buffer memory is prepared for operation in its read/restore operational mode by which the data may be read out to the scoreboard and also restored in the memory without being destroyed. This is accomplished by the low signal at the $\overline{Q}$ output of flip-flop 2038 which is NOR'd at gate 2048 and inverted by negator 2050 to actuate the single shot multivibrator 2052. A 10 microsecond low going pulse therefore appears on the read/restore bus 2054 and is delivered thereby to the buffer memory control circuits in FIG. 19. From junction 1946 the 10 microsecond low going pulse is fed to a reset input of flip-flop 1914 to provide a low signal to the read/write control input of the butter memory. This low input signifies a read operation mode for the buffer 711.

The low at junction 1946 also resets flip-flop 1920 causing a high input to the BQ terminal and a low input to the memory/buffer terminal. These inputs prepare the buffer memory so that each data word in its contents will first be readout to the data lines and then read back into the proper data addresses in the buffer for further storage. The clear address register terminal CL.AR also receives a negative signal through NOR gate 1948 and negator 1950 which performs the function of clearing the buffer address register so that the buffer contents can be read out from the first address to the last in the same sequence that the data had been read in.

Returning to FIG. 20, when the 1.8 millisecond inhibiting pulse at the input of gate 2046 ceases, the gate opens to trigger the BMPOB sync gate flip-flop 2056 to its set condition producing a high at one input of NAND gate 2058. Gate 2058 is thus enabled to pass strobe signals therethrough from the 2 kc. clock 1936 and strobe conductor 1952. The 2 kc. pulses are fed from the strobe gate 2058 over the sync A conductor 2060 through NOR gate 1954 and negator 1956 to the sync A input of the buffer memory Pulses from strobe gate 2058 are also applied through negator 2062, NAND gate 2064, count conductor 2066, NOR gate 1958 and negator 1960 to the count input terminal of the buffer memory. The sync A and count pulses thus automatically cycle the contents of the buffer to read the data to the signal logic 702 and the scoreboard as well as restore the date in the buffer memory. The buffer contents continue to cycle until the address register 511 is detected at the address register outputs by the NAND gate 1962 which produces a low signal on the AR511 conductor to reset terminals of the BMPOB SYNC gate flip-flop 2056 and the read/restore flip-flop 2038 through NOR gate 2068 and negator 2070. The buffer memory address 511 indicates that the full contents of the buffer have been read out of the buffer onto the data lines to the signal logic and stops the read/restore operation.

It was mentioned in the description of the block diagram of Fig. 7 that provisions are made in the memory control logic for reading the contents of the buffer memory into the magnetic tape memory 710 and the punched tape typewriter and reader 708. These functions may be controlled by circuits quite similar to that just described for reading the buffer memory contents to the scoreboard and since they may be easily fabricated by a skilled artisan from the teachings herein, they are not shown on the schematic diagram or discussed in detail in the specification.

## UPDATING FUNCTION

As will be recalled, the updating function is normally used to change old information stored in the buffer memory to new information. The message to be updated is inserted into the buffer memory usually from the magnetic tape where it is stored for repeated useage. The particular portion of the message to be updated is identified in the buffer by the address of the indicator on which the information is to be displayed. That is, the buffer contents are circulated therethrough and when the data pertaining to the indicator on which the updated information is to be displayed appears at the buffer output the circulation of the data is stopped automatically.

The updating function will perhaps be best understood first by a simplified discussion with respect to the block diagram of FIG. 23 followed by a detailed description with respect to the schematic diagram of FIGS. 15—21.

The message to be updated is entered in to the buffer memory 711 by any suitable means but ordinarily from the magnetic tape storage 710. The address of the particular indicator to be updated will be present somewhere of the particular indicator to be updated will be present somewhere in the message contained in the buffer memory The address of the desired indicator is written by single button address keys or by the console keyboard into the address encoder 712 where it is stored during the update function. An Update Enable signal is generated on conductor 1566 by the address and word control 716 upon storage of the address data to start the automatic update function. The contents of the buffer memory is circulated therethrough and the address for each data segment is checked in an address comparator 2300 with the address encoded and stored in the address encoder circuit 712. Each address circulating through the buffer memory is compared digit by digit with the address in the address encoder 712. The address digit counter 736 in the signal logic acts as the synchronizing means for matching the digits of the stored address in the encoder 712 with the respective digits of the circulating addresses in the buffer memory 711 in the following manner.

The contents of the buffer memory are caused to cycle automatically by means of clock pulses and the data at its output is provided over board data bus 715 to the character decoder interface 730.

Each time an indicator address appears in the data output of the buffer memory and at the character decoder interface 730 the address counter 736 is caused to produce a pulse for each digit of the address. These pulses are transmitted over count 1 through 4 conductors 1068*a* through *d* to the address and word control 716 where they trigger the readout pulses ROYTA, ROYUA, ROXTA and ROXUA. The readout pulses cause the sequential readout of each digit of the address stored in the address encoder 712, on the $\overline{AC\,1}$ through $\overline{AC\,4}$ conductors to the address comparator 2300.

The buffer output is also transmitted to the address comparator 2300 via the conductors 1980*a* through *d*. Thus, each of the address digits from the buffer memory and from the ad-

dress encoder appear simultaneously in the address comparator **2300** where they are checked for identity. If all four digits of the address are not identical the buffer memory will continue to cycle to the next address coded in the buffer contents message which again triggers the address counter **736** to cause the sequential readout of the digits of the encoded address in the address encoder **712** for comparison with the address digits at the output of the buffer memory **711**.

When all four digits of the buffer memory address compare identically with the encoded address an update coincident signal appears on conductor **2128** which through the memory logic control **718** stops the cycling of the buffer memory contents and restores the remainder of the circuits for ordinary operation. The keyboard **302, 304** may now be used to correct the character display data associated with he address found in the buffer memory.

The date circulating through the buffer memory and to the character decoder interface **730** during the update function is prevented from being sent to the scoreboard for display be means of an update enable signal on conductor **1566** generated in the address and word control **716** responsive to a readout signal from the address encoder **712** on conductor **1502** indicating that an address has been stored therein along with an update set signal on conductor **2102** generated in the memory logic control **718** responsive to operation of the message update switch **628**.

The address of the indicator to be updated may be read into the address encoder **712** by means of one of the single button address keys such as shown in the console portion **602** or it may be written in a digit at a time by means of the numeric keyboard **302**. If the single button address is used the readout signal on conductor **1502** appears immediately upon the storage of the address to signal the address and word control to generate the update enable signal and start the address seeking function as previously described. If the address is to be inserted by means of the keyboard **302**, the update enable signal is prevented, as well as the operation of the buffer memory to circulate the data, until the address has been encoded in the address encoder **712** in the following manner.

THe address data is encoded into the storage circuit in the address encoder **712** by means of the Y and X storage circuits in the signal logic **702**. The special character SA and the four address digits are read into the Y address storage **738** and the X address storage **740** in the signal logic in the manner described for the direct keyboard input to the scoreboard. Upon completion of the storage of the address digits in the address storages **738** and **740** and address stored (AS) signal is applied to the address and word control **716** which in turn produces an update readout (UDRO) signal on conductor **1592** to the Y and X address storage circuits to cause them to read the address digits over a multiline conductor **1080***a—f* to the input of the address encoder **712**, causing them to be stored therein. The readout signal is now generated on conductor **1502** which initiates the address search in the manner previously described for the single button address input.

Referring now to the schematic diagram FIGS. **10** through **21**, the detailed description of the updating function will now be made.

For the purpose of this explanation it will be assumed that the inning number appearing on indicator **115** (address **Y03X01**) for the Out of Town Games display is to be changed from **8** to **9**. As previously described, this indicator may be addressed by the appropriate keys in the Out of Town Games format portion **602** of the console.

The update function is initiated by depressing the update message button **628** (FIG. 6) which closes contact **628***a* to set the update message flip-flop **2100** (FIG. 21). The Q output produces a high going update set signal on the UD Set line **2102**. The high signal is used to enable gate **1562** in the address and word control **716** (FIG. 15) and prepares NAND gate **1982** in the buffer memory control circuits (FIG. 19). The operator then presses Out of Town Games format buttons, **604, 606** and **608** to address the indicator displaying the inning number 8 in the Out of town Game display. The address for this indicator being **Y01—X03** causes low inputs to set the appropriate address encoder flip-flops **1404***b*, **1404***c* and **1404***h* . The low inputs to the flip-flops **1404***b c* and *h* are also delivered through appropriate ones of the **ST1—11** conductors to the NOR gates **1500***a* , **1500***b* (FIG. 15) to produce a high going readout signal on conductor **1502** to the other input of the update set enabled NAND gate **1562**. The update flip-flop **1510** is thus set. The ground $\overline{Q}$ output inhibits gate **1533** preventing the clear storage B signal and inhibits gate **1508** to prevent triggering of the 1 to 15 counter **1512**. The ground $\overline{Q}$ signal is also inverted by negator **1564** to provide the update enable signal on the Ud En conductor **1566**.

The Ud En signal enabled NAND gates **1568***a* through d and is also transmitted to the Y and X address storage circuits **738** and **740** in conductor **1566** to prevent storage of address data therein. The high going UD EN signal is inverted by negators **1060, 1062, 1064** and **1066** to inhibit NAND gates **1026, 1034***a*through *d*, **1114***a* and *b*, and **1116***a* through *d* placing high voltage at the set inputs of each of the storage flip-flops in the Y and X address storage circuits. The inverted UD EN signal taken from the inputs of NAND gates **1114***a* and **1114***b* in the X address storage circuit (FIG. 11) on the conductor **1170** is passed through two isolating negators **1172, 1174** to produce a low signal on the erase reset conductor **1220**. As previously described, the erase reset forms an input to the lamp strober enabling gate **1218**, and consequently the lamp strober is inhibited from operation during the update function.

With the address storage circuits and the lamp strober in the signal logic inhibited the indicator address data in the buffer storage message may be sought in order to perform the update. The circulation of the buffer contents for comparing the address data therein, with the address data stored in the address encoder **712** is initiated by the low going signal on conductor **2103** (FIG. 21) at one of the set inputs to Nor gate flip-flop **2104**, the low going signal being developed by negator **2106** from the UD EN signal on conductor **1566**. The high going signal from flip-flop **2104** in Nanded at gate **2108** with the high Q output of the previously set update message flip-flop **2100**, placing a low signal on conductor **2110** to the buffer memory control circuit, to cause the buffer memory to perform a read/restore operation. That is, the low input to NOR gate **2048** which also appears as a low at the output of inverter **2050** causes the 10 microsecond low going pulse to be produced on the bus read/restore conductor **2054** which causes the proper control inputs for performing the read/restore function of the buffer memory **711** in the manner previously set forth in the section for Posting the Buffer Contents on the Board. The sync A and count pulses for circulating the buffer memory contents are also initiated by the UD EN signal which enables strobe gate **1970** (FIG. 19) through delaying Nand gate **1972** and negator **1974**, the output of gate **1970** feeding the input of the sync A and count Nor gates **1954** and **1958**, respectively. The buffer contents are circulated by 20 KC master clock pulses delivered to the other input of the strobe gate **1970**, and these pulses are in actuality derived from the master clock **1214** in the signal logic lamp strobe circuit **750**.

The circulating buffer data is read out to the signal logic **702** via the board data bus **715** since the UD EN signal enables the buffer memory readout gates **1944***a—g* through negators **1978** and **1976**. In addition, the real and inverted signals of the first four bits of the buffer memory data output are transmitted over multiline conductor **1980** to the address comparison circuit **2300** (FIG. 21), the first four bits being all that is required for identifying numerical digits.

Each block of address data in the buffer contents fed to the signal logic will, of course, be recognized by the special address character SA which precedes all address data. The SA character steps the 1 to 5 counter **1004** in the address counter **736** to its first count and each of the succeeding four address digits received from the buffer successively step the counter **1004** through its second to fifth counts in the same manner as

described during the description of the signal logic circuits. Since the Y and X address storage flip-flops have been disabled by the UD EN signal the address counter counts have no effect on these circuits. Rather, count 1, count 2, count 3 and count 4 signals are produced on conductors 1068*a*—*d* which lead to the previously enabled NAND gates 1568*a*—*d* in the address and word control 716 through negators 1750*a*—*d*. The NAND gates 1568*a* through *d* produce sequentially appearing update 1, update 2, update 3 and update 4 pulses at their outputs which at the outputs of NOR gates 1519*a* through 1519*d* appear as the readout Y ten's address (ROYTA), readout Y units address (ROYUA), readout X ten's address (ROXTA), readout X units address (ROXUA). These readout signals strobe the NAND gates 1406*a* through *k* in the address encoder (FIG. 14) in the manner described for single button addressing to cause the readout at the outputs of the NOR gates 1408*a* through *f* of the address data stored in the address encoder flip-flops 1404*a* through 1404*k*. The address data is not read out to the signal logic since the nonoperation of the S.K.I. switch contacts 1411*b* disenable NAND gates 1410*a* through 1410*g*. Bits 1 through 4 are applied to NAND gates 1440*a* through *d*, previously enabled by the UD EN signal and the outputs thereof are fed via the $\overline{AC1}$ through $\overline{AC8}$ conductors to the address comparison circuit 2300 (FIG. 21).

Thus, it may be visualized that each time an address appears in the buffer contents circulating past the buffer output, the address counter in the signal logic is actuated by recognition of the SA character and each numeral character in the address. At the same time the first four bits of the buffer contents data are being presented directly to the address comparison circuit 2300. The address counter controls the readout signals to the address encoder to read out the numeric data for the corresponding address digits stored to the address comparison 2300 in synchronism with the respective digits from the buffer. Therefore, the Y ten's address digit from the buffer output appears at the address comparison circuit 2300 coincident with the Y ten's address digit from the address encoder 712, and likewise for the Y units digit, the X ten's digit, and the X units digit.

The address comparison circuit 2300 (FIG. 21) operates in the following manner to compare the first four bits of the address digits from the buffer memory with the address digits from the address encoder. As may be seen in FIG. 21, a series of 8 NAND gates 2112*a* through *d* and 2114*a* through *d* receive input signals from the various outputs of the buffer memory and the address encoder. For example, NAND gate 2112*a* compares bit 1 (binary weight 1) of the address encoder output with the inverse of the bit 1 output from the buffer memory 711. Gate 2112*b* compares the second bit output (binary weight 2) of the address encoder with the inverse of the second bit output of the buffer, and gate 2112*c* compares the third bit output (binary weight 4) of the address encoder with the third bit output from the buffer memory, and likewise for NAND gate 2112 (binary weight 8). Gates 2114 on the other hand compare the real bit four outputs of the buffer memory with the inverse bit outputs of the address encoder. Each of the NAND gates 2112*a* through *d*, 2114*a* through *d* is strobed by the 20 kc. master clock through NAND gate 2116 and negator 2118 so that the comparison function is synchronized with the circulating data in the buffer memory.

It can be determined that unless each and every bit from the buffer memory compares with each and every bit from the address encoder for each digit of the addresses, a low signal will appear on at least one of the NAND gate output conductors 2119, 2120 connected to reset terminals of the NOR gate flip-flop 2122. The flip-flop 2122 is pulsed to its set state for each address circulating in the buffer memory by means of the special address character on the SA line 734 from the alpha-numeric decoder 732 in the signal logic. Thus, if any one of the digits in the buffer memory address does not compare with the corresponding digit of the encoded address, one of the gates 2112*a*—*d*, 2114*a*—*d* will be satisfied resetting flip-flop 2112, and the input conductor 2124 to the update coincidence NAND gate 2126 will go low before the completion of the comparison. If, however, each and every bit of the four address digits do compare, the flip-flop 2122 is not disturbed from its set condition and a high therefor appears on conductor 2124 to the coincidence gate 2126. This is NANDed with the update 4 count produced in the address and word control 716 (FIG. 15) which of course results in the readout X ones (ROXUA) address signal to the encoder. The update 4 signal prevents a coincidence signal until the last digit of the address has been compared. The coincidence gate 2126 is further synchronized by clock pulses from the master clock, and a low going pulse is provided on the UD coincidence conductor 2128 to the set input of the coincidence flip-flop 2130.

Consider the example in which the character data for the inning appearing on indicator Y03—X01 is to be updated. The address comparison gate will ignore all addresses appearing in the buffer contents to formulate the Out of Town Games display shown in FIG. 1 except the desired address. The address and character display data for the word AMERICAN as well as INN, R, P and 1G for both sides of the board will all cause the flip-flop 2122 to be reset as they are compared with the encoded address or indicator Y03—X01.

For example, the first address appearing in the buffer contents will be the address for indicator 105 (FIG. 1) displaying the letter A. This indicator has an address of Y01–X11. When the Y ten's digit zero is compared with the ten's digit of the encoded address Y03–X01 there will be a coincidence and hence no reset signal on either of conductors 2119 or 2120 of the address comparison circuit. The Y units digits do not coincide, however, since the encoded digit is a 3 while the buffer memory address digit is *a*1. Thus, the encoded digit has the binary code 0011 and the buffer memory address digit has the code 0001. The bit 1 gates 2112*a* and 2114*a* are not satisfied since the inputs to these gates are opposite each other, when there is coincidence in the address data. Gate 2112*b* is satisfied, however, because the $\overline{AC2}$ line provides a high signal representing the binary weight 2 in the code for the number 3 and the inversed second bit from the buffer memory is also high representing a zero for the binary weight 2 bit of the buffer memory number. Thus, a low appears at the output of gate 2112*b* causing a reset of the flip-flop 2122. It remains in the reset condition until the SA character of the next address is encountered in the buffer memory. Coincident of any of the remaining digits of the address has no effect since the flip-flop 2122 is already reset.

When the buffer memory address Y03 X01 is encountered none of the NAND gates 2112*a* through *d* or 2114*a* through *d* will be satisfied and the flip-flop 2122 will remain in its set condition through out the comparison of all four digits of the address.

The low going update coincidence signal controls the operation of the buffer memory control circuits to stop the buffer contents circulation and reset all of the circuits for insertion of the updated display data. The update coincidence signal is transmitted on conductor 2128 to the address and word control 716 (FIG. 15) where it is NOR'd at gate 1572 with the AR 511 signal from the output of NAND gate 1962 which detects the address register number 511 indicating the end of a message in the buffer. Thus, a low signal is presented to the set terminal of flip-flop 1574 through negator 1576 if the encoded address is found in the buffer memory, or if the end of the buffer message is reached without finding a coincidence. The high Q output of flip-flop 1574 is NANDed at Gate 1578 with a high signal developed through negator 1580 from the normally low readout conductor 1502. The low output of gate 1578 is NOR'd in gate 1582 producing a low at the output of negator 1584 to reset the update flip-flop 1510. The low going $\overline{Q}$ output of flip-flop 1510 resets the flip-flop 1574 and the high going Q output of 1510 causes the removal of the UD EN signal. Thus, the Y and X address storage circuits are restored for normal operation and the address comparison function is

disabled. A clear storage B signal appears on conductor **1535** in view of the high going $\overline{Q}$ outputs of flip-flops **1506** and **1510**, which resets the storage flip-flops in the address encoder and the circuits are essentially back to normal in preparation for insertion of the updating character display data to be inserted in the buffer memory contents in the position immediately following the desired address.

The update coincident low going signal also pulses a set terminal of the read/write flip-flop **1914** in the buffer control. This sets the buffer for a clear/write operation which consists of erasing whatever is stored within the buffer at the particular address location and writing new information into that location.

The data is inserted into the buffer from the console keyboards **302** or **304** as previously described and the keyboard sync B signal on conductor **1824** is converted to a keyboard sync A pulse by means of NAND gate **1982** which pulses the count and sync A inputs of the buffer memory. It will be noted that the update set signal and an update message indicator signal are NANDed by gate **1826** (FIG. **18**) to enable the keyboard to buffer memory data NAND gates **1820***a* through **1820***f*. The update message indicator signal is developed on conductor **2132** from the high Q output of the update coincidence flip-flop **2130** FIG. **21**) which also actuates a light **2134** in the Update Message button **628** to indicate the desired address has been found.

The console numerical keyboard may be used to encode the address of the indicator for updating in place of the single button address keys as previously described. As in the previous case the update function is initiated by depressing the update message key **628** which, by means of update message flip-flop **2100**, provides the high going update set signal on conductor **2102**. This signal is inverted by negator **1827** and NOR'd in gate **1816** to provide the keyboard to data bus enabling gates **1802***a* through **1802***g* with an enabling signal and permit the signals generated by the keyboard to flow via the board data bus **715** to the signal logic **702**.

The operator then presses the special address character button SA which is recognized by the alpha decoder **732** (FIG. **12**) in the ordinary manner to set the Y and X address storage circuits for storage of the succeeding address data. The SA signal, which is a ground signal on conductor **734**, is delivered to the address and word control circuit **716** where it is first inverted by a negator **1586** and NANDed at gate **1588** with the update set signal to set the keyboard update flip-flop **1590**. The high Q output therefrom forms one input to a NAND gate **1591** which also has a high third input from the Q output of the update flip-flop **1510** which is still in its reset condition. The gate **1591** remains closed, however, until an address stored signal is received which, as previously described, appears when all four of the address digits have been stored in the Y and X address storage circuits. When this occurs, the gate **1591** is satisfied and a high update readout (UDRO) signal appears on conductor **1592** from the output of negator **1594**. The UDRO signal strobes NAND gates **1070***a* through *e* at the output of the Y address storage **738** as well as the NAND gates **1176***a* through *f* at the output of the X address storage **740**. The outputs of the NAND gates **1070***a* through *e* and **1172***a* through *f* have appropriate connections **1080***a* through *e* and **1180***a* through *f* to the inputs of the associated NOR gates **1400***a* through **1400***k* in the address encoder **712** (FIG. **14**). Thus, the UDRO signal causes the readout of the Y and X addresses from the respective storage circuits to the address encoder wherein the appropriate flip-flops **1404***a* through **1404***k* are pulsed to their set condition. The read in of the address causes signals on the appropriate ST1 through **11** conductors and the NOR gates **1500***a*, **1500***b* therefor produce a readout signal to set the update flip-flop **1510**. The update enable signal UD EN is thus generated in the manner prescribed for single button address input updating function. From here the circuit operates in exactly the same manner as previously described to seek out the encoded address in the buffer memory contents so that the updated display character data may be inserted in its proper place in the buffer contents.

What we claim is:

**1**. In a display system having a display board, a plurality of display devices at address locations on said board, a logic control system, a storage memory input means having stored therein serially time sequenced segments of address and display data to address and actuate desired display devices for displaying a particular message, and means in the logic control operative responsive to the input of each data segment from said storage memory input means for selecting and actuating each addressed display device, apparatus for updating the display data for at least one of said desired display devices comprising means for encoding address data of said one display device, means for comparing the encoded address data of said one display device with the address data in each data segment in said storage memory input means to locate the data to be updated, and manually operable means for erasing the display data for said one display device in said storage memory input means and for entering the updating display data.

**2**. The display system of claim **1** wherein said display devices are located by numerical addresses and wherein said storage memory input means contains the address data for said desired display devices in binary coded decimal form.

**3**. The display system of claim **2** wherein said address data encoding means comprises at least one bistable device for each digit of the address data to register said address data in binary coded decimal form and manually operable means for setting each bistable device to one of its bistable states dependent on the value of the digit to be represented, and wherein said comparing means compares each digit of the address data circulating in said buffer memory means with each corresponding digit registered by said address encoder bistable devices.

**4**. The display system of claim **3** wherein said address encoder manually operable means comprises a single key for registering simultaneously each digit of the address for said one display device to be updated in said bistable devices.

**5**. The display system of claim **3** wherein said address encoder manually operable means comprises a typewriter-type keyboard and means responsive to said keyboard for serially registering each digit of the address for said one display device to be updated in said bistable devices.

**6**. A display system having a display board, a plurality of display devices at address locations on said board, a logic control system, a storage memory input means having stored therein serially time sequenced segments of address and display data to address and actuate desired display devices for displaying a particular message, and means in the logic control operative responsive to the input of each data segment for selecting and actuating each addressed display device, in combination therewith: apparatus for updating the display data for at least one of said desired display devices comprising buffer memory means having an input and output for receiving and storing the data segments of the particular message from said storage memory means, means for encoding address data of said one display device, means for causing said buffer memory to cycle the data segments therein past said buffer memory output, means for comparing the encoded address data of said one display device with the address data in each data segment as it passes said buffer memory means output, means responsive to the coincidence of the encoded address data with the corresponding cycling address data in said comparing means for stopping the cycling of said data segments in said buffer memory means, manually operable means for erasing the display data for said one display device in said buffer memory memory means and for writing in the updating display data, and means for returning all of said data segments to said storage memory input means in the original serial time sequence.

**7**. The display system of claim **6** wherein said display devices are located by numerical addresses, wherein said storage memory input means contains the address data for said desired display devices in binary coded decimal form and wherein said buffer memory means receives, stores and cycles the address data for said desired display devices in binary coded decimal form.

8. The display system of claim 7 wherein said address data encoding means comprises at least one bistable device for each digit of the address data to register said address data in binary coded decimal form and manually operable means for setting each bistable device to one of its bistable states dependent on the value of the digit to be represented, and wherein said comparing means compares each digit of the address data circulating in said buffer memory means with each corresponding digit registered by said address encoder bistable devices.

9. The display system of claim 8 wherein said address encoder manually operable means comprises a single key for registering simultaneously each digit of the address for said one display device to be updated in said bistable devices.

10. The display system of claim 8 wherein said address encoder manually operable means comprises a typewriter type keyboard and means responsive to said keyboard for serially registering each digit of the address for said one display device to be updated in said bistable devices.

11. A display system comprising a display board, a plurality of display devices at address locations on said board, a logic control system, a buffer memory, means for entering and holding serially timed sequenced address and display data segments pertaining to desired indicators and desired display data into said buffer memory, means for selectively entering said serially time sequenced segments of data from said buffer into said logic control to address and actuate desired display devices, means in said logic control for decoding each data segment to select and actuate each addressed display device and means for selectively reading said serially timed sequence segments of data back to said data entering means.

12. The display system of claim 11 wherein said data entering means comprises a punched tape typewriter and reader, and wherein said data reading back means is adaptable to cause said typewriter and reader to type out said data segments.

13. The display system of claim 11 wherein said data entering means comprises a punched tape typewriter and reader and wherein said data reading back means is adaptable to cause said typewriter and reader to punch a tape in accordance with said data segments.

14. The display system of claim 11 wherein said data entering means comprises a magnetic tape storage memory capable of having stored therein serially time sequenced segments of address and display data for addressing and actuating desired display devices for displaying a particular message, and means for transferring data from said tape storage memory to said buffer memory.

15. The display system of claim 14 comprising means for transferring data stored in said buffer memory into said magnetic tape storage memory.

16. In the system of claim 14 wherein means are provided for reading serially time sequenced segments of data from said buffer into said magnetic tape storage memory to store said data therein.

17. The display system of claim 14 comprising in addition means for entering address and display data into said signal logic directly from said magnetic tape storage member.

18. The display system of claim 12 comprising in addition apparatus for updating the display data in said buffer memory for at least one of the desired indicators, said apparatus comprising means including said keyboard for encoding address data of said one display device, means for comparing the encoded address data of said one display device with the address data in each data segment in said buffer memory to locate the data to be updated, and manually operable means for erasing the display data for said one display device in said buffer memory and for entering the updating display data.

19. The display system of claim 14 comprising in addition apparatus for updating a data segment pertaining to one of the display devices for said particular message comprising means for encoding the address data of said one display device, means for comparing said encoded address data with the address data in each of the data segments of said particular message transferred into said buffer memory from said tape storage memory to locate the data to be updated, and means including a manually operable keyboard for erasing the display data for said one display device in said buffer memory and for entering the updating display data.

20. The display system of claim 19 comprising in addition means for transferring data from said buffer memory to said tape storage memory.