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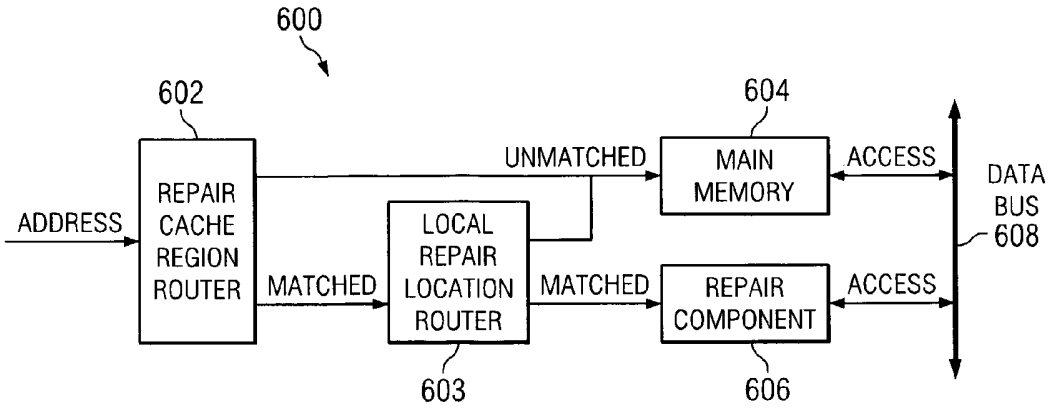
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(54) **Title:** SET ASSOCIATIVE REPAIR CACHE SYSTEMS AND METHODS



(57) **Abstract:** The invention facilitates scaling of memory devices and operation thereof by employing a set associative repair cache system to correct or repair identified faulty memory cells. A repair cache region router (602) compares a repair region portion of a memory address to repair cache regions to identify a matching repair cache region. Then, a local repair location router (603) compares a repair address portion of the memory address to a local repair location addresses particular to the matching repair cache region to identify a matching local repair address. If a matching local repair address is identified, a repair component (606) provides access to a repair data location according to the matching local repair address and the matching repair cache region. Otherwise, a main memory (604) provides access to a memory location according to the memory address. Other systems and methods are disclosed.

WO 2006/039406 A1

SET ASSOCIATIVE REPAIR CACHE SYSTEMS AND METHODS

The invention relates generally to memory devices; and, more particularly, to systems and methods for repairing/replacing faulty memory locations in memory devices.

BACKGROUND

Storage capacities of semiconductor memory devices continue to increase while integrated circuit dies on which the memory devices are fabricated continue to decrease. As a result, the number of memory cells present in memory devices and the complexity of the memory devices continues to increase, as well. Additional memory cells and complexity require additional sense amplifiers, charge supply circuitry, addressing mechanisms, decoders, and the like. Further, the dimensions of components and structures present in memory devices necessarily shrink in response to the additional storage capacity. As a consequence, memory cells of memory devices can be more sensitive to defects, residues, and contaminants than memory cells of prior, smaller storage capacity memory devices. Such defects and contaminants can cause memory cells to be inoperable and unusable.

One way to mitigate defects and contaminants and reduce the number of resulting defective cells is by using tighter semiconductor fabrication process control and layout design or architecture. However, the ever-shrinking dimensions and increase in storage capacity can counteract the benefits of tighter process control and improvements in layout design or architecture. As a result, a significant number of memory devices are fabricated that include one or more defective memory cells. Without some type of correction mechanism, such memory devices can be unusable or introduce errors by their use.

One type of correction mechanism is to fabricate a number of redundant rows for memory devices. The numbers of redundant rows are formed in addition to original rows of memory cells. Then, during testing, faulty memory cells and associated rows are identified. Subsequently, a selection device, such as a fuse, is employed to enable redundant rows to replace identified defective rows. As a result, addressing to memory cells in the original rows is rerouted to the replacement, redundant rows of memory cells. Thus, defective memory cells/rows are not apparent to external devices.

Another type of correction mechanism is to fabricate a number of redundant columns for memory devices, in addition to original columns of memory cells. Defective or faulty memory cells/columns are then identified during testing. Subsequently, associated columns

are replaced by one or more of the redundant columns by utilizing a selection mechanism, such as a fuse. Accordingly, addressing to memory cells located in defective/faulty columns is rerouted to assigned redundant columns of memory cell. These defective memory cells/columns are not known to external devices.

One problem with the above correction mechanisms, redundant row replace and redundant column replace, is that large numbers of non-faulty cells can be needlessly replaced. For example, a single faulty memory cell, under a redundant row mechanism, requires that the entire row containing the single faulty memory cell be replaced. A single row in a memory device can have a large number of memory cells present, such as 512 or 1024 memory cells. Thus, one faulty memory cell can cause the other cells in the row, such as 511 or 1023, to be replaced. Such inefficiencies can reduce the storage capacity of memory devices by consuming valuable space on dies in order to provide for redundant rows and/or columns.

SUMMARY

The invention facilitates scaling of memory devices and operation thereof. A relatively efficient repair cache system is employed to correct or repair an identified faulty memory cell, instead of a complete row or column replacement. The possible increased efficiency can allow for fewer repair memory cells to be employed than conventional mechanisms, thereby saving die area.

The repair cache system stores a list of repair cache regions and lists of local repair location addresses associated with the repair cache regions. Additionally, the repair cache system maintains repair data locations that can be employed to repair or replace faulty memory cells present in main memory. The repair data locations are accessed by a matching repair cache region and a matching local repair location address during operation. Other systems and methods are disclosed.

Advantages and features of the invention will become apparent from the detailed description of example embodiments below.

BRIEF DESCRIPTION OF THE DRAWINGS

Example embodiments of the invention are described with reference to accompanying drawings, wherein:

FIG. 1A is a schematic view, illustrating random, isolated defects that can result from

chemical mechanical planarization.

FIG. 1B is a schematic sectional view, illustrating random, isolated defects that can result from via and contact voids during memory device fabrication.

FIG. 1C schematically depicts formation of a blister in an example semiconductor device.

FIG. 2A illustrates a memory array of non-volatile memory with random defects therein.

FIG. 2B shows a non-volatile memory cell.

FIG. 3A illustrates repair row correction mechanisms.

FIG. 3B illustrates repair column correction mechanisms.

FIG. 3C illustrates block repair correction mechanisms.

FIG. 4 illustrates operation of a repair cache in accordance with principles of the invention.

FIG. 5 illustrates a portion of a memory array configured for a set associative repair cache in accordance with principles of the invention.

FIG. 6 is a block diagram illustrating a repair cache system in accordance with principles of the invention.

FIG. 7 is a block diagram illustrating an associative repair cache system in accordance with principles of the invention.

FIG. 8 illustrates an example repair register bank in accordance with principles of the invention.

FIG. 9 depicts repair data locations for a first repair cache region and a second repair region in accordance with principles of the invention.

FIG. 10 is a flow diagram illustrating a method of operating a set associative repair cache in accordance with principles of the invention.

FIG. 11 is a flow diagram illustrating a method of configuring a repair cache system in accordance with principles of the invention.

DETAILED DESCRIPTION OF EMBODIMENTS

The invention facilitates scaling of memory devices and operation thereof by disclosing a repair cache employed for repairing or replacing identified faulty memory cells. The repair cache can attain increased efficiencies relative to conventional row or column

replacement correction mechanisms. The increased efficiency can mitigate the number of repair cells or locations employed, thereby reducing die area consumption.

Redundant rows of memory, redundant columns of memory, and redundant blocks of memory are commonly employed to recover from faulty/defective memory cells. Faulty columns and/or rows that respectively contain one or more faulty memory cells are identified during testing. Then, the faulty columns and/or rows are "corrected" or replaced by an identical number of redundant rows and/or columns. If, for example, entire rows of memory cells are faulty, replacement of the rows by redundant rows is relatively efficient. However, if only a single memory cell within a row is faulty, replacement of the entire row by a redundant row is relatively inefficient.

Some fabrication induced, large area defects can impact large portions of rows, columns, or blocks. For such large area defects, row, column, and/or block replacement mechanisms can be relatively efficient and practical. However, other fabrication defects include random, isolated defects that affect a small, isolated number of memory cells (e.g., one). For these random isolated defects, row, column, and/or block replacement mechanisms are relatively inefficient.

FIG. 1A shows random, isolated defects that can result from chemical mechanical planarization (CMP). In a typical CMP process, precision polishing machines use a fine ceramic slurry to make semiconductor wafer surfaces flat (planar) to, for example, ensure good resolution for later micro-lithography integrated circuit fabrication steps. Some layers formed on semiconductor devices can require a flattening, polishing layer operation in order to promote uniformity and to permit additional layers to be formed thereon. The illustrated CMP process employs a rotating head 102 that is brought into contact with a wafer rotated in an opposite direction. The slurry flows across the wafer surface between the counter-rotating head and wafer. The slurry includes chemicals and particles that facilitate planarization of the wafer. However, the slurry or CMP head can undesirably include residue 104 that causes isolated, random damage to the wafer and memory devices formed thereon. The residue 104 can, for example, abrasively contact metal layers resulting in scratches or missing metal, leading to unwanted open circuits or increased resistance. The random damage can result in random, isolated defects and, as a consequence, random, isolated, faulty memory cells.

FIG. 1B shows random, isolated defects that can result from via and contact voids

during memory device fabrication. Via formation and metallization are commonly performed during memory device fabrication in order to provide electrical connection to capacitors and other structures present within memory devices. However, vias or plugs can be defective in that they are not completely filled or that they were etched improperly thereby not properly connecting underlying structures. As an example, FIG. 1B shows a capacitor 106, a via 108, and a metal interconnect layer 110. In this example, the via 108 was not properly filled and, as a result, there is a void 112 present that breaks or prevents connection from the capacitor 106 to the via 108 and, therefore the metal interconnect layer 110. The void 112 can cause failure of a single memory cell by preventing access to the capacitor 106, but does not generally impact neighboring memory cells. As a result, the void 112 creates a random, isolated defect.

FIG. 1C shows random, isolated defects that can result from etch or CMP residue during memory device fabrication. Etching processes are commonly performed during memory device fabrication, particularly with respect to capacitor formation and metallization. Etch residue from etch processes, such as plasma etching, can remain after completion of the etch process. Additionally, residue from planarization processes can also remain after completion. Subsequently formed layers cover the residue thereby trapping the residue. The formed layers become malformed or distorted as a result. Planarization processes, such as CMP, can damage the distorted layers by sheering off protruding crests, referred to as blisters.

FIG. 1C (see lower view) depicts formation of a blister in an example semiconductor device. An etch process is performed that leaves undesired etch residue 114 on the device. A field oxide layer (FOX) 116, in this example, is formed and distorted due to the presence of the residue 114. A metal layer deposition and planarization process 120 are then performed that results in formation of a blister 118 that breaks the field oxide layer 116. The blister 118 can lead to shorting and/or other problems and result in faulty memory cells. The blisters, such as the blister 118, are a result of the undesired etch residue that remains after etching. The residue is typically randomly distributed. As a result, the blisters formed, and therefore the memory cells impacted, are also randomly distributed.

FIG. 2A shows an example memory array 200 of non-volatile memory with random defects therein. The memory array 200 may be formed of recent nonvolatile memory types,

such as ferroelectric memory (FeRAM), Magnetoresistive Random Access Memory (MRAM), or Ovonic Unified Memory (OUM). These memories include new layers for memory elements that exist between a substrate and upper metal layers that, therefore, have a high probability of being damaged by CMP or etch process residues that can result in random, isolated bit failures. The newer non-volatile memories contain electrodes and special films or layers for electric fields, magnetic fields, and simple resistance. Random defects to these electrode layers or special films or layers are potential sources for weak or faulty bits, which likely are isolated random defects not efficiently solved by replacing entire rows, columns, or blocks. These defects can result from CMP processes, etching and leaving residues, plasma etching and leaving residues, forming oxide layers and leaving residues, forming other layers and leaving residues, etc., and can introduce open circuits into the electrodes or special layers.

FeRAM memory cells utilize ferroelectric capacitors that possess two characteristics required for a nonvolatile memory cell: That is, to have two stable states corresponding to the two binary levels in a digital memory, and to retain their states without electrical power.

MRAM is a method of storing data bits using magnetic charges instead of the electrical charges used by DRAM (dynamic random access memory). A metal is defined as magnetoresistive if it shows a slight change in electrical resistance when placed in a magnetic field. By combining the high speed of static RAM and the high density of DRAM, proponents say MRAM could be used to significantly improve electronic products by storing greater amounts of data, enabling it to be accessed faster while consuming less battery power than existing electronic memory.

OUM uses thin-film materials to store information economically and with excellent solid-state memory properties. The thin-film material is a phase-change chalcogenide alloy similar to the film used to store information on commercial CD-RW and DVD-RAM optical disks.

Optical memory disks use laser light to write small spots by converting the thin film back and forth from amorphous (disordered atomic structure) to crystalline (regular, highly repetitive, and ordered atomic structure). The digital data of 1s and 0s are stored as amorphous (high resistance and non-reflective) or crystalline (low resistance and reflective) structures. OUM devices store data in a similar manner but use electrical energy controlled

by small transistors to electronically convert the material to crystalline or to amorphous (thus a 1 or a 0). This electronic solid-state memory stores data in a much smaller area and with higher speeds for both read and write than its optical counterpart.

The operating speed of OUM memory technology is similar to DRAM and many orders of magnitude faster than Flash write. Also, unlike conventional Flash memory, OUM memory is fully random accessible for memory addressing. Any given bit can be uniquely addressed and then written or read by the customer. Further, Flash memory "wears out" (fails) after 100,000 write cycles, while the OUM memory state can be written more than 10 trillion times, making this memory useful for program storage (Flash) as well as general purpose interactive (DRAM) data storage memory.

The memory array 200 of FIG. 2A is illustrated with two defective memory cells 202 and 204. Defects to special films present in the memory cells cause the cells 202 and 204 to improperly operate, thereby being defective or faulty.

FIG. 2B show a non-volatile memory cell 210. The memory cell 210 is of a more recent design, such as FeRAM, OUM, and MRAM. The memory cell 210 includes a lower electrode 212, a special film 214, an upper electrode 216, and an extra via 218. The special film 214 has properties dependent on the type of memory (e.g., ferroelectric, magnetoresistive, phase-change ability) and can be sensitive to random defects. The special film 214, if damaged, only impacts the memory cell 210 and does not negatively impact other or surrounding memory cells. Similarly, damage to the lower electrode 212 and the upper electrode is limited to the memory cell 210.

The above figures and descriptions illustrate examples of some types of random defects that can occur in semiconductor device fabrication that lead to random, isolated memory cell or bit failures. Some other types of random defects include oxide defects, blisters, missing metal/conductive material, CMP scratches, and CMP residue.

FIG. 3A illustrates repair row correction mechanisms. A memory array 300 is shown comprised of a number of rows of memory cells/bits. Testing identifies first and second faulty memory cells 302 and 304 within the array 300. Redundant repair rows 306 are employed to replace the rows containing the faulty memory cells 302 and 304. A typical row in a memory device includes 1024 memory cells. Therefore, a single defective memory cell requires 1024 memory cells to be replaced. This type of replacement is relatively inefficient

because other cells in the replaced rows were not necessarily defective.

FIG. 3B illustrates repair column correction mechanisms. Here, a memory array 310 is comprised of a number of columns of memory cells/bits. Testing has identified first and second faulty memory cells 312 and 314 within the array 310. Under this correction mechanism, redundant repair columns 316 replace both columns comprising the first and second faulty memory cells 312 and 314. Typical columns are about 512 memory cells tall. Thus, in this example, replacement of a single faulty memory cell requires replacement of 512 memory cells (of which 511 are not defective). Again, this correction mechanism is relatively inefficient for isolated random defects because a large number of cells were replaced that operated correctly.

FIG. 3C illustrates block repair correction mechanisms. A memory array 320 is comprised of blocks of memory cells. Respective blocks are comprised of a fixed number of rows and columns. In order to correct a defective memory cell, an entire block comprising the defective/faulty memory cell is replaced. Testing identified first and second faulty memory cells 302 and 304. In order to correct the identified faulty memory cells 302 and 304, two redundant blocks of memory cells 326 are employed. Once again, this correction mechanism is relatively inefficient as a large number of properly working memory cells are unnecessarily replaced.

FIG. 4 illustrates operation of a repair cache in accordance with an example implementation of the invention. The repair cache is operative to repair/correct faulty memory cells, including those that result from random, isolated defects, in a relatively efficient manner. FIG. 4 shows a memory array 400 comprised of a number of rows and columns. Due to random, isolated defects incurred during fabrication, such as those previously described, a number of faulty memory cells 402 are present. Typically, testing is performed that includes reading and writing to cells within the memory array 400, wherein cells that fail to properly store and maintain correct values are deemed faulty. A repair cache system of the invention is operable to efficiently repair/correct the faulty memory cells 402.

Respective faulty memory locations 402 are replaced by repair data locations 406, also referred to as repair resources and/or repair locations, on a one for one basis. The repair data locations can store a varied number of bits such as, for example, 1 bit, 8 bits, 16 bits, 32 bits, and the like. It is noted that the repair data locations can be a single memory cell. The

faulty memory locations can, likewise, respectively comprise a varied number of bits or a single memory cell. It is further noted that memory cells can be single bit memory cells or multi bit memory cells (e.g., 2 or more bits). Addresses to the faulty memory cells 402 are redirected towards the replacement data caches by address caches 404 that store pointers to the replacement data caches 406. As a result, only a single memory cell or small number of memory cells can be employed to correct a defective memory cell and is, therefore, typically more efficient than row replacement, column replacement, and/or block replacement mechanisms for random, isolated defects.

The repair cache of the invention differs from typical, conventional memory caches. The repair cache of the invention maintains a list of only identified faulty memory addresses and includes separate repair resources aside from a main memory or array. In contrast, a conventional memory cache only maintains a list of cached memory addresses and does not maintain separate resources for the cached addresses. Furthermore, the conventional memory cache stores data from a main memory whereas the repair cache of the invention replaces data from a main memory.

FIG. 5 shows a portion of a memory array 500, configured for a set associative repair cache in accordance with an aspect of the invention. The memory array 500 is given as an example; however, the invention contemplates other memory arrays having alternate sizes or configurations. The memory array 500 has a number of memory locations that are employed to store, maintain, and provide information content. The memory array 500 can be volatile or non-volatile memory and can be of a suitable memory type, such as FeRAM, OUM, and MRAM. The memory locations typically store a word (e.g., 16-bits, 32-bits, 54-bits, etc.) of information content and are addressable by a memory address 501.

At some point, the memory locations are tested in order to identify faulty memory cell locations 504. A number of suitable mechanisms can be employed. One example is to write selected patterns of data to memory cells, read patterns of data from the memory cells, and then compare the read patterns to the written patterns to identify faulty memory cells. Another example is to repeat cycles of writing different values to the memory cells, and then reading the stored values back out of the memory cells, and comparing them. Other suitable mechanisms of identifying faulty memory locations can be employed.

The memory locations of the array 500 are organized or configured into memory

regions 502, which are associated with blocks or groups of memory locations. FIG. 5 depicts the memory regions 502 as blocks, however they can be also be organized in other configurations including, such as rows and columns. Repair cache regions 510 are memory regions 502 that are cached and are allocated repair locations. Typically, only some of the memory regions 502 have identified faulty memory locations. Therefore, only a subset of the memory regions are normally assigned as repair cache regions 510.

A portion of the memory address, referred to as a repair region address 503, is employed to identify memory regions with which faulty memory locations are associated. Accordingly, the repair region address 503 also identifies repair cache regions if the particular memory locations are present in repair cache regions. The repair cache regions 503 respectively include one or more local repair registers or repair locations 506 that can be employed to repair or correct identified faulty memory locations 504 within the respective repair region. A local repair address 507, which is also a portion of a memory location's memory address 501, is employed to access the local repair locations 506 within the repair cache regions.

During read/write operations for the memory array 500, requests for identified faulty memory locations are routed to a particular repair cache region according to the repair region address 503 and a particular local repair location or register within the particular repair region according to the local repair address 507.

FIG. 6 illustrates a repair cache system 600 in accordance with an aspect of the invention. The system 600 is operable to correct for faulty memory cells/locations by having redundant memory cells located in a repair component. The redundant memory cells/locations are accessed instead of the faulty memory cells within a main memory for read/write operations. By employing repair locations, faulty memory cells located within main memory can be accounted for while mitigating the number of redundant memory cells required to do so.

The repair cache system 600 includes a repair cache region router 602, a local repair location router 603, a main memory 604, a repair component 606, and a data bus 608. The system 600 routes memory operations to the main memory 604 or the repair component 606 by analyzing requests for matching repair cache regions and then by local repair locations.

The repair cache region router 602 receives memory addresses for read/write

operations and routes the request to the main memory 604 or the local repair location router 603 according to a repair region portion of the memory addresses. The repair cache region router 602 can comprises tables, data structures, pointers, comparators, and other components that facilitate determining which component to route the request to. The local repair location router 603 receives matching region information from the repair cache region router 602 and routes the request to the main memory 604 or the repair component 606 according to a local region portion of the memory addresses. The local repair location router 603 can also comprises tables, data structures, pointers, comparators, and other components that facilitate determining which component to route the request to.

The main memory 604 comprises volatile and/or non-volatile memory locations, each of which can comprise one or more memory cells (e.g., a word of memory). The memory locations of the main memory 604 are identified as faulty or valid by a suitable testing mechanism, as described below. It is appreciated that suitable testing mechanisms can be employed and yet mistakenly identify valid memory locations.

The repair component 606 also comprises volatile and/or non-volatile memory locations, each of which can comprise one or more memory cells (e.g., a 32 bits). Both the main memory 604 and the repair component 606 can be comprised of a suitable memory type including, but not limited to, ferroelectric memory, magnetoresistive random access memory, ovonic unified memory, dynamic random access memory, and the like.

Prior to performing operational read and/or write operations, the main memory 604 is tested and/or scanned to identify zero or more faulty memory locations within the main memory 604. The faulty memory locations include memory cell(s) of which at least one memory cell is determined or identified as faulty. A number of suitable mechanisms can be employed to identify faulty memory cells and, therefore, faulty memory locations. One example of a suitable mechanism is to write selected patterns of data to memory cells, read patterns of data from the memory cells, and then compare the read patterns to the written patterns to identify faulty memory cells. Another example of a suitable mechanism is to repeatedly perform cycles of writing a first value to memory cells and then read back from the memory cells expecting the first value to be read back and then writing a second value to the memory cells and then reading back from the memory cells expecting the second value to be read back. Other suitable mechanisms of identifying faulty memory locations can be

employed.

Memory locations of the main memory 604 are arranged or configured into memory regions that typically have a fixed number of memory locations therein. After identifying the faulty memory locations, memory regions containing the faulty memory locations are designated as repair cache regions and the faulty memory locations are assigned repair data locations referenced within the repair cache regions by a local address portion of their memory addresses. The repair cache regions for the repair data locations, which replace the identified faulty memory locations, are referenced according to a repair region portion of the identified faulty memory locations' memory addresses. Then, during read/write memory operations, the repair data locations can then be employed instead of the faulty memory locations during device operation.

For read/write operations, the repair cache region router 602 receives a memory address and determines whether the memory address is within a valid repair cache region according to a repair region portion of the memory address. If a matching repair cache region is identified, the matching region is passed to the local repair location router 603, which determines whether the memory address has a valid repair data location according to a local address portion of the memory address. If the local repair location router 603 identifies a matching repair location address, the matching repair cache region and local address are passed to the repair component 606. The matching repair location or register is selected in the repair component 606 according to the repair cache region or the repair address (a portion of the memory address) and the local address (another portion of the memory address). The selected repair location is then coupled to the data bus 608 for read/write access in place of the faulty memory location located within the main memory.

If a matching repair cache region and/or a matching repair location are not identified, the memory address is provided to the main memory 604. A memory location of the main memory 604 referenced by the memory address is then coupled to the data bus 608 for read/write access.

FIG. 7 is a block diagram illustrating an associative repair cache system 700 in accordance with an aspect of the invention. The system 700 is operable to correct for faulty memory cells by having redundant memory cells located in repair data locations, which are accessed instead of the faulty memory cells for read/write operations. By employing repair

regions and repair data locations within regions, storage requirements for addressing repair data locations and contents thereof can be reduced compared with conventional row, column, and/or block repair mechanisms. Furthermore, the reduced storage requirements mitigate die area employed for repairing or correcting faulty memory cells.

The system 700 includes a central processor unit 702, a repair region register bank 708, repair region comparators 709, repair sets 710, local address comparators 718, a repair data bank 722, a main memory 730, and a data bus 726.

The central processor unit 702 is operable to access memory locations of the main memory 730 by memory addresses in order to read to and write from addressed memory locations. It is appreciated that the central processor unit 702 performs other processor related functions and can be one of a number of processors present in an electronic device. The central processor unit 702, as well as some or all of the system 700, can be part of an electronic device such as, but not limited to, a personal computer, a personal digital assistant, a mobile/cellular telephone, a laptop computer, a notebook computer, a digital camera, and the like.

Memory locations of the main memory 730 are arranged and configured into memory regions of a fixed size. Generally, a subset of the memory regions are allocated repair cache locations for repairing or replacing identified faulty memory locations. The subset of memory regions are referred to as repair cache regions. As an example, a main memory comprising 1024 memory regions having 256 memory locations may have only 48 repair cache regions associated with 48 of the memory regions. A further description of this relationship is provided infra. The memory locations of the main memory 730 are addressed by memory addresses. Both the memory regions and repair cache regions are indicated or referenced by a portion of the memory addresses referred to as a repair region address 704. Repair data locations 723, which are associated with particular repair cache regions, are indicated or referenced by another portion of the memory address referred to as a local address 706.

The repair region register bank 708 comprises a list of repair cache regions. Generally, the repair register bank 708 is comprised of volatile or non-volatile memory that stores repair cache region addresses as entries. The repair region comparators 709 are respectively associated with individual repair cache regions and receive the repair region

address and compare the received repair region address with the list of repair cache regions from the repair register bank 708 to identify a matching repair cache region. Additionally, the matching comparator, if a matching region is identified, generates an enable signal that indicates the matching repair cache region.

The repair sets 710 maintain M local repair location addresses or pointers 712, also referred to as TAGs and have a single local repair location address per repair cache region, as entries where M is the number of repair cache regions in the system 700. The number of repair sets 710 present, N, is related to the number of local repair addresses selected per repair cache region. Thus, if there are eight local repair addresses per region, N is equal to eight and there are eight repair sets. The local repair locations addresses 712 include an address that is a local address for repair data locations within particular repair cache regions. The local repair location addresses 712 can optionally also include a repair enable indicator (not shown), which can be a single bit indicating whether to local repair location address is a valid repair or not. In operation, the repair sets 710 each provide a selected local repair location address according to the enable signals 708 for the repair region 704.

The repair sets 710 receive the enable signal from the repair region comparators 709 on a matching repair cache region being identified. The enable signal selects repair locations addresses or pointers for the matching repair cache region. The local address comparators 718 compare the selected local repair location addresses with the local address 706 to identify a matching local repair location address. The matching local comparator, on identifying the matching local repair location address, generates a local match or HIT signal 716 that indicates the matching local repair location address. Sense amps 711 can optionally be present and employed to provide the selected local repair location addresses to the local comparators 718.

The repair data bank 722 includes a plurality of repair register banks 724 and a plurality of data bank decoders 725. Typically, there is one repair register bank per repair cache region and one data bank decoder per repair register bank. The repair register banks respectively comprise repair data locations or registers 723 associated with one particular repair cache region.

The repair register banks 724 are selected via the data bank decoders 725 according to a selected repair cache region, which is identified from the enable signal generated by the

encoder 714. It is appreciated that alternate aspects of the invention can select a repair register bank according to other mechanisms that select according to the repair region address, which corresponds to a repair cache region. Repair data locations 723 are selected from individual repair register banks according to the local match signal 716, which causes one repair data location to be selected per repair register bank 704. It is appreciated that alternate aspects of the invention can select repair data locations according to other mechanisms that select according to the local address 706.

The repair register banks 724 can be comprised of non-volatile or volatile memory. When comprised of volatile memory, the repair data locations 723 can be maintained external to the system 700 and then loaded or written into the assigned repair register banks upon initialization or startup of the system 700.

A data bus 726 is present and allows information content/data, including memory addresses, write data, read data, to be transferred to and from the CPU 702 and the main memory 730. A repair mode circuit 720 controls access to the main memory 730 by way of a data bus switch 728, which connects and disconnects the main memory 730 to and from the data bus 726. If a matching repair cache region and a matching local repair address are found, access to the data bus 726 by the main memory 730 is disabled. Otherwise, access to the data bus 726 by the main memory 730 is enabled.

FIG. 7 is illustrated with examples of specific bit lengths and regions in order to facilitate a better understanding of the invention. It is appreciated that invention is contemplated as being employed for any suitable bit sizes, memory address size, number of repair regions, and the like. Additionally, other components can be present in the system such as, sense amps and decoders. Decoders and sense amplifiers can be shared by the repair data bank 722 and the main memory 730.

FIG. 8 is a diagram illustrating an example repair register bank 800 in accordance with an aspect of the invention. In this example, the repair register bank 800 is present in a memory array/device having 1024 memory regions. A subset of these regions are cached, which means that they have assigned repair data locations associated with identified faulty memory cells, and are referred to as repair cache regions. In this example, out of 1024 memory regions, 48 are arranged or configured as repair cache regions. Both the memory regions and the repair cache regions can be identified according to a selected portion of

memory addresses for memory locations of the memory device. These selected portions are referred to as repair region addresses and repair cache region addresses.

Accordingly, a repair cache region address, also a repair region address, corresponds to a particular repair cache region and memory region of the memory device. As an example, of 1024 possible memory regions, 48 regions can be selected as repair cache regions for repair/correction during testing of the memory device in the present example. As stated previously, a repair address and local address are derived from individual memory addresses. As a result, the size of the repair address and the local address are related to the size of the memory address. As an example, for memory addresses that are 18-bits in length, an example repair region address size of 8-bits can be selected and employed to configure and/or arrange memory regions and repair cache regions. Further, an example local address size of 10-bits can be selected and employed to assign local repair data locations to identified faulty memory locations.

The repair register bank 800 is depicted in FIG. 8 as comprising eight local repair data locations 804 that can be employed to repair/replaced identified faulty memory locations. The repair data locations 804 have a storage size 802, typically a word (e.g., 16-bits, 32-bits, and the like) that generally corresponds to a storage size for the memory locations of the memory device. The repair register bank 800 is associated with a particular repair cache region identifiable via the repair address portion. The individual local repair data locations 804 are associated with memory locations and identifiable via the local address portion.

The organization and configuration of the repair region 800 is given by way of example and it is appreciated that the invention contemplates other configurations. For example, repair register banks can be employed with a greater or lesser number of repair data locations.

As described above, the invention enables replacing of bits or small numbers of bits or cells without replacing entire rows or columns. However, in some circumstances it can be advantageous to replace entire rows or columns. The invention can be adapted to replace entire rows or columns. In order to do so, multiple regions can be linked in order to form a complete row or column repair.

FIG. 9 is a diagram illustrating an example row repair in accordance with an aspect of

the invention. A single row of a memory array comprises 512 bits. In the example of FIG. 9, 48 repair cache regions are present and respectively include eight 32 bit repair addresses. As a result, each repair region can replace 256 (consecutive) bits.

FIG. 9 depicts repair data locations for a first repair cache region 902 and a second repair region 904 in accordance with an aspect of the invention. Combined, the regions 902 and 904 are operable to replace or correct 512 bits which is also the number of bits in a row of the memory array. Accordingly, the first repair region 902 and the second repair region 904 can both be employed to replace 512 bits of a faulty or defective row as a single replacement row 906. In the present example, 48 repair regions with eight 32 bit word repairs permit a total of 24 complete row repairs for the memory array. It is appreciated that the invention includes other common row lengths, such as 1024 bits, differing numbers of repair regions, differing numbers of repair addresses or locations, and differing numbers of bit sizes for the repair addresses.

In view of the foregoing structural and functional features described above, methodologies in accordance with various aspects of the invention will be better appreciated with reference to the above figures. While, for purposes of simplicity of explanation, the methodologies of FIGS. 10 and 11 are depicted and described as executing serially, it is to be understood and appreciated that the invention is not limited by the illustrated order, as some aspects could, in accordance with the invention, occur in different orders or concurrently with other aspects from that depicted and described herein. Moreover, not all illustrated features may be required to implement a methodology in accordance with an aspect the invention.

FIG. 10 is a flow diagram illustrating a method 1000 of operating a set associative repair cache in accordance with an aspect of the invention. The method re-routes requests for identified faulty memory locations of a memory device/array to repair data locations or registers within a repair component (e.g., repair data banks).

The method 1000 begins at block 1002, wherein a request for access to a memory location having a memory address is received. The request includes read and/or write access to the memory address. Typically, a requestor has no knowledge as to whether the memory location in the memory device addressed by the memory address is faulty or not.

A repair region address of the memory address is obtained at block 1004. The repair

region portion typically comprises a specific number of consecutive bits of the memory address (e.g., the upper 10 bits). The repair region address corresponds to and identifies a memory region of the memory device.

A local address of the memory address is obtained at block 1006. The local address portion also typically comprises a specific number of consecutive bits of the memory address (e.g., the lower 10 bits). The local address portion corresponds to and identifies the memory location with reference to the memory region in which it is located.

The repair region address is compared to a list of repair cache regions to identify a matching repair cache region at block 1008. The repair cache regions are also identified via an address that is equal to the size (e.g., 10-bits) of the repair cache addresses. The list of repair cache regions is a number of regions associated with a subset of memory regions of the memory device that have one or more faulty locations associated therewith. Typically, there are less repair cache regions than memory regions.

The number of repair cache regions present can vary depending upon a number of factors and can be established during testing of the memory device. For example, a larger number of errors can suggest more regions present within the list of repair cache regions. Other factors include array density, randomness, and the like.

The number of bits employed to identify the repair cache regions and the memory regions is also implementation dependent. The more bits employed to represent and identify the repair cache regions, the smaller the regions are. Conversely, less bits employed to represent and identify the repair cache regions results in larger repair cache regions. Factors that affect the number of bits employed include error rate, randomness of errors, array density, operating speed, and the like.

If a matching repair cache region is identified at block 1010, a list of local repair cache addresses that are associated with the matching repair cache region is provided at block 1012. Otherwise, the memory location within the main memory is selected according to the memory address and data access is provided to the memory location at block 1013 and the method 1000 ends. The list of local repair addresses is a list of pointers to repair data locations which are employed to replace or correct identified faulty memory cells/bits of the device. Continuing, the local address portion of the memory address is compared with the list of local repair addresses to identify a matching local repair address at block 1014.

The number of bits employed for the local repair addresses and the local address (e.g., 10 bits) is also implementation dependent. The more bits employed to represent and identify the repair cache addresses, the more data locations present per repair cache region. Conversely, less bits employed to represent and identify the local repair addresses results less data locations present per repair cache region. Factors that affect the number of bits employed include error rate, randomness of errors, array density, operating speed, and the like.

If the matching repair address is identified at 1016, data access is provided to a data location according to the matching repair region and the matching local repair address at block 1018. The data location stores a number of bits that depends on implementation such as, for example, 10 bits, 16 bits, 32 bits, 1 bit, and the like. Otherwise, the memory location within the main memory is selected according to the memory address and data access is provided to the memory location at block 1020 and the method 1000 ends.

FIG. 11 is a flow diagram illustrating a method 1100 of configuring a repair cache system in accordance with an aspect of the invention. The method 1100 is operable to test and identify faulty memory bits or cells or locations located within a memory array and configure the repair cache system so that repair data locations are employed in place of identified faulty memory cells.

The method 1100 begins at block 1102 wherein a memory array comprising a number of memory cells and locations is provided. The memory cells can be single bit memory cells and/or multi bit memory cells.

The memory cells of the array are tested in order to identify faulty memory locations at block 1104. The faulty memory locations are comprised of and store a selected number of bits such as, for example, 1 bit, 8 bits, 16 bits, 32 bits, 64 bits, and the like, wherein at least one memory cell for the memory locations is faulty.

The memory locations of the device are arranged into memory regions at block 1106. The memory regions are of a fixed size and can be sized and arranged according to factors such as, but not limited to, location of identified faulty memory locations, error rate, device size, and the like.

A number of repair cache regions and a number of repair data locations are selected according to repair factors such as, the identified faulty memory locations at block 1108.

Other factors that can be considered include the number of bits employed, error rate, randomness of errors, array density, operating speed, and the like. In alternate aspects of the invention, the number of repair cache regions, memory regions and the repair data locations are predetermined. The number of repair cache regions is less than the number of memory regions.

Repair cache regions are selectively assigned to memory regions of the device that include identified faulty memory locations at block 1110. As a result, the identified faulty memory locations are assigned to particular repair cache regions. It is noted that the repair cache regions are associated with the same memory locations as the associated memory regions. The repair cache regions can be identified with a repair address portion of memory addresses for memory locations within the memory region (e.g., upper 10-bits).

Continuing with the method 1100, the identified faulty memory locations are assigned local repair cache addresses and associated repair data locations at block 1112. The local repair cache addresses can simply be a local address portion (e.g., lower 8-bits) of the identified faulty memory locations assigned there to.

Those skilled in the art to which the invention relates will appreciate that modifications, additions and substitutions can be made in the described example embodiments, without departing from the scope of the invention.

CLAIMS

1. A repair cache system, comprising:

a repair region register that maintains a list of repair cache regions;

a repair region comparator, coupled to the repair region register, that receives a repair region address of a memory address, and compares the repair region address to the list of repair cache regions to identify a matching repair cache region;

a repair set that maintains a local repair location addresses and provides a local repair location address selected according to the matching repair cache region;

a local comparator coupled to the repair set, that compares the provided local repair location address to a local address of the memory to identify a matching local repair location address; and

a repair data bank that maintains a repair data location, and provides read/write access to a repair data location of the repair data location according to the matching repair cache region and the matching local repair location address.

2. The system of claim 1, further comprising:

a main memory;

a central processor unit,

a data bus connected to the central processor unit;

a repair mode circuit that controllably connects the central processor unit to the data bus on failure of the repair region comparator to identify the matching repair cache region and the local comparator to identify the matching local repair location address.

3. The system of claim 1, wherein the repair region comparator, upon identifying the matching repair cache region generates an enable signal that identifies the matching repair cache region.

4. A repair cache system, comprising:

a repair cache region router that receives a request for access to a memory location having a memory address, that maintains a list or repair cache regions, and routes the request to a memory component on failure to identify a matching repair cache region, and routes the request to a local repair location router according to a repair address portion of the memory address on identifying a matching repair cache region;

the local repair location router that maintains a list of local repair location

addresses and selectively routes the request to the main memory on failure to identify a matching repair location address or to a repair component according to a local address portion of the memory address on identifying a matching local repair location address;

the main memory that provides access to a memory location addressed by the memory address in response to the request; and

the repair component that provides access to a repair data location addressed by the matching repair cache region and the matching local repair location address.

5. The system of claim 4, wherein the repair cache region router further comprises repair region comparators that compare the list of repair cache regions to the repair address to identify the matching repair cache region.

6. The system of claim 4 or 5, wherein the local repair location router further comprises local comparators that compare a subset of the list of local repair location addresses selected according to the matching repair cache region to the local address to identify the matching local repair location address.

7. A method of operating a repair cache comprising:

receiving a request for access to a memory address;

comparing a repair region portion of the memory address to a list of repair cache regions to identify a matching repair cache region;

providing a list of local repair location addresses associated with the matching repair cache region;

comparing a local address portion of the memory address to the list of local repair location addresses to identify a matching local address; and

on the matching repair cache region and the matching local address being identified, providing access to a repair data location according to the matching repair cache region and the matching repair address.

8. The method of claim 7, further comprising providing read/write access to a memory location within a main memory according to the memory address on the matching repair cache region being unidentified.

9. A method of configuring a set associative repair cache system comprising:

providing a memory array comprising one or more memory cells;

testing memory cells of the array to identify faulty memory cells and faulty

memory locations;

arranging memory locations of the array into memory regions;

selecting a number of repair cache regions and repair data locations according to repair factors;

selectively assigning repair cache regions to memory regions having one or more identified faulty memory locations;

selectively assigning repair data locations, arranged according to the assigned repair cache regions, to the identified faulty memory locations.

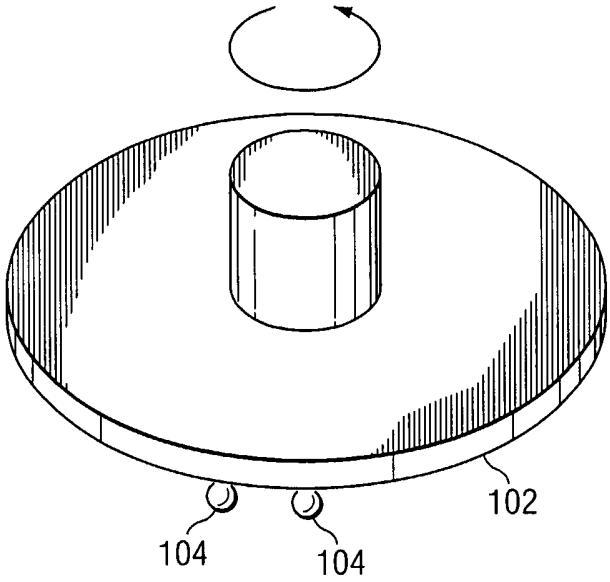


FIG. 1A

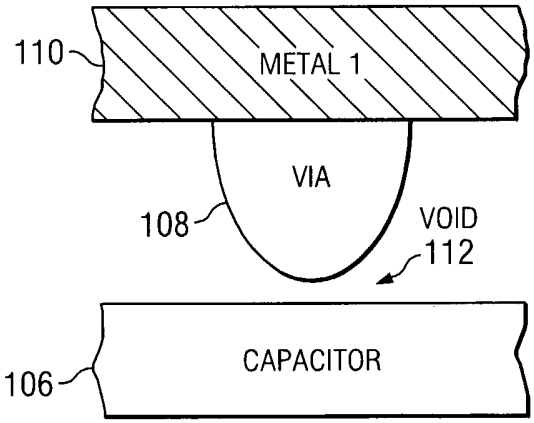


FIG. 1B

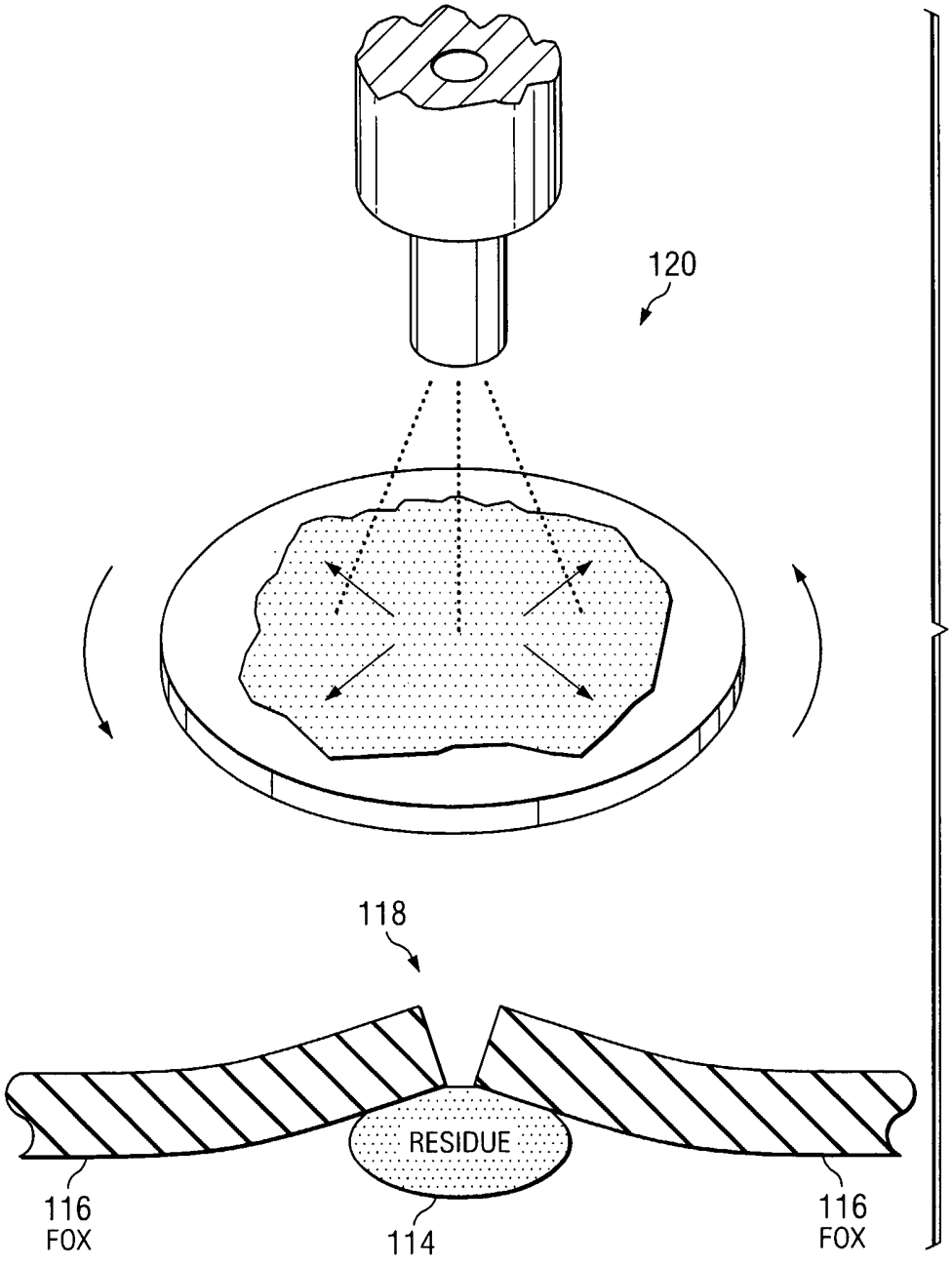


FIG. 1C

FIG. 2B

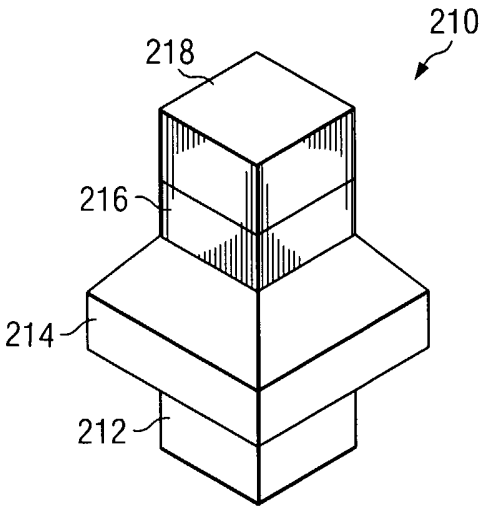
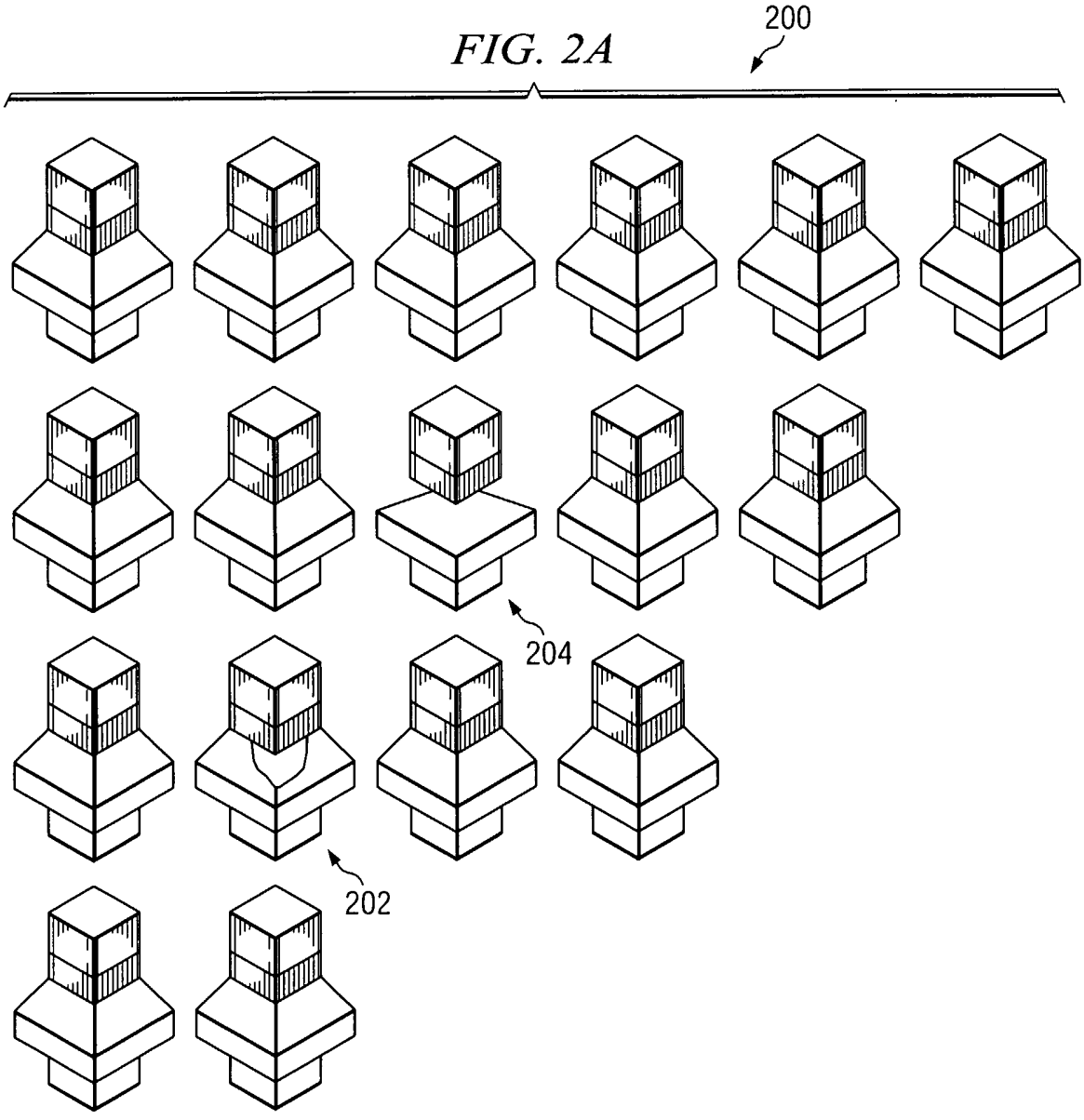


FIG. 2A



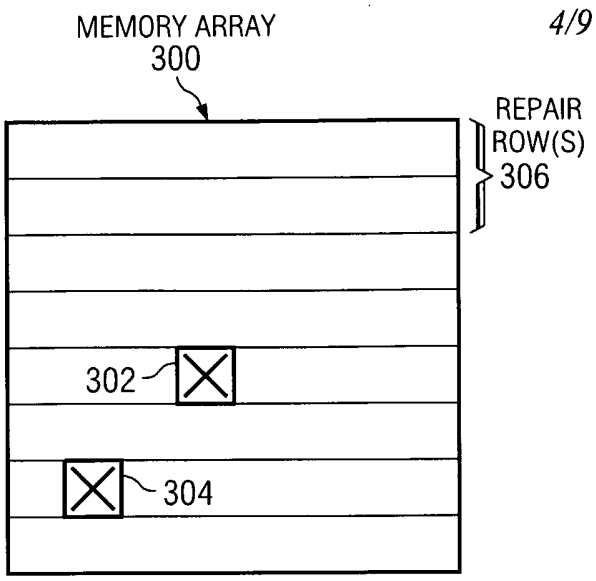


FIG. 3A

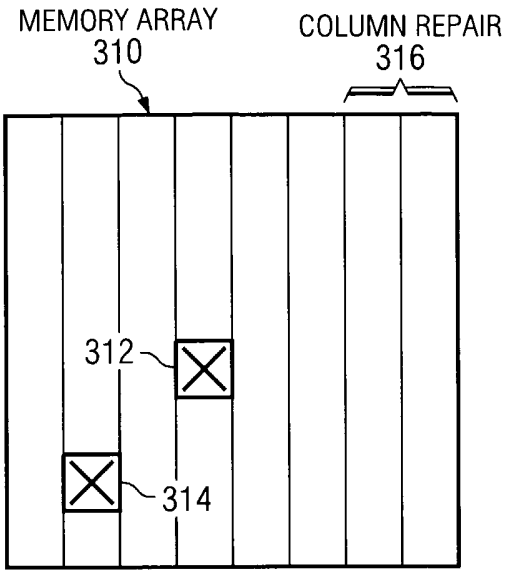


FIG. 3B

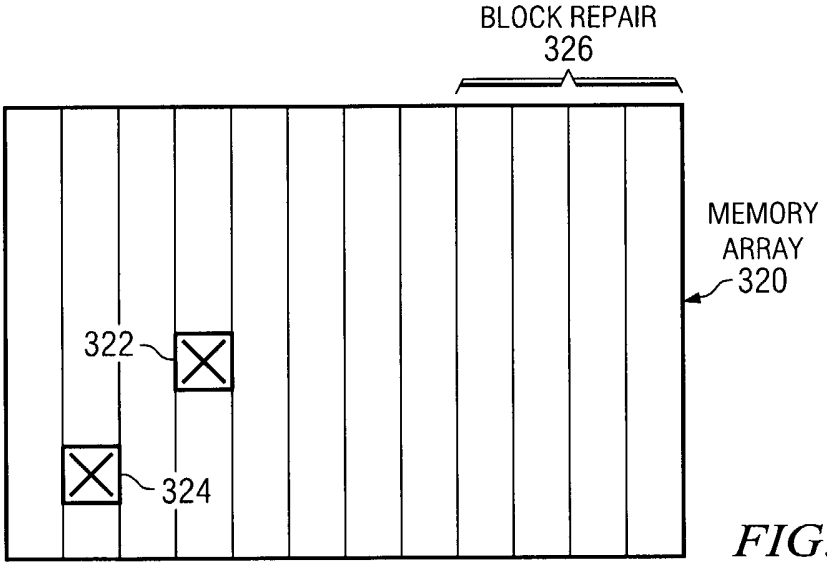


FIG. 3C

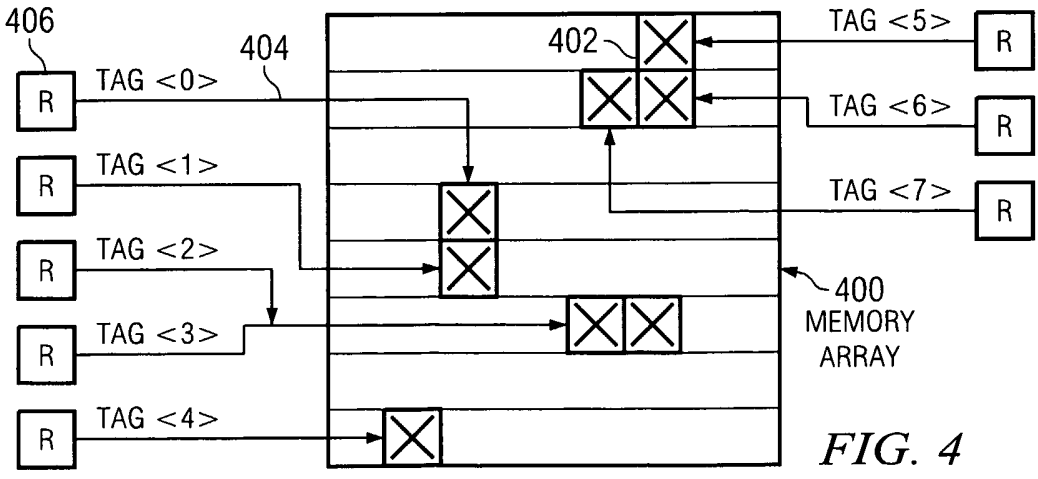


FIG. 4

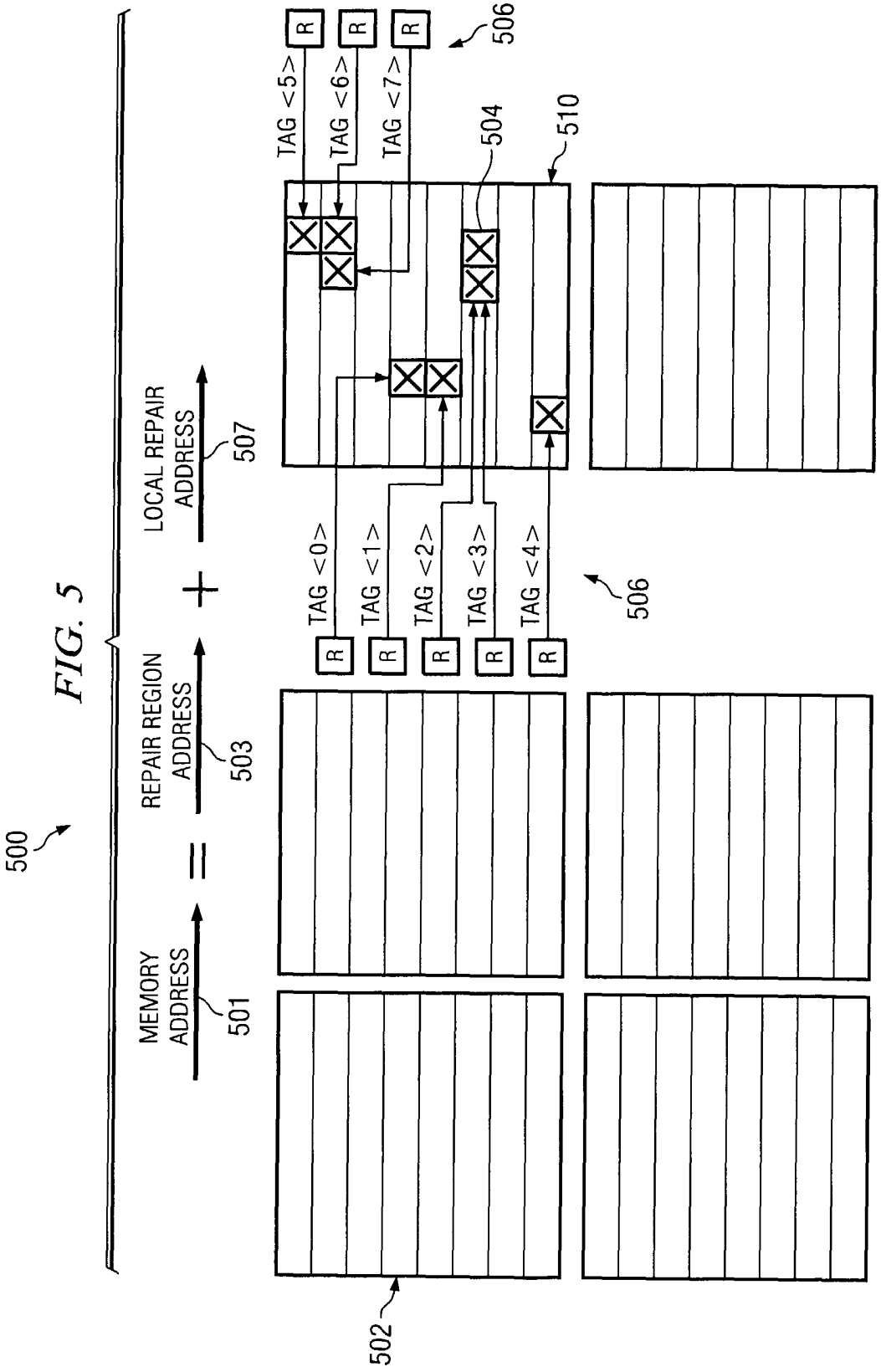

500
MEMORY ADDRESS
501
=
REPAIR REGION ADDRESS
503
+
LOCAL REPAIR ADDRESS
507
TAG <0>
TAG <1>
TAG <2>
TAG <3>
TAG <4>
TAG <5>
TAG <6>
TAG <7>
R
504
506
510
502

FIG. 5

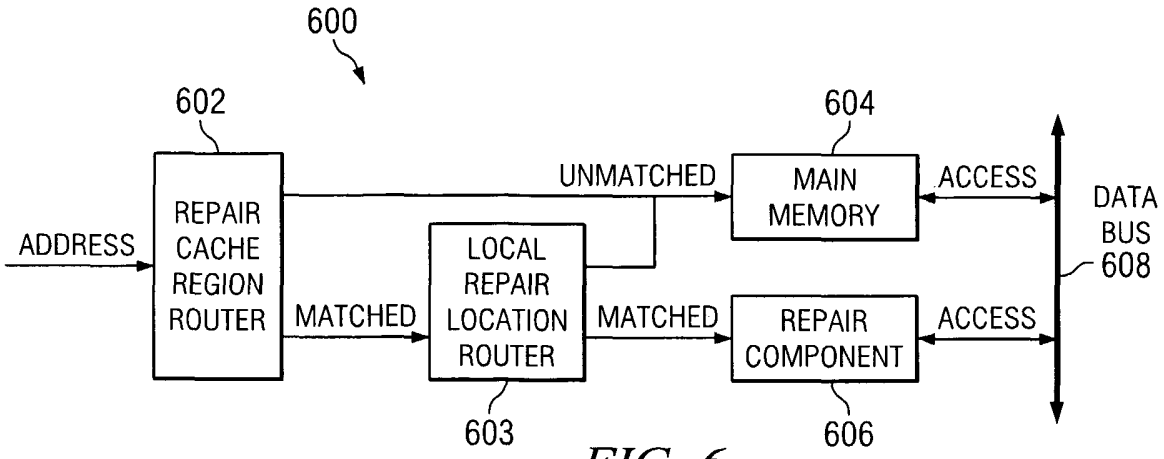
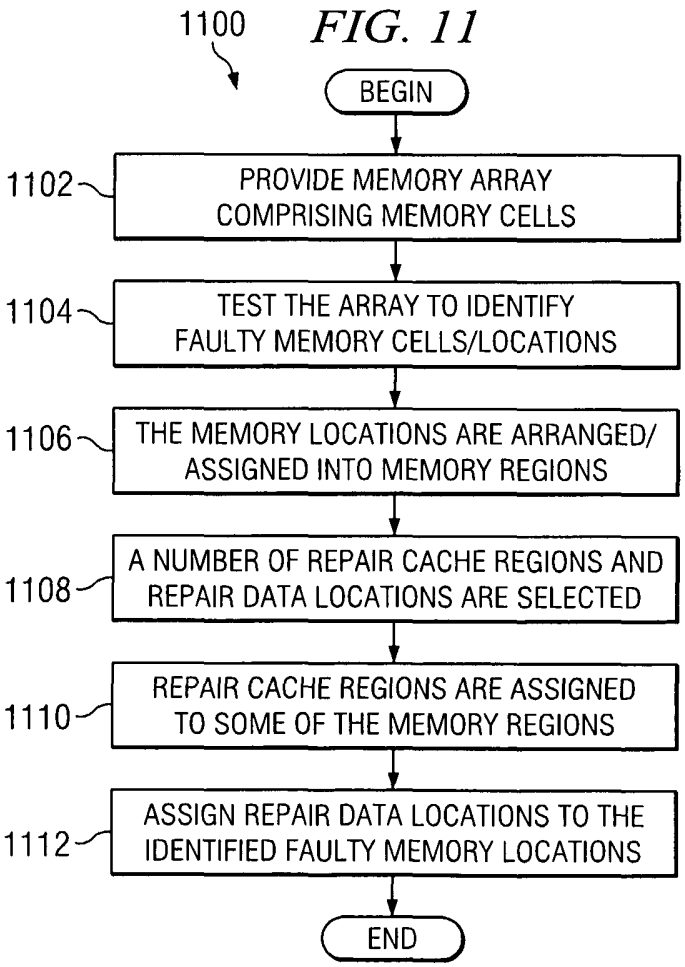

600
602
604
ADDRESS
REPAIR CACHE REGION ROUTER
UNMATCHED
MAIN MEMORY
ACCESS
DATA BUS
608
MATCHED
LOCAL REPAIR LOCATION ROUTER
MATCHED
REPAIR COMPONENT
ACCESS
603
606

FIG. 6

FIG. 11


1100
BEGIN
1102
PROVIDE MEMORY ARRAY COMPRISING MEMORY CELLS
1104
TEST THE ARRAY TO IDENTIFY FAULTY MEMORY CELLS/LOCATIONS
1106
THE MEMORY LOCATIONS ARE ARRANGED/ ASSIGNED INTO MEMORY REGIONS
1108
A NUMBER OF REPAIR CACHE REGIONS AND REPAIR DATA LOCATIONS ARE SELECTED
1110
REPAIR CACHE REGIONS ARE ASSIGNED TO SOME OF THE MEMORY REGIONS
1112
ASSIGN REPAIR DATA LOCATIONS TO THE IDENTIFIED FAULTY MEMORY LOCATIONS
END

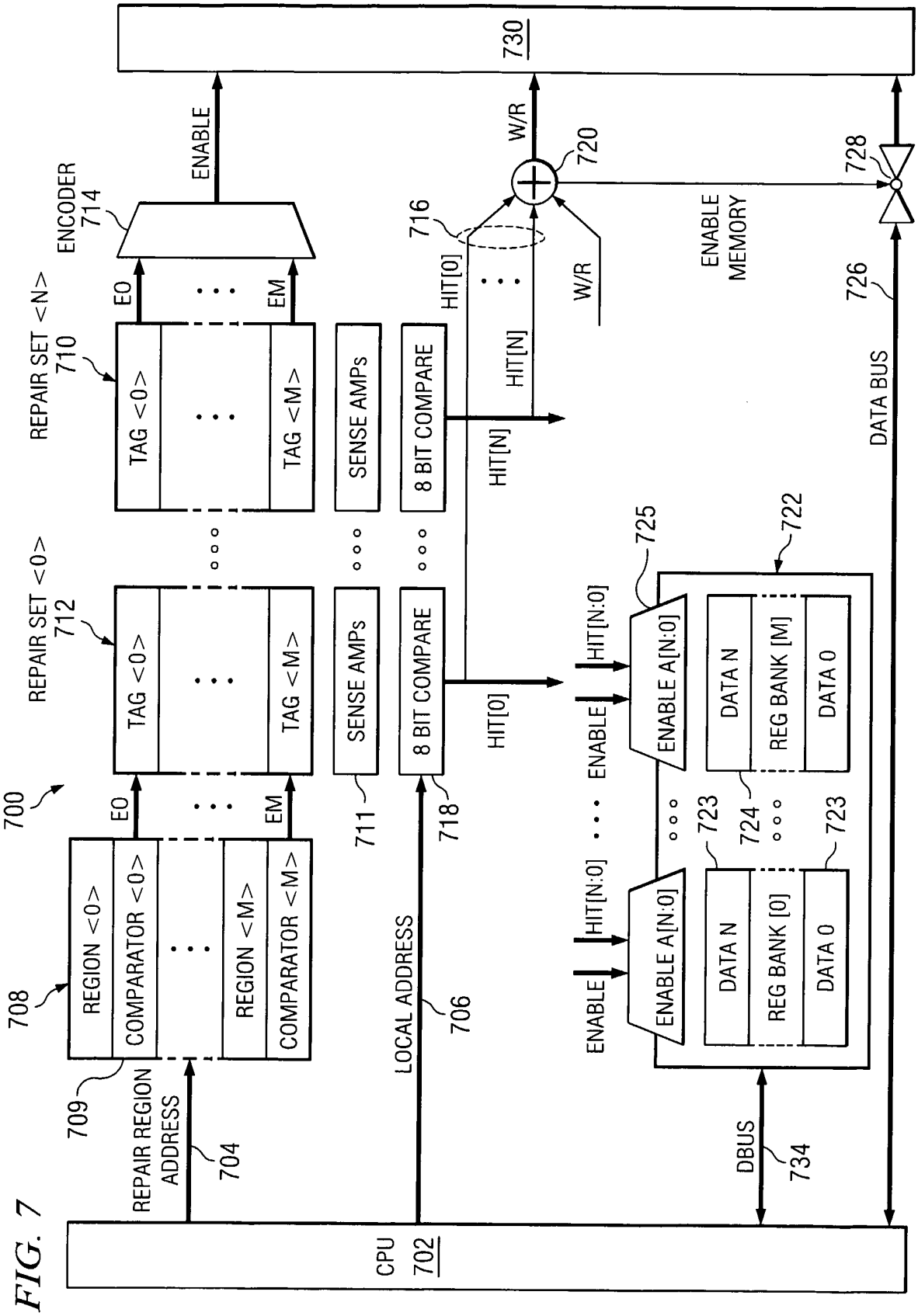

730
ENABLE
ENCODER
714
REPAIR SET <N>
710
REPAIR SET <0>
712
EO
EM
TAG <0>
TAG <M>
SENSE AMPs
8 BIT COMPARE
HIT[0]
HIT[N]
716
W/R
720
728
ENABLE MEMORY
726
DATA BUS
700
708
REGION <0>
COMPARATOR <0>
REGION <M>
COMPARATOR <M>
709
REPAIR REGION ADDRESS
704
LOCAL ADDRESS
706
711
718
HIT[N:0]
ENABLE
725
ENABLE A[N:0]
722
DATA N
REG BANK [M]
DATA 0
REG BANK [0]
723
724
DBUS
734
CPU
702

FIG. 7

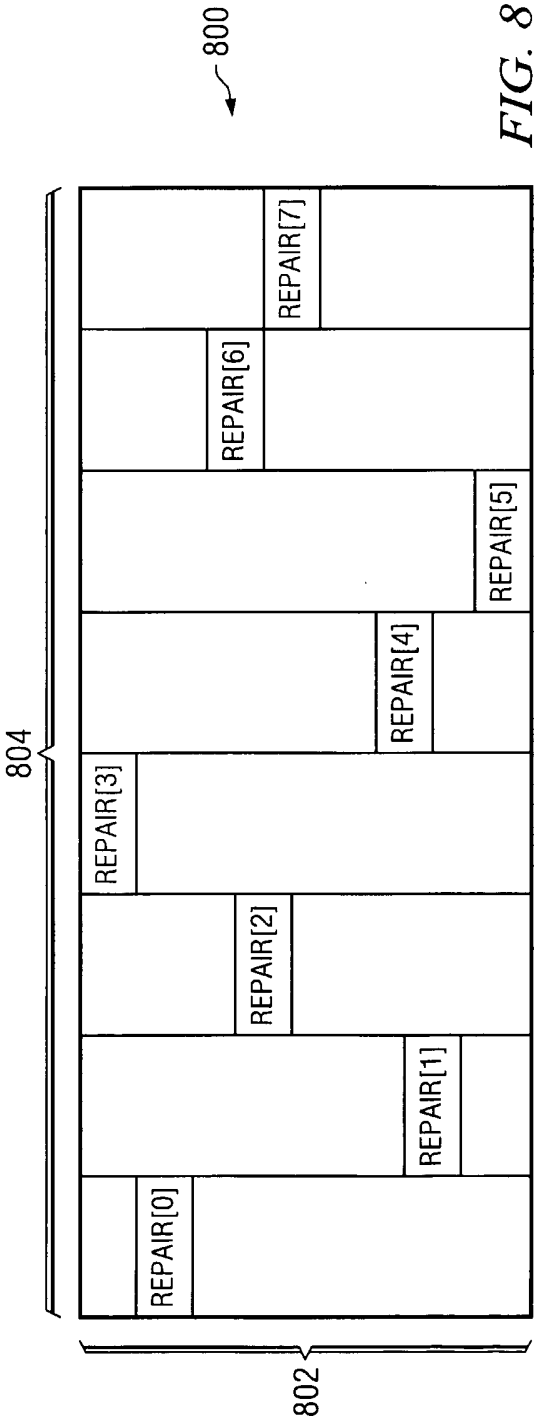

800
804
802
REPAIR[0]
REPAIR[1]
REPAIR[2]
REPAIR[3]
REPAIR[4]
REPAIR[5]
REPAIR[6]
REPAIR[7]

FIG. 8

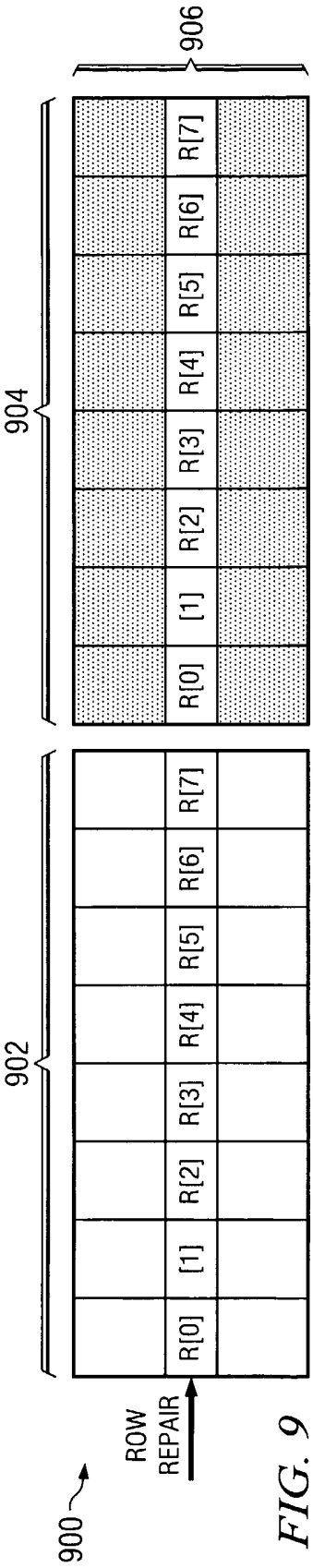
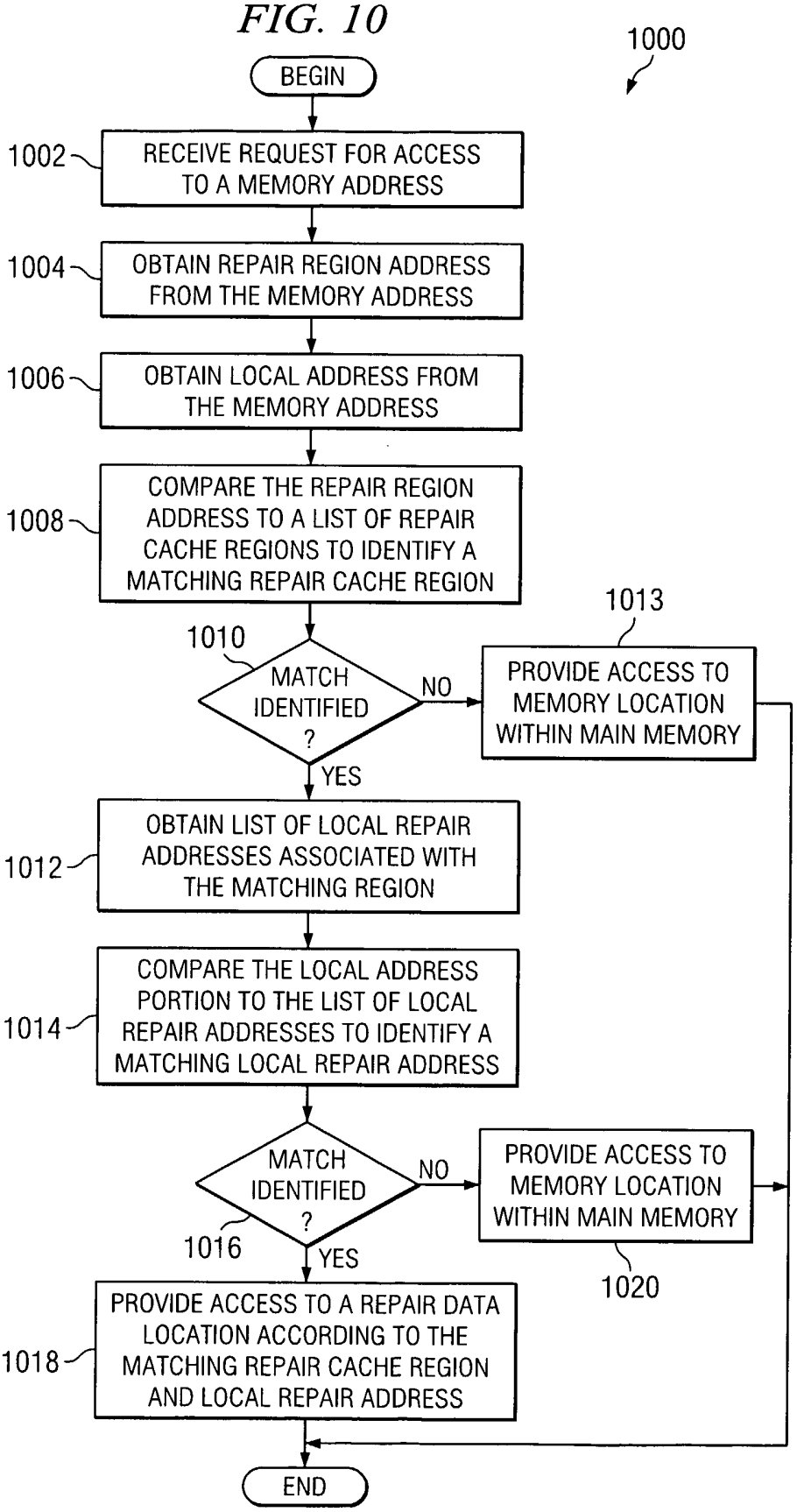

900
ROW REPAIR
902
904
906
R[0]
[1]
R[2]
R[3]
R[4]
R[5]
R[6]
R[7]

FIG. 9

FIG. 10


1000
BEGIN
1002
RECEIVE REQUEST FOR ACCESS TO A MEMORY ADDRESS
1004
OBTAIN REPAIR REGION ADDRESS FROM THE MEMORY ADDRESS
1006
OBTAIN LOCAL ADDRESS FROM THE MEMORY ADDRESS
1008
COMPARE THE REPAIR REGION ADDRESS TO A LIST OF REPAIR CACHE REGIONS TO IDENTIFY A MATCHING REPAIR CACHE REGION
1010
MATCH IDENTIFIED ?
NO
1013
PROVIDE ACCESS TO MEMORY LOCATION WITHIN MAIN MEMORY
YES
1012
OBTAIN LIST OF LOCAL REPAIR ADDRESSES ASSOCIATED WITH THE MATCHING REGION
1014
COMPARE THE LOCAL ADDRESS PORTION TO THE LIST OF LOCAL REPAIR ADDRESSES TO IDENTIFY A MATCHING LOCAL REPAIR ADDRESS
MATCH IDENTIFIED ?
1016
NO
PROVIDE ACCESS TO MEMORY LOCATION WITHIN MAIN MEMORY
1020
YES
1018
PROVIDE ACCESS TO A REPAIR DATA LOCATION ACCORDING TO THE MATCHING REPAIR CACHE REGION AND LOCAL REPAIR ADDRESS
END

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US05/35028

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : G06F 11/00
US CL : 714/8
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 714/8, 710

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6,055,204 A (BOSSHART et al) 25 April 2000 (25.04.2000), col. 1-25.	1-3, 7-9
A,P	US 2004/0255209 A1 (GROSS) 16 December 2004 (16.12.2004), abstract.	1-9
A	US 4,355,376 A (GOULD) 19 October 1982 (19.10.1982), abstract.	1-9
A	US 4,380,066 A (SPENCER et al) 12 April 1983 (12.04.1983), abstract.	1-9
A	US 5,937,435 A (DOBBEK et al) 10 August 1999 (10.08.1999), abstract	1-9
A	US 6,052,798 A (JEDDELOH) 18 April 2000 (18.04.2000), abstract.	1-9
A	US 6,201,655 B1 (WATANABE et al) 13 March 2001 (13.03.2001), abstract.	1-9
A	US 6,671,822 B1 (ASHER et al) 30 December 2003 (30.12.2003), abstract.	1-9

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"E" earlier application or patent published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance, the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

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Date of the actual completion of the international search
03 February 2006 (03.02.2006)

Date of mailing of the international search report
16 MAR 2006

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