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[54] **TAPE ACTIVATED PIANO AND ORGAN PLAYER**

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[52] **U.S. Cl.** **84/115,** 84/1.03, 84/462

[51] **Int. Cl.** **G10f 5/00**

[58] **Field of Search** 84/5, 19, 115, 1.01, 1.03, 84/161, 462

[56] **References Cited**

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[57] **ABSTRACT**

A system for recording piano or organ music on a recording tape and replaying the tape to actuate a reproduction of the music on a playback piano or organ, the system including electrical means to sample, store and transmit signals from the individual keys of the first instrument to a recording tape, means to count a predetermined number of these signals and to continuously reset the system to sample, store and transmit a further predetermined number of signals after each predetermined number has been transmitted, and means to receive the transmitted signals from the tape, and reproduce these signals on the second instrument by means of causing each signal to actuate a means to play a corresponding key on the second instrument.

5 Claims, 7 Drawing Figures

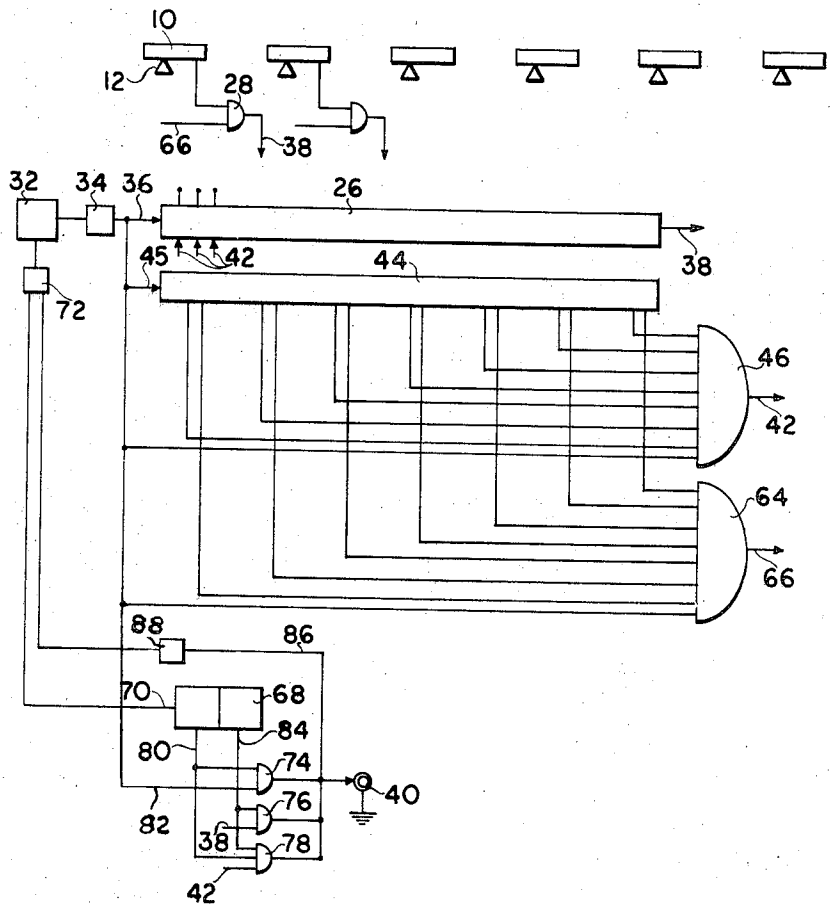


FIG. 1

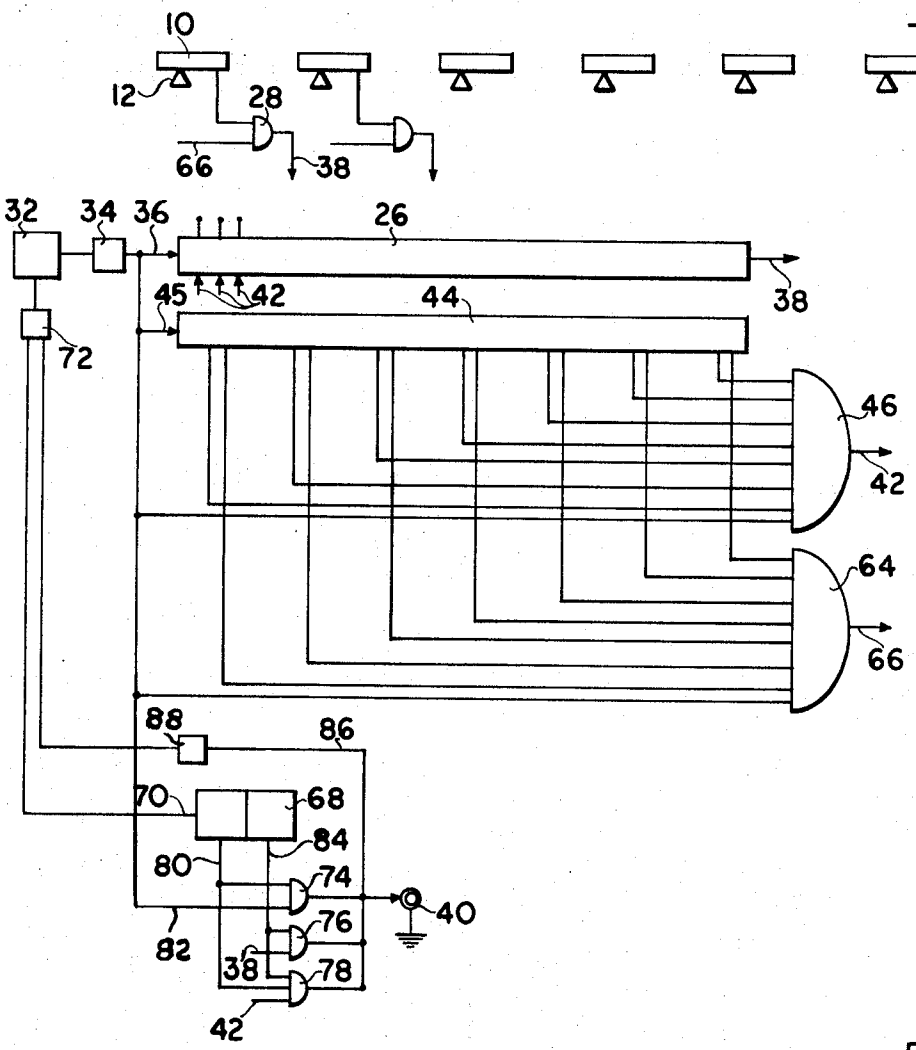


FIG. 2

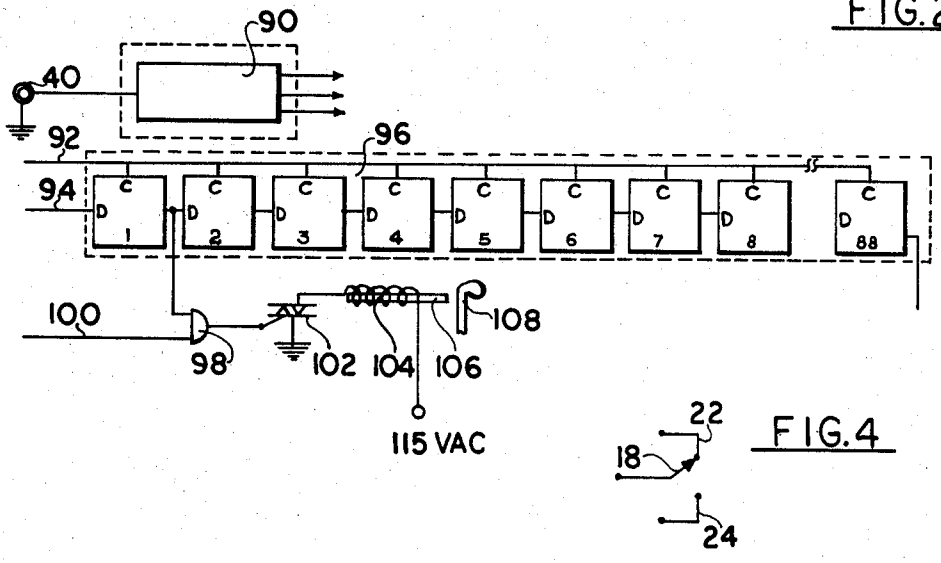


FIG. 4

FIG.3

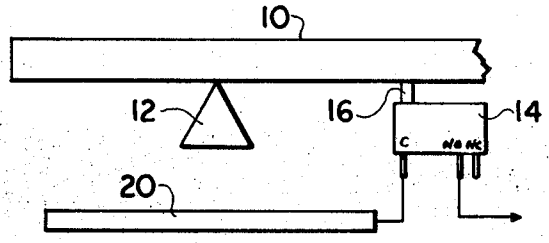


FIG.5

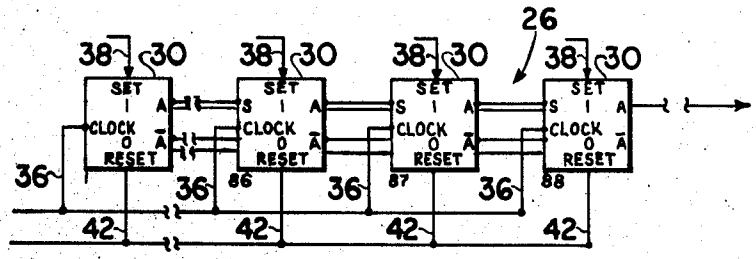


FIG.6

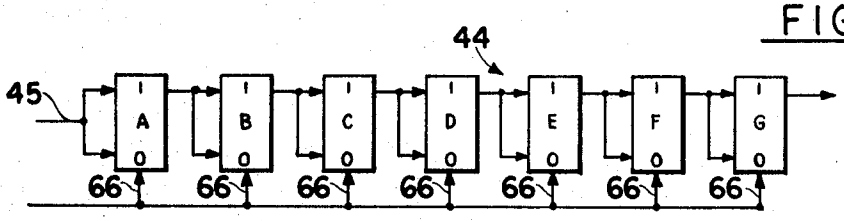
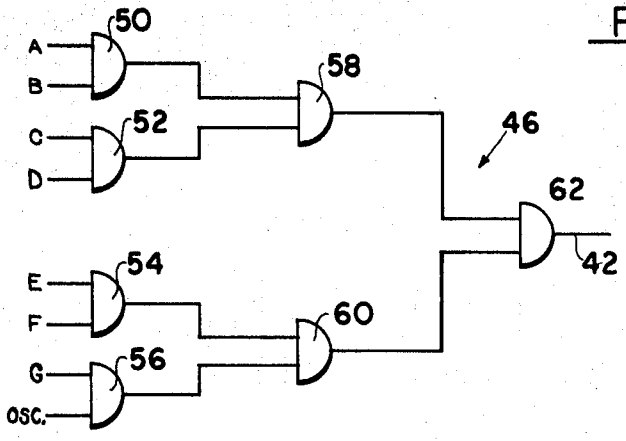


FIG.7



TAPE ACTIVATED PIANO AND ORGAN PLAYER

This invention relates to a system for recording piano or organ music on a tape recorder and, thereafter, replaying the tape to cause the keys of the piano or organ to be activated in similar manner to the so-called "player-piano" which utilized punched paper rolls.

The old roll-type "player-piano" had many disadvantages.

Among these disadvantages were the large space needed for storing the paper rolls, the high cost of the rolls, the inconvenience of loading and unloading the rolls in the piano, the high cost of repairing the player-piano, and the complexity of the player-piano which required the use of bellows or vacuum pumps which, in turn, were subject to air leaks.

In accordance with the present invention, tapes are used to record and play back the music of a piano or organ. The advantages of the use of such tapes are that the piano or organ is less complex and less expensive to build and maintain, there is no problem of fumbling and tearing of the recorded music, the tapes hold much more recorded media in a relatively small space and are, consequently, easier to handle and store, and they are much less costly and easier to produce than perforated rolls. Furthermore, if a cassette type tape means is used, it is never necessary to touch the actual tape which is simply plugged in or out.

It is, therefore, one object of the present invention to overcome the disadvantages of prior paper-roll type pianos and organs by utilizing tapes, especially of the cassette type, for the purpose of recording and playing back musical data.

Another object of the present invention is to provide tape-actuated player-type pianos and organs which are relatively simple in construction, easy to use, and inexpensive to build and maintain.

Other objects and many of the attendant advantages of this invention will be readily appreciated as the same becomes better understood by reference to the following description when read in conjunction with the accompanying drawings wherein:

FIG. **1** is a schematic view of a recording system embodying the present invention.

FIG. **2** is a schematic view of a play-back system embodying the present invention.

FIG. **3** is a diagrammatic view of the piano key and switch construction utilized in the recording system of this invention.

FIG. **4** is a schematic view of a micro-switch construction utilized in the recording system of the present invention.

FIG. **5** is a schematic view of the shift register utilized in the recording system of the present invention.

FIG. **6** is a schematic view of the binary counter utilized in the recording system of the present invention.

FIG. **7** is a schematic view of a sync pulse generator utilized in the recording system of the present invention.

Referring now in greater detail to the figures of the drawings, there is shown in FIG. **1** a series of piano or organ keys **10**, totaling **88** in number. Each key **10** (as best seen in FIG. **3**) is mounted on a fulcrum **12**. Spaced from the fulcrum **12** is a micro-switch **14** having a plunger **16** in contact with the underside of the key **10**. The micro-switch **14** comprises a switch blade **18** connected to a ground through a metal frame **20** enclosed in the instrument. The blade **18** is normally closed against a contact or sensor **22** connected to the key and is normally spaced from the contact **24** which is in electrical connection with a shift register device **26** through a computer logic AND gate **28**.

The key **10** normally presses down on the plunger **16**, and the plunger exerts pressure on the blade **18**, with which it is engaged, to hold the blade **18** against the contact **22**. This provides a ground inhibit which prevents electrical flow through the AND gate. When the key **10** is depressed, the pressure of the plunger **16** is released and the blade **18** moves away from the sensor contact **22** and against the contact **24**. The blade **18** is thereby removed from the common ground network and is now "floating". This serves to remove the ground inhibit from the corresponding computer logic AND gate **28** and permits passage of the key pulses from the AND gate **28** into the shift register **26**.

The shift register **26** is an 88 stage "parallel in, serial out". Each stage comprises a flip-flop unit which is set by a signal from the corresponding AND gate **28**.

The shift register **26** is shown schematically in greater detail in FIG. **5** and includes 88 stages **30**, the first and the last three of which are illustrated. Each stage comprises a flip-flop consisting of two transistors, indicated as "1" and "0". When one of these transistors is conducting, the other is non-conducting. Normally, the "0" transistors are conducting but are made non-conducting while the "1" transistors are made conducting by a square wave constituting the clock pulse.

The clock pulse is generated by a master oscillator **32** (see FIG. **1**) which is provided with a frequency divider (not shown) of standard construction. This arrangement permits the generation of two sine waves, one of which has twice the frequency of the other. The smaller frequency wave is sent through a square wave generator **34**, which may be of the type known as a "Schmidt trigger". The square wave generated thereby constitutes the "clock" pulse, indicated at **36**, which is passed to each stage **30**. This clock pulse acts to shift the stored key pulses **38** from one stage to the next.

The key pulses **38** are provided by the corresponding AND gates **28**. If a key **10** is struck it acts to "set" the key pulse in the "1" transistor of the corresponding stage **30** of the shift register. These key pulses are then shifted from one stage to the next by the clock pulses **36**. If the key **10** for a particular stage **30** is not struck, no key pulse is present at that stage and the clock pulse passes no data therefrom.

The key pulse generated by the last stage **30** of the shift register **26** is passed onto a recording tape **40** through a multiplexer unit hereinafter more fully described. When 88 keys have been sampled, the shift register is cleared by a sync pulse and is then reset for the sampling of another 88 key pulses.

The sync pulse, for clearing and resetting the shift register is indicated at **42** (see FIG. **5**). This sync pulse **42** is provided by the action of a binary counter **44** through a sync pulse generator **46**. The sync pulse **42** acts to move the "0" transistors in each stage of the shift register **26** to conducting and the "1" transistors to non-conducting. The sync pulse **42** is also passed through the multiplexer assembly (hereinafter described) to the tape **40**.

The binary counter **44** is shown schematically in greater detail in FIG. **6** and comprises seven flip-flop stages, indicated respectively as A, B, C, D, E, F and G.

This binary counter **44** receives square wave pulses **45**, similar to the square wave pulses **36**, from the master oscillator **32** and the square wave generator **34.** These square wave pulses **45** are generated simultaneously with the pulses **36.** The stages A through G of the binary counter are similar to the stages **30** of the shift register in that each has an "0" transistor and a "1" transistor which are alternately conducting and non-conducting. Each square wave pulse **45** generates a change in state from conducting to non-conducting of the "0" and "1" transistors, thereby triggering the next adjacent flip-flop stage.

The signals from the stages A through G are transmitted to a sync pulse generator **46,** shown schematically in FIG. **7,** which is constructed to count to 88 pulses before generating the sync pulse **42.** The sync pulse generator **46** consists of the respective AND gates **50, 52, 54, 56, 58, 60** and **62.** The AND gate **50** must receive pulses from both stages A and B of the binary counter **44** before generating a signal, the AND gate **52** must, similarly, receive pulses from both stages C and D, the AND gate **54** must, similarly, receive pulses from stages E and F, and the AND gate **56** must, similarly, receive pulses from stage G and from the square wave generator **34.** The AND gates **50** and **52** combine to generate a signal to AND gate **58** and the AND gates **54** and **56** combine to generate a signal to AND gate **60.** The AND gates **58** and **60,** in turn, must combine to generate a signal to AND gate **62.** The AND gate **50** receives its signals from the "0" sides of flip-flops A and B; the AND gate **52** receives its signals from the "0" side of C and the "1" side of D; the AND gate **54** receives its signals from the "1" side of E and the "0" side of F; and the AND gate **56** receives its signals from the "1" side of G and from the oscillator. The sync pulse generator **46** is arranged to generate the sync pulse **42** from AND gate **62** when 88 square wave pulses have been counted.

A second sync pulse generator, generally designated **64,** is identical to the generator **46** except that it receives its signal into the AND gate **50** from the "1" side of A and is constructed to count to 89 before generating a sync pulse **66.** This sync pulse **66** is directed into the AND gates **28** to enable these AND gates to receive a further sampling of the 88 key pulses. The sync pulse **66** is also directed into the seven stages of the binary counter **44** to reset the binary counter (see FIG. **6**) to enable it to begin a new counting sequence.

The multiplexer unit (see FIG. **1**) comprises a binary counter **68,** which is similar to binary counter **44,** except that it contains only two stages which count only to three and then reset. The binary counter **68** receives a square wave clock pulse **70** from the master oscillator **32** and square wave generator **72.** This wave has twice the frequency of the wave **36.**

The binary counter **68** is in circuit with three AND gates **74, 76,** and **78.** The AND gate **74** is activated by a pulse **80** from the first stage of the binary counter **68** and a clock pulse **82** from the square wave generator **34.** The second AND gate **76** is activated by a pulse **84** from the second stage of the binary counter **68** and the key pulse **38** from the shift register **26.** The third AND gate **78** is activated by the combination of pulses **80** and **84** plus the sync pulse **42.**

When each AND gate **74, 76** and **78** is activated, it sends a corresponding signal to the tape **40.**

The binary counter **68** resets itself and begins another count on the count of four.

Superimposed on the clock pulse from the AND gate **74** is a square wave pulse **86,** from the square wave generator **72,** which has been amplified by amplifier **88.** This superimposed clock pulse **86** is preferably applied to the tape in order to generate a more definite control clock signal to the play-back system.

The tape **40** is used to play back the recorded data by means of the system illustrated in FIG. **2.** This system sends the clock pulse, key pulse and sync pulse from the tape **40** through a switching and AND gate assembly, generally designated **90,** which is identical to that shown at **74, 76** and **78** in FIG. **1** but operating in reverse. The clock pulses and key pulses, indicated respectively at **92** and **94,** are fed from the assembly **90** into shift register **96,** identical to shift register **26** but functioning as a "serial in, parallel out" device. The clock pulses step the key pulses through the shift register **96.** Any data impressed on the key pulses are passed to the corresponding AND gates **98** to which is also passed the sync pulses from the tape, indicated at **100.** Upon activation of a particular AND gate **98,** it activates a corresponding triac **102** operatively connected to a solenoid **104.** The solenoid **104** actuates a plunger **106** which impinges against a corresponding piano or organ hammer **108,** thereby replaying the keys as originally recorded on the tape.

The invention claimed is:

1. An apparatus for recording and reproducing music on a keyboard instrument comprising a keyboard having a plurality of keys, each key being operatively connected to a switch means, each of said switch means being actuatable by depression of the corresponding key to send a key pulse to an electrical impulse storage means, said storage means being constructed and arranged to provide a sampling of each key through the open or closed position of its corresponding switch to determine whether the key has been depressed, means to shift each sampling from said storage means to a recording tape, and means to reset said storage means for a further sampling of said keys after a predetermined number of keys have been sampled; said storage means being an electrical shift register having a series of stages, each stage corresponding to a key on said keyboard, each of said stages comprising a flip-flop transistor assembly, a separate signal gate in circuit between the switch means of each key of said keyboard and said shift register, said signal gates being actuatable to send a signal to the corresponding stages of the shift register upon actuation of the corresponding switch means by depression of the corresponding key of said keyboard, oscillator means in electrical circuit with said shift register to send clock pulses through said shift register to shift the signals from said signal gates from stage to stage of said shift register onto said recording tape, and a binary counter in electrical circuit with said shift register, said binary counter also being in electrical circuit with said oscillator and being constructed and arranged to count the number of clock pulses from said oscillator in synchronism with the clock pulses sent to said shift register, said binary counter being in electrical circuit with two sync pulse generators, one of said sync pulse generators being constructed and arranged to send a sync pulse signal to said shift register to reset all the stages of said shift register after a first predetermined number of clock pulses have been counted by said bi-

nary counter, and the other sync pulse generator being constructed and arranged to send a second sync pulse signal to said signal gates and to said binary counter to reset said signal gates and said binary counter after a second predetermined number of clock pulses have been counted by said binary counter.

2. The apparatus of claim **1** including playback means to receive the samplings from said recording tape and apply them to the keyboard of a second instrument, said playback means including an actuating means for each key of said second keyboard, each actuating means being responsive to a corresponding key pulse from said recording tape and being constructed and arranged to actuate the corresponding key on said second keyboard.

3. The apparatus of claim **1** wherein a multiplexer assembly is constructed and arranged to receive said key pulse, clock pulse and first sync pulse and to pass said pulses to said recording tape.

4. The apparatus of claim **3** wherein said multiplexer assembly comprises a second binary counter in electrical circuit with said oscillator to receive pulses therefrom, said second binary counter being in electrical circuit with a plurality of signal gates, each signal gate being constructed and arranged to receive either a key pulse, a clock pulse or a first sync pulse and to pass such corresponding pulses to said recording tape upon receiving a signal from the corresponding stages of said second binary counter.

5. The apparatus of claim **4** wherein an amplified clock pulse from said oscillator is superimposed onto the clock pulse sent to said recording tape by said multiplexer assembly.

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