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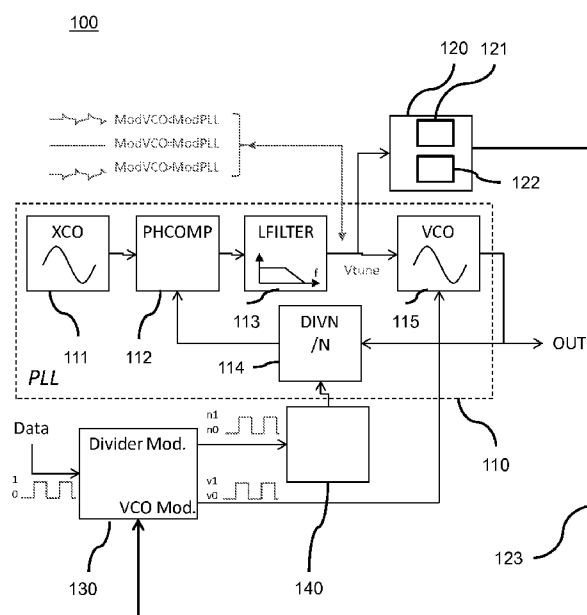
(54) Title: CALIBRATION ARRANGEMENT FOR FREQUENCY SYNTHESIZERS

Fig.1

(57) Abstract: An electronic device has a calibration arrangement (120) for controlling a frequency characteristic of a PLL circuit having a phase comparator (112) having an output for generating a phase difference signal, a voltage controlled oscillator (115) and a divider (114). The divisor of the divider is programmable, and the oscillator is also directly modulated by an oscillator modulation signal. A modulation unit (130) has a modulation input for receiving a modulation signal and generates the oscillator modulation signal and the divisor such that modulation generates a predefined change of the output frequency and a change of the divisor proportional to said predefined change. The calibration arrangement receives the phase difference signal, and has a ripple detector (121) for providing a detector output signal by detecting a ripple on the phase difference signal correlated to edges in the modulation signal. A calibration control unit (122) adjusts the oscillator modulation signal based on the detector output signal such that the ripple is reduced.

Title: Calibration Arrangement for Frequency SynthesizersField of the invention

5 This invention relates to electronic devices having a calibration arrangement for controlling a frequency characteristic of a circuit. More specifically, the invention is in the field of frequency synthesizers and digitally controlled oscillators having two modulation inputs and comprising the calibration arrangement.

10 Background of the invention

 United States patent application US2007/0252654 describes designs for a frequency modulator based on a voltage controlled oscillator (VCO). A frequency modulator is provided for generating an output signal with a frequency that is a function of a modulation signal, wherein the modulation signal can assume different discrete modulation values, and a predetermined frequency
15 value of the output signal is associated with each modulation value. The modulator contains a closed phase locked loop (PLL) with a loop filter for providing a first control voltage, with a voltage controlled oscillator for generating the output signal, and with a switchable frequency divider for deriving a frequency-divided signal. The divisor is the factor by which the input frequency of the divider is divided. Also a modulation unit is provided which gives, at a first output, values of the
20 divisor that are a function of the modulation signal, and at a second output, a second control voltage that is a function of the modulation signal. The oscillator has a first control input connected to the loop filter and has a second control input connected to the second output of the modulation unit, and is designed to generate the output signal as a function of the first control voltage and the second control voltage. The frequency divider is connected to the first output of the modulation unit
25 and is designed to derive the frequency-divided signal in such a manner that it has instantaneous frequencies that are a function of the divisor values.

 A problem of the device known from US2007/0252654 is that a frequency step due to modulation does not accurately follow the modulation input.

30 Summary of the invention

 The present invention provides an electronic device, and a method, as described in the accompanying claims.

 Specific embodiments of the invention are set forth in the dependent claims. Aspects of the
35 invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

Brief description of the drawings

 Further details, aspects and embodiments of the invention will be described, by way of
40 example only, with reference to the drawings.

Figure 1 shows an example of an electronic device having a calibration arrangement,

Figure 2 shows an example of a calibration arrangement having a ripple detector,

Figure 3 shows an example of signals during a calibration process, and

Figure 4 shows an example of a method of controlling a frequency characteristic of a circuit
5 of an electronic device.

Elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. In the Figures, elements which correspond to elements already described may have the same reference numerals.

10 Detailed description of the preferred embodiments

Figure 1 shows an example of an electronic device having a calibration arrangement. The device may include a frequency generator, for example for use in phase or frequency modulation for data transmission. The device 100 has a calibration arrangement 120 for controlling a frequency characteristic of a circuit 110, in the example a phase locked loop (PLL).

15 The circuit has a phase comparator 112 (PHCOMP) having a first input for receiving a feedback signal and a second input for receiving a reference frequency from a reference source 111, for example a crystal oscillator indicated by XCO. The phase comparator has a comparator output, which is coupled to an input of a voltage controlled oscillator (VCO) 115 via a low pass filter (LFILTER) 113 for generating a phase difference signal (Vtune).

20 The voltage controlled oscillator 115 has a first control input coupled to the phase comparator output and a second control input for receiving a second control signal. The oscillator has an oscillator output for outputting an oscillator signal at an oscillation frequency controlled by the first and second control input. The oscillator signal provides the output signal of the circuit. Changing either the first or the second control signal will change the oscillator frequency, enabling
25 a dual port control for modulating the frequency of the output signal. The oscillator may be a digitally controlled oscillator having an arrangement of switched capacitors such as varactors for changing the oscillator frequency.

The circuit further has a divider 114 (DIVN) having an input coupled to the oscillation signal and an output for generating the feedback signal, the divisor (indicated by /N) of the divider being
30 programmable via a divisor input. The divisor input may be coupled to a tuning unit 140, which determines a nominal value for the divisor for generating a required frequency, e.g. a nominal carrier wave frequency. The tuning unit may have an input for receiving a digital modulation value representing a change of the divisor value, and may calculate an actual value for the divisor based on the nominal divisor value and the digital modulation value.

35 For example, Phase Shift keying (PSK) is a digital modulation scheme that conveys data by changing, or modulating, the phase of a reference signal (called the carrier wave). Also, a Frequency Shift Keying (FSK) modulation may be applied. Instead of operating with respect to a constant reference wave, a broadcast can operate with respect to itself. Digital modulation schemes use a finite number of distinct signals to represent digital data. PSK uses a finite number
40 of phases, each phase assigned to a unique pattern of binary digits. Usually, each phase encodes

an equal number of bits. Each pattern of bits forms the symbol that is represented by the particular phase. The demodulator, which is designed specifically for the symbol-set used by the modulator, determines the phase of the received signal and maps it back to the symbol it represents, thus recovering the original data. Quadrature phase-shift keying (QPSK) uses a constellation diagram with Gray coding. Each adjacent symbol only differs by one bit. QPSK uses four points on the constellation diagram, equispaced around a circle. With four phases, QPSK can encode two bits per symbol. A further system called Offset quadrature phase-shift keying (OQPSK) is a variant of phase-shift keying modulation using 4 different values of the phase to transmit. In the example, changing the divisor in the divider will lead to a steady state different frequency. OQPSK may be considered a particular case of FSK with specific frequency deviation and data rate.

For digital modulation such as described above modulating a PLL is a possible, and it is proposed to modulate both the VCO and the divider to accommodate the large bandwidth of the data, which is called dual port modulation of the PLL. To have correct modulation for a minimum BER (Bit Error Rate), it is required to minimize the Error Vector Magnitude (EVM). This can be accomplished by having a precise modulation gain on the VCO. Due to the analog nature of the VCO, a calibration is required to define this gain. Thereto the calibration arrangement as described below in detail optimizes the resources and the time needed for this calibration.

The circuit has, for dual port modulation, a modulation unit 130 having a modulation input for receiving a modulation signal (Data) and a first modulation output (VCO Mod) coupled to the second control input of the voltage controlled oscillator and a second modulation output (Divider Mod) coupled to the divisor input. The modulation of the VCO can be done by providing various voltages step. Alternatively, various digital words may be provided to the VCO to switch various capacitors banks or varicaps. The modulation unit is controllable by a control signal 123 from the calibration arrangement 120 as described now.

In operation, the data signal provides a digital modulation pattern of logical signal values 0 and 1, as schematically indicate in the Figure near the Data input. The first output VCO Mod generates an oscillator modulation signal corresponding to the Data input, which signal varies between voltage levels v_0 and v_1 or respective digital control values. The second output Divider Mod generates two values for the divisor n_0 and n_1 , which divisor values provide a nominal modulation of the frequency generated via the PLL, also indicated by ModPLL. Effectively the circuit constitutes a controllable oscillator based on the phase locked loop 110, enabling on a first port direct modulation via said VCO mod signal which modulation is matched by on a second port digitally setting the oscillator frequency by changing said divisor. Hence a change of the modulation signal Data generates a predefined change of the output frequency via said oscillator modulation signal (VCO mod) and a change of the divisor (Divider Mod) proportional to said predefined change via said divisor values. When modulation is perfect the direct frequency modulation of VCO equals the frequency modulation of PLL (as programmed by divider), and the error voltage on V_{tune} is zero. For reducing the error voltage a calibration process is used to adjust VCO modulation gain, e.g. by effectively changing the amplitude of the modulation signal or the digital control words, depending on the phase difference signal (V_{tune}).

The calibration arrangement 120 has a calibration input for receiving the phase difference signal (Vtune) and a ripple detector 121. The ripple detector is arranged for providing a detector output signal by detecting a ripple on the phase difference signal correlated to edges in the modulation signal. Optionally, the ripple detector may have a peak to peak detector, and may include a filter tuned to filter out the ripple corresponding to the frequency of the data signal. For example, in a calibration mode, a predefined data signal may be supplied as a calibration test signal to the Data input of the modulation unit, and the filter may be set to correspondingly filter such frequency components from the phase difference signal Vtune.

In Figure 1, indicated by an arrow to the phase difference signal (Vtune), examples of said ripple on the phase difference signal are schematically shown. The upper example, marked $\text{ModVCO} < \text{ModPLL}$ indicating the proportional relationship between said oscillator modulation signal (VCO Mod) and the nominal, intended modulation via the divisor values, shows a ripple occurring when the direct modulation signal effectively achieves a too small change of the modulation frequency. The middle example, marked $\text{ModVCO} = \text{ModPLL}$, shows no ripple, which occurs when the direct modulation signal effectively achieves the intended change of the modulation frequency. The lower example, marked $\text{ModVCO} > \text{ModPLL}$, shows a ripple occurring when the direct modulation signal effectively achieves a too large change of the modulation frequency.

The calibration arrangement further has a calibration control unit 122 for adjusting the second control signal of the oscillator (VCO), i.e. said oscillator modulation signal (VCO mod), based on the detector output signal such that the ripple is reduced. For example the modulation unit 130 is controlled via said control signal 123 to output different values for said voltage levels v_0 and v_1 , so that the direct modulation of the VCO more closely follows the nominal change of the oscillator frequency as determined by said divisor values n_0 and n_1 .

Optionally the ripple detector detects the polarity of the ripple with respect to the edges in the modulation signal (Data). The calibration control unit adjusts the oscillator modulation signal in a direction opposite to the detected polarity so that the ripple will be reduced. For example, a successive approximation method may be applied to determine the amount of adjustment. Alternatively, the ripple detector may detect the amplitude of the ripple and derive the adjustment based thereon.

Optionally the calibration arrangement is arranged for said adjusting the second control signal (said oscillator modulation signal VCO Mod) by setting a modulation gain. The modulation gain may be set by adjusting a parameter in the oscillator VCO, for example a bias current. As such, various further options to change the modulation gain of an oscillator are known.

Optionally, the calibration arrangement is arranged for setting the modulation gain via changes of said gain according to a successive approximation process. In such process, known as such, a sequence of successive changes is applied, each change smaller than the previous one, and the direction of change being determined based on the polarity of the ripple. An example is elucidated with reference to Figure 3 below.

Figure 2 shows an example of a calibration arrangement having a ripple detector. The calibration arrangement 200 has a calibration input for receiving the phase difference signal (Vtune). The ripple detector is arranged for providing a detector output signal (CalOut) by detecting a ripple on the phase difference signal correlated to edges in the modulation signal. The ripple detector may have a filter section to effectively filter and amplify the ripple. In the example, the filter sector includes a high pass filter 221 (HPF), followed by a low pass filter 222 (LPF) and an amplifier 223 (Amp) to generate a filtered ripple signal AmpOut.

The ripple detector has a sample and hold unit 210 (marked S&H1) coupled to the calibration input via an input section (via signal AmpOut in the Figure), and a detector 215 having a detector input coupled to a sample and hold output signal of the sample and hold unit. The detector may be a comparator, which compares the sample and hold output signal to a reference level. For example, the reference level may be a predetermined level. Then the DC signal of Vtune is to be filtered out. The sample and hold unit 210 receives a sample signal from a control unit 230 (TXDIG), which sample signal has sample pulses on edges of a predetermined polarity in the modulation signal. The sample signal for the first sample and hold unit S&H1, and the corresponding ripple in the phase difference signal Vtune, and the corresponding filtered signal AmpOut, are shown in the Figure below the filter section. Also the detector output signal CalOut is shown having logical values 0 or 1 depending on the polarity of the ripple, as indicated by an arrow.

The calibration control unit 230 (TXDIG) also receives the detector output signal CalOut, and further controls the calibration process, such as determining a Data signal for modulating during calibration, e.g. a predetermined modulation pattern. Optionally calibration may also be performed based on actual operational modulation signals, so that modulation gain may be adjusted while operating.

Optionally, the ripple detector has a second sample and hold unit 211 (S&H2) coupled to the calibration input, for example receiving the filtered ripple signal AmpOut. Now said first sample and hold unit 210 is arranged for generating the first sample and hold output signal by sampling on positive edges in the modulation signal, and the second sample and hold unit 211 is arranged for generating a second sample and hold output by sampling on negative edges in the modulation signal. The detector 215 has a second detector input coupled to the second sample and hold output signal of the sample and hold unit, and being arranged for detecting a difference between said first detector input and the second detector input.

Optionally, the ripple detector has a further low-pass filter coupled to the calibration input, the low-pass filter being arranged for generating a reference signal by low-pass filtering the phase difference signal. The further low pass effectively removes the ripple signal, and only passes an average level, e.g. a DC level. The detector has a second detector input coupled to the reference signal, and, in operation, detects a difference between the phase difference signal on said first detector input and the reference level on the second detector input. The low-pass filter may have a longer reaction time, whereas using two S&H units enables a faster reaction irrespective of the DC value.

Optionally, the detector may be a difference amplifier for providing the detector output signal. The output level on the detector output corresponds to the peak level of the ripple as sampled by said sample and hold unit or units. The output level may be determined by the calibration control unit, and used for setting a correction of the modulation gain.

5 Optionally, the detector comprises a multi threshold comparator. In operation, such comparator provides, as the detector output signal, a respective one of a set of output values when the phase difference signal exceeds a respective threshold of multiple thresholds. The respective output value may be used by the calibration control unit for setting a respective, corresponding amount of correction of the modulation gain.

10 In a practical implementation various elements of the above circuit may be combined with the calibration arrangement in a single entity, such as an integrated semiconductor circuit (IC). For example, the device may include a digitally controlled oscillator constituting the voltage controlled oscillator. Also, the device may include the phase locked loop comprising the phase comparator, the divider and the modulation unit.

15 Figure 3 shows an example of a calibration process. Four corresponding curves show different signals during calibration. The first graph 310 shows an example of a phase difference signal during the calibration process. The Vtune voltage is filtered and sampled, ripple value is stored in a sample and hold unit. The second curve 320 shows the detector output signal of the ripple detector, which indicates the polarity of the ripple. The polarity of the ripple is checked by the
20 comparator that provides a digital output. The third curve 312 shows the oscillator modulation signal (VCO Mod), the amplitude of which is adjusted by gain adjustments in dependence of the detector output. The comparator output is used by the logic to run a successive approximation algorithm to optimize VCO gain. Finally, the fourth curve shows the output frequency, which should follow a modulation data signal. This curve shows, in the initial part, relatively strong deviation of
25 the desired modulation pattern, while the final part shows that the frequency has the desired modulation pattern. Hence the modulation is adjusted up to a substantially perfect one by reducing any analog errors.

In a practical example the gain on the modulation signal input of the VCO is calibrated to optimize the EVM. A test signal at 200KHz is sent by a modulation unit on the 2 ports and the
30 mismatch between the divisor change and the VCO gain is measured via a ripple on the phase difference signal (Vtune). Vtune is filtered and amplified, and then sampled, to determine the ripple level and sign. The timing of the sampling needs to be well controlled, and may be programmable. The calibration unit measures the ripple of Vtune. If the frequency step is exactly 1MHz there is only noise on Vtune (around 40uVpp). When an error is present on the VCO gain a ripple appears
35 on Vtune (around 400uVpp for 3% error). The ripple is synchronous with the data signal so phase delay of the ripple from the data is indicative of a direction of changes of the gain.

For example, in a circuit as shown in Figure 2, Vtune is high pass (100 kHz), and then low pass, filtered (low pass, 2nd order, 300KHz) and amplified (40dB). The filtered voltage is then sampled and hold by two sample and hold units controlled by two clocks based on respective
40 positive or negative edges in the modulation signal. When the clock is high the switch is on

(sample), when the clock is low the switch is off (hold). The comparator output indicates which signal is the highest, which determines the gain change direction.

Figure 4 shows an example of a method of controlling a frequency characteristic of a circuit of an electronic device. The circuit may be a phase locked loop as described above, and provides a phase difference signal indicative of a frequency error due to modulating. The calibration method 400 starts when a calibration is required at node CALIB 410. A first step MOD_PH 420 provides a modulation and receives a corresponding phase difference signal. A second step DET_RIP 430 detects a ripple on the phase difference signal correlated to edges in the modulation signal. A third step ADJ_G 440 adjusts the gain on the modulation signal based on the detector output signal such that the ripple is reduced. Then, in step REDUC 450, it is determined whether the ripple is reduced. If the reduction is still insufficient, the method returns to the first step. If the required reduction is achieved the calibration process stops at node END 460.

In the foregoing specification, the invention has been described with reference to specific examples of embodiments of the invention. It will, however, be evident that various modifications and changes may be made therein without departing from the broader spirit and scope of the invention as set forth in the appended claims. For example, the connections may be any type of connection suitable to transfer signals from or to the respective nodes, units or devices, for example via intermediate devices. Accordingly, unless implied or stated otherwise the connections may for example be direct connections or indirect connections.

Because the apparatus implementing the present invention is, for the most part, composed of electronic components and circuits known to those skilled in the art, circuit details will not be explained in any greater extent than that considered necessary as illustrated above, for the understanding and appreciation of the underlying concepts of the present invention and in order not to obfuscate or distract from the teachings of the present invention.

Although the invention has been described with respect to specific conductivity types or polarity of potentials, skilled artisans appreciated that conductivity types and polarities of potentials may be reversed.

Also, the invention is not limited to physical devices or units implemented in non-programmable hardware but can also be applied in programmable devices or units able to perform the desired device functions by operating in accordance with suitable program code. Furthermore, the devices may be physically distributed over a number of apparatuses, while functionally operating as a single device.

Furthermore, the units and circuits may be suitably combined in one or more semiconductor devices.

In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word 'comprising' does not exclude the presence of other elements or steps than those listed in a claim. Furthermore, the terms "a" or "an," as used herein, are defined as one or more than one. Also, the use of introductory phrases such as "at least one" and "one or more" in the claims should not be construed to imply that the introduction of another claim element by the indefinite articles "a" or "an" limits any particular claim containing such introduced claim element to

inventions containing only one such element, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite articles such as "a" or "an." The same holds true for the use of definite articles. Unless stated otherwise, terms such as "first" and "second" are used to arbitrarily distinguish between the elements such terms describe. Thus, these terms are not necessarily intended to indicate temporal or other prioritization of such elements. The mere fact that certain measures are recited in mutually different claims does not indicate that a combination of these measures cannot be used to advantage.

Claims

1. An electronic device, the device (100) comprising a calibration arrangement (120, 200) for
5 controlling a frequency characteristic of a circuit, the circuit comprising
- a phase comparator (112) having a first input for receiving a feedback signal and a second input for receiving a reference frequency and a comparator output for generating a phase difference signal,
 - a voltage controlled oscillator (115) having a first control input coupled to the phase comparator
10 output and a second control input for receiving a second control signal, and an oscillator output for outputting an oscillator signal at an oscillation frequency controlled by the first and second control input,
 - a divider (114) having an input coupled to the oscillation signal and an output for generating the feedback signal, the divisor of the divider being programmable via a divisor input,
 - 15 - a modulation unit (130) having a modulation input for receiving a modulation signal and a first modulation output coupled to the second control input of the voltage controlled oscillator and a second modulation output coupled to the divisor input such that a change of the modulation signal generates a predefined change of the output frequency and a change of the divisor proportional to said predefined change,
- 20 the calibration arrangement comprising
- a calibration input for receiving the phase difference signal,
 - a ripple detector (121) for providing a detector output signal by detecting a ripple on the phase difference signal correlated to edges in the modulation signal,
 - a calibration control unit (122) for adjusting the second control signal based on the detector output
25 signal such that the ripple is reduced.
2. The device as claimed in claim 1, wherein the ripple detector comprises at least one sample and hold unit (210) coupled to the calibration input, and a detector (215) having a detector input coupled to a sample and hold output signal of the sample and hold unit,
30 the sample and hold unit being arranged for generating the sample and hold output signal by sampling on edges in the modulation signal.
3. The device as claimed in claim 2, wherein the ripple detector comprises a second sample and hold unit (211) coupled to the calibration input,
35 said first sample and hold unit (210) being arranged for generating the first sample and hold output signal by sampling on positive edges in the modulation signal, and the second sample and hold unit (211) being arranged for generating a second sample and hold output by sampling on negative edges in the modulation signal, and the detector (215) having a second detector input coupled to the second sample and hold output
40 signal, and being arranged for detecting a difference between said first detector input and the

second detector input.

4. The device as claimed in claim 2, wherein the ripple detector comprises a low-pass filter coupled to the calibration input, the low-pass filter being arranged for generating a reference signal by low-pass filtering the phase difference signal, and the detector having a second detector input coupled to the reference signal, and being arranged for detecting a difference between said first detector input and the second detector input.

5. The device as claimed in claim 2, 3 or 4, wherein the detector (215) comprises a comparator for providing the detector output signal.

6. The device as claimed in claim 2, 3 or 4, wherein the detector (215) comprises a multi threshold comparator for providing, as the detector output signal, a respective one of a set of output values when the phase difference signal exceeds a respective threshold of multiple thresholds.

7. The device as claimed in any of the preceding claims, wherein the device comprises a digitally controlled oscillator constituting the voltage controlled oscillator (115).

8. The device as claimed in any of the preceding claims, wherein the device comprises a phase locked loop (110) comprising the phase comparator, the divider and the modulation unit.

9. The device as claimed in any of the preceding claims, wherein the calibration arrangement is arranged for said adjusting the second control signal by setting a modulation gain.

10. The device as claimed in claim 9, wherein the calibration arrangement is arranged for setting the modulation gain via changes of said gain according to a successive approximation process.

11. An integrated circuit comprising at least one electronic device according to any one of the preceding claims.

12. A method of controlling a frequency characteristic of a circuit of an electronic device, the circuit comprising

- a phase comparator having a first input for receiving a feedback signal and a second input for receiving a reference frequency and a comparator output for generating a phase difference signal,
- a voltage controlled oscillator having a first control input coupled to the comparator output and a second control input for receiving a second control signal, and an oscillator output for outputting an oscillator signal at an oscillation frequency controlled by the first and second control input,
- a divider having an input coupled to the oscillation signal and an output for generating the feedback signal, the divisor of the divider being programmable via a divisor input,

- a modulation unit having a modulation input for receiving a modulation signal and a first modulation output coupled to the second control input of the voltage controlled oscillator and a second modulation output coupled to the divisor input such that a change of the modulation signal generates a predefined change of the output frequency and a change of the divisor proportional to

- 5 said predefined change,
the method comprising
- receiving (420) the phase difference signal,
 - detecting (430) a ripple on the phase difference signal correlated to edges in the modulation signal,
 - 10 - adjusting (440) the second control signal based on the detector output signal such that the ripple is reduced.

13. The method as claimed in claim 12, wherein the ripple detector comprises at least one sample and hold unit coupled to the calibration input, and the method comprises generating a sample and hold output signal by sampling on edges in the modulation signal, and detecting the ripple on the

15 sample and hold output signal.

14. The method as claimed in claim 13, wherein the ripple detector comprises a second sample and hold unit coupled to the calibration input, and the method comprises

20 generating, via said first sample and hold unit, the first sample and hold output signal by sampling on positive edges in the modulation signal,
generating, via the second sample and hold unit, a second sample and hold output by sampling on negative edges in the modulation signal, and
detecting a difference between first sample and hold output signal and the second sample and hold

25 output signal.

15. The method as claimed in claim 13, wherein the ripple detector comprises a low-pass filter coupled to the calibration input, the low-pass filter being arranged for generating a reference signal by low-pass filtering the phase difference signal, and the method comprises

30 detecting the detector a difference between the sample and hold output signal and the reference signal.

16. The method as claimed in claim 13, 14 or 15, wherein the method comprises detecting a respective one of a set of output values when the difference of the difference peak signal and the

35 reference signal exceeds a respective threshold of multiple thresholds.

17. The method as claimed in any of the claims 12 to 16, wherein the method comprises adjusting the second control signal by setting a modulation gain.

18. The method as claimed in claim 17, wherein the method comprises setting the modulation gain via changes of said gain according to a successive approximation process.

1/4

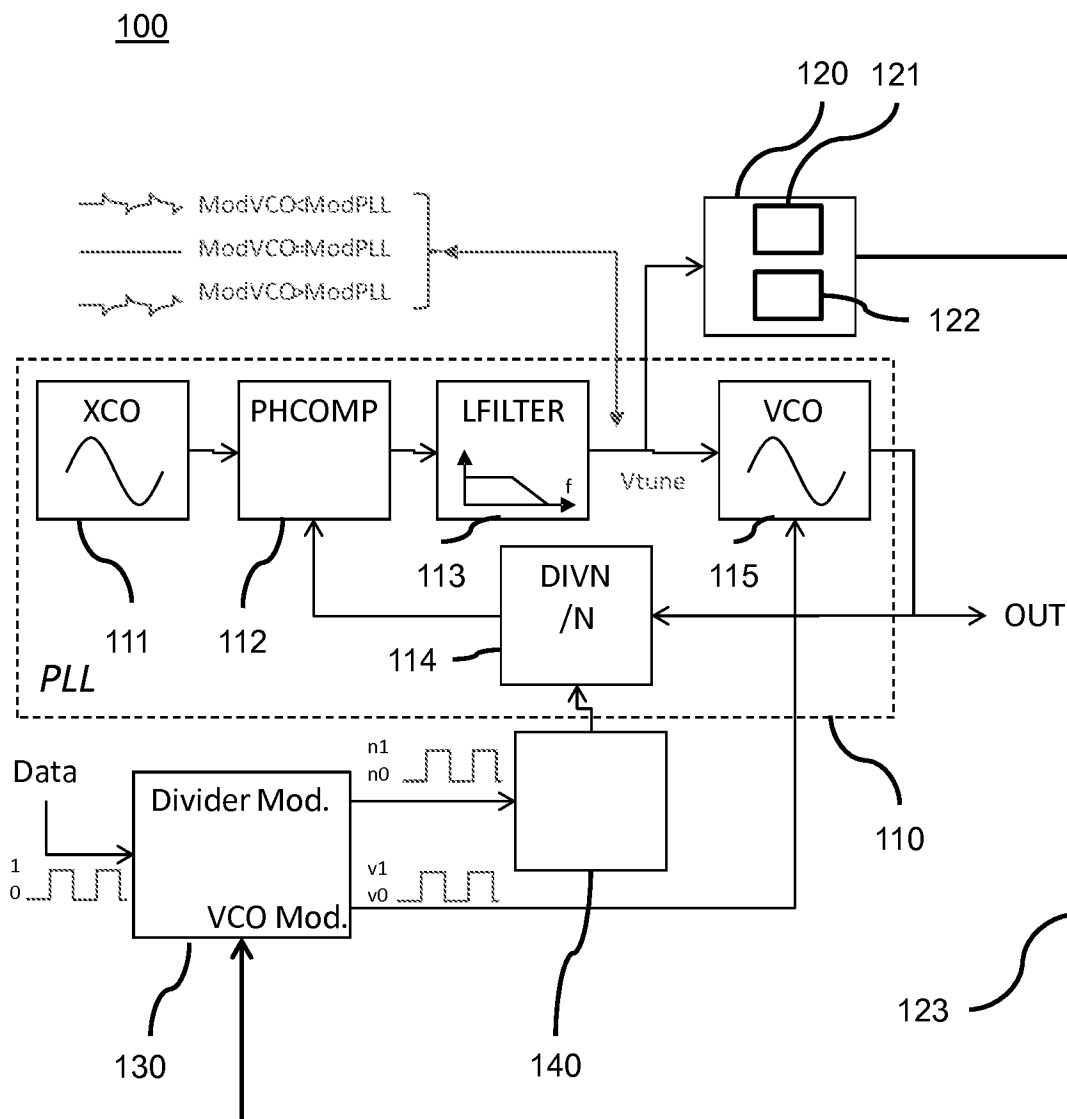


Fig.1

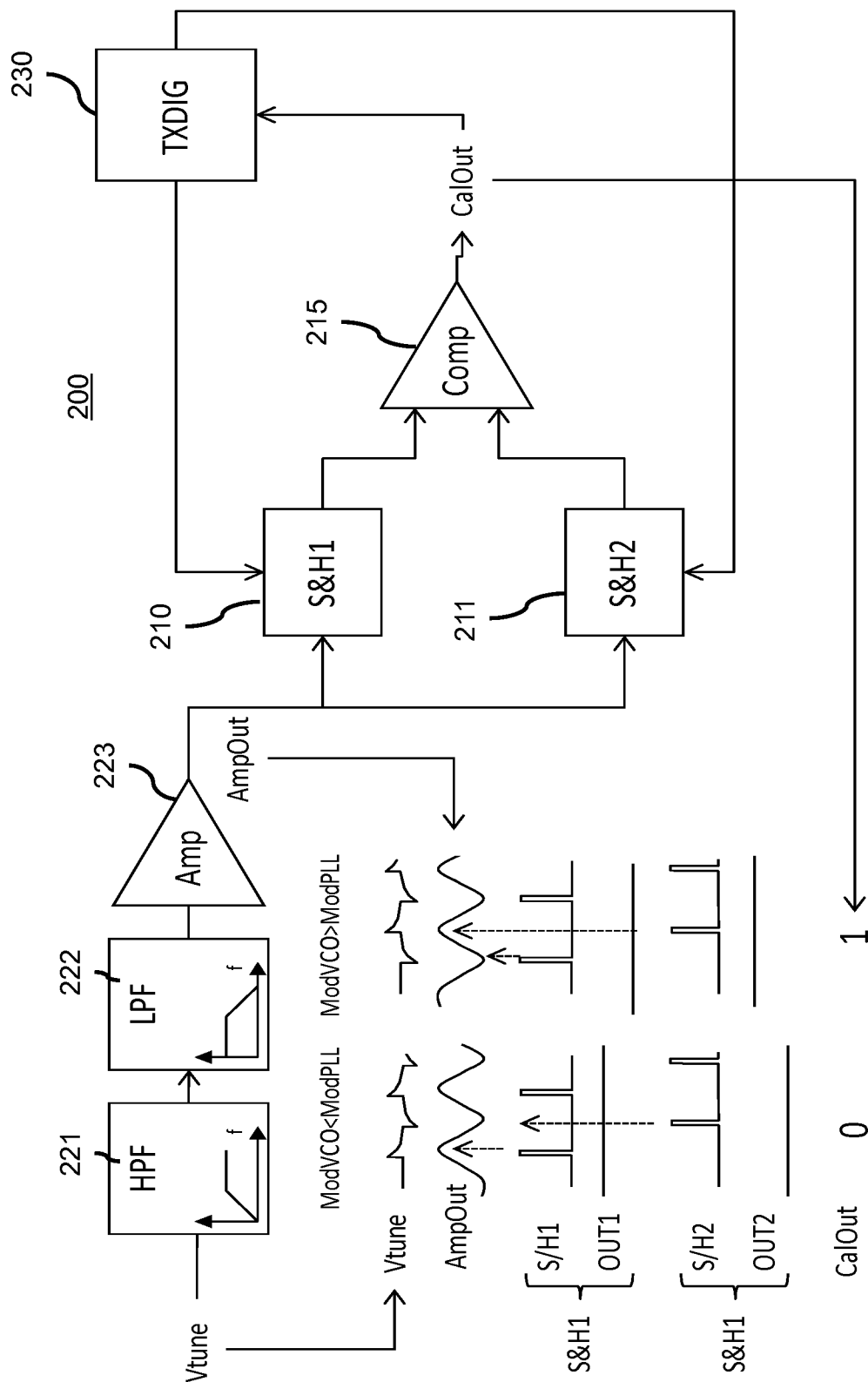


Fig. 2

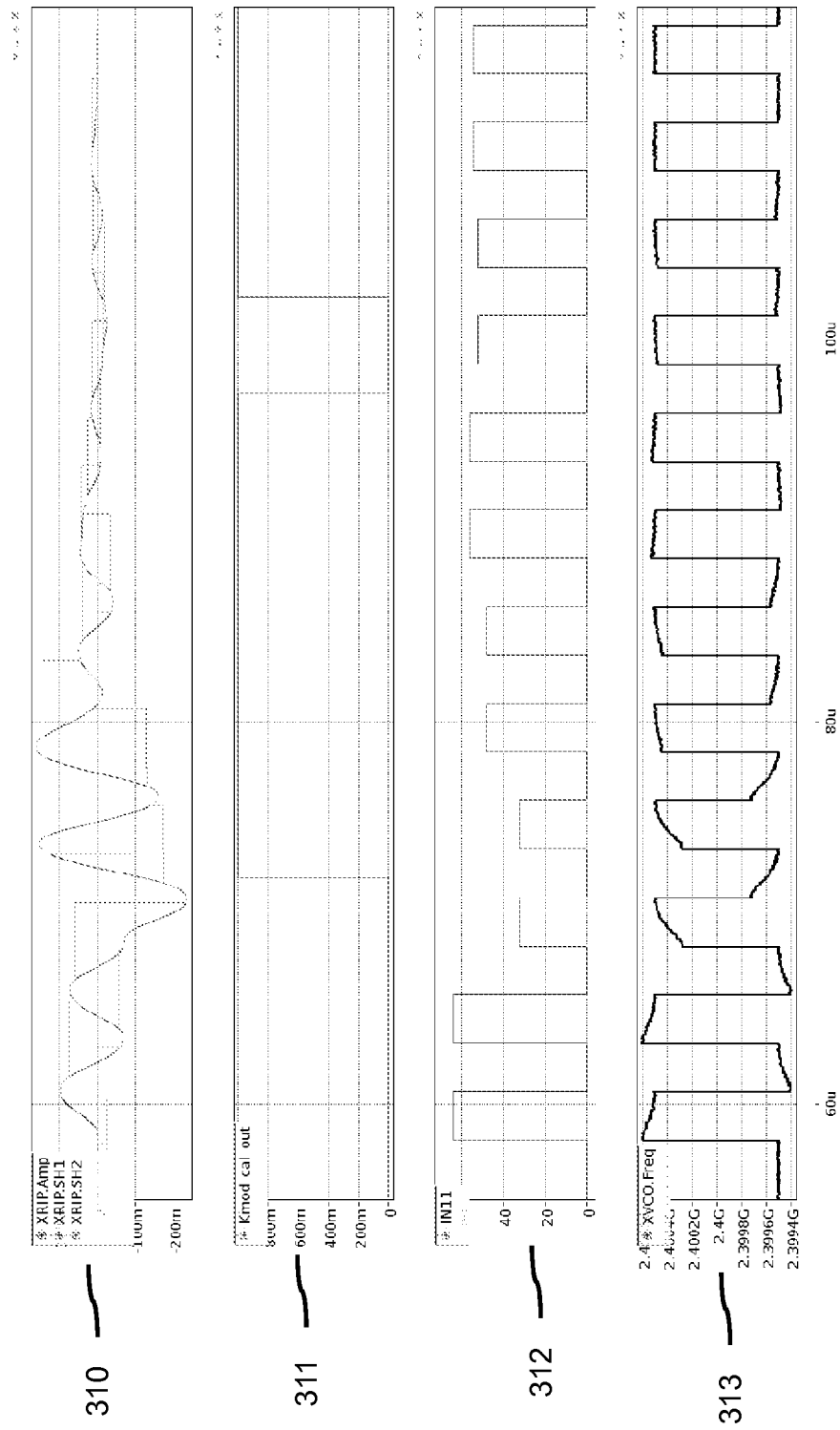


Fig. 3

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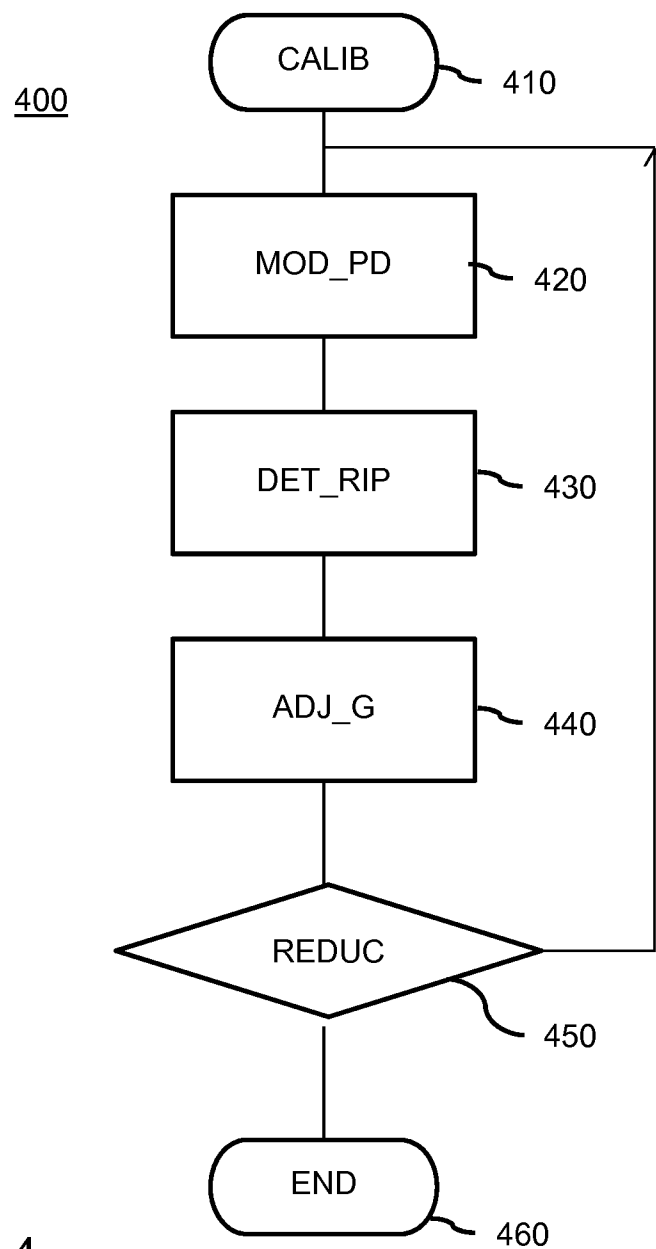


Fig. 4

A. CLASSIFICATION OF SUBJECT MATTER**H03L 7/08(2006.01)i, H03L 7/099(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03L 7/08; H03L 7/00; H03L 7/197; H03L 7/18; H04L 27/36; H03C 3/09; H03L 7/087

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: phase comparator, VOC, divider, modulation, frequency, synthesizer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2006-0267697 A1 (LEE, CHANG-HYEON et al) 30 November 2006 See abstract, claims 1-20 and figures 1-2	1-18
A	US 05568098 A (HORIE; HIROSHI et al.) 22 October 1996 See abstract, claims 1-9 and figures 7-9	1-18
A	EP 0357996 B1 (NEC CORPORATION) 26 November 1997 See abstract, claim 1 and figure 1	1-18
A	US 05495206 A (HIETALA; ALEXANDER W.) 27 February 1996 See abstract, claim 1 and figure 4	1-18
A	US 2010-0329388 A1 (KO, SANG-SOO) 30 December 2010 See abstract, claim 1 and figure 1	1-18



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

29 April 2013 (29.04.2013)

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

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