



(10) International Publication Number
WO 2010/029480 A2

(43) International Publication Date
18 March 2010 (18.03.2010)

PCT

- (51) **International Patent Classification:** Not classified
- (21) **International Application Number:** PCT/IB2009/053873
- (22) **International Filing Date:** 4 September 2009 (04.09.2009)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:** 08105281.3 9 September 2008 (09.09.2008) EP
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- (81) **Designated States** (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ,

CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO,
DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP,
KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD,
ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI,
NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD,
SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT,
TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

Published:

- *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

- (54) Title:** MEMORY CONTROLLER

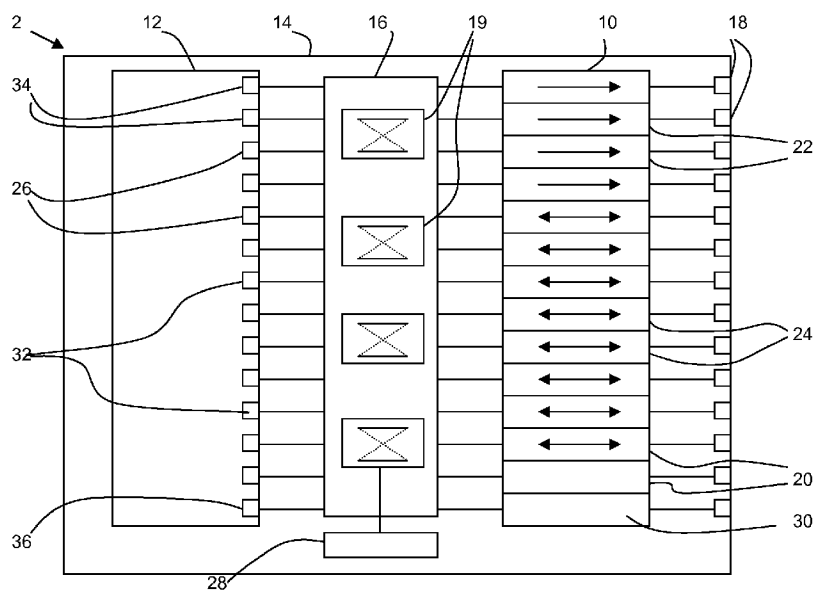


Fig. 1

- (57) Abstract:** A memory controller 2 for controlling DDR SDRAM includes a physical layer block 10 connected to output pads 18 for driving the output pads with electrical signals, and a memory control block 12 for generating and receiving data signals, address signals and control signals and passing them to the physical layer block which converts these signals into the electrical signals actually transmitted from the controller. A multiplexer 16 is provided, not between the physical layer block 10 and the output pads 18, but between the memory control block 12 and the physical layer block 10.

DESCRIPTION

MEMORY CONTROLLER

5 The invention relates to a memory controller and a method for operating the memory controller.

 In a computer or other electronic circuit, a memory is accessed by means of a memory controller that connects to the memory using a number of
10 lines, typically including a number of data lines, a number of address lines and miscellaneous other lines such as a clock. These lines are typically connected from outputs, i.e. pads, pins or balls on the memory controller by interconnects across a substrate to outputs, again as pads pins or balls, on the memory.

 As memory devices become more advanced they become faster and in
15 order to ensure good signal integrity timing of the signals on the interconnects becomes more critical.

 For this reason, the routing of the interconnect signals is important and it is generally necessary to avoid crossings of interconnects. In order to do this, the pin, pad or ball outputs of the memory controller need to match the
20 outputs of the memory. Normally, therefore, when designing memory controllers, including memory controllers integrated into systems on chips, the assignments of the outputs of the memory controllers are carefully assigned to ensure that they match with the outputs of the memory.

 Such an alignment is particularly important for double data rate (DDR)
25 synchronous dynamic random access memory (SDRAM) devices. Note in this connection that DDR is used in the present text to refer not merely to first generation DDR devices but also to subsequent generations such as those sometimes referred to as DDR2, DDR3, GDDR2, GDDR3 etc. DDR chips generally use both the rising and falling edges of the clock to transfer data,
30 unlike conventional memories using only one rising or falling edge on each clock cycle.

However, a problem can arise since the design of a memory controller and memory can occur at the same time and the output arrangement of one may not be finalised before the output arrangement of the other needs to be finalised. This can occur, for example, in the design of multichip packages, in particular, as well as many other areas.

In some technology areas it is known to provide a variable output arrangement of pins, balls or pads, connected for example using a crosspoint switch between the pads and the remainder of the circuit. Such an approach causes difficulty for the control of some memories, such as DDR SDRAMs, because of the extremely tight timing constraints on the signals between memory controller and memory that cannot normally be met when using such a crosspoint switch.

According to the invention, there is proposed a memory controller according to claim 1.

By controlling a multiplexer it is effectively possible to vary the arrangement of outputs of the memory controller after the design of the chip. By arranging the multiplexer between the physical layer block and the memory protocol block the multiplexer does not affect the transmission of the data signals themselves, so the integrity of the data transfer between memory controller and memory is not significantly impaired. Thus, the invention makes it possible to exchange outputs of the memory controller for DDR which would not be feasible with a conventional pin multiplex arrangement with a multiplexer between the pins and the circuit.

In a preferred embodiment, the multiplexer is reconfigured in software.

For a better understanding of the invention, embodiments will now be described, purely by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a schematic illustration of a memory controller according to an embodiment of the invention; and

Figure 2 illustrates the memory controller of Figure 1 in use.

The control of memories takes place in a number of layers. A physical layer, normally referred to as PHY, deals with generating the physical data signals. A memory protocol layer deals with the higher level memory protocol.

5 These two can be provided as separate modules that can communicate with one another, for example using a proprietary protocol. Alternatively, a public protocol has been proposed as a standard, known as the DDR PHY (DFI) interface standard proposed by a consortium of a number of companies and available at <https://www.denali.com/ddr-phy/en>.

10 In the embodiment of Figure 1, a memory controller 2 is configured with the physical layer dealt with in a physical layer block 10 and the higher level memory protocol in a memory control block 12. Both of these blocks are implemented using hardware on the surface of a system on chip device 14 in combination with software.

15 A multiplexer 16 is provided both electrically and physically between the memory control block 12 and the physical layer block 10. Outputs, here pads 18, are provided connected directly to the physical layer block. The multiplexer includes a plurality of multiplex elements 19 that allow the multiplexer to be controlled in software.

20 The physical layer block 10 includes a number of physical interface circuits 20. Some of these circuits are bidirectional double data rate circuits 24 which can pass data either to or from the outputs 18 at a double data rate, clocked on both the rising and falling clock pulse.

Other physical interface circuits 20 are unidirectional single data rate circuits 22 which pass data in a single direction at a single data rate, clocked on either the rising or the falling clock pulse.

The memory control block 12 has a number of memory control block outputs 26. These outputs all correspond to different memory signals. Thus the outputs include data outputs, address outputs, and any other outputs
30 required to control the memory. These may include clock outputs (CK), clock enable outputs (CKE#) write enable (WE#) outputs and mask outputs. These outputs carry the logical signals at the internal logic levels of the memory

control block but not the actual physical electrical signals - it is the physical layer block 10 that converts these logical signals into the appropriate electrical signals on the outputs 18.

In use, as illustrated in Figure 2, the memory controller 2 is connected
5 to DDR SDRAM memory module 4 by means of interconnects 6 on substrate 8. The multiplexer 16 connects the physical layer block 10 and memory control block 12, so that the outputs 18 are correctly configured to connect to the pads 40 of memory module 4 without requiring any crossings of the interconnects 6.

10 Note that DDR SDRAM has some constraints on interchanging outputs. This is because the physical layer does not have exactly the same function on all outputs. In particular, data outputs deal with bidirectional signals clocked on both the rising and falling edges of the clock, and address outputs are unidirectional and are clocked only on one of the rising and falling edges.

15 For this reason, bidirectional bits, and the corresponding outputs, may be exchanged. These bidirectional memory control block outputs 32 (group (a)) include data bits and mask bits.

Although in conventional DDR drivers, the mask is handled by a unidirectional physical interface circuit, in the present embodiment the mask is
20 handled by a bidirectional physical interface circuit which is only used in one direction by the controller. This allows the mask bit to be exchanged with data bits.

In particular, the data bits for a byte DQ0, DQ1 ... DQ7 may be exchanged with the mask bit for a byte DM0.

25 It is also possible to exchange the outputs and hence the corresponding bits that use unidirectional physical interface circuits. These Unidirectional memory control block outputs 34 (group (b)) include the following: Address, Bank Address, RAS#, CAS#, WE#, and CS# where the abbreviations have meanings as follows: RAS# is the row address strobe, CAS# is the column
30 address strobe, WE# is the write enable bar signal, and CS# is the column select bar signal.

Some bits and corresponding outputs cannot be exchanged, these may be referred to as group (c), fixed memory control block outputs 36, including the Clock and CKE outputs, where CKE is the clock enable signal.

The multiplexer 16 is connected to multiplex controller 28 which is
5 arranged to ensure that only suitable connections are made, i.e. that fixed memory control block outputs 36 are not multiplexed but always connected to the same fixed physical interface circuits 30, bidirectional memory control block outputs 32 are connected to bidirectional physical interface circuits 24 and unidirectional memory control block outputs 34 are connected to
10 unidirectional physical interface circuits 22.

Thus, if the multiplexer 16 is considered to exchange outputs, such exchanges are made only between outputs that share the same physical layer implementation. This is achieved by only allowing exchanges between the outputs in group (a) and between the outputs in group (b), but not between the
15 outputs in different groups or within group (c).

Although this may seem to be a serious constraint, in many cases it is not. Typically, the signals indicated as part of a group are in any event grouped together on outputs, so in practice it is frequently only necessary to exchange outputs within group (a) and within group (b) to ensure compatibility
20 of the memory controller with memory devices.

The clock and CKE signals can be routed first to ensure that the output location of these special signals is fixed and makes no unwanted crossings.

By exchanging bits in a multiplexer between the physical layer and a higher layer, no additional components are used between the physical
25 interface circuits 22 and the DDR memory. Thus, the stringent timing demands are not affected by the multiplexer.

In an alternative embodiment conventional unidirectional physical layer interface circuits are used for the mask. In this case, it is not possible to exchange mask and data bits. However, using this alternative embodiment
30 the published DDR PHY interface standard may be used without any modification.

Those skilled in the art will understand that the above embodiments are provided only by way of example and that modifications may be made.

For example, although the above description describes multiplex elements that are controlled in software, alternative multiplex elements that are
5 programmed during manufacture of an individual chip are also possible, such as optical antifuses and other controllable elements as known to those skilled in the art.

Further, although the above embodiments describe specific memory control block outputs, the memory control block outputs may be varied to adapt
10 to the control of any particular type of memory. If different generations or designs of DDR SDRAM require different control signals, appropriate memory control block outputs may be used.

CLAIMS

1. A memory controller for controlling double data rate - DDR - synchronous dynamic random access memory - SDRAM, the memory controller comprising:
- 5 an array of outputs (18) for connecting to DDR memory;
- a physical layer block (10) comprising a plurality of DDR physical interface circuits directly connected to respective outputs for sending and receiving physical signals through the outputs;
- 10 a memory control block (12) for sending and receiving data and control signals to and from the physical layer block, the memory control block comprising a plurality of memory control block outputs (26); and
- a multiplexer (16) arranged to selectably connect the plurality of memory control block outputs to the DDR physical interface circuits to select
- 15 which memory control block outputs are connected to which DDR physical interface circuits.
2. A memory controller according to claim 1, wherein the multiplexer (16) contains software-controlled multiplex elements (19) for
- 20 controllably selecting in use which memory control block outputs are connected to which DDR physical interface circuits.
3. A memory controller according to claim 1 or 2, wherein the DDR physical interface circuits include:
- 25 bidirectional dual data rate interface circuits (24) for passing data in either direction through the interface circuit at a double data rate; and
- unidirectional single data rate interface circuits (22) for passing data in one direction through the interface circuit at a single data rate.
- 30 4. A memory controller according to claim 3 wherein:

the memory control block outputs include bidirectional memory control block outputs (32), including outputs for transferring data, and unidirectional control block outputs (34), including outputs for transferring the address, and the multiplexer is arranged to selectably connect the bidirectional
5 memory control block outputs (32) to the bidirectional dual data rate interface circuits (24) and the unidirectional memory control block outputs (34) to the unidirectional interface circuits (22), but not to connect the bidirectional memory control block outputs (32) to the unidirectional interface circuits (22) nor the unidirectional memory control block outputs (34) to the bidirectional
10 interface circuits (24).

5. A memory controller according to claim 4 wherein the bidirectional memory control block outputs (32) further include mask outputs for transferring a mask
15

6. A memory controller according to any of claims 1 to 5 wherein the memory control block outputs (26) further include fixed memory control block outputs (36) and wherein the fixed memory control block outputs are connected to fixed interface circuits (30) in the physical layer block (10).
20

7. A memory controller according to any of claims 1 to 6 wherein the physical layer block (10) and the memory control block (12) are arranged to communicate using the DDR PHY interface standard.

25 8. A system on chip circuit (14) including a memory controller according to any preceding claim.

9. A circuit comprising:
a memory controller (2) according to any of claims 1 to 7; and
30 a DDR SDRAM (4) having outputs connected to respective outputs of the memory controller through respective interconnects.

10. Use of a circuit according to claim 9, comprising:
controlling the multiplexer (16) to selectably connect the memory control block outlets (12) to the corresponding outputs (40) of the DDR SDRAM.

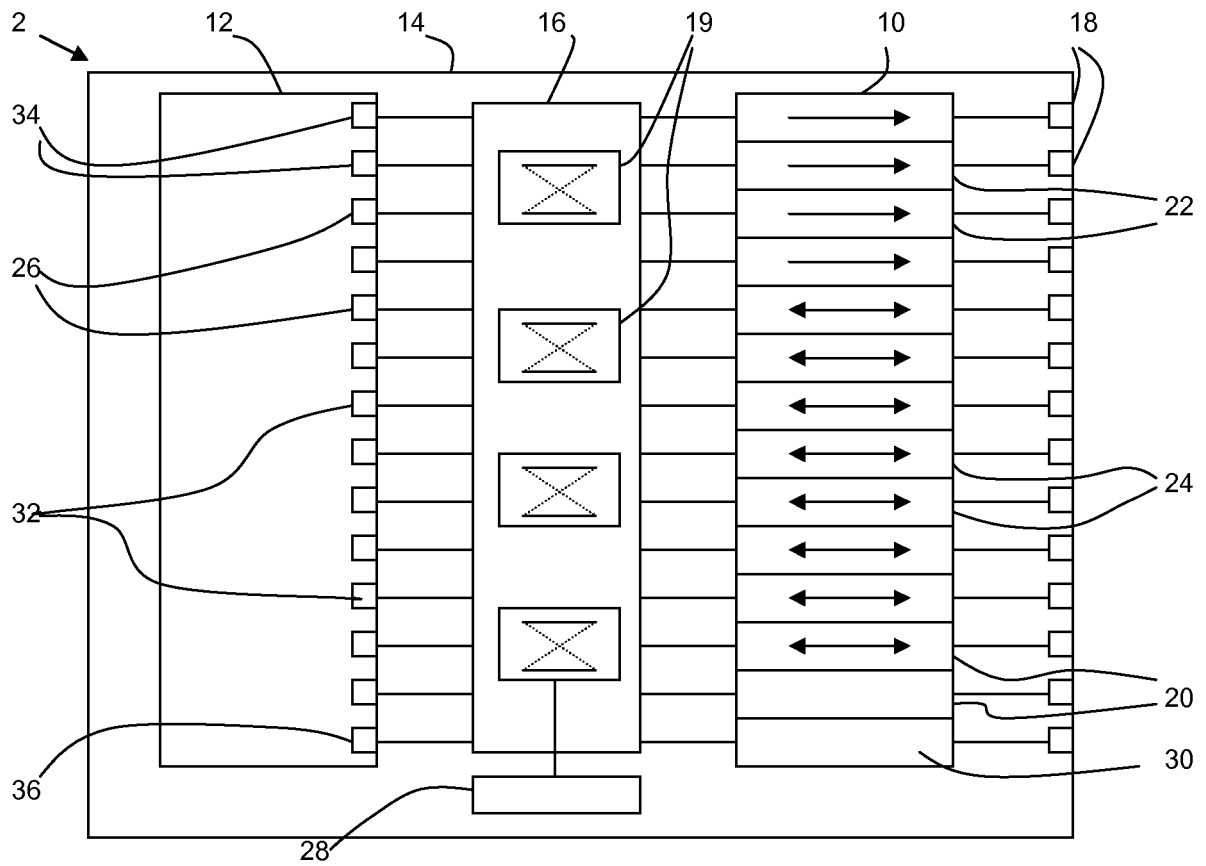


Fig. 1

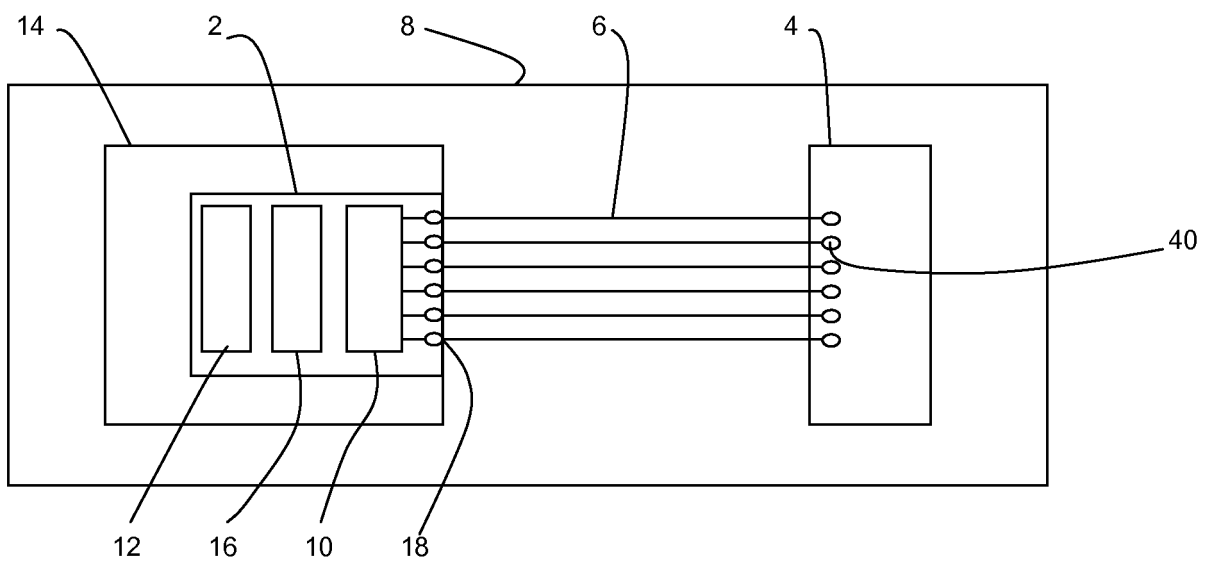


Fig. 2