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**(71) Applicant:** RAMBUS, INC. [US/US]; 2465 Latham Street, Mountain View, CA 94040 (US).

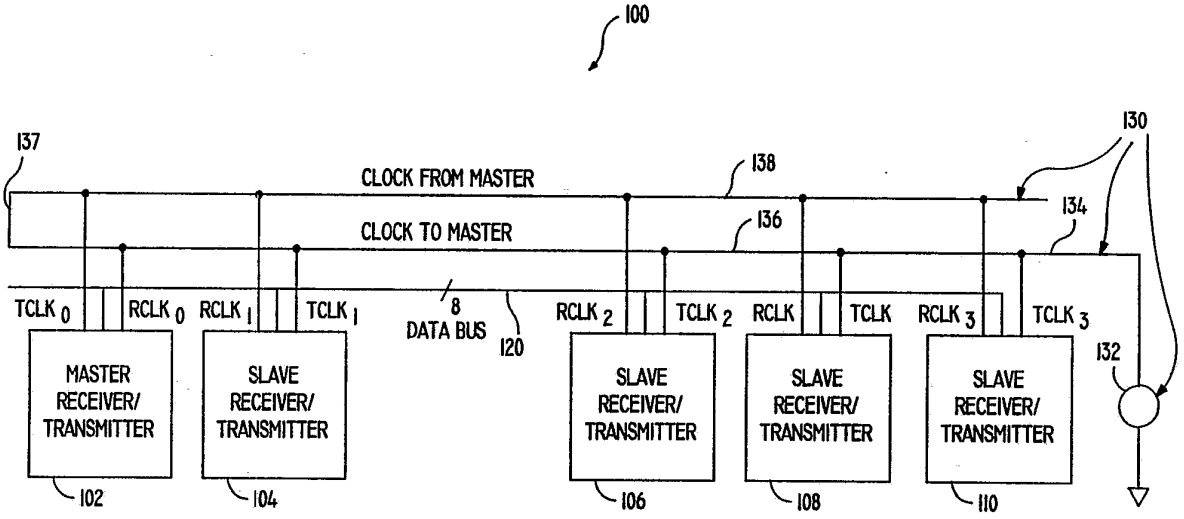
**(72) Inventors:** GASBARRO, James, Anthony ; 1613 Notre Dame Drive, Mountain View, CA 94040 (US). HOROWITZ, Mark, Alan ; 2024 Columbia Street, Palo Alto, CA 94306 (US). BARTH, Richard, Maurice ; 787 Los Robles, Palo Alto, CA 94306 (US). LEE, Winston, K., M. ; 119 Adrian Avenue, South San Francisco, CA 94080 (US). LEUNG, Wingyu ; 10450 Orange Avenue, Cupertino, CA 95014 (US). FARMWALD, Paul, Michael ; 190 Golden Oak Drive, Portola Valley, CA 94028 (US).

**(74) Agents:** VINCENT, Lester, J. et al.; Blakely, Sokoloff, Taylor & Zafman, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, CA 90025 (US).

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**(54) Title:** METHOD AND CIRCUITRY FOR MINIMIZING CLOCK-DATA SKEW IN A BUS SYSTEM




**(57) Abstract**

A bus system is described that minimizes clock-data skew. The bus system includes a data bus, a clockline and synchronization circuitry. The clockline has two clockline segments. Each clockline segment extends the entire length of the data bus and is joined to the other clockline segment by a turnaround at one end of the data bus. The clockline ensures that clock and data signals travel in the same direction. Synchronization circuitry within transmitting devices synchronizes data signals to be coupled onto the data bus with the clock signal used by other devices to receive the data.

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# METHOD AND CIRCUITRY FOR MINIMIZING CLOCK-DATA SKEW IN A BUS SYSTEM

## FIELD OF THE INVENTION

The present invention relates to synchronous bus systems. More particularly, the present invention relates to a bus system for minimizing clock-data skew in order to avoid errors, wherein data transmission is synchronized with respect to a passing clock signal.

## BACKGROUND OF THE INVENTION

Computer systems typically utilize a bus system. Several devices are typically coupled to a data bus. Some prior bus systems operate synchronously, i.e., using a clock signal to validate data signals. Within synchronous bus systems, clock-data skew can be a concern because such skew can prevent the clocking of valid data. Thus, data errors can result from clock-data skew. Clock-data skew results from the difference between data signal propagation delay and clock signal propagation delay.

For certain prior art synchronous bus systems with sufficiently short bus and clockline lengths, clock-data skew might not be a concern because clock and data signals have only a short distance to travel and arrive nearly instantaneously. Within a synchronous bus system with a long data bus and a long clockline, clock-data skew is often a concern, however, especially if high clock speeds are desired. Within many prior art synchronous bus systems, a clock period must exceed clock signal propagation delay. Put another way, clock speed must generally slow as clockline length increases. This prior art relationship is expressed by Expression 1:

(1) Clock Period > set-up time of data-to-clock signal +

hold time of data-to-clock signal +

clock-data skew

One prior art scheme for reducing clock-data skew error is illustrated in Figure 1. Rather than using a single clock source, multiple clock sources are used. That is, many matched clock lines are coupled to a single clock generator. The clock lines are matched so that a clock signal arrives at each device at substantially the same point in time, despite long clockline lengths. Thus, the bus system shown must operate with a clock period that is greater than or equal to the data propagation delay of the bus plus clock-to-data-skew plus clock-to-data hold time.

One disadvantage of the bus system of Figure 1, however, is the relative complexity of that bus system. A clockline is required for each device that is clocked and each clockline typically must be carefully tuned to ensure simultaneous clocking of all devices. Another disadvantage of the bus system of Figure 1 is that its clock period is limited by the propagation delay of the data bus.

Figure 2 illustrates a different prior art synchronous bus system scheme utilizing a long data bus. The master device generates two clock signals -- namely, a receive clock, RCLK, and a transmit clock, TCLK. In conjunction with appropriate frame control signals, the receive clock is used to clock both the transmission of data by slave devices and the reception of data by the master device. The bus system of Figure 2 thus decouples clock period from the propagation delay of the data bus.

A disadvantage of the bus system scheme of Figure 2 is that two clock sources are required (rather than a single clock source) in addition to control signals. A further disadvantage is that the bus system of Figure 2 permits only one master device.

SUMMARY AND OBJECTS OF THE INVENTION

One object of the present invention is to reduce or eliminate clock and data timing errors.

Another object of the present invention is to provide a data bus that allows high speed clocking of data while reducing clock and data timing errors.

Another object of the present invention is to minimize clock-data skew to avoid errors in a bus system with a relatively long bidirectional data bus.

Another object of the present invention is to minimize clock-data skew to avoid errors in a bus system with a relatively long clockline.

Another object of the present invention is to minimize clock-data skew to avoid errors in a computer system having a relatively high speed bus.

Another object of the present invention is to avoid having a speed of a bus be limited by clockline length or bus length.

Another object of the present invention is to provide a synchronous bus system in which clock-data skew is reduced or eliminated.

Another object of the present invention is to avoid the necessity of multiple clocks for a high speed bus system with a relatively long bus.

A further object of the present invention is to provide a high speed synchronous data bus.

Another object of the present invention is to provide a synchronous data bus that accommodates a fixed latency protocol between devices on the bus.

Another object of the present invention is to provide a data bus that accommodates a multiplicity of master devices.

A further object of the present invention is to provide a data bus in which a clock period is independent of bus length.

A bus system is described that has a topology that minimizes clock-data skew. The bus system includes a data bus, a clockline, and means for sending a data signal to the data bus. The clockline has two segments, each segment extending the entire length of the data bus. The segments are joined by a turnaround at one end of the data bus. Devices in the bus system use one clockline segment as a receive clock and the other clockline segment as a transmit clock. Means are provided for sending a data signal onto the data bus such that the data signal will travel on the data bus in a constant phase relationship with respect to the clock signal The result of the bus topology is that a data signal sent onto the data bus contemporaneously travels in the same direction as the clock signal used to receive the data.

The bus system uses synchronization circuitry to send a data signal to the data bus such that the data signal will travel on the data bus in a constant phase relationship with respect to the clock signal. The synchronization circuitry synchronizes data with the transmit clock of the particular device. The synchronization circuitry includes a phase comparator, which generates a select signal by comparing the receive clock to the transmit clock. A multiplexer uses the select signal to select between delayed and undelayed versions of data, data which is aligned with the receive clock. The multiplexer output is coupled the input of a latch, the enable input of which is coupled to the transmit clock. The

latch thus outputs data synchronized with the transmit clock of the particular device.

Other objects, features, and advantages of the present invention will be apparent from the accompanying drawings and the detailed description that follows.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings in which like references indicate similar elements and in which:

Figure 1 is a block diagram of one prior art bus system.

Figure 2 is a block diagram of another prior art bus system.

Figure 3 is a block diagram of a clock distribution system.

Figure 4A shows examples of clock signal waveforms for a device located near the turnaround of the clockline.

Figure 4B shows examples of clock signal waveforms for a device located in the middle of the clockline.

Figure 4C shows examples of clock signal waveforms for a device located relatively far from the turnaround.

Figure 5 is a block diagram of synchronization circuitry.

Figure 6 is a schematic diagram of the synchronization circuitry.

Figure 7A is a timing diagram for synchronization circuitry located near the turnaround.

Figure 7B is a timing diagram for synchronization circuitry located near the middle of the clockline.

Figure 7C is a timing diagram for synchronization circuitry located relatively far from the turnaround.

Figure 8 is a block diagram of an alternative synchronization scheme.

DETAILED DESCRIPTION

Figure 3 illustrates in block diagram form one preferred synchronous bus system 100. As will be described in more detail below, bus system 100 reduces or eliminates clock-data skew. To do so, bus system 100 uses a clock distribution system together with synchronization circuitry within each device.

The clock distribution system includes a clockline having two segments. One segment extends from one end of the data bus to a turnaround point near the second end of the data bus. The other clock segment extends from the turnaround back to the second end of the data bus. This topology ensures that data signals coupled by a device onto the data bus contemporaneously travel in the same direction as the clock signal used by a second device to receive the data.

Synchronization circuitry of bus system 100 thus allows data to be transmitted substantially at the time the transmit clock arrives so that clock and data signals travel together. In other words, the synchronization circuitry sends a particular data signal to the data bus such that the data signal will travel on the data bus in a constant phase relationship with respect to the clock signal. This serves to minimize clock-data skew, which in turn helps to reduce or eliminate errors caused by clock-data skew.

High-speed synchronous bus system 100 includes a master device 102 and slave devices 104, 106, 108 and 110. Master device 102 is coupled to slave devices 104, 106, 108 and 110 via data bus 120. Master device 102 is preferably located near the turnaround in the clockline.

As used herein, the terms "master" and "slave" differ somewhat from their conventional meanings. Within bus system 100, a master is a device that can communicate both with other masters and with slaves, and is located near the turnaround in the clockline. In contrast, slaves can only communicate with masters and may be located anywhere along data bus 120.

For one embodiment, master 102 is a microprocessor. For another embodiment, master device 102 is a peripheral controller.

For one embodiment, slave devices 104, 106, 108, and 110 are high speed memories. For example, slave devices 104, 106, 108, and 110 can be DRAMs. For another embodiment, slave devices 104, 106, 108, and 110 are bus transceivers. For another embodiment, slave devices 104, 106, 108, and 110 are peripheral devices. For another embodiment, slave devices 104, 106, 108, and 110 function as input/output ("I/O") ports.

Synchronous bus system 100 may include many slave devices, even though only four are illustrated in Figure 3. Alternatively, synchronous communications system 100 may include multiple masters. In those embodiments including multiple masters, master devices should be located close together near the turnaround in the clock line to facilitate rapid communication.

Master device 102 initiates an exchange of data by broadcasting an access request packet. Each slave device of devices 104, 106, 108, and 110 decodes the access request packet and determines whether it is the selected slave device and the type of access requested. The selected slave device then responds appropriately, either reading or writing a packet of data in pipelined fashion.

Synchronous bus system 100 preferably utilizes a fixed latency protocol to exchange data over data bus 120. A fixed latency protocol requires that a fixed number of clock cycles occur between a request for data by master device 102 and the clocking in of the first byte of that data by master device 102, irrespective of which slave device transmits the data. A fixed latency protocol also requires control information transmitted use fixed latency.

Data bus 120 provides a high-speed bidirectional direct interconnection between master device 102 and slave devices 104, 106, 108, and 110. Data bus 120 preferably operates at approximately 250 megahertz ("MHZ") with dual-edge transfer. In other words, transfers may occur approximately every 2 nanoseconds. The end-to-end signal propagation delay of data bus 120 is significant as compared to the clock period. In fact, for one embodiment of synchronous communications system 100, the end-to-end propagation delay of data bus 120 is approximately half that of the clock period, which is approximately 4 nanoseconds. This data signal propagation delay might introduce unacceptable clock-data skew in some prior synchronous systems.

Devices coupled to data bus 120 must include input circuitry having very low latency to receive data and receive clock signals. For example, a phase locked loop, a delay locked loop or clock compensation circuitry would all provide acceptably low latency.

Clock distribution system 130 aids in eliminating clock-data skew by causing clock and data signals to travel in the same direction. Clock distribution system 130 includes clock 132 and clockline 134. Clock 132 is external to and independent of devices 102, 104, 106, 108, and 110. Because clock generation is independent, bus system 100

accommodates multiple masters. Clock 132 is coupled to an end of clockline 134 so that the clock signal travels in only one direction, from clock 132 toward the opposite end of clockline 134. Clockline 134 carries the clock signal to all devices within bus system 100. Clockline 134 is long, nearly twice the length of data bus 120, and doubles back, or turns around, near one end of data bus 120. Thus, clockline 134 may be thought of as two clockline segments. Segment 136 extends from one end of data bus 120 to turnaround point 137, which is located at the other end of data bus 120. The other segment, segment 138, extends from turnaround point 137 back to the opposite end of data bus 120.

The propagation delay of each clockline segment 136 and 138 is substantially equal to the propagation delay of data bus 120, in the preferred embodiment.

The clock signal on segment 136 travels from clock 132 toward master device 102. For this reason, the clock signal on segment 136 is named CLOCKTOMASTER. CLOCKTOMASTER travels in the same direction as data signals sent by slave devices 104, 106, 108, and 110 to master device 102 via data bus 120. Transmit clock inputs of slave devices 104, 106, 108 and 110 are coupled to CLOCKTOMASTER. In Figure 3 this is shown by connection of slave device transmit clock inputs $TCLK_1$, $TCLK_2$, $TCLK_3$ to segment 136. Master device 102 uses the clock signal on segment 136 to receive data signals on data bus 120. Thus, the receive clock input, RCLK0, of master device 102 is coupled to segment 136.

Turnaround 137 causes the clock signal on segment 138 to change direction and travel toward the opposite end of the data bus. This is the same direction that data signals travel from master device 102

to slave devices 104, 106, 108, and 110 travel. For this reason master device 102 uses this signal, called CLOCKFROMMASTER, as its transmit clock, TCLK0. In a symmetrical fashion, slave devices 104, 106, 108, and 110 use CLOCKFROMMASTER as receive clock inputs. Data signals from master device travel to the slave devices in the same direction as the active CLOCKFROMMASTER signal on segment 138.

Having clock and data signals travel in the same direction is not sufficient to eliminate clock-data skew. The length of clockline 134 is such that active clock pulses do not reach each device 102, 104, 106, 108, and 110 simultaneously. Therefore each device 102, 104, 106, 108 and 110 must couple data signals onto data bus 120 just at the moment its active transmit clock travels past. This is analogous to surfing, in which the surfer watches and anticipates the crest of the wave to catch it and travel with it. The synchronization dilemma faced by devices 102, 104, 106, 108, and 110 is, however, more complicated than surfing because each device receives data with a receive clock and transmits data with a separate transmit clock.

Within clock distribution system 130 the transmit clock and receive clock always have the same frequency because only one clock source is used. Given the position of a device relative to turnaround 137, however, the phase between CLOCKFROMMASTER and CLOCKTOMASTER varies. Figures 4A, 4B, and 4C illustrate this difference in phase between CLOCKFROMMASTER and CLOCKTOMASTER for an embodiment of bus system 100 in which the propagation delay of data bus 120 is approximately equal to one clock period. The exact amount of phase shift, of course, varies as clock period and the data bus length vary.

Figure 4A illustrates the timing of clock signals for slave device 104, which is located very near turnaround 137. At this location, the phase difference between CLOCKFROMMASTER/$RCLK_1$ 160 and CLOCKTOMASTER/$TCLK_2$ 16 is nearly 0°.

Figure 4B illustrates the timing of receive clock $RCLK_2$ 160 and TCLK2 162 for slave device 106, which is located approximately half the length of data bus 120 away from turnaround 137. At this location, the phase difference between CLOCKFROMMASTER/$RCLK_2$ 160 and CLOCKTOMASTER/$TCLK_2$ 162 is approximately 180°.

Figure 4C illustrates the timing of signals for slave device 110. Far from turnaround 137 the phase difference between CLOCKFROMMASTER/$RCLK_3$ 160 and CLOCKTOMASTER/$TCLK_3$ is approximately 360°.

The phase difference experienced by each device within bus system 100 presents a challenge to utilization of identical devices within bus system 100. Satisfying this desire requires identical circuitry that accounts for variable phase difference between device receive and transmit clocks.

Figure 5 illustrates in block diagram form synchronization circuitry 150, which compensates for variable phase difference. Synchronization circuitry 150 is included in each device 102, 104, 106, 108, and 110. Briefly described, synchronization circuitry 150 synchronizes with the transmit clock data signals aligned with a receive clock. Synchronization circuitry 150 thus ensures that data signals coupled by one device onto the data bus contemporaneously travel together with the clock signal used by another device to receive the data.

Synchronization circuitry 150 includes phase comparator 152, delay element 154, two to one (2:1) multiplexer 156, and latch 158.

Phase comparator 152 compares a receive clock input RCLK 160 to a transmit clock input TCLK 162 to determine the relative phase between the two signals. In slave devices 104, 106, 108, and 110, CLOCKFROMMASTER is coupled to input RCLK 160 and CLOCKTOMASTER is coupled to input TCLK 162.

The signal output from phase comparator 152, SKIP 164, represents the relative phase between the two inputs 160 and 162. SKIP 164 is low for slave devices near turnaround 137 and high for slave devices far from turnaround 137. At the center of data bus 120 the level of SKIP 164 is uncertain, but this does not matter, as will be explained later.

SKIP 164 selects which of the two inputs to multiplexer 156 will be output to latch 158. One input to multiplexer 156 is undelayed receive data 155. The second input to multiplexer 156 is a delayed version of receive data 155, DELAYED RECEIVED DATA 157. DELAYED RECEIVED DATA 157 is generated by delay element 154. For slave devices far from turnaround 137, no delay is needed and SKIP 164 selects UNDELAYED RECEIVED DATA 155. At the opposite end of system 100, near turnaround 137, SKIP 164 selects DELAYED RECEIVED DATA 157 to compensate for the short propagation delay for those devices.

Latch 158 captures the output of multiplexer 156 and synchronizes the data to TCLK 162.

Additional stages 163, which are synchronized to the device's transmit clock, may be inserted after latch 158 prior to coupling data onto the data bus 120.

Figure 6 is a schematic diagram of synchronization circuitry 150. For the sake of simplicity, synchronization circuitry for a single data bit is illustrated. Synchronization for an entire data word is achieved simply by using a number of delay elements 154, 2:1 multiplexers 156 and latches 158 in parallel. Only one phase comparator 152 is necessary per slave device.

Synchronization circuitry 150 differ slightly from that described with respect to Figure 5. This ensures that receive data is centered on the transition of the device's transmit clock. Put another way, synchronization circuitry 150 ensures that data coupled onto the bus by a first device will be centered around the transition of a second device's receive clock. This is done by synchronizing data to an advanced version of TCLK 162, TCLK+90° 166. TCLK+90° 166 is generated from TCLK 162 using a phase locked loop, which is also included in each device 102, 104, 106, 108, and 110. The phase locked loop also generates a complement to TCLK+90° 166, TCLK+90°B 167, where "B" stands for bar, or complement.

Within synchronization circuitry 150, phase comparator 152 is comprised of two edge-triggered D flip-flops, 168 and 170. D flip-flop 168 samples TCLK 162 on the falling edge of RCLKD 161. RCLKD 161 is a slightly delayed version of RCLK 160. This slight delay biases the timing of D flip-flop 168 to ensure that the its output is low for devices near turnaround 137, i.e., when CLOCKTOMASTER and CLOCKFROMMASTER are in phase.

The output 180 of D flip-flop 168 is high for devices far from turnaround 137 and low for devices near turnaround 137. Output 180 is uncertain, and may even be meta-stable, for devices near the middle of data bus 120. D flip-flop 170 samples output 180, guaranteeing that SKIP 164 settles properly. D flip-flop 170 samples output 180 using a signal that indicates the start of a packet, PKTSTART 182. Each slave device generates its own PKTSTART 182 when the slave determines that master device 102 has requested access to that slave. There is sufficient time between the falling edge of PKTSTART 182 and when SKIP 164 is used to allow SKIP 164 to settle properly. As will be discussed later, at the center of data bus 120 it does not matter whether SKIP 164 settles high or low because the timing at master device 102 will be acceptable in either case.

Within synchronization circuitry 150, latch 186 corresponds to delay element 154. Latch 184 captures data to be transmitted, RDATA 187, using RCLK 160 as an enable input. Latch 186 captures the output of latch 184, RDE 188, and delays it by half a clock cycle by using RCLKB 189. RCLKB 189 is the complement of RCLK 160.

As the phase difference between RCLK 160 and TCLK 162 approaches zero, synchronizing data clocked with RCLK 160 to TCLK 162 is difficult because both clock signals change state simultaneously. Latch 186 helps alleviate this problem by changing the clocking of data to RCLKB 189 from RCLK 160.

Inputs of multiplexer 156 are coupled to RDO 190 and RDE 188. SKIP 164 selects between the two multiplexer inputs.

Latches 200 and 202 correspond generally to latch 158. Two latches are used to transfer data between RCLK and TCLK domains while avoiding possible timing hazards.

The data signal received by master device 102 after propagation down bus 120 is denominated TDATA 204. TDATA 204 is a time delayed version of TDO 203. The amount of delay depends on delay caused by additional stages 163 and the signal propagation delay between master device 102 and each slave device.

Figures 7A, 7B, and 7B illustrate the operation of synchronization circuitry 150 at three different locations relative to turnaround 137. Regardless of the device transmitting data, data is centered on the transitions of the transmitting devices's transmit clock, e.g., CLOCKTOMASTER for slave devices 104, 106, 108 and 110. In other words, each slave 104, 106, 108, and 110 transmits data centered around transitions in the master's receive clock. Thus, master 102 always clocks in valid date.

Certain notations and conventions are used in Figures 7A, 7B, and 7C. The synchronization circuitry signals in these three devices are differentiated from one other by numeric subscripts. For example, SKIP 164 in slave device 104 is referred to as $SKIP_1$ and in slave device 108 as $SKIP_3$. The signals $RCLKD_1$, $RCLKD_2$, and $RCLKD_3$ are not represented by separate waveforms. The falling edges of these signals signals are represented by dashed lines on the waveforms of $RCLK_1$, $RCLK_2$, and $RCLK_3$. The waveforms for RDE 188, RDO 190, TDE 201, TDO 203 , and TDATA 204 indicate only when these signals are valid or invalid and not their values. Periods when these signals are invalid are

indicated by multiple "X"s. Typically, a signal is invalid while one of the signals from which it is generated is changing state.

Figure 7A illustrates timing for slave device 104, which is near turnaround 137. $TCLK_1$ 162 is low by the time $RCLKD_1$ 161 falls, thus $SKIP_1$ 164 is low. Multiplexer 156 responds to $SKIP_1$ 164 by coupling $RDO_1$ 190 to latch 200. After converting the data from the receive clock domain to the transmit clock domain, latch 202 outputs $TDO_1$. Because there is virtually no signal propagation delay between slave device 104 and master device 102, the waveforms for $TDO_1$ 203 and $TDATA_1$ 204 are the same. As can be seen, $TDATA_1$ 204 is always centered on the $RCLK_0$ 162 transition. This is indicated for one instance by vertical line 212, which is aligned with a transition of $RCLK_0$ 162 and intersects $TDATA_1$ 204.

Before discussing the timing near the middle of data bus 120, consider the easier case of timing far from turnaround 137. This case is illustrated in Figure 7C. At this end of data bus 120, $TCLK_3$ 162 is still high when $RCLKD_3$ 161 falls, therefore $SKIP_3$ 164 is high. Multiplexer 156 responds to $SKIP_3$ 164 by coupling $RDE_3$ 188 to latch 200. After converting the data from the receive clock domain to the transmit clock domain, latch 202 outputs $TDO_3$ 203. $TDATA_3$ 204 is always centered on the $RCLK_0$ 162 transition. This is indicated for one instance by vertical line 212, which is aligned with a transition of $RCLK_0$ 162 and intersects $TDATA_3$ 204.

Figure 7B illustrates the timing for slave device 106, which is near the middle of data bus 120 . When $RCLKD_2$ 161 falls, $TCLK_2$ 162 may be high or low, thus $SKIP_2$ 164 may be high or low. This is shown in Figure 7B by two lines for $SKIP_2$ 164, one high and one low. As a result,

multiplexer 156 may output to latch 200 either $RDE_2$ 188 or $RDO_2$ 190. The output of latch 200, $TDE_2$ 201, is enabled to follow its input while TCLK+90° $_2$ 166 is high. $TDE_2$ 201 is uncertain for a short period after the rising edge of TCLK+90° $_2$ 166. $TDE_2$ 201 may remain uncertain for a bit longer because one of its possible inputs, $RDO_2$ 190, is uncertain for a bit after latch 200 opens. $TDE_2$ 201, however, settles before TCLK+90°$B_2$ 167 goes high, regardless of which signal is selected by $SKIP_2$ 164. As a result, the output of latch 202, $TDO_2$ 203, is uncertain only for a short period after the rising edge of TCLK+90°$B_2$ 167. $TDO_2$ 203 is eventually coupled to data bus 120 and reaches master device 102 as $TDATA_2$ 204 after some propagation delay. $TDATA_2$ 204 is always centered on the $RCLK_0$ 162 transition. This is indicated for one instance by vertical line 212, which is aligned with a transition of $RCLK_0$ 162 and intersects $TDATA_3$ 204.

Figures 7A, 7B, and 7C together thus illustrate that bus system 100 reduces clock-data skew by having clock and data signals travel together and arrive together at master device 102.

Bus system 100 also accommodates fixed latency protocols because data always reaches master device 102 at the same time regardless of the slave device transmitting the data. In some prior bus systems the variable signal propagation delay from slave to master would prevent the use of a fixed latency protocol.

The reason why variable signal propagation delay poses a challenge to a fixed latency protocols can be better understood with respect to the following Equation 2:

(2) Latency = 2*(master-to-slave signal propagation delay)
+ Slave access delay

Of the two terms in Equation 2, within bus system 100, only signal propagation delay is variable. The access delay is the same for all slave devices, assuming all devices are the same. In contrast, signal propagation delay in bus system 100 can vary depending upon the location of the device relative to the turnaround and the length of the clockline. Consequentially, latency could vary by twice the master-to-slave propagation delay if synchronization circuitry 150 were absent.

Figures 7A, 7B, and 7C illustrate that synchronization circuitry 150 helps to ensure that the first byte of data arrives at master device 102 on the same rising edge of $RCLK_0$ 162. The first byte of data to arrive at master device 102 is denominated "A" of TDATA 204. The clock pulse of $RCLK_0$ 162 on which byte A should be valid is denominated "X". As can be seen in Figure 7, vertical line 212 is aligned with the rising edge of pulse X and intersects valid byte A data of $TDATA_1$, $TDATA_2$, and $TDATA_3$.

Figure 8 illustrates in block diagram form an alternative synchronization system 200. System 200 is suited for designs in which the number of bits per data word that must be synchronized is large. A single instance of synchronization circuitry 150 is used to to realign multiple bits by coupling TLOAD 202 to synchronization circuitry 150, rather than RDATA 187. Synchronization circuitry 150 generates control signal 206, which needed to translate data from the receive clock domain to the transmit clock domain. Control signal 206 is a pulsed signal that occurs two clock cycles before RLOAD 204 goes active. Control signal 206 is held active for one clock cycle. Control signal 206 is held inactive after that one cycle until the next data word is to be synchronized.

Operation of synchronization is controlled, in part, by TLOAD 202 and RLOAD 204, which are both receive clock domain signals. TLOAD 202 is active on its positive going edge, which occurs two clock cycles before RLOAD 204 becomes active. This allows system 200 to account for the propagation delay through synchronization circuitry 150. RLOAD 204 is brought and held active high for the entire first clock cycle of every data word being synchronized. RLOAD 204 is held inactive until the next data word is received.

Thus, a bus system has been described that minimizes clock-data skew. The bus system includes a data bus, a clockline and synchronization circuitry. The clockline has two clockline segments. Each clockline segment extends the entire length of the data bus and is joined by a turnaround at one end of the data bus to the other clockline segment. The clockline ensures that clock and data signals travel in the same direction. Synchronization circuitry helps to ensure that data signals are placed onto the data bus such that data signals contemporaneously travel together with the clock signal used by a receiving device to receive the data.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. A synchronous bus system for minimizing clock-data skew, the bus system comprising:

a) a single clock source,

b) a data bus having a first end and a second end;

c) a clockline carrying a clock signal, the clockline having:

i) a first clockline segment extending from the first end of the data bus to a turnaround near the second end of the data bus; and

ii) a second clockline segment extending from the turnaround to the first end of the data bus.

d) means for sending a data signal to the data bus such that the data signal will travel on the data bus in a constant phase relationship with respect to the clock signal.

2. The synchronous bus system of claim 2, wherein the means for sending a data signal onto the data bus at a particular point in time comprises synchronization circuitry having transmit clock input coupled to a one of the first clockline segment and the second clockline segment.

3. A synchronous bus system for minimizing clock-data skew, the bus system comprising:

a) a single clock source,

b) a data bus having a first end and a second end;

c) a clockline carrying a clock signal, the clockline having:

i) a first clockline segment extending from the first end of the data bus to a turnaround near the second end of the data bus; and

ii) a second clockline segment extending from the turnaround to the first end of the data bus;

d) synchronization circuitry having a transmit clock input coupled to a one of the first clockline segment and the second clockline segment wherein the synchronization circuitry synchronizes a data signal with the transmit clock input and sends the data signal to the data bus.

4. The synchronous bus system of claim 3, wherein the synchronization circuitry comprises:

a) a phase comparator for comparing a receive clock input to the transmit clock input to generate a select signal;

b) a first delay element having a first data input, a first data output, and a first enable input, the first data input being coupled to the first data signal and the first enable input being coupled to the receive clock input;

c) a second delay element having a second data input, a second data output, and a second enable input, the second data input being coupled to the first data output and the second enable input being coupled to a complement of the receive clock input;

d) a multiplexer having a mux output, a first mux input coupled to the first data output and a second mux input coupled to the second data output, the multiplexer selecting between the first mux input and the second mux input in response to the select signal;

e) a first latch having a fourth data input, a fourth data output and a fourth enable input, the fourth data input being coupled to the mux

output, the fourth enable input being coupled to an advanced phase version of the transmit clock input; and

f) a second latch having a fifth data input, a fifth data output and a fifth enable input, the fifth data input being coupled to the fourth output, the fifth enable input being coupled to a complement of the advanced phase version of the transmit clock input, and the fifth data output outputting a second data signal.

5. The synchronous bus system of claim 4 wherein the first delay element comprises a latch and the second delay element comprises a latch.

6. The synchronous bus system of claim 4 further comprising a clock coupled to an end of a one of the first segment and the second clockline segment.

7. The synchronous bus system of claim 4 further comprising a multiplicity of devices coupled to the data bus, each of the devices including synchronization circuitry.

8. A synchronous bus system for minimizing clock-data skew, the bus system comprising:

a) a data bus having a first end and a second end;

b) a clockline carrying a clock signal, the clockline having:

i) a first clockline segment extending from the first end of the data bus to a turnaround near the second end of the data bus;

ii) a second clockline segment extending from the turnaround to the first end of the data bus; and

c) a first device coupled to the data bus for transmitting data to a second device, including synchronization circuitry, the synchronization circuitry synchronizing a data signal and the clock signal on a transmit clockline segment, the second device having the transmit clockline segment, the transmit clockline segment being a selected one of the first and second clockline segments, the synchronization circuitry including:

i) a phase comparator for comparing a receive clock input to a transmit clock input to generate a select signal, the transmit clock input being the transmit clockline segment;

ii) a delay element coupled to the data signal and outputting a delayed data signal;

iii) a multiplexer for selecting between the data signal and the delayed data signal in response to the select signal, the multiplexer having a mux output; and

iv) a latch having an input coupled to the mux output, the latch having an enable input coupled to the transmit clock input, and an output outputting a second data signal aligned with the transmit clock input.

9. The synchronous bus system of claim 8 wherein the delay element comprises a latch.

10. The synchronous bus system of claim 8 wherein the phase comparator comprises a latch.

11. The synchronous bus system of claim 8 further comprising a clock coupled to an end of a one of the first and second clockline segments.

12. A synchronous bus system for minimizing clock-data skew, the bus system comprising:

a) a data bus having a first end and a second end;

b) a clockline carrying a clock signal, the clockline having:

i) a first clockline segment extending from the first end of the data bus to a turnaround near the second end of the data bus;

ii) a second clockline segment extending from the turnaround to the first end of the data bus; and

c) synchronization circuitry for synchronizing a multiplicity of data signals with the clock signal on a transmit clockline segment and for sending the multiplicity of data signals to the data bus, the transmit clockline segment being a selected one of the first and second clockline segments, the synchronization circuitry including:

i) a phase comparator for comparing a receive clock input to a transmit clock input to generate a select signal, the transmit clock input being the transmit clockline segment;

ii) a delay element coupled to a first control signal and outputting a delayed first control signal;

iii) a multiplexer for selecting between the first control signal and the delayed first control in response to the select signal, the multiplexer having a mux output;

iv) a first latch having an input coupled to the mux output, the latch having an enable input coupled to the transmit clock input, and

an output outputting a second control signal aligned with the transmit clock input;

v) a second latch having a multiplicity of inputs coupled to the multiplicity of data signal and having an enable input coupled to a third control signal, and having a multiplicity of second latch outputs;

vi) a third latch having a multiplicity of inputs coupled to the multiplicity of second latch outputs, an enable coupled to second control signal and a multiplicity of third latch outputs coupled to data bus.

13. The synchronous bus system of claim 12 wherein the delay element comprises a latch.

14. The synchronous bus system of claim 12 wherein the phase comparator comprises a latch.

15. The synchronous bus system of claim 12 further comprising a clock coupled to an end of a one of the first and second clockline segments.

16. A method for minimizing clock-data skew in a synchronous bus system having devices coupled to a data bus and a clockline, the data bus having a first end and a second end, the clockline having a first segment extending from the first end of the data bus to a turnaround near the second end of the data bus and a second segment extending from the turnaround to the first end of the data bus, and a clock coupled to an end of a one of the first and second clockline segments, the method comprising the steps of:

a) transmitting a first clock signal on the clockline such that the first clock signal travel in a first direction on the first segment towards the turnaround and in a second direction on the second segment away from the turnaround;

b) sending a first data signal to data bus such that the data signal will travel on the data bus in a constant phase relationship with respect to the clock signal.

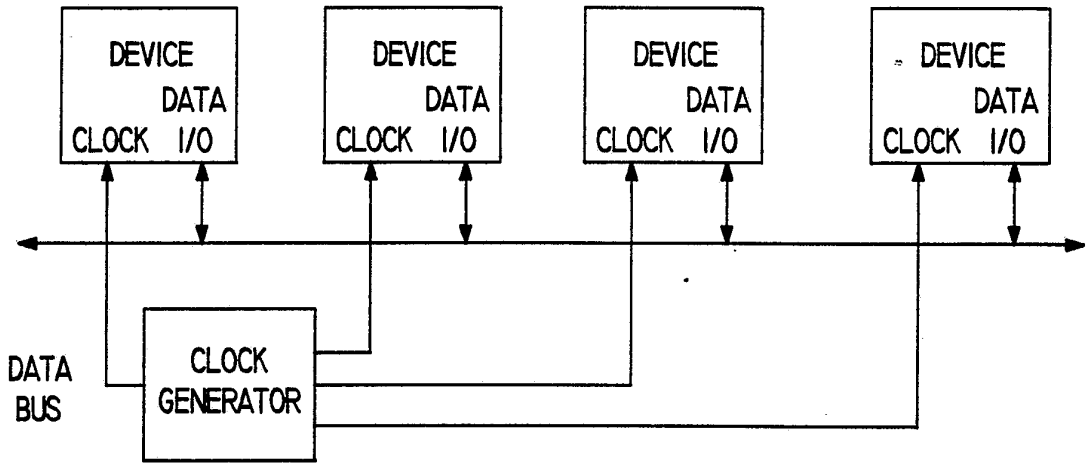



**FIG. 1**

(PRIOR ART)

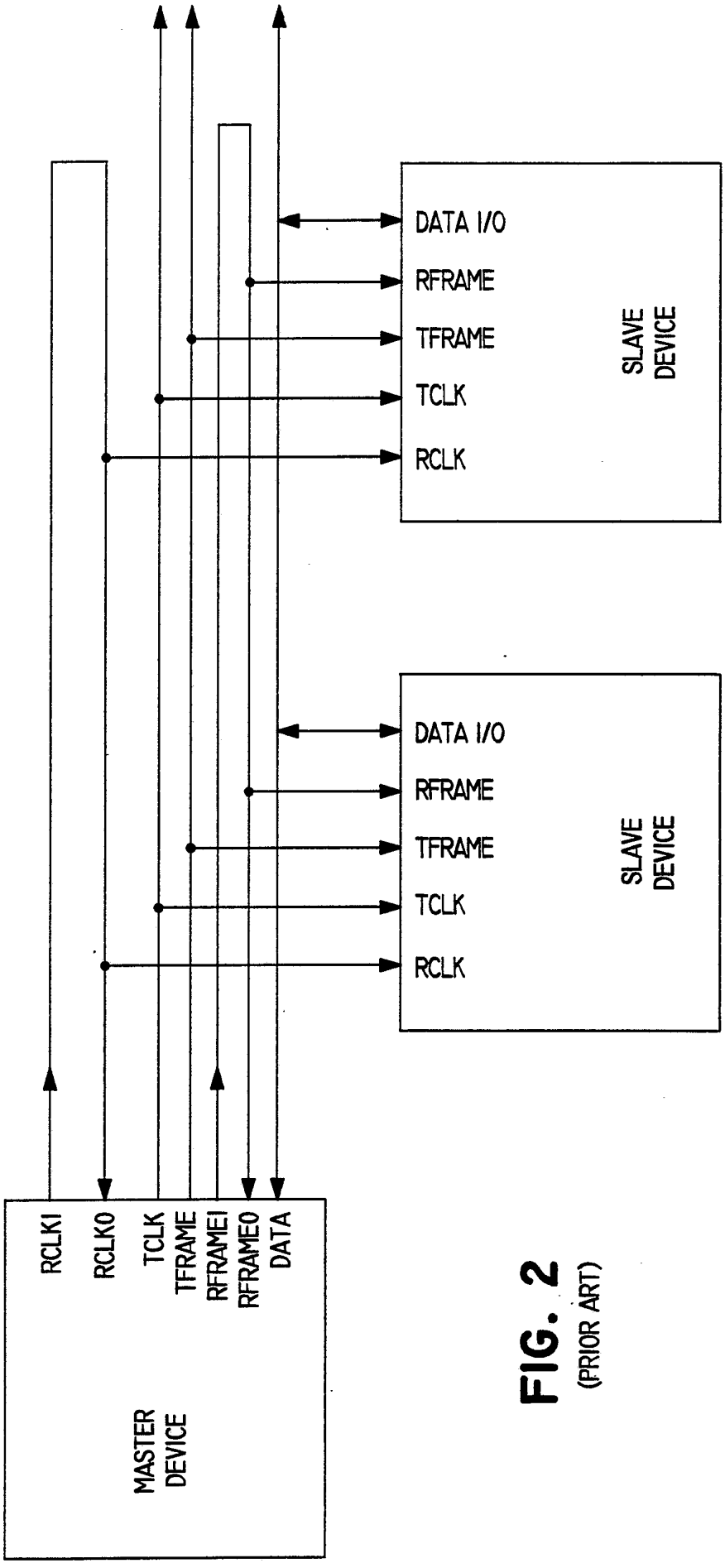



FIG. 2
(PRIOR ART)

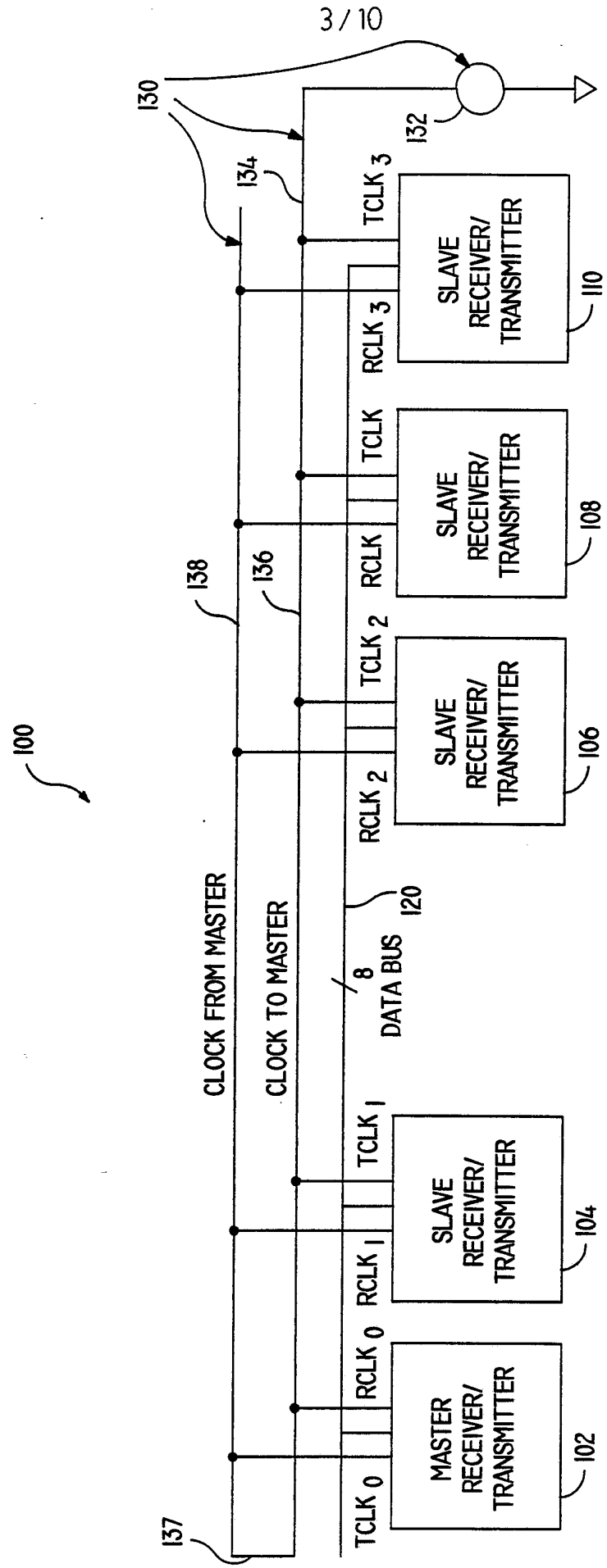

100
130
132
134
136
138
137
120
CLOCK FROM MASTER
CLOCK TO MASTER
8
DATA BUS
TCLK 3
RCLK 3
TCLK
RCLK
TCLK 2
RCLK 2
TCLK 1
RCLK 1
RCLK 0
TCLK 0
SLAVE RECEIVER/ TRANSMITTER
110
SLAVE RECEIVER/ TRANSMITTER
108
SLAVE RECEIVER/ TRANSMITTER
106
SLAVE RECEIVER/ TRANSMITTER
104
MASTER RECEIVER/ TRANSMITTER
102

FIG. 3

FIG. 4A

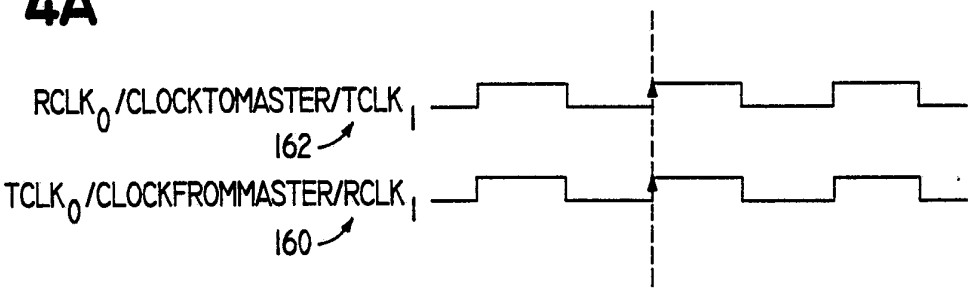



FIG. 4B

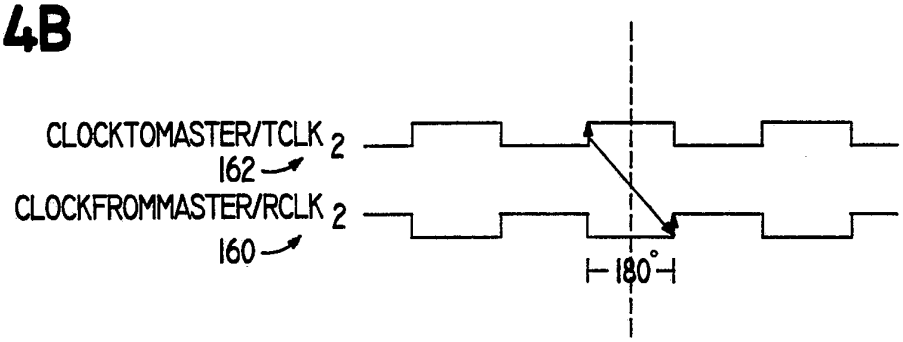
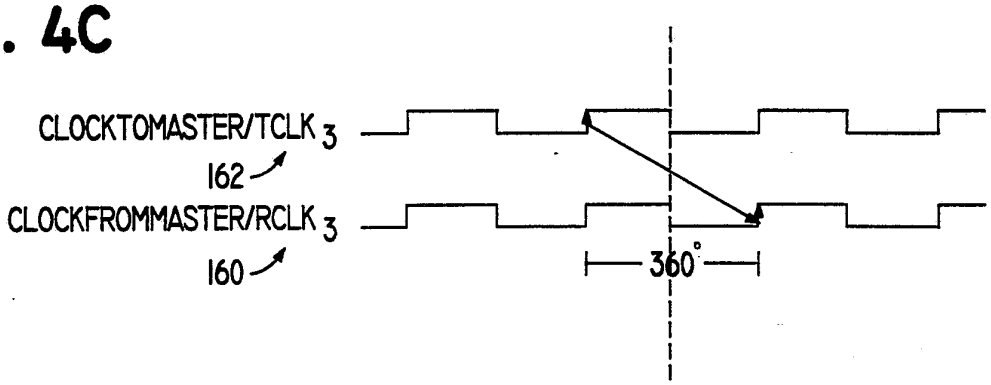



FIG. 4C



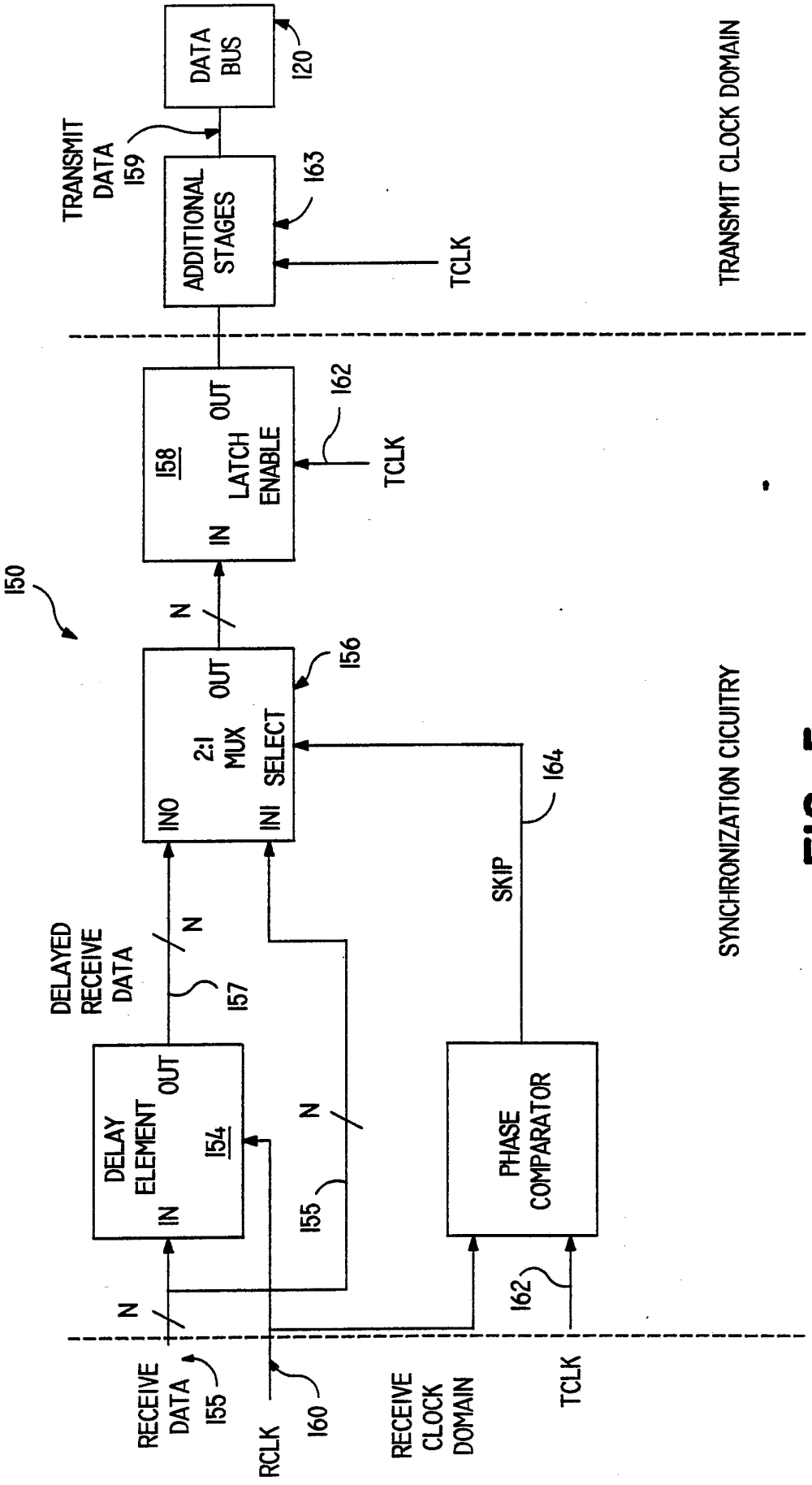

DATA BUS
120
TRANSMIT DATA 159
ADDITIONAL STAGES
163
TCLK
TRANSMIT CLOCK DOMAIN
158
LATCH ENABLE
IN
OUT
162
TCLK
150
N
2:1 MUX
IN0
IN1
SELECT
OUT
156
SKIP
164
DELAYED RECEIVE DATA
N
157
DELAY ELEMENT
IN
154
OUT
N
155
PHASE COMPARATOR
SYNCHRONIZATION CICUITRY
N
RECEIVE DATA 155
RCLK
160
RECEIVE CLOCK DOMAIN
162
TCLK

FIG. 5

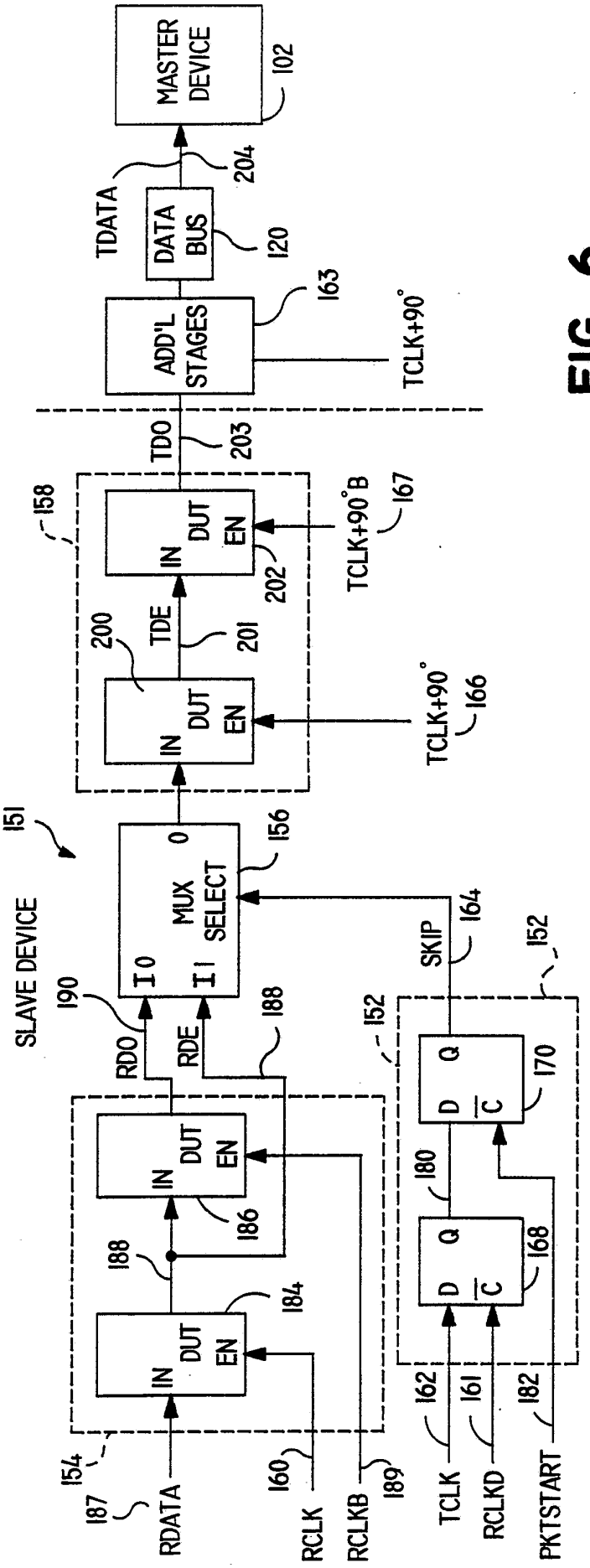

MASTER DEVICE
102
TDATA
204
DATA BUS
120
ADD'L STAGES
163
TCLK+90°
TDO
203
158
IN DUT EN
202
TCLK+90°B
167
200
TDE
201
IN DUT EN
TCLK+90°
166
151
SLAVE DEVICE
MUX SELECT
156
I0
I1
SKIP
164
152
190
RDO
RDE
188
IN DUT EN
186
184
D Q C
170
180
168
162
161
182
154
187
RDATA
160
RCLK
RCLKB
189
TCLK
RCLKD
PKTSTART

FIG. 6

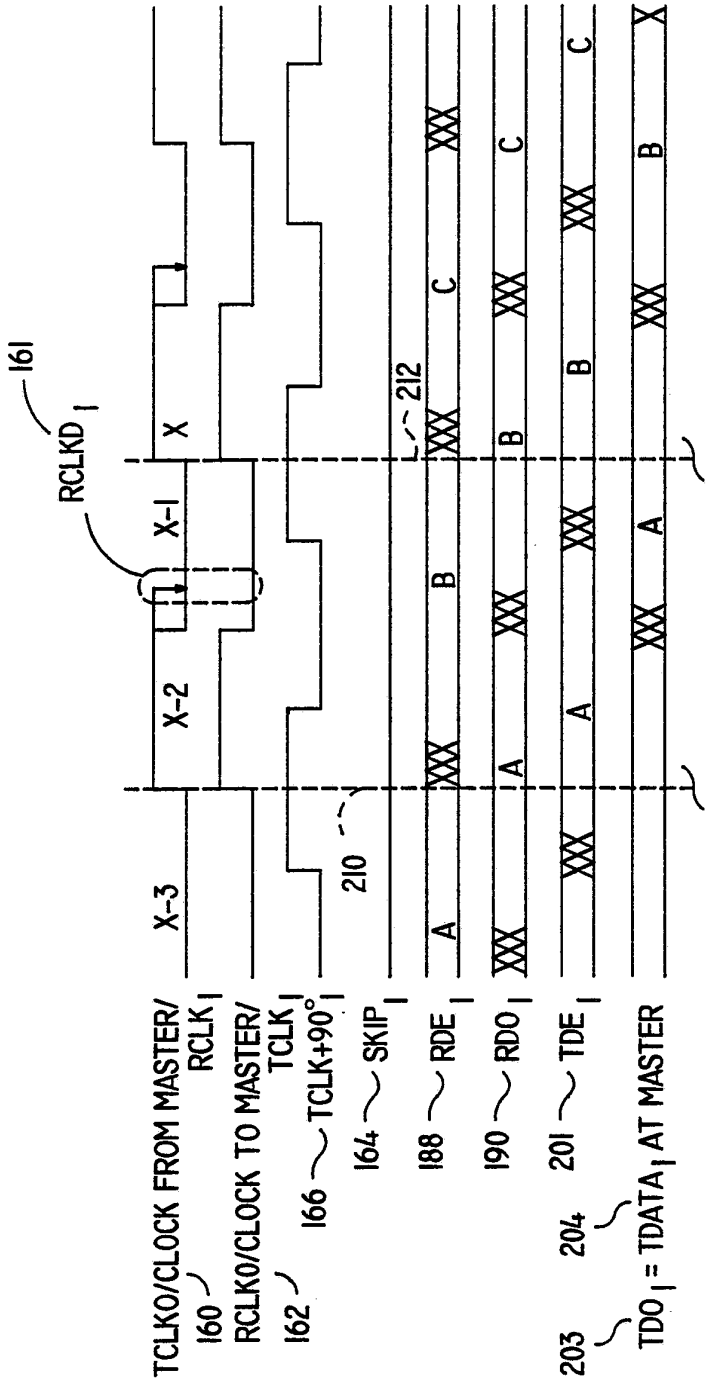

161
RCLKD
X-3
X-2
X-1
X
210
212
TCLKO/CLOCK FROM MASTER/ RCLK
160
RCLKO/CLOCK TO MASTER/ TCLK
162
166 TCLK+90°
164 SKIP
188 RDE
190 RDO
201 TDE
204
203 TDO = TDATA AT MASTER
A
B
C
XX
X

FIG. 7A

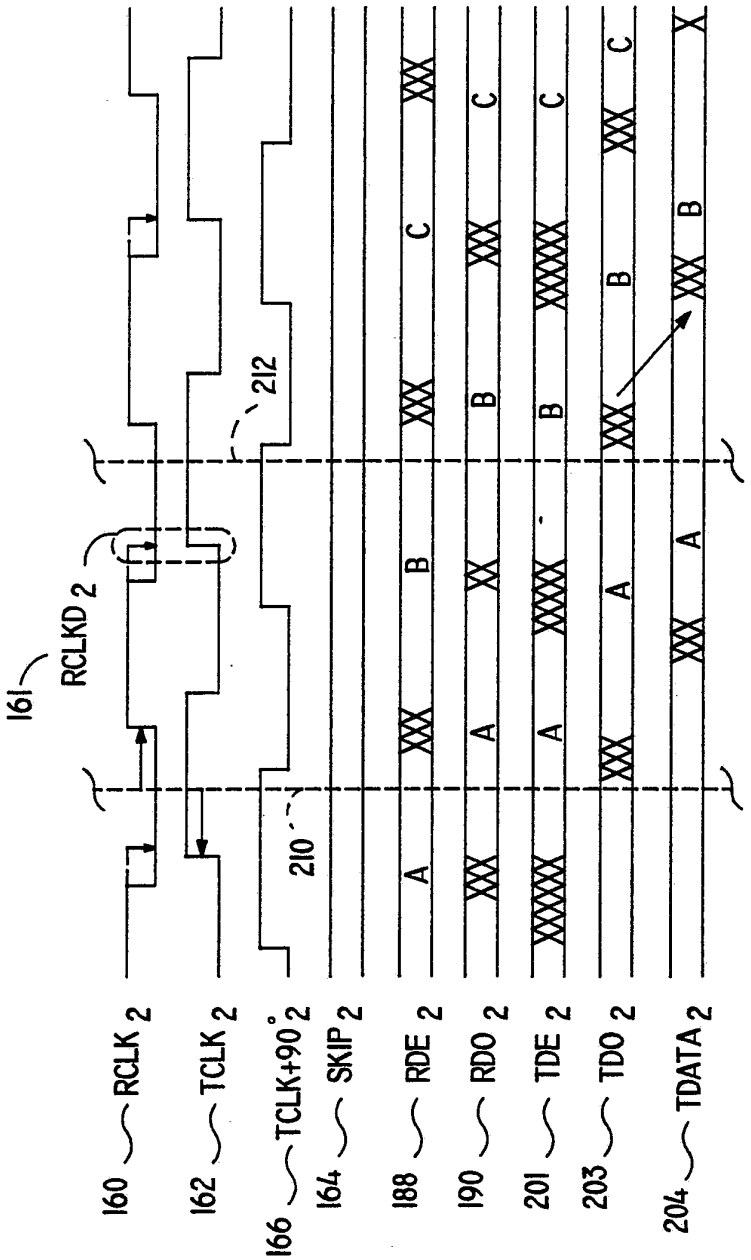

161
RCLKD 2
212
210
160 RCLK 2
162 TCLK 2
166 TCLK+90° 2
164 SKIP 2
188 RDE 2
190 RDO 2
201 TDE 2
203 TDO 2
204 TDATA 2
A
B
C

FIG. 7B

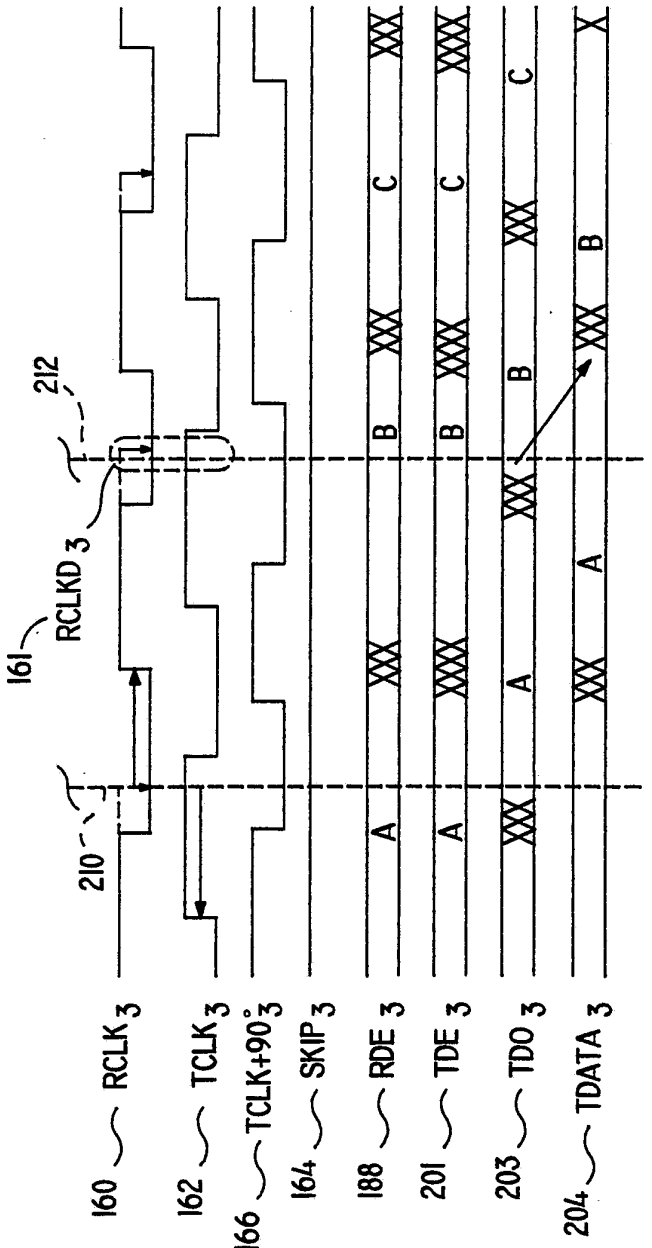

160 RCLK 3
162 TCLK 3
166 TCLK+90° 3
164 SKIP 3
188 RDE 3
201 TDE 3
203 TDO 3
204 TDATA 3
161
RCLKD 3
210
212
A
B
C
X

FIG. 7C

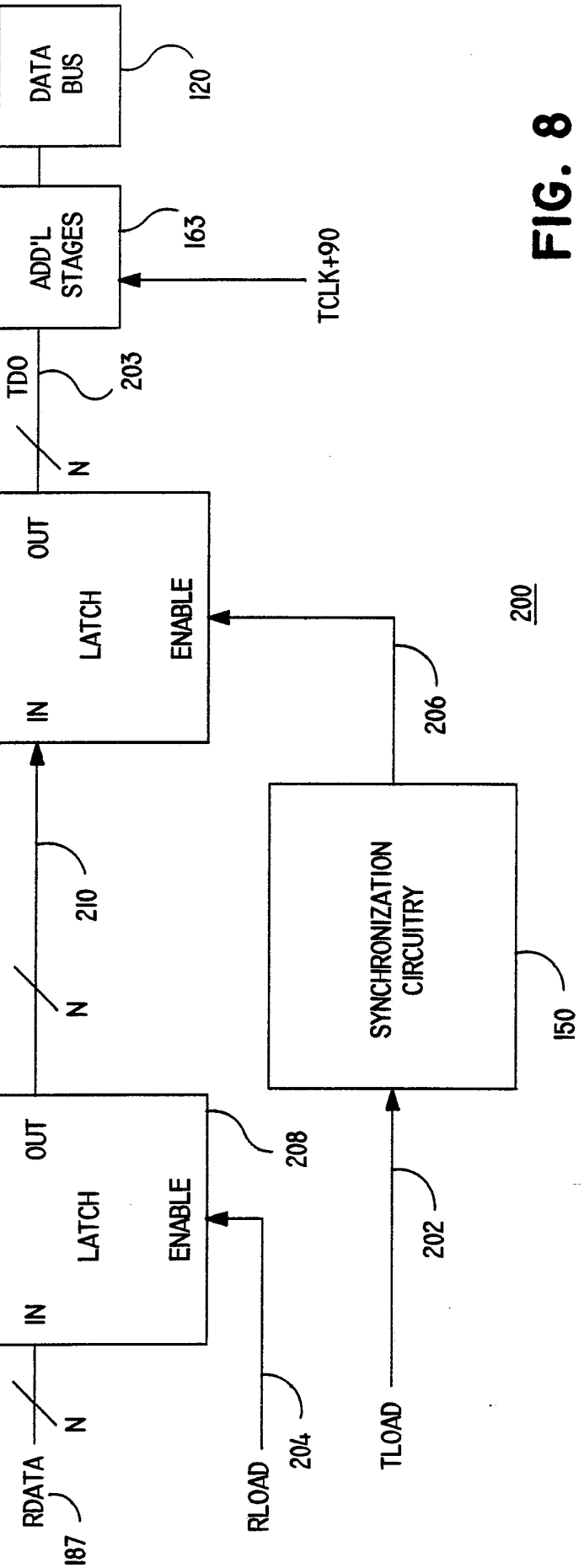

DATA BUS
120
ADD'L STAGES
163
TCLK+90
TDO
203
N
OUT
LATCH
ENABLE
IN
206
200
210
N
SYNCHRONIZATION CIRCUITRY
150
208
202
RDATA
187
N
RLOAD
204
TLOAD

FIG. 8

# INTERNATIONAL SEARCH REPORT

International Application No PCT/US 93/01726

**I. CLASSIFICATION OF SUBJECT MATTER** (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 G06F13/42

**II. FIELDS SEARCHED**

Minimum Documentation Searched[7]

| Classification System | Classification Symbols |
|---|---|
| Int.Cl. 5 | G06F |

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

**III. DOCUMENTS CONSIDERED TO BE RELEVANT**[9]

| Category ° | Citation of Document,[11] with indication, where appropriate, of the relevant passages[12] | Relevant to Claim No.[13] |
|---|---|---|
| X | EP,A,0 347 557 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 27 December 1989 | 1-3,16 |
| A | see column 4, line 51 - column 5, line 4<br>see column 5, line 12 - column 7, line 17<br>see column 7, line 49 - column 8, line 51<br>see claim 1; figure 3 | 4-15 |
| | --- | |
| X | WO,A,8 400 219 (ELXSI) 19 January 1984 | 1-3,16 |
| A | see page 3, line 5 - line 18<br>see page 7, line 6 - line 10<br>see page 8, line 4 - line 10<br>see page 9, line 17 - page 10, line 20<br>see figures 1,2A | 4-15 |
| | --- | |
| | -/-- | |

° Special categories of cited documents :[10]

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

**IV. CERTIFICATION**

| Date of the Actual Completion of the International Search | Date of Mailing of this International Search Report |
|---|---|
| 09 JUNE 1993 | 30. 06. 93 |
| **International Searching Authority** | **Signature of Authorized Officer** |
| EUROPEAN PATENT OFFICE | NGUYEN XUAN HIEP C. |

Form PCT/ISA/210 (second sheet) (January 1985)

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

| Category ° | Citation of Document, with indication, where appropriate, of the relevant passages | Relevant to Claim No. |
|---|---|---|
| X | EP,A,0 175 564 (INTERNATIONAL COMPUTERS LIMITED)<br>26 March 1986<br>see page 1, line 15 - page 2, line 19<br>see page 10, line 6 - page 11, line 11<br>see figure 1<br>----- | 1-16 |

# ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO.

US 9301726
SA 71125

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on
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| Patent document cited in search report | Publication date | Patent family member(s) | | Publication date |
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| | | AU-A- | 4766285 | 27-03-86 |
| | | DE-A- | 3584751 | 09-01-92 |
| | | US-A- | 4691294 | 01-09-87 |