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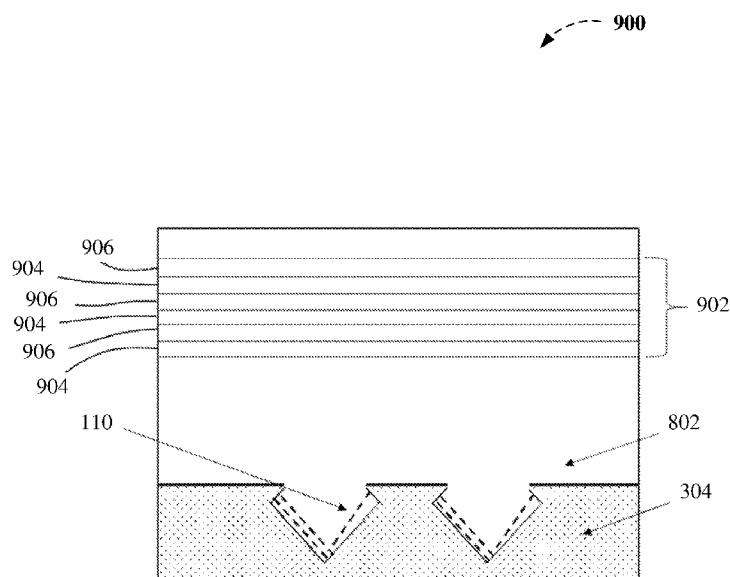


FIG. 9

(57) Abstract: Group III-V material metamorphic buffer template substrates are provided herein. Substrates as described herein can comprise an exact oriented (100) silicon (Si) substrate comprising diamond-shaped trenches, which facilitates defect trapping at the group III-V material, silicon interface, wherein diamond-shaped trenches are bounded at least in part by four (111) Si surfaces in the exact oriented (100) Si substrate, and in which group III-V semiconductor materials can be deposited. In addition, process are describe for forming diamond-shaped trenches, depositing group III-V semiconductor materials in the diamond-shaped trenches, and fabricating group III-V semiconductor thin films therewith.



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METHODS FOR GROWING III-V COMPOUND SEMICONDUCTORS FROM DIAMOND-SHAPED TRENCHES ON SILICON AND ASSOCIATED DEVICES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. Provisional Patent Application Serial No. 62/497,631, filed on November 28, 2016, and entitled GROWING III-V COMPOUND SEMICONDUCTORS FROM DIAMOND-SHAPED TRENCHES ON SILICON, the entirety of which is hereby incorporated by reference.

TECHNICAL FIELD

[0002] The subject disclosure is directed to group III-V semiconductors on silicon, and is more particularly related to epitaxial growth of high crystalline quality III-V nanoscale crystals and thin film buffer templates on (100) oriented Si substrates.

BACKGROUND

[0003] Heterogeneous integration of III-V semiconductors on silicon (Si) substrates has the potential to advance high speed electronics and achieve large-scale integrated silicon photonics for data processing and communications. Conventionally, wafer bonding and epitaxial growth are primarily used for III-V compound semiconductor integration on Si. While wafer bonding is the most mature technology and has demonstrated the most advanced integrated devices and photonic circuits, direct epitaxial growth of III-V compound semiconductors on Si substrates would provide a monolithic approach to III-V compound semiconductor integration on Si that has the capacity to provide beneficial improvements that are desirable, long term.

[0004] For instance, conventional processes to obtain high quality III-V thin films on foreign Si substrates by heteroepitaxy face many fundamental roadblocks. As an example, the large crystal lattice mismatch between III-V materials and Si gives rise to a high dislocation density on the order of $10^9 - 10^{10}$ per square centimeters (cm^2). As another example, mismatch in thermal expansion coefficients results in residual stresses and macroscopic cracks in III-V thin films beyond a certain critical thickness. In addition, growth of polar III-V semiconductor materials on non-polar Si substrates leads to antiphase-domains (APDs), which is one type of planar defects.

[0005] As a further example, conventional blanket epitaxial growth of III-V thin films on blank Si wafers typically employs Si substrates with a 4–6° special offcut angle to attempt to suppress APDs. Additionally, III-V compound semiconductor films typically employ thick transitional buffer layers to achieve a desired lattice constant with an acceptable dislocation density suitable for device fabrication. In addition, compared to conventional blanket heteroepitaxy, Si substrate patterning can allow for effective strain relaxation and can provide additional defect trapping benefits. However, conventional techniques of Si substrate patterning and can rely on residual patterned dielectric on Si for defect trapping, which may be undesirable for particular III-V semiconductor material thin films and related devices.

[0006] The above-described deficiencies of conventional processes for growing III-V semiconductor material thin films are merely intended to provide an overview of some of the problems of conventional systems and methods, and are not intended to be exhaustive. Other problems with conventional systems and corresponding benefits of the various non-limiting embodiments described herein may become further apparent upon review of the various non-limiting embodiments of the following description.

SUMMARY

[0007] The following presents a simplified summary of the specification to provide a basic understanding of some aspects of the specification. This summary is not an extensive overview of the specification. It is intended to neither identify key or critical elements of the specification nor delineate any scope particular to any embodiments of the specification, or any scope of the claims. Its sole purpose is to present some concepts of the specification in a simplified form as a prelude to the more detailed description that is presented later.

[0008] In various non-limiting embodiments, the disclosed subject matter provides group III-V compound semiconductors on diamond-shaped trenches on silicon (Si) (*e.g.*, an exact oriented (100) Si substrate), which can facilitate fabrication of exemplary group III-V material metamorphic buffer template substrates, as described herein.

[0009] Accordingly, non-limiting embodiments of the disclosed subject matter can comprise depositing group III-V semiconductor materials diamond-shaped trenches in an exact oriented (100) Si substrate, and growing the group III-V semiconductor materials into a group III-V semiconductor material thin film on the exact oriented (100) Si substrate. In

addition, further non-limiting embodiments disclosed subject matter can comprise forming diamond-shaped trenches in the exact oriented (100) Si substrate and depositing group III-V semiconductor materials in the diamond-shaped trenches in an exact oriented (100) Si substrate.

[0010] In addition, further example implementations directed group III-V material metamorphic buffer template substrates can comprise an exact oriented (100) Si substrate comprising a set of diamond-shaped trenches, wherein a diamond-shaped trench of the set of diamond-shaped trenches is characterized by being bounded at least in part by four (111) Si surfaces in the exact oriented (100) Si substrate, and a first composition of group III-V semiconductor materials located in the set of diamond-shaped trenches, as further detailed herein.

[0011] These and other features of the disclosed subject matter are described in more detail below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The devices, components, systems, and methods of the disclosed subject matter are further described with reference to the accompanying drawings in which:

[0013] FIG. 1 depicts a schematic representation of aspect ratio trapping, illustrating growth of III-V crystals between patterned dielectric on V-groove patterned Si substrate;

[0014] FIG. 2 depicts another schematic representation of growth of III-V thin films over the patterned dielectric on V-groove patterned Si substrate;

[0015] FIG. 3 depicts an exemplary process for the formation of diamond-shaped Si trenches, according to non-limiting aspects disclosed herein;

[0016] FIG. 4 shows cross-sectional transmission electron microscope (TEM) images of exemplary GaAs crystals grown inside diamond-shaped trenches separated by SiO₂ sidewalls, in further non-limiting aspects;

[0017] FIG. 5 shows a tilted-view scanning electron microscope (SEM) image of an exemplary InGaAs alloy grown inside the diamond-shaped trenches separated by SiO₂ sidewalls, in other non-limiting aspects;

[0018] FIG. 6 depicts a tilted-view SEM image of an exemplary InP composition grown inside the diamond-shaped trenches separated by SiO₂ sidewalls, according to further non-limiting aspects;

[0019] FIG. 7 depicts another tilted-view SEM image of an exemplary InP composition grown inside the diamond-shaped trenches separated by SiO₂ sidewalls, in further non-limiting aspects;

[0020] FIG. 8 depicts an exemplary process for the formation of an exemplary III-V thin film from exemplary III-V crystals grown in the diamond-shaped trenches on Si, as further described herein;

[0021] FIG. 9 depicts an exemplary process for the formation of an exemplary superlattice over an exemplary III-V thin film, according to further non-limiting aspects.

[0022] FIG. 10 shows an atomic-force microscopy image of an exemplary GaAs metamorphic buffer template in accordance with exemplary processes described herein;

[0023] FIG. 11 depicts another exemplary process for the formation of an exemplary III-V thin film from exemplary III-V crystals grown in the diamond-shaped trenches on Si, as further described herein;

[0024] FIG. 12 illustrates an example non-limiting flow diagram of methods for performing aspects of embodiments of the disclosed subject matter; and

[0025] FIG. 13 illustrates another example non-limiting flow diagram of methods for performing aspects of embodiments of the disclosed subject matter.

DETAILED DESCRIPTION

Overview

[0026] As described above, direct epitaxial growth of III-V compound semiconductors on Si substrates can provide a monolithic approach to III-V compound semiconductor integration on Si that has the capacity to provide beneficial improvements that are desirable, long term. However, as further described above, while Si substrate patterning can allow for effective strain relaxation and can provide additional defect trapping benefits over conventional blanket heteroepitaxy techniques, conventional techniques of Si substrate patterning and can rely on residual patterned dielectric on Si for defect trapping, which may be undesirable or provide unsatisfactory results for particular III-V semiconductor material thin films and related devices.

[0027] For instance, in a patterned growth technology referred to as “aspect ratio trapping” technique (or epitaxial necking effect) III-V semiconductor materials are selectively grown in high aspect ratio holes or trenches formed by a patterned dielectric on Si, whereby

dislocations generated at the III-V/Si interface are guided to the dielectric sidewalls and thus terminate there, leaving a low-dislocation density region at the top of the trenches/holes where devices can be built, for example as described in reference to FIGS. 1-2, below.

[0028] Non-limiting examples are provided herein as an aid in understanding the inherent difficulties in producing defect free III-V compound semiconductor thin films by conventional processes, and not limitation. In a non-limiting example, FIG. 1 depicts a schematic representation 100 of aspect ratio trapping, illustrating growth of III-V crystals 102 between patterned dielectric 104 on V-groove patterned Si substrate 106. FIG. 1 depicts Si substrate 106 covered by a dielectric 104 layer, which can be patterned by a combination of vertical dry etching and subsequent anisotropic wet etching, which produces V-grooved Si with (111) surfaces 108 separated by dielectric 104 sidewalls. III-V crystals 102 can be deposited inside the trenches by metal-organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE). The growth of polar III- materials on Si (111) surfaces 108 suppresses the generation of antiphase-domains. Stacking faults 110 and threading dislocations 112 originated from the III-V/Si interface at Si (111) surfaces 108 are guided to the dielectric 104 sidewalls and terminate there. The upper region of the III-V crystals 102 can achieve a low defect density for device fabrication. However, increased planar defects (twins, stacking faults) originated from the III-V/dielectric 104 interface are often observed.

[0029] Accordingly, in another non-limiting example, FIG. 2 depicts another schematic representation 200 of growth of III-V thin films 202 over the patterned dielectric 104 on V-groove patterned Si substrate 106. The III-V materials are grown above the height of the dielectric 104 sidewalls and further extend laterally on top of the dielectric 104 until merging with those from neighboring trenches. In this approach, the existence of dielectric 104 patterns in the epitaxial lateral overgrowth in III-V thin films 202 typically results in hard-to-control asymmetries and irregularities of faceted growth regions, leading to higher coalescence defects and rough surface morphology in the resulting III-V thin films 202. As such, chemical mechanical polishing (CMP) is usually required to smoothen the surface for device fabrication.

[0030] In various non-limiting embodiments, the subject disclosure provides group III-V compound semiconductors on silicon (Si) by facilitating epitaxial growth of high crystalline quality III-V nanoscale crystals and thin film buffer templates on (100) oriented Si substrates. In a non-limiting aspect, exemplary buffer templates can serve as a “virtual substrate” that provides

the capability for device fabricators to engineer group III-V compound semiconductor substrates with designer-chosen surface lattice constants, thus allowing for the integration of a variety of group III-V compound semiconductor devices on readily available and industrial-standard Si, rather than specially manufactured, niche Si substrates.

[0031] While a brief overview has been described above in order to provide a basic understanding of some aspects of the specification, various non-limiting devices, systems, and methods are now described as a further aid in understanding the advantages and benefits of various embodiments of the disclosed subject matter. To that end, it can be understood that such descriptions are provided merely for illustration and not limitation.

III-V COMPOUND SEMICONDUCTORS FROM DIAMOND-SHAPED TRENCHES ON SILICON

[0032] Accordingly, in various embodiments, the subject disclosure describes employing diamond-shaped Si trenches instead of conventional Si V-grooves to grow III-V materials on Si substrates. In a non-limiting aspect, exemplary diamond-shaped pockets can be bounded at least in part by four Si (111) surfaces to facilitate providing better defect confinement than conventional V-grooves, which are typically bounded by only two Si (111) surfaces. In a further non-limiting aspect, selective area growth of nanometer scale III-V crystals inside the diamond-shaped Si trenches can be performed by MOCVD or MBE, and/or other suitable technologies, using pattern dielectric and/or other materials as a mask. Subsequently, dielectric sidewalls can be removed, and these pre-defined III-V crystals from two or more adjacent trenches can coalesce into a planar III-V semiconductor material thin film that is free of antiphase-domains, in further non-limiting aspect.

[0033] In various embodiments, disclosed processes facilitate retention of a defect trapping capability associated with an epitaxial necking effect as a result of two upper Si (111) surfaces in the diamond-shaped Si cavities, which can effectively stop stacking faults at the hetero-interface from propagating into the upper layers of the provided III-V semiconductor material thin films. In non-limiting aspects, as a result of the removal of the dielectric spacers in the lateral overgrowth process as disclosed herein, the resultant large-area III-V semiconductor material thin film can be relatively smooth, without the need to employ chemical mechanical polishing as in conventional technology, thus reducing the process complexity and

manufacturing cost. Thus, various embodiment described herein can be employed in the production of III-V metamorphic buffer templates to simulate commercially available III-V native substrates and to provide the capability for device fabricators to engineer group III-V compound semiconductor substrates with designer-chosen surface lattice constants not otherwise offered by commercial substrates.

[0034] As a non-limiting example, FIG. 3 depicts an exemplary process 300 for the formation of diamond-shaped trenches 302 on Si 304, according to non-limiting aspects disclosed herein. In non-limiting aspects, exemplary Si 304 can comprise an exact oriented (100) Si substrate 304, which can be covered with a layer of dielectric 306. In a further non-limiting aspect, exemplary dielectric 306 can be patterned (*e.g.*, pattern into stripes, *etc.*), which can be accomplished by vertical dry etching into exemplary Si 304, as shown in FIG. 3 (top). In another non-limiting aspect, subsequent anisotropic wet etching, for example by potassium hydroxide (KOH) or tetramethylammonium hydroxide (TMAH) etching, can be employed to create one or more diamond-shaped Si structures (*e.g.*, diamond-shaped trenches 302, *etc.*), as shown in FIG. 3 (bottom). In still another non-limiting aspect, a diamond-shaped trench 302 can be characterized by being bounded at least in part by four Si (111) surfaces 308 in the exact oriented (100) Si 304 substrate and/or by having a dimension of an opening 310 in the diamond-shaped trench 302 with a dimension ranging from about 1 nanometer (nm) to about 500 nm. As further described herein, the one or more the diamond-shaped trenches 302 can facilitate depositing group III-V semiconductor materials, which can comprise one or more of gallium arsenide (GaAs), gallium phosphide (GaP), gallium nitride (GaN), gallium antimonide (GaSb), indium arsenide (InAs), indium phosphide (InP), indium antimonide (InSb), indium nitride (InN), aluminum arsenide (AlAs), aluminum nitride (AlN), aluminum antimonide (AlSb), aluminum phosphide (AlP), a ternary semiconductor alloy, a quaternary semiconductor alloy, *etc.*, and/or combinations or permutations thereof, without limitation.

[0035] As a further non-limiting example, FIG. 4 shows cross-sectional transmission electron microscope (TEM) images 402, 404 of exemplary GaAs crystals 406 grown inside diamond-shaped trenches 302 on Si 304, separated by dielectric 306 (*e.g.*, comprising SiO₂, *etc.*) sidewalls, in further non-limiting aspects. The zoomed-in image in FIG. 4 (bottom) highlights the function of the upper two Si (111) surfaces 308 in the trapping of the stacking faults 110 originating at the GaAs/Si interface.

[0036] FIG. 5 shows a tilted-view scanning electron microscope (SEM) image 500 of an exemplary InGaAs alloy 502 grown inside the diamond-shaped trenches 302 on Si 304 separated by dielectric 306 (*e.g.*, comprising SiO₂, *etc.*) sidewalls, in other non-limiting aspects. As depicted in FIGS. 4 and 5, for example, exemplary GaAs crystals 406 and exemplary InGaAs alloy 502 grown inside diamond-shaped trenches 302 on Si 304 exhibit smooth and uniform surface facets, according to non-limiting aspects described herein.

[0037] FIG. 6 depicts a tilted-view SEM image 600 of an exemplary InP 602 composition inside the diamond-shaped trenches 302 on Si 304 separated by dielectric 306 (*e.g.*, comprising SiO₂, *etc.*) sidewalls, according to further non-limiting aspects. FIG. 7 depicts another tilted-view SEM image 700 of an exemplary InP 602 composition inside the diamond-shaped trenches 302 on Si 304 separated by dielectric 306 (*e.g.*, comprising SiO₂, *etc.*) sidewalls, in further non-limiting aspects. Note that trench width of the exemplary diamond-shaped trenches 302 is around 300 nm in FIG. 6 and around 65 nm in FIG. 7. As depicted in FIGS. 6 and 7, for example, exemplary InP 602 composition grown inside diamond-shaped trenches 302 on Si 304 exhibit smooth and uniform surface facets, according to non-limiting aspects described herein.

[0038] FIG. 8 depicts an exemplary process 800 for the formation of an exemplary III-V semiconductor material thin film 802 from exemplary III-V crystals 804 grown in exemplary diamond-shaped trenches 302 on Si 304, as further described herein. As described above, exemplary III-V crystals 804 can be deposited or grown in exemplary diamond-shaped trenches 302 on Si 304 by MOCVD, MBE, or otherwise, using selective area epitaxy, as shown in FIG. 8 (top). In a further non-limiting aspect, exemplary dielectric pattern 306 can be removed, leaving an array of exemplary III-V crystals 804 in exemplary diamond-shaped trenches 302 on Si 304. As described herein, the one or more the diamond-shaped trenches 302 can facilitate depositing or growing group III-V semiconductor materials, which can comprise one or more of gallium arsenide (GaAs), gallium phosphide (GaP), gallium nitride (GaN), gallium antimonide (GaSb), indium arsenide (InAs), indium phosphide (InP), indium antimonide (InSb), indium nitride (InN), aluminum arsenide (AlAs), aluminum nitride (AlN), aluminum antimonide (AlSb), aluminum phosphide (AlP), a ternary semiconductor alloy, a quaternary semiconductor alloy, *etc.*, and/or combinations or permutations thereof, without limitation. As further depicted in FIG. 8 (bottom), the array of exemplary III-V crystals 804 in exemplary diamond-shaped trenches 302 on Si 304

can be coalesced (*e.g.*, from two or more exemplary diamond-shaped trenches 302 on Si 304, *etc.*), which can facilitate growing the group III-V semiconductor materials of exemplary III-V crystals 804 into the exemplary III-V semiconductor material thin film 802 on Si 304. Note that as depicted in FIG. 8, most of the stacking faults 110 generated at the III-V/Si (111) interface are localized in the diamond-shaped trenches 302 on Si 304 as a function of the upper two Si (111) surfaces 308 at the III-V/Si interface.

[0039] FIG. 9 depicts an exemplary process 900 for the formation of an exemplary group III-V material superlattice 902 over an exemplary III-V semiconductor material thin film 802, according to further non-limiting aspects. In a non-limiting aspect, formation of an exemplary group III-V material superlattice 902 over an exemplary metamorphic III-V semiconductor material thin film 802 can further reduce the surface roughness, for example, as further illustrated herein. In further non-limiting aspects, an exemplary group III-V material superlattice 902 can be composed of alternately stacked layers (*e.g.*, forming a periodic structure of successive layers 904, 906 of a number of group III-V materials) of a number of III-V semiconductor compounds of a first composition (*e.g.*, layer 904) and one or more second compositions 906.

[0040] As described herein, the group III-V material superlattice 902 can comprise one or more of gallium arsenide (GaAs), gallium phosphide (GaP), gallium nitride (GaN), gallium antimonide (GaSb), indium arsenide (InAs), indium phosphide (InP), indium antimonide (InSb), indium nitride (InN), aluminum arsenide (AlAs), aluminum nitride (AlN), aluminum antimonide (AlSb), aluminum phosphide (AlP), another ternary semiconductor alloy, or another quaternary semiconductor alloy, *etc.*, and/or combinations or permutations thereof, without limitation. In another non-limiting aspect, exemplary group III-V material superlattice 902 can comprise a periodic structure of successive layers of a number of group III-V materials, wherein each of the successive layers 904, 906, wherein each of the successive layers 904, 906, can be characterized by a thickness ranging from ranges from about 1 nm to about 20 nm. In another non-limiting aspect, exemplary group III-V material superlattice 902 can comprise a periodic structure of successive layers 904, 906, wherein a count of the successive layers can range from about 5 layers to about 20 layers. In various non-limiting embodiments as described herein, selections of one or more materials associated with one or more of exemplary III-V crystals 804, exemplary III-V semiconductor material thin film 802, exemplary group III-V material superlattice 902, and

so on can be selected according to one or more of a desired surface roughness, desired lattice constant, desired composition, desired doping, *etc.*, to facilitate providing exemplary group III-V material metamorphic buffer template substrates.

[0041] As a non-limiting example, FIG. 10 shows an atomic-force microscopy (AFM) image 1000 of an exemplary GaAs metamorphic buffer template in accordance with exemplary processes described herein. For instance, FIG. 10 depicts an exemplary GaAs metamorphic buffer template fabricated as described above regarding FIG. 9, for example, employing 15 periods of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{GaAs}$ (5 nm/5 nm - thickness), wherein AFM scan area is 5×5 (micrometers squared) μm^2 , thereby demonstrating the ability of embodiments described herein to reduce the room-mean-square roughness 1002 to 0.4 nm.

[0042] As a further non-limiting example, FIG. 11 depicts another exemplary process 1100 for the formation of an exemplary III-V semiconductor material thin film 1102 from exemplary III-V crystals 804 grown in exemplary diamond-shaped trenches 302 on Si 304, as further described herein. For example, as depicted in FIG. 11, an exemplary III-V semiconductor material thin film 1102 can be grown from exemplary III-V crystals 804 in exemplary diamond-shaped trenches 302 on Si 304, wherein the exemplary III-V semiconductor material thin film 1102 can differ from exemplary III-V crystals 804 in one or more of lattice constant, composition, doping, *etc.*, as further described herein. As a non-limiting example, as described above, selections of one or more materials associated with one or more of exemplary III-V crystals 804, exemplary III-V semiconductor material thin film 802, 1102, exemplary group III-V material superlattice 902, and so on can be selected according to one or more of a desired surface roughness, desired lattice constant, desired composition, desired doping, *etc.*, to facilitate providing exemplary group III-V material metamorphic buffer template substrates. Accordingly, in further non-limiting aspects, exemplary III-V semiconductor material thin film 1102 can comprise group III-V semiconductor materials comprising at least one of gallium arsenide (GaAs), gallium phosphide (GaP), gallium nitride (GaN), gallium antimonide (GaSb), indium arsenide (InAs), indium phosphide (InP), indium antimonide (InSb), indium nitride (InN), aluminum arsenide (AlAs), aluminum nitride (AlN), aluminum antimonide (AlSb), aluminum phosphide (AlP), the ternary semiconductor alloy (*e.g.*, of exemplary III-V crystals 804), the quaternary semiconductor alloy (*e.g.*, of exemplary III-V crystals 804), a semiconductor material that is the same as the group III-V semiconductor materials (*e.g.*, of exemplary III-V crystals

804), or a different semiconductor material, and wherein the different semiconductor material comprises a material having one or more of a different lattice constant, a different composition, or a different doping level from the group III-V semiconductor materials (*e.g.*, of exemplary III-V crystals 804).

[0043] Accordingly, in various non-limiting embodiments, the subject disclosure provides group III-V compound semiconductors on diamond-shaped trenches 302 on Si 304 (*e.g.*, an exact oriented (100) silicon (Si) substrate), which can facilitate fabrication of exemplary group III-V material metamorphic buffer template substrates. In a non-limiting aspect, an exemplary semiconductor substrate as described herein can comprise an exact oriented (100) silicon (Si) substrate (*e.g.*, Si 304, *etc.*) comprising a set of diamond-shaped trenches (*e.g.*, diamond-shaped trenches 302, *etc.*), wherein a diamond-shaped trench of the set of diamond-shaped trenches (*e.g.*, diamond-shaped trenches 302, *etc.*) is characterized by being bounded at least in part by four (111) Si surfaces (*e.g.*, Si (111) surfaces 308) in the exact oriented (100) Si substrate (*e.g.*, Si 304, *etc.*), for example, as further described herein, regarding FIGS. 3-13.

[0044] In another non-limiting aspect, an exemplary semiconductor substrate as described herein can comprise a first composition of group III-V semiconductor materials (*e.g.*, group III-V semiconductor materials 804, *etc.*) located in the set of diamond-shaped trenches (*e.g.*, diamond-shaped trenches 302, *etc.*), for example, as further described herein, regarding FIGS. 3-13. In yet another non-limiting aspect, an exemplary semiconductor substrate as described herein can comprise a group III-V semiconductor material thin film (*e.g.*, III-V semiconductor material thin film 802, III-V semiconductor material thin film 1102, *etc.*) on the exact oriented (100) Si substrate (*e.g.*, Si 304, *etc.*) comprising at least a portion of the group III-V semiconductor materials (*e.g.*, group III-V semiconductor materials 804, *etc.*), for example, as further described herein, regarding FIGS. 3-13.

[0045] In still another non-limiting aspect, an exemplary semiconductor substrate as described herein can comprise a second composition of group III-V semiconductor materials (*e.g.*, III-V semiconductor material thin film 1102, group III-V material superlattice 902, *etc.*) on the group III-V semiconductor material thin film (*e.g.*, III-V semiconductor material thin film 802, III-V semiconductor material thin film 1102, *etc.*), for example, as further described herein, regarding FIGS. 3-13. In a further non-limiting aspect, an exemplary second composition of group III-V semiconductor materials (*e.g.*, group III-V material superlattice 902, *etc.*) can

comprise a group III-V material superlattice (*e.g.*, group III-V material superlattice 902, *etc.*) comprising a periodic structure of successive layers of two or more group III-V materials, for example, as further described above regarding FIG. 9.

[0046] In view of the example embodiments described *supra*, methods that can be implemented in accordance with the disclosed subject matter will be better appreciated with reference to the flowcharts of FIGS. 12-13, for example. While for purposes of simplicity of explanation, the methods are shown and described as a series of blocks, it is to be understood and appreciated that the claimed subject matter is not limited by the order of the blocks, as some blocks may occur in different orders and/or concurrently with other blocks from what is depicted and described herein. Where non-sequential, or branched, flow is illustrated via flowchart, it can be understood that various other branches, flow paths, and orders of the blocks, can be implemented which achieve the same or a similar result. Moreover, not all illustrated blocks may be required to implement the methods described hereinafter. Additionally, it should be further understood that the methods and/or functionality disclosed hereinafter and throughout this specification are capable of being stored on an article of manufacture to facilitate transporting and transferring such methods to computers, for example, as further described herein.

EXAMPLE METHODS

[0047] FIG. 12 illustrates an example non-limiting flow diagram of methods 1200 for performing aspects of embodiments of the disclosed subject matter. For instance, referring to FIG. 12, methods 1200 for growing III-V compound semiconductors from diamond-shaped trenches 302 on Si 304 (*e.g.*, an exact oriented (100) silicon (Si) substrate) can comprise, at 1202, depositing group III-V semiconductor materials (*e.g.*, group III-V semiconductor materials 804, *etc.*) in two or more diamond-shaped trenches (*e.g.*, diamond-shaped trenches 302, *etc.*) (*e.g.*, diamond-shaped trenches (*e.g.*, diamond-shaped trenches 302, *etc.*) 302, *etc.*) in an exact oriented (100) silicon (Si) substrate (*e.g.*, Si 304, *etc.*). As a non-limiting example, depositing the group III-V semiconductor materials (*e.g.*, group III-V semiconductor materials 804, *etc.*) can comprise depositing one or more of gallium arsenide (GaAs), gallium phosphide (GaP), gallium nitride (GaN), gallium antimonide (GaSb), indium arsenide (InAs), indium phosphide (InP), indium antimonide (InSb), indium nitride (InN), aluminum arsenide (AlAs), aluminum

nitride (AlN), aluminum antimonide (AlSb), aluminum phosphide (AlP), a first ternary semiconductor alloy, or a first quaternary semiconductor alloy, for example, as further described herein, regarding FIGS. 8-9, 11, *etc.*

[0048] In addition, methods 1200 can comprise growing crystals of the group III-V semiconductor materials (*e.g.*, group III-V semiconductor materials 804, *etc.*) in the two or more diamond-shaped trenches (*e.g.*, diamond-shaped trenches 302, *etc.*) in the exact oriented (100) Si substrate (*e.g.*, Si 304, *etc.*), as further described herein. In a non-limiting example, methods 1200 can further comprise the depositing the group III-V semiconductor materials (*e.g.*, group III-V semiconductor materials 804, *etc.*) comprises depositing the group III-V semiconductor materials (*e.g.*, group III-V semiconductor materials 804, *etc.*) via one or more of MOCVD, MBE), *etc.*, as further described herein. In another non-limiting example, growing the crystals of the group III-V semiconductor materials (*e.g.*, group III-V semiconductor materials 804, *etc.*) in the two or more diamond-shaped trenches (*e.g.*, diamond-shaped trenches 302, *etc.*) can comprise one or more of growing the crystals substantially flush with an upper limit of the two or more diamond-shaped trenches (*e.g.*, diamond-shaped trenches 302, *etc.*) defined by a top surface of the exact oriented (100) Si substrate (*e.g.*, Si 304, *etc.*), growing the crystals to have upper surfaces having (111) surfaces, or growing the crystals to have the upper surfaces having (100) surfaces.

[0049] Additionally and/or alternatively, as described above, methods 1200 can further comprise, growing the group III-V semiconductor materials (*e.g.*, group III-V semiconductor materials 804, *etc.*) into a group III-V semiconductor material thin film (*e.g.*, III-V semiconductor material thin film 802, *etc.*) on the exact oriented (100) Si substrate (*e.g.*, Si 304, *etc.*), at 1204, as described herein. As a non-limiting example, growing the group III-V semiconductor materials (*e.g.*, group III-V semiconductor materials 804, *etc.*) into the group III-V semiconductor material thin film (*e.g.*, III-V semiconductor material thin film 802, *etc.*) can comprise growing the group III-V semiconductor materials (*e.g.*, group III-V semiconductor materials 804, *etc.*) comprising one or more of gallium arsenide (GaAs), gallium phosphide (GaP), gallium nitride (GaN), gallium antimonide (GaSb), indium arsenide (InAs), indium phosphide (InP), indium antimonide (InSb), indium nitride (InN), aluminum arsenide (AlAs), aluminum nitride (AlN), aluminum antimonide (AlSb), aluminum phosphide (AlP), the first ternary semiconductor alloy, the first quaternary semiconductor alloy, a semiconductor material

that is the same as the group III-V semiconductor materials (*e.g.*, group III-V semiconductor materials 804, *etc.*), or a different semiconductor material, and wherein the different semiconductor material comprises a material having one or more of a different lattice constant, a different composition, or a different doping level from the group III-V semiconductor materials (*e.g.*, group III-V semiconductor materials 804, *etc.*), as further described herein, regarding FIGS. 8-9, 11, *etc.*

[0050] Additionally and/or alternatively, as described herein, methods 1200 can further comprise, at 1206, depositing additional group III-V semiconductor materials (*e.g.*, III-V semiconductor material thin film 1102, group III-V material superlattice 902, *etc.*) on the group III-V semiconductor material thin film (*e.g.*, III-V semiconductor material thin film 802, *etc.*). In a non-limiting example, depositing the additional group III-V semiconductor materials (*e.g.*, III-V semiconductor material thin film 1102, group III-V material superlattice 902, *etc.*) on the group III-V semiconductor material thin film (*e.g.*, III-V semiconductor material thin film 802, *etc.*) can comprise establishing a composition gradient within one or more of the group III-V semiconductor material thin film (*e.g.*, III-V semiconductor material thin film 802, *etc.*) or the additional group III-V semiconductor materials (*e.g.*, III-V semiconductor material thin film 1102, group III-V material superlattice 902, *etc.*), as further described herein, regarding FIGS. 8-9, 11, *etc.*

[0051] Additionally and/or alternatively, as described herein, methods 1200 can further comprise, at 1208, forming a group III-V material superlattice (*e.g.*, group III-V material superlattice 902, *etc.*) on the group III-V semiconductor material thin film (*e.g.*, III-V semiconductor material thin film 802, *etc.*). As a non-limiting example, forming the group III-V material superlattice (*e.g.*, group III-V material superlattice 902, *etc.*) can comprise forming the group III-V material superlattice (*e.g.*, group III-V material superlattice 902, *etc.*) comprising one or more of gallium arsenide (GaAs), gallium phosphide (GaP), gallium nitride (GaN), gallium antimonide (GaSb), indium arsenide (InAs), indium phosphide (InP), indium antimonide (InSb), indium nitride (InN), aluminum arsenide (AlAs), aluminum nitride (AlN), aluminum antimonide (AlSb), aluminum phosphide (AlP), a second ternary semiconductor alloy, or a second quaternary semiconductor alloy, for example, as further described herein, regarding FIG. 9. In another non-limiting example, methods 1200 can further comprise forming a periodic structure of successive layers of two or more group III-V materials (*e.g.*, forming a periodic

structure of successive layers 904, 906 of a number of group III-V materials), wherein each of the successive layers is characterized by a thickness ranging from about 1 nm to about 20 nm, or wherein a count of the successive layers ranges from about 5 layers to about 20 layers.

[0052] In addition, methods 1200 can further comprise selecting the group III-V semiconductor materials (*e.g.*, group III-V semiconductor materials 804, *etc.*) according to one or more of a predetermined lattice constant or a predetermined composition, for example, as further described herein. Additionally, methods 1200 can further comprise forming the two or more diamond-shaped trenches (*e.g.*, diamond-shaped trenches 302, *etc.*) in the exact oriented (100) Si substrate (*e.g.*, Si 304, *etc.*), for example, as further described herein, regarding FIG. 3. In a non-limiting example, methods 1200 can further comprise forming the two or more diamond-shaped trenches (*e.g.*, diamond-shaped trenches 302, *etc.*), wherein a diamond-shaped trench of the two or more diamond-shaped trenches (*e.g.*, diamond-shaped trenches 302, *etc.*) is characterized by one or more of being bounded at least in part by four (111) Si surfaces (*e.g.*, Si (111) surfaces 308) in the exact oriented (100) Si substrate (*e.g.*, Si 304, *etc.*), or having a dimension of an opening in the diamond-shaped trench with a dimension ranging from about 1 nm to about 500 nm, as further described above. In another non-limiting example, forming the two or more diamond-shaped trenches (*e.g.*, diamond-shaped trenches 302, *etc.*) can comprise patterning a dielectric layer (*e.g.*, dielectric layer 306, *etc.*) on the exact oriented (100) Si substrate (*e.g.*, Si 304, *etc.*), as described herein. In yet another non-limiting example, forming the two or more diamond-shaped trenches (*e.g.*, diamond-shaped trenches 302, *etc.*) can comprise patterning a dielectric layer (*e.g.*, dielectric layer 306, *etc.*) on the exact oriented (100) Si substrate (*e.g.*, Si 304, *etc.*), can comprise patterning a silicon oxide dielectric layer (*e.g.*, dielectric layer 306, *etc.*), can comprise patterning a silicon nitride dielectric layer (*e.g.*, dielectric layer 306, *etc.*), and/or can comprise patterning the dielectric layer (*e.g.*, dielectric layer 306, *etc.*) having a stripe width ranging from about 1 nm to about 500 nm. In still another non-limiting example, forming the two or more diamond-shaped trenches (*e.g.*, diamond-shaped trenches 302, *etc.*) can comprise vertical dry etching the exact oriented (100) Si substrate (*e.g.*, Si 304, *etc.*) defined by remaining portions of the dielectric layer on the exact oriented (100) Si substrate (*e.g.*, Si 304, *etc.*), can comprise anisotropic wet etching the exact oriented (100) Si substrate (*e.g.*, Si 304, *etc.*) defined by the remaining portions of the dielectric layer (*e.g.*, dielectric layer

306, *etc.*), and/or can comprise removing the remaining portions of the dielectric layer (*e.g.*, dielectric layer 306, *etc.*), as further described above, regarding FIG. 3.

[0053] Referring to FIG. 13, methods 1300 for growing III-V compound semiconductors from diamond-shaped trenches 302 on Si 304 (*e.g.*, an exact oriented (100) silicon (Si) substrate) can comprise, at 1302, forming diamond-shaped trenches (*e.g.*, diamond-shaped trenches 302, *etc.*) in an exact oriented (100) silicon (Si) substrate (*e.g.*, Si 304, *etc.*), wherein the diamond-shaped trenches (*e.g.*, diamond-shaped trenches 302, *etc.*) are characterized by being bounded at least in part by four (111) Si surfaces (*e.g.*, Si (111) surfaces 308) in the exact oriented (100) Si substrate (*e.g.*, Si 304, *etc.*), as further described herein, regarding FIGS. 3-11.

[0054] In a non-limiting example, methods 1300 can further comprise forming diamond-shaped trenches (*e.g.*, diamond-shaped trenches 302, *etc.*), wherein the diamond-shaped trenches (*e.g.*, diamond-shaped trenches 302, *etc.*) is characterized by having a dimension of an opening in the diamond-shaped trenches with a dimension ranging from about 1 nm to about 500 nm, as further described above. In another non-limiting example, forming the diamond-shaped trenches (*e.g.*, diamond-shaped trenches 302, *etc.*) can comprise patterning a dielectric layer (*e.g.*, dielectric layer 306, *etc.*) on the exact oriented (100) Si substrate (*e.g.*, Si 304, *etc.*), as described herein. In yet another non-limiting example, forming the diamond-shaped trenches (*e.g.*, diamond-shaped trenches 302, *etc.*) can comprise patterning a dielectric layer (*e.g.*, dielectric layer 306, *etc.*) on the exact oriented (100) Si substrate (*e.g.*, Si 304, *etc.*), can comprise patterning a silicon oxide dielectric layer (*e.g.*, dielectric layer 306, *etc.*), can comprise patterning a silicon nitride dielectric layer (*e.g.*, dielectric layer 306, *etc.*), and/or can comprise patterning the dielectric layer (*e.g.*, dielectric layer 306, *etc.*) having a stripe width ranging from about 1 nm to about 500 nm. In still another non-limiting example, forming the diamond-shaped trenches (*e.g.*, diamond-shaped trenches 302, *etc.*) can comprise vertical dry etching the exact oriented (100) Si substrate (*e.g.*, Si 304, *etc.*) defined by remaining portions of the dielectric layer on the exact oriented (100) Si substrate (*e.g.*, Si 304, *etc.*), can comprise anisotropic wet etching the exact oriented (100) Si substrate (*e.g.*, Si 304, *etc.*) defined by the remaining portions of the dielectric layer (*e.g.*, dielectric layer 306, *etc.*), and/or can comprise removing the remaining portions of the dielectric layer (*e.g.*, dielectric layer 306, *etc.*), as further described above, regarding FIG. 3.

[0055] In addition, at 1304, methods 1300 can further comprise depositing group III-V semiconductor materials (*e.g.*, group III-V semiconductor materials 804, *etc.*) in the diamond-

shaped trenches (*e.g.*, diamond-shaped trenches 302, *etc.*) in the exact oriented (100) Si substrate (*e.g.*, Si 304, *etc.*), for example, as further described above regarding FIGS. 8, 12, *etc.*

Additionally and/or alternatively, methods 1300 can further comprise, at 1306, growing the group III-V semiconductor materials (*e.g.*, group III-V semiconductor materials 804, *etc.*) into a group III-V semiconductor material thin film (*e.g.*, III-V semiconductor material thin film 802, *etc.*) on the exact oriented (100) Si substrate (*e.g.*, Si 304, *etc.*), for example, as further described above regarding FIGS. 8, 11-12, *etc.*

[0056] Additionally and/or alternatively, methods 1300 can further comprise, at 1308, depositing additional group III-V semiconductor materials (*e.g.*, III-V semiconductor material thin film 1102, group III-V material superlattice 902, *etc.*) on the group III-V semiconductor material thin film (*e.g.*, III-V semiconductor material thin film 802, *etc.*). As further described above, depositing the additional group III-V semiconductor materials on the group III-V semiconductor material thin film (*e.g.*, III-V semiconductor material thin film 802, *etc.*) can comprise forming a group III-V material superlattice (*e.g.*, group III-V material superlattice 902, *etc.*) on the group III-V semiconductor material thin film (*e.g.*, III-V semiconductor material thin film 802, *etc.*), in a further non-limiting example, as further described above regarding FIGS. 8-9, 11-12, *etc.*

[0057] Various aspects of the disclosure have been described above. It should be apparent that the teachings herein may be embodied in a wide variety of forms and that any specific structure, function, or both being disclosed herein is merely representative. Based on the teachings herein one skilled in the art should appreciate that an aspect disclosed herein may be implemented independently of any other aspects and that two or more of these aspects may be combined in various ways. For example, an apparatus may be implemented or a method may be practiced using any number of the aspects set forth herein. In addition, such an apparatus may be implemented or such a method may be practiced using other structure, functionality, or structure and functionality in addition to or other than one or more of the aspects set forth herein.

[0058] It is understood that any specific order or hierarchy of steps in any disclosed process is an example of a sample approach. Based upon design preferences, it is understood that the specific order or hierarchy of steps in the processes may be rearranged while remaining within the scope of the present disclosure. The accompanying method claims present elements

of the various steps in a sample order, and are not meant to be limited to the specific order or hierarchy presented.

[0059] While the various embodiments of the subject disclosure have been described in connection with various non-limiting aspects, it will be understood that the embodiments of the subject disclosure may be capable of further modifications. This application is intended to cover any variations, uses or adaptation of the subject disclosure following, in general, the principles of the subject disclosure, and including such departures from the present disclosure as come within the known and customary practice within the art to which the subject disclosure pertains.

[0060] With respect to substantially any plural and/or singular terms used herein, those having skill in the art can translate from the plural to the singular and/or from the singular to the plural as can be appropriate to the context and/or application. The various singular/plural permutations may be expressly set forth herein for the sake of clarity, without limitation.

[0061] It will be understood by those skilled in the art that, in general, terms used herein, and especially in the appended claims (*e.g.*, bodies of the appended claims) are generally intended as “open” terms (*e.g.*, the term “including” should be interpreted as “including but not limited to,” the term “having” should be interpreted as “having at least,” the term “includes” should be interpreted as “includes, but is not limited to,” *etc.*). It will be further understood by those skilled in the art that, if a specific number of an introduced claim recitation is intended, such an intent will be explicitly recited in the claim, and in the absence of such recitation no such intent is present. For example, as an aid to understanding, the following appended claims may contain usage of the introductory phrases “at least one” and “one or more” to introduce claim recitations. However, the use of such phrases should not be construed to imply that the introduction of a claim recitation by the indefinite articles “a” or “an” limit any particular claim containing such introduced claim recitation to embodiments containing only one such recitation, even when the same claim includes the introductory phrases “one or more” or “at least one” and indefinite articles such as “a” or “an” (*e.g.*, “a” and/or “an” should be interpreted to mean “at least one” or “one or more”); the same holds true for the use of definite articles used to introduce claim recitations. In addition, even if a specific number of an introduced claim recitation is explicitly recited, those skilled in the art will recognize that such recitation should be interpreted to mean at least the recited number (*e.g.*, the bare recitation of “two recitations,” without other modifiers, means at least two recitations, or two or more recitations). Furthermore, in those

instances where a convention analogous to “at least one of A, B, and C, *etc.*” is used, in general such a construction is intended in the sense one having skill in the art would understand the convention (*e.g.*, “a system having at least one of A, B, and C” would include, but not be limited to, systems that have A alone, B alone, C alone, A and B together, A and C together, B and C together, and/or A, B, and C together, *etc.*). In those instances where a convention analogous to “at least one of A, B, or C, *etc.*” is used, in general such a construction is intended in the sense one having skill in the art would understand the convention (*e.g.*, “a system having at least one of A, B, or C” would include but not be limited to systems that have A alone, B alone, C alone, A and B together, A and C together, B and C together, and/or A, B, and C together, *etc.*). It will be further understood by those skilled in the art that virtually any disjunctive word and/or phrase presenting two or more alternative terms, whether in the description, claims, or drawings, should be understood to contemplate the possibilities of including one of the terms, either of the terms, or both terms. For example, the phrase “A or B” will be understood to include the possibilities of “A” or “B” or “A and B.”

[0062] In addition, where features or aspects of the disclosure are described in terms of Markush groups, those skilled in the art will recognize that the disclosure is also thereby described in terms of any individual member or subgroup of members of the Markush group.

[0063] As will be understood by one skilled in the art, for any and all purposes, such as in terms of providing a written description, all ranges disclosed herein also encompass any and all possible sub-ranges and combinations of sub-ranges thereof. Any listed range can be easily recognized as sufficiently describing and enabling the same range being broken down into at least equal halves, thirds, quarters, fifths, tenths, *etc.* As a non-limiting example, each range discussed herein can be readily broken down into a lower third, middle third and upper third, *etc.* As will also be understood by one skilled in the art all language such as “up to,” “at least,” and the like include the number recited and refer to ranges which can be subsequently broken down into sub-ranges as discussed above. Finally, as will be understood by one skilled in the art, a range includes each individual member. Thus, for example, a group having 1-3 cells refers to groups having 1, 2, or 3 cells. Similarly, a group having 1-5 cells refers to groups having 1, 2, 3, 4, or 5 cells, and so forth.

[0064] From the foregoing, it will be noted that various embodiments of the disclosed subject matter have been described herein for purposes of illustration, and that various

modifications may be made without departing from the scope and spirit of the subject disclosure. Accordingly, the various embodiments disclosed herein are not intended to be limiting, with the true scope and spirit being indicated by the appended claims.

[0065] In addition, the words “example” and “non-limiting” are used herein to mean serving as an example, instance, or illustration. For the avoidance of doubt, the subject matter disclosed herein is not limited by such examples. Moreover, any aspect or design described herein as “an example,” “an illustration,” “example” and/or “non-limiting” is not necessarily to be construed as preferred or advantageous over other aspects or designs, nor is it meant to preclude equivalent example structures and techniques known to those of ordinary skill in the art. Furthermore, to the extent that the terms “includes,” “has,” “contains,” and other similar words are used in either the detailed description or the claims, for the avoidance of doubt, such terms are intended to be inclusive in a manner similar to the term “comprising” as an open transition word without precluding any additional or other elements, as described above.

[0066] While the disclosed subject matter has been described in connection with the disclosed embodiments and the various figures, it is to be understood that other similar embodiments may be used or modifications and additions may be made to the described embodiments for performing the same function of the disclosed subject matter without deviating therefrom. In other instances, variations of process parameters (*e.g.*, configuration, number of components, aggregation of components, process step timing and order, addition and/or deletion of process steps, addition of preprocessing and/or post-processing steps, *etc.*) can be made to further optimize the provided structures, devices and methods, as shown and described herein. In any event, the structures and/or devices, as well as the associated methods described herein have many applications in various aspects of the disclosed subject matter, and so on. Accordingly, the subject disclosure should not be limited to any single embodiment, but rather should be construed in breadth, spirit and scope in accordance with the appended claims.

CLAIMS

What is claimed is:

1. A method, comprising:
depositing group III-V semiconductor materials in a plurality of diamond-shaped trenches in an exact oriented (100) silicon (Si) substrate; and
growing the group III-V semiconductor materials into a group III-V semiconductor material thin film on the exact oriented (100) Si substrate.
2. The method of claim 1, wherein the depositing the group III-V semiconductor materials comprises depositing at least one of gallium arsenide (GaAs), gallium phosphide (GaP), gallium nitride (GaN), gallium antimonide (GaSb), indium arsenide (InAs), indium phosphide (InP), indium antimonide (InSb), indium nitride (InN), aluminum arsenide (AlAs), aluminum nitride (AlN), aluminum antimonide (AlSb), aluminum phosphide (AlP), a first ternary semiconductor alloy, or a first quaternary semiconductor alloy.
3. The method of claim 2, wherein the growing the group III-V semiconductor materials into the group III-V semiconductor material thin film comprises growing the group III-V semiconductor materials comprising at least one of gallium arsenide (GaAs), gallium phosphide (GaP), gallium nitride (GaN), gallium antimonide (GaSb), indium arsenide (InAs), indium phosphide (InP), indium antimonide (InSb), indium nitride (InN), aluminum arsenide (AlAs), aluminum nitride (AlN), aluminum antimonide (AlSb), aluminum phosphide (AlP), the first ternary semiconductor alloy, the first quaternary semiconductor alloy, a semiconductor material that is the same as the group III-V semiconductor materials, or a different semiconductor material, and wherein the different semiconductor material comprises a material having at least one of a different lattice constant, a different composition, or a different doping level from the group III-V semiconductor materials.
4. The method of claim 1, wherein the depositing the group III-V semiconductor materials comprises depositing the group III-V semiconductor materials via at least one of metal-organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE).

5. The method of claim 1, further comprising:
selecting the group III-V semiconductor materials according to at least one of a predetermined lattice constant or a predetermined composition.
6. The method of claim 1, wherein the depositing the group III-V semiconductor materials comprises growing crystals of the group III-V semiconductor materials in the plurality of diamond-shaped trenches in the exact oriented (100) Si substrate.
7. The method of claim 6, wherein the growing the crystals of the group III-V semiconductor materials in the plurality of diamond-shaped trenches comprises at least one of growing the crystals substantially flush with an upper limit of the plurality of diamond-shaped trenches defined by a top surface of the exact oriented (100) Si substrate, growing the crystals to have upper surfaces having (111) surfaces, or growing the crystals to have the upper surfaces having (100) surfaces.
8. The method of claim 1, further comprising:
forming the plurality of diamond-shaped trenches in the exact oriented (100) Si substrate.
9. The method of claim 8, wherein the forming the plurality of diamond-shaped trenches comprises forming the plurality of diamond-shaped trenches, wherein a diamond-shaped trench of the plurality of diamond-shaped trenches is characterized by at least one of being bounded at least in part by four (111) Si surfaces in the exact oriented (100) Si substrate, or having a dimension of an opening in the diamond-shaped trench with a dimension ranging from about 1 nanometer (nm) to about 500 nm.
10. The method of claim 8, wherein the forming the plurality of diamond-shaped trenches comprises patterning a dielectric layer on the exact oriented (100) Si substrate.

11. The method of claim 10, wherein the patterning the dielectric layer comprises at least one of patterning a silicon oxide dielectric layer, patterning a silicon nitride dielectric layer, or patterning the dielectric layer having a stripe width ranging from about 1 nm to about 500 nm.
12. The method of claim 11, wherein the forming the plurality of diamond-shaped trenches further comprises vertical dry etching the exact oriented (100) Si substrate defined by remaining portions of the dielectric layer on the exact oriented (100) Si substrate.
13. The method of claim 12, wherein the forming the plurality of diamond-shaped trenches further comprises anisotropic wet etching the exact oriented (100) Si substrate defined by the remaining portions of the dielectric layer.
14. The method of claim 13, further comprising:
removing the remaining portions of the dielectric layer.
15. The method of claim 1, further comprising:
depositing additional group III-V semiconductor materials on the group III-V semiconductor material thin film.
16. The method of claim 15, wherein the depositing the additional group III-V semiconductor materials on the group III-V semiconductor material thin film comprises establishing a composition gradient within at least one of the group III-V semiconductor material thin film or the additional group III-V semiconductor materials.
17. The method of claim 1, further comprising:
forming a group III-V material superlattice on the group III-V semiconductor material thin film.
18. The method of claim 17, wherein the forming the group III-V material superlattice comprises forming the group III-V material superlattice comprising at least one of gallium arsenide (GaAs), gallium phosphide (GaP), gallium nitride (GaN), gallium antimonide (GaSb),

indium arsenide (InAs), indium phosphide (InP), indium antimonide (InSb), indium nitride (InN), aluminum arsenide (AlAs), aluminum nitride (AlN), aluminum antimonide (AlSb), aluminum phosphide (AlP), a second ternary semiconductor alloy, or a second quaternary semiconductor alloy.

19. The method of claim 17, wherein the forming the group III-V material superlattice comprises forming a periodic structure of successive layers of a plurality of group III-V materials, wherein each of the successive layers is characterized by a thickness ranging from about 1 nanometer (nm) to about 20 nm, or wherein a count of the successive layers ranges from about 5 layers to about 20 layers.

20. A method, comprising:

forming diamond-shaped trenches in an exact oriented (100) silicon (Si) substrate, wherein the diamond-shaped trenches are characterized by being bounded at least in part by four (111) Si surfaces in the exact oriented (100) Si substrate;

depositing group III-V semiconductor materials in the diamond-shaped trenches in the exact oriented (100) Si substrate;

growing the group III-V semiconductor materials into a group III-V semiconductor material thin film on the exact oriented (100) Si substrate; and

depositing additional group III-V semiconductor materials on the group III-V semiconductor material thin film.

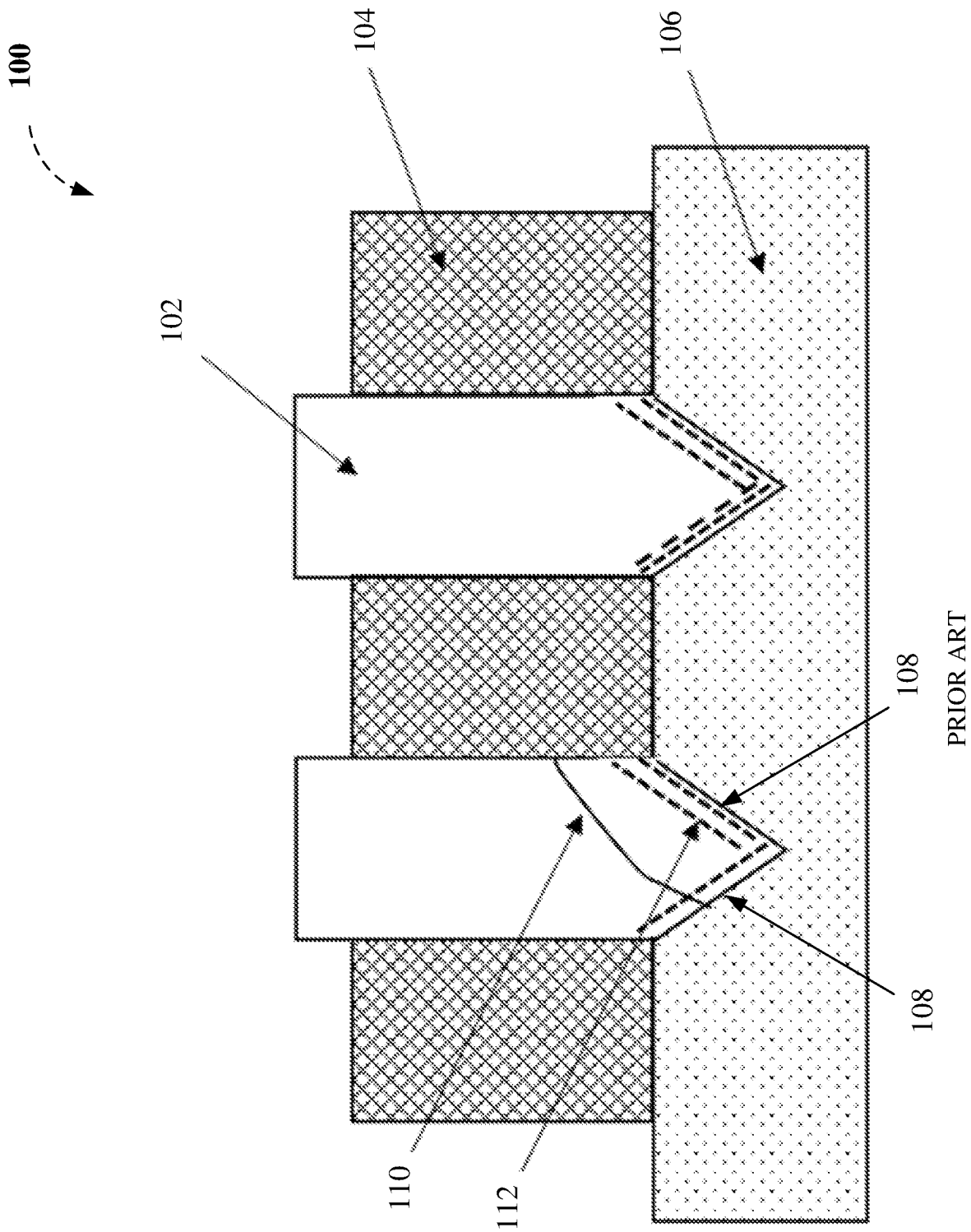
21. The method of claim 20, wherein the depositing the additional group III-V semiconductor materials on the group III-V semiconductor material thin film comprises forming a group III-V material superlattice on the group III-V semiconductor material thin film.

22. A semiconductor substrate, comprising:

an exact oriented (100) silicon (Si) substrate comprising a set of diamond-shaped trenches, wherein a diamond-shaped trench of the set of diamond-shaped trenches is characterized by being bounded at least in part by four (111) Si surfaces in the exact oriented (100) Si substrate; and

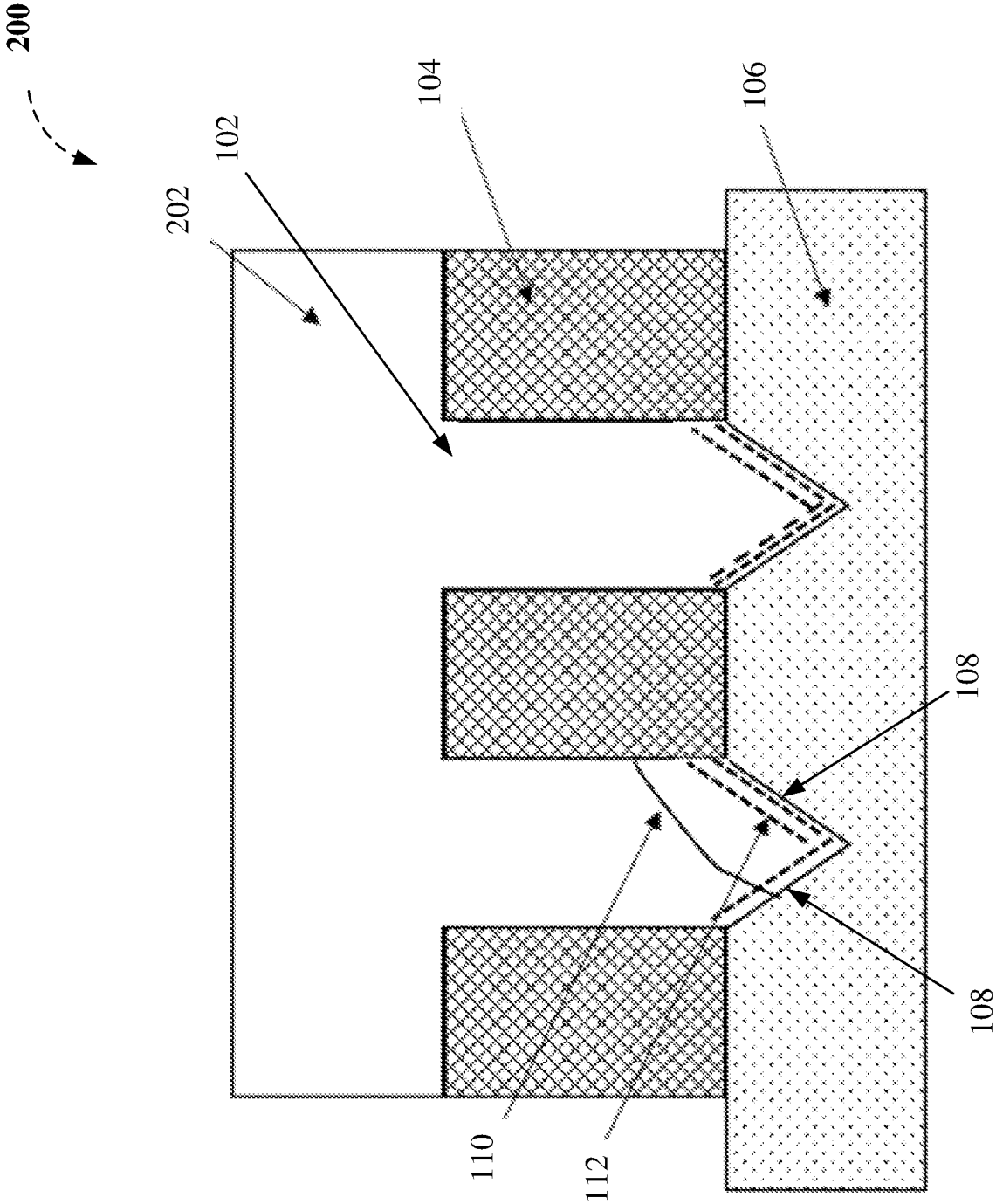
a first composition of group III-V semiconductor materials located in the set of diamond-shaped trenches.

23. The semiconductor substrate of claim 22, further comprising:
a group III-V semiconductor material thin film on the exact oriented (100) Si substrate comprising at least a portion of the group III-V semiconductor materials.
24. The semiconductor substrate of claim 23, further comprising:
a second composition of group III-V semiconductor materials on the group III-V semiconductor material thin film.
25. The semiconductor substrate of claim 24, wherein the second composition of group III-V semiconductor materials comprises a group III-V material superlattice comprising a periodic structure of successive layers of a plurality of group III-V materials.



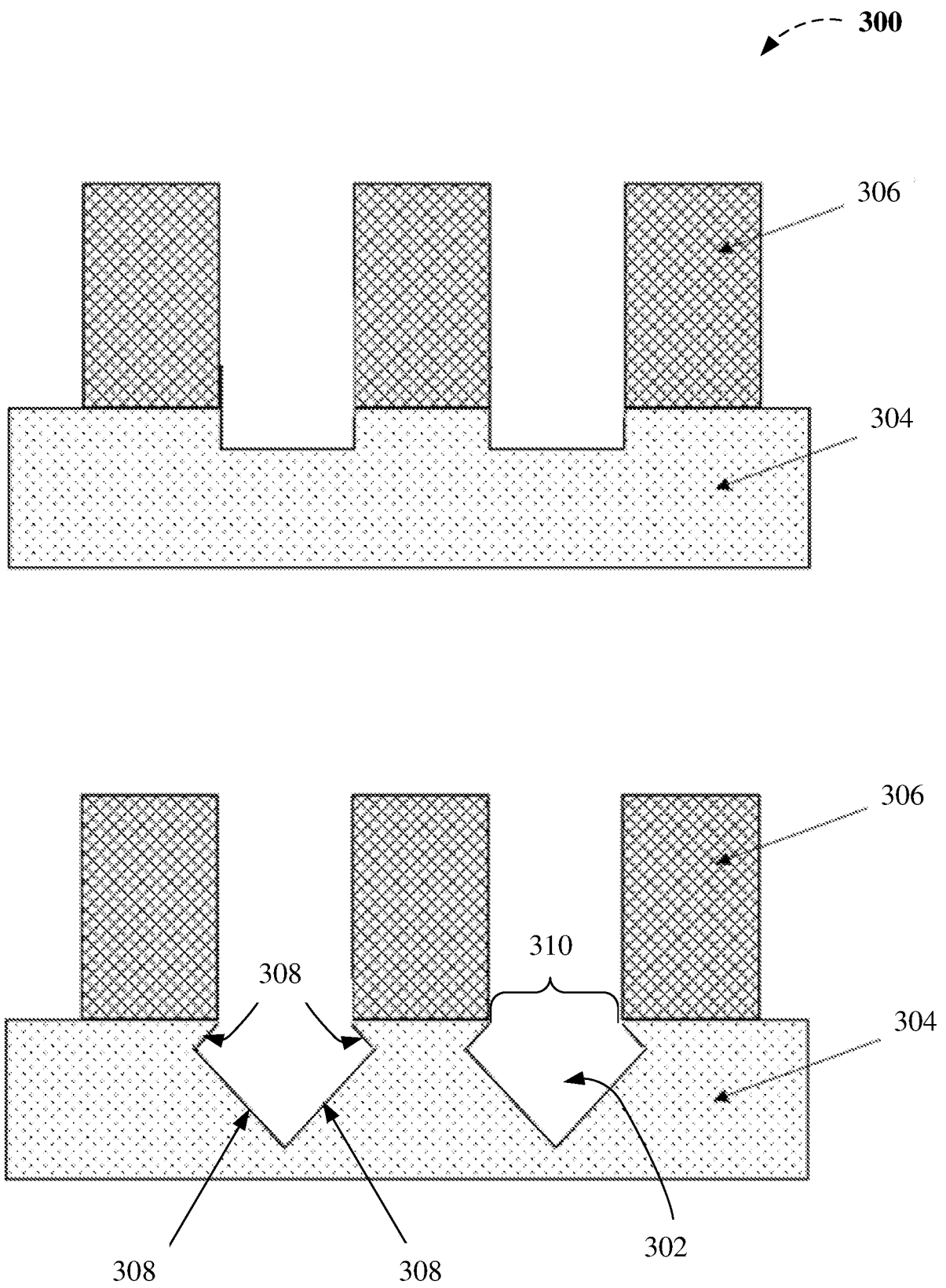
PRIOR ART

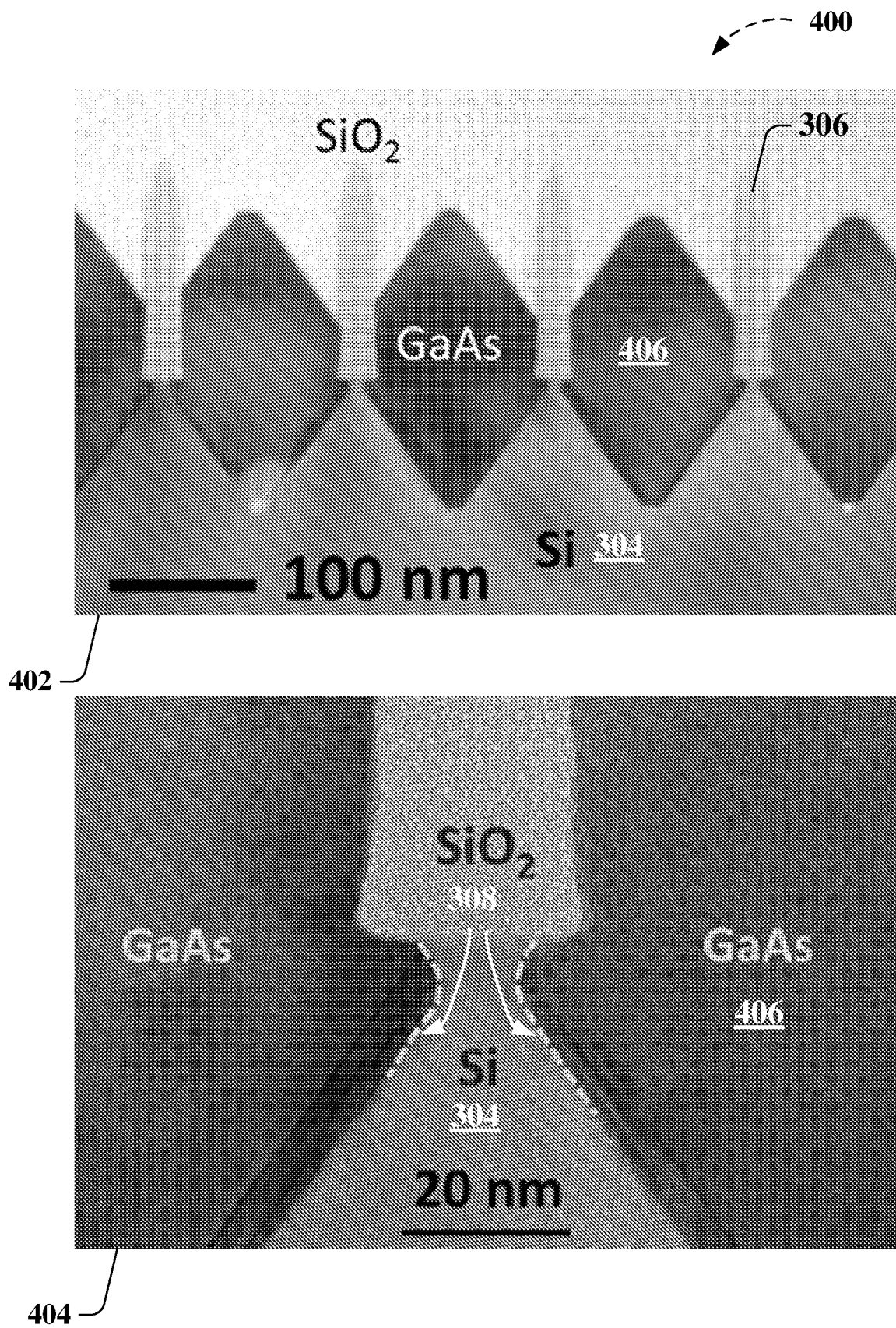
FIG. 1

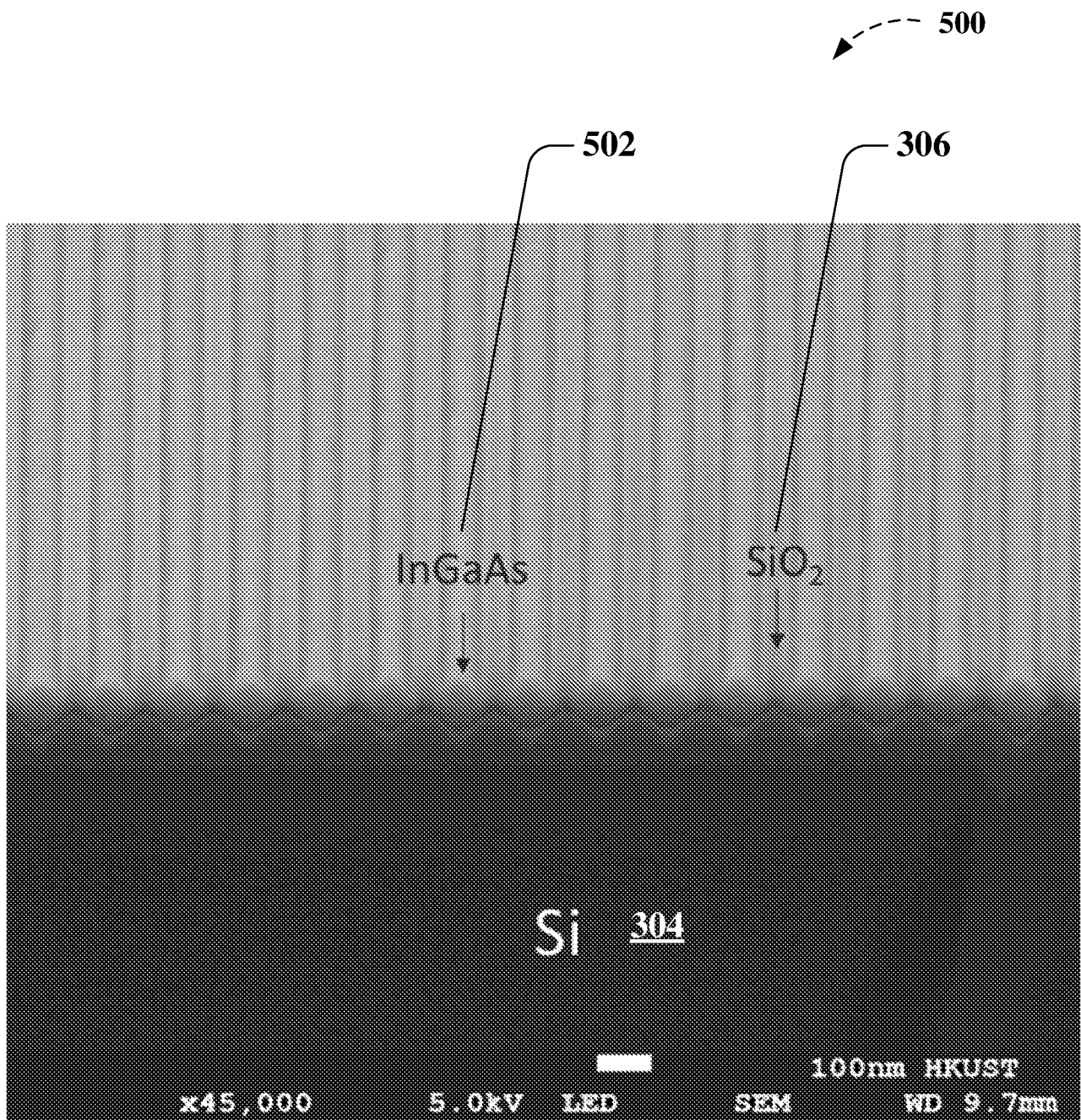


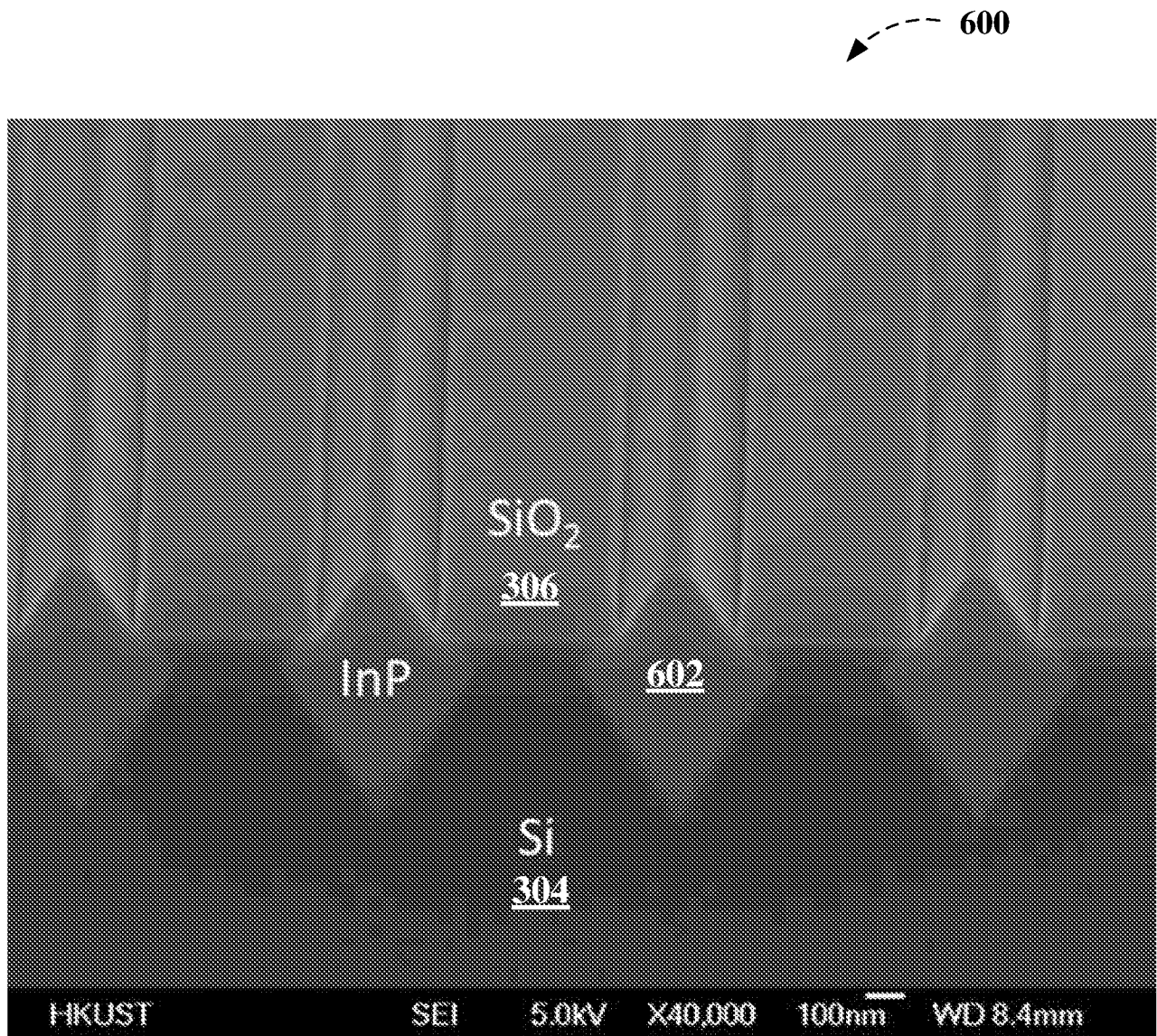
PRIOR ART

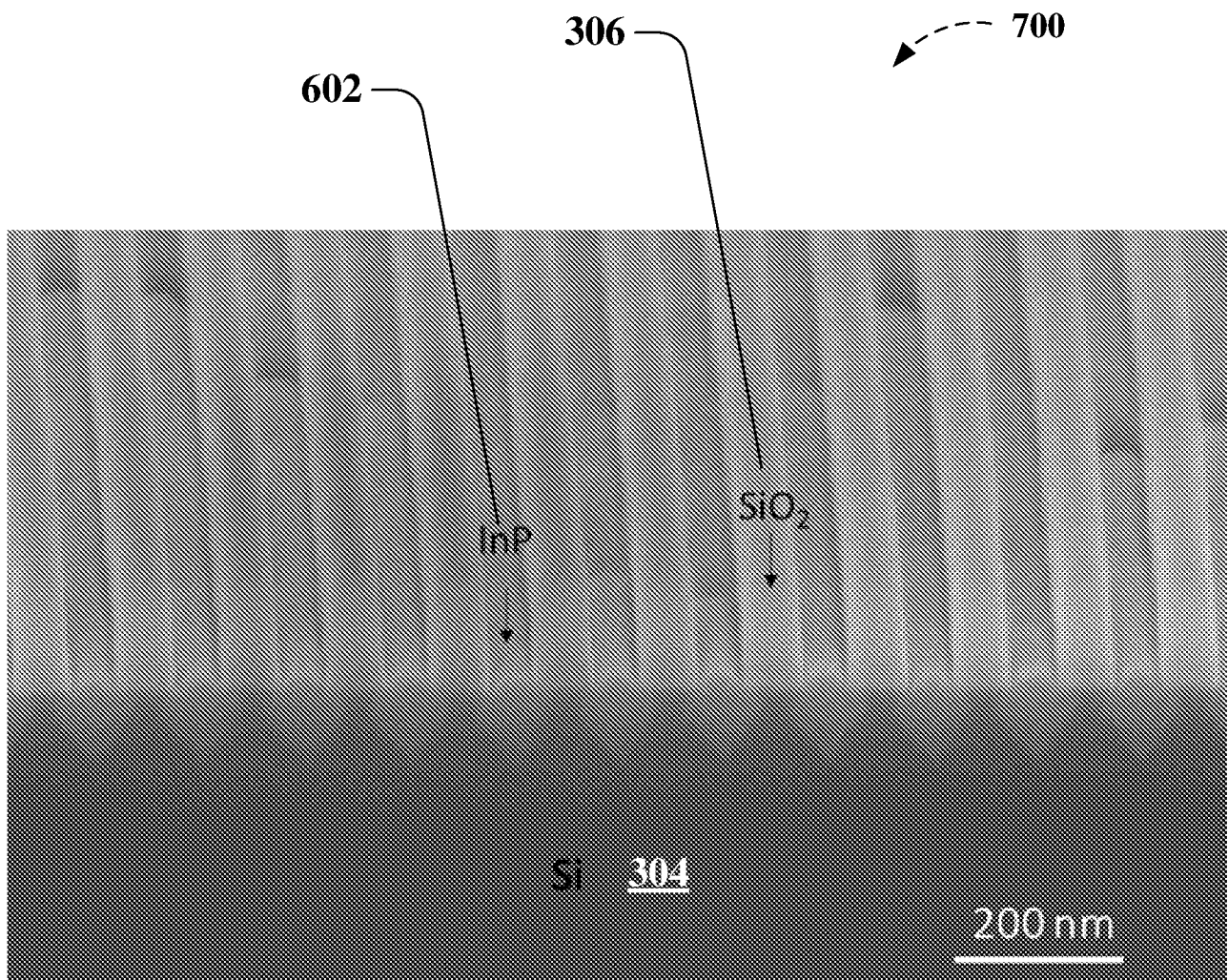
FIG. 2

**FIG. 3**

**FIG. 4**

**FIG. 5**

**FIG. 6**

**FIG. 7**

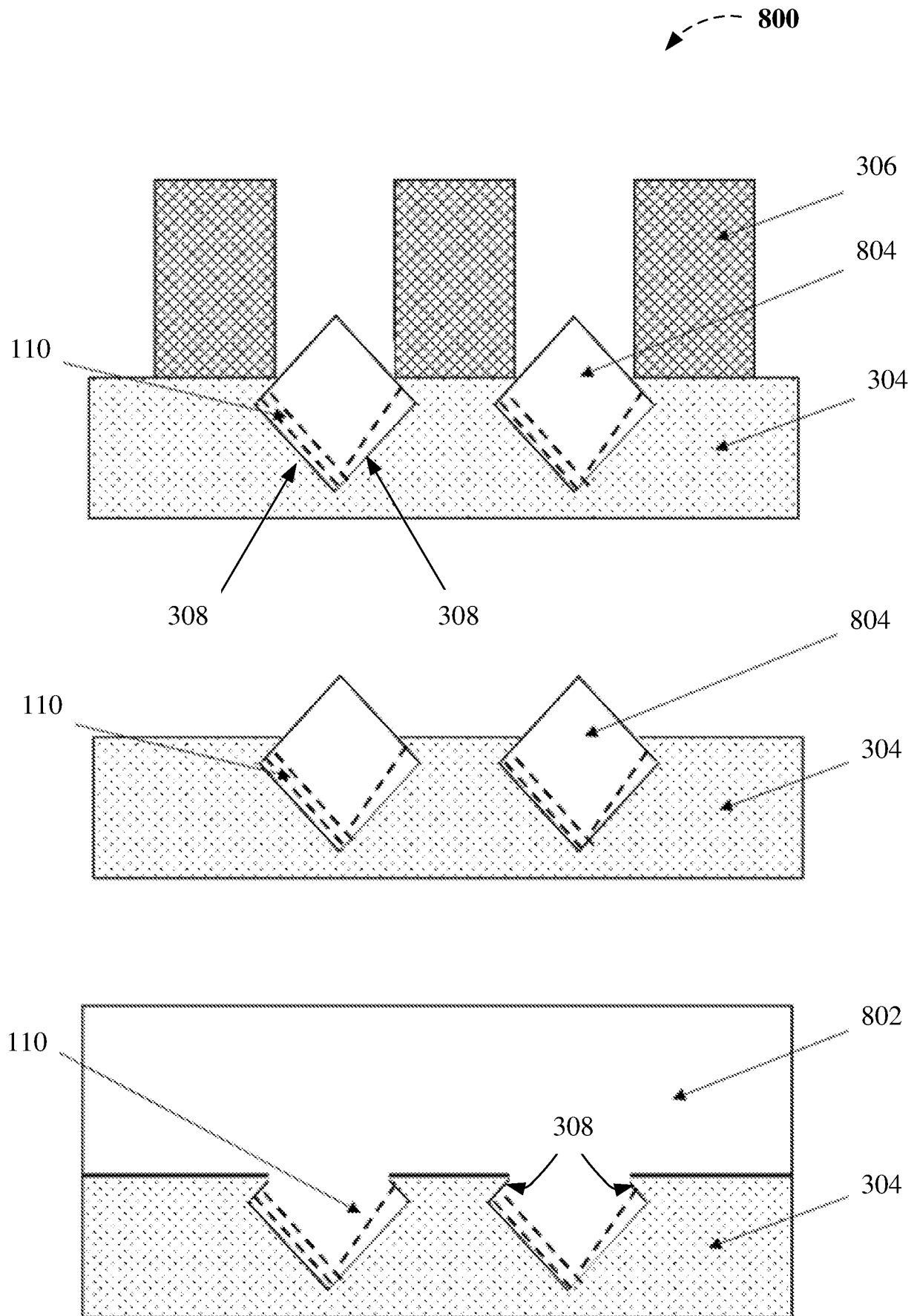
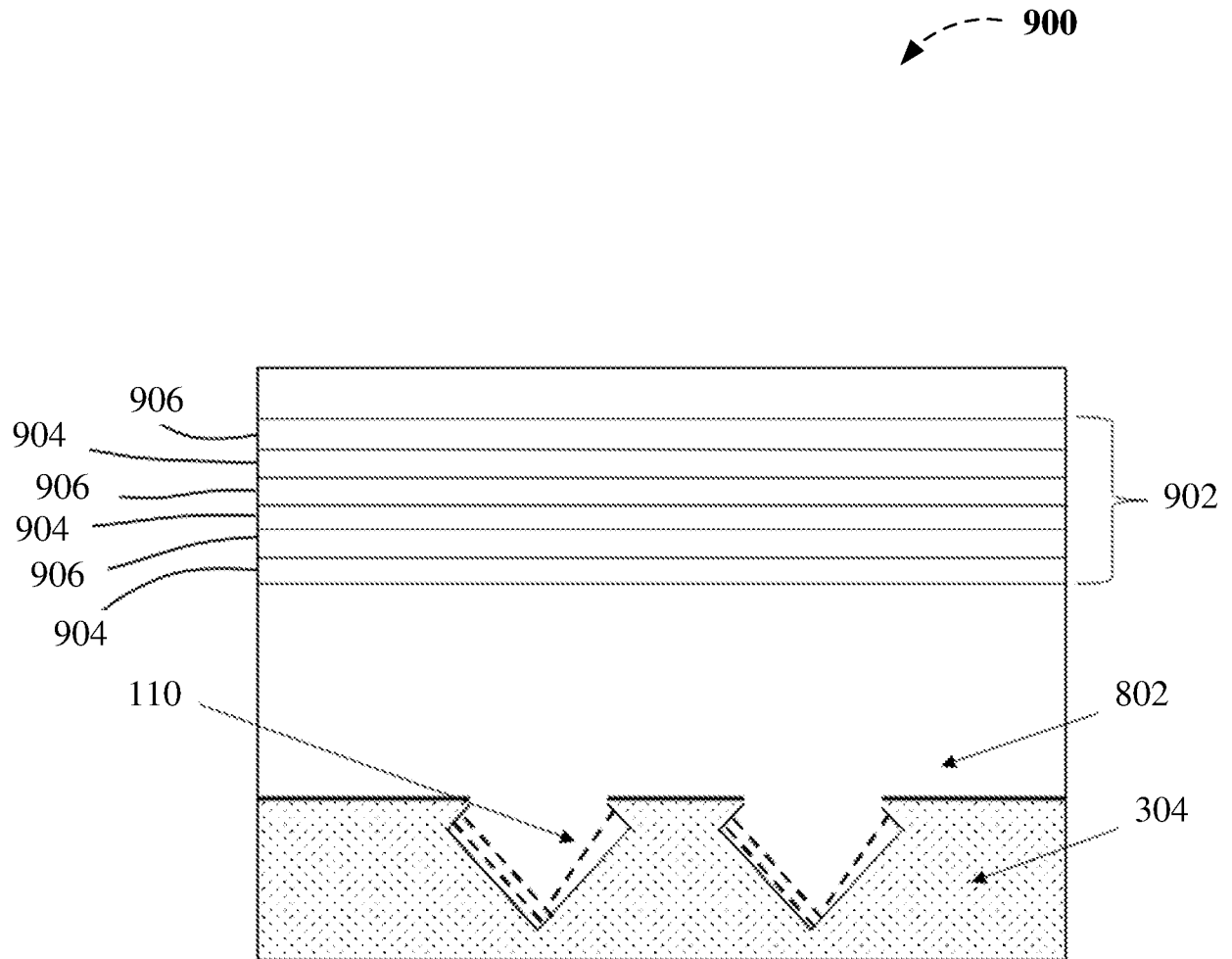


FIG. 8

**FIG. 9**

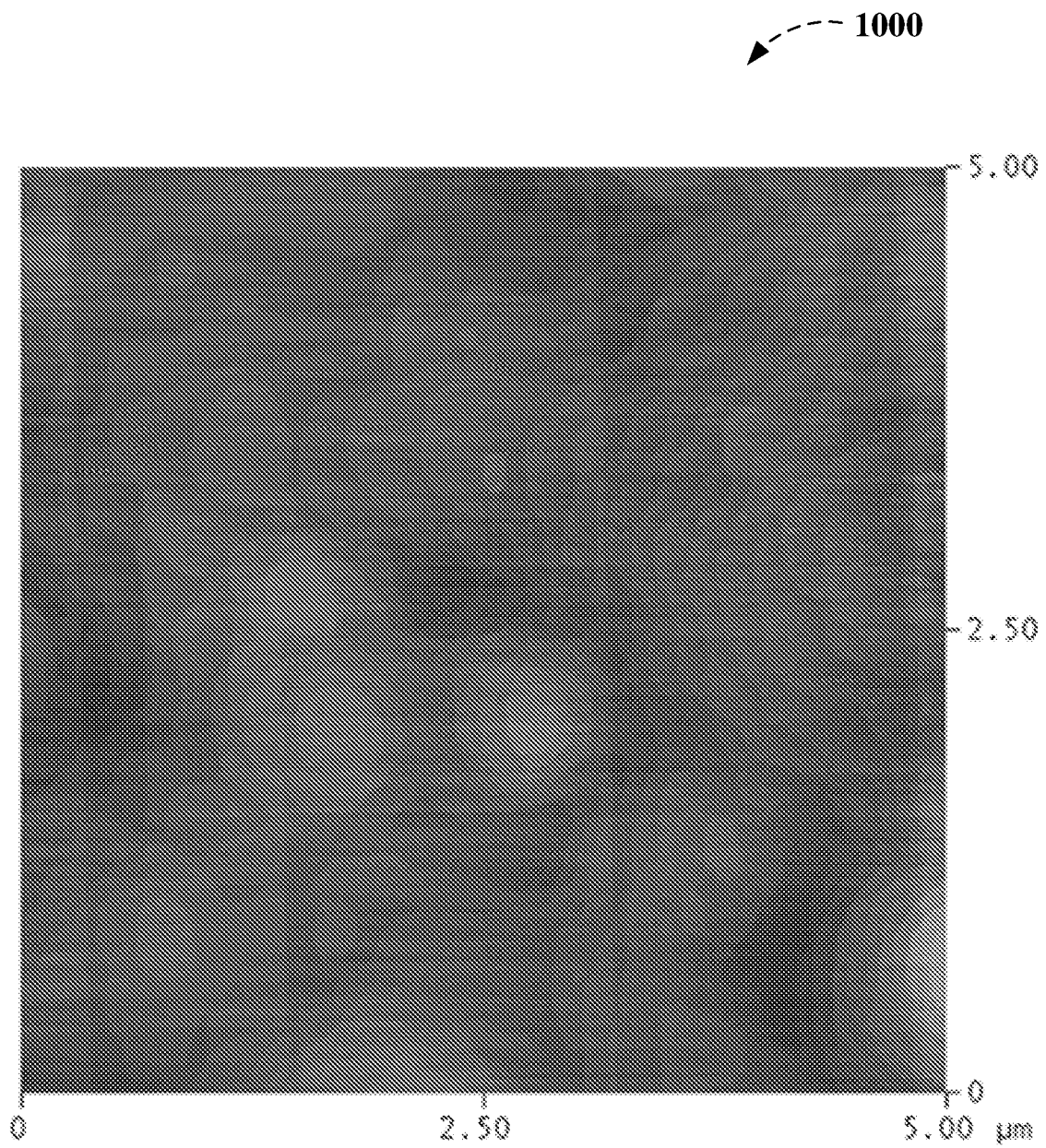


Image Statistics

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Img. Rms (Rq)	0.411 nm

Box Statistics

Rms (Rq)

1002

FIG. 10

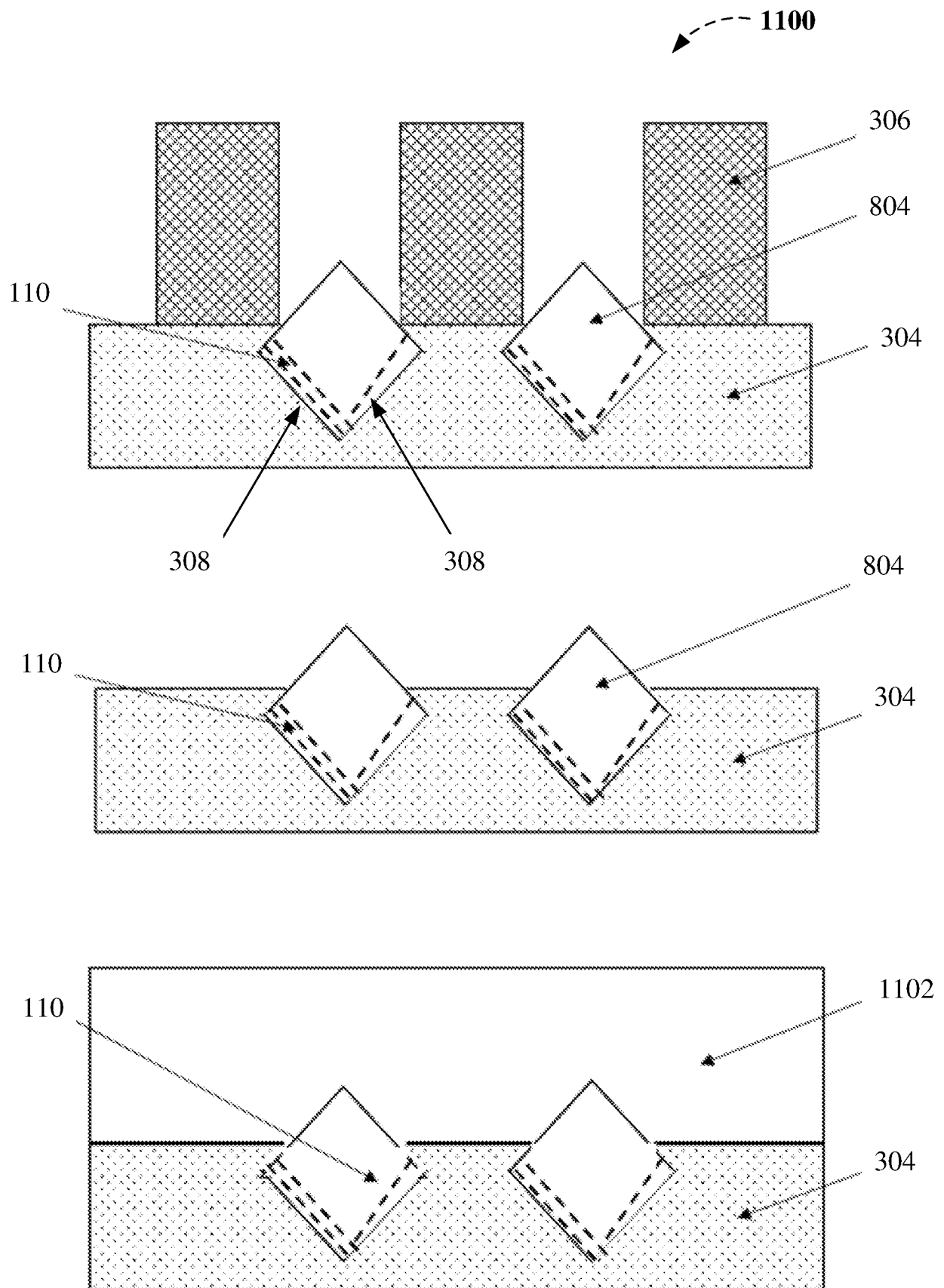
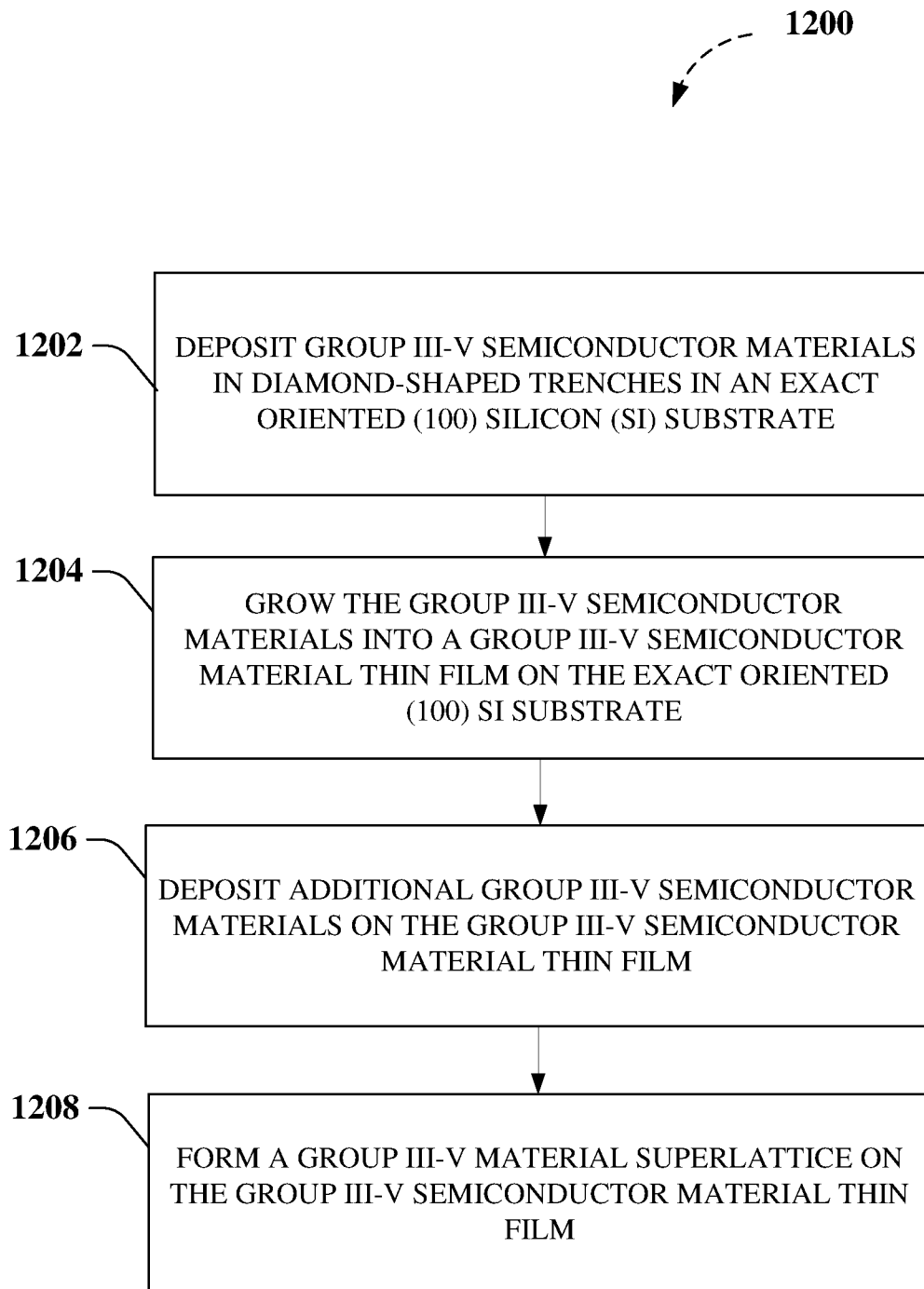
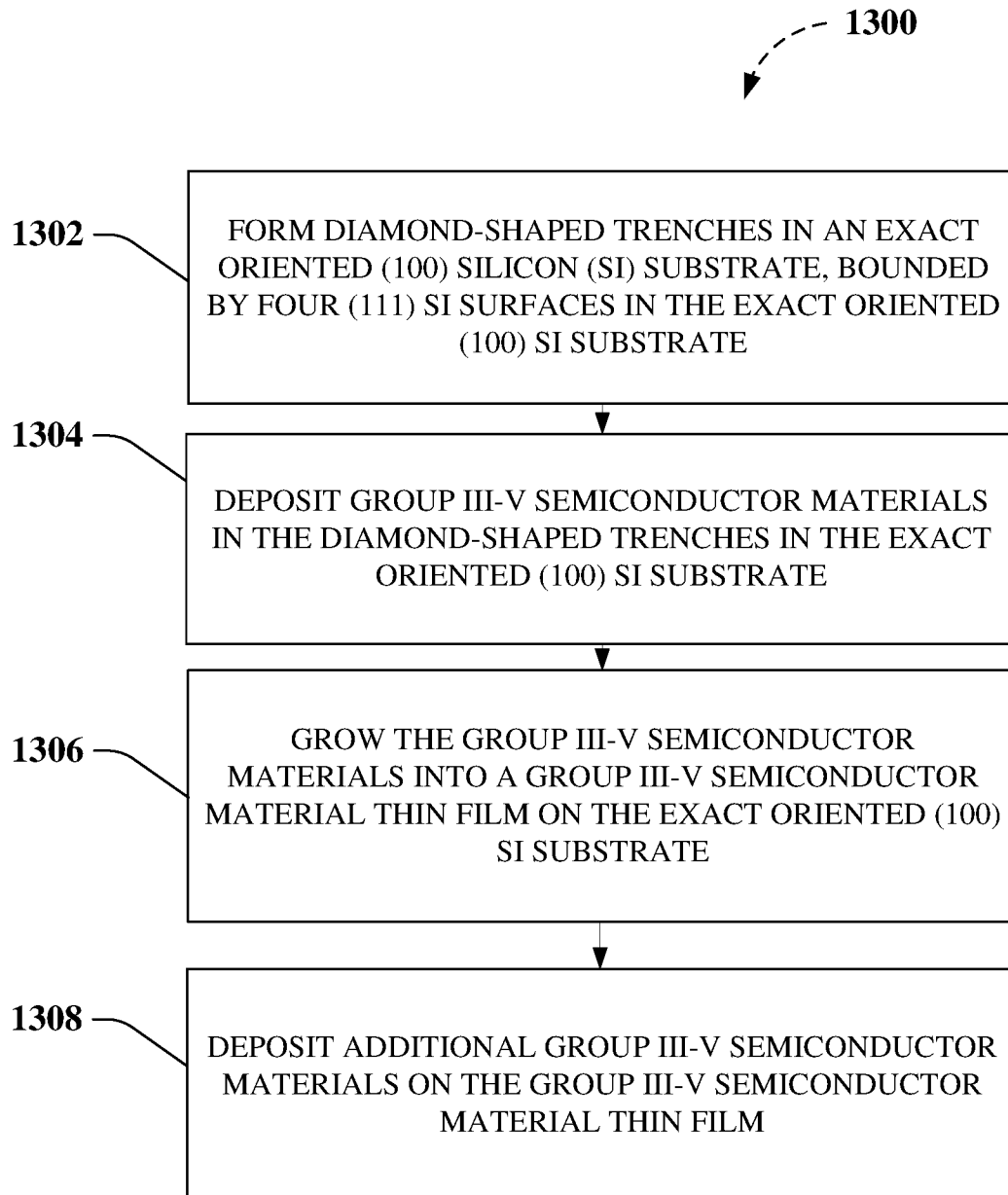


FIG. 11

**FIG. 12**

**FIG. 13**

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2017/088966

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/336(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

USTXT;CNABS;VEN;CNKI;WPI;EPODOC: diamond shaped, trenches, silicon, III-V, 100, growing, depositing, semiconductors, Si

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 105874587 A (INTEL CORP.) 17 August 2016 (2016-08-17) paragraphs[0046]-[0050], [0096]-[0112], figures 3A-3G	1-25
A	CN 105655383 A (SEMICONDUCTOR MFG INT. SHANGHAI CORP.) 08 June 2016 (2016-06-08) paragraphs [0006]-[0024]	1-25
A	CN 104282548 A (UNIV. ELECTRONIC SCI. & TECHNOLOGY) 14 January 2015 (2015-01-14) paragraphs [0006]-[0020]	1-25
A	CN 103794498 A (SEMICONDUCTOR MFG INT. SHANGHAI CORP.) 14 May 2014 (2014-05-14) paragraphs [0008]-[0031]	1-25
A	US 2012138568 A1 (YUN-CHUNG N. NA) 07 June 2012 (2012-06-07) paragraphs [0015]-[0018], figures 1-3	1-25

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

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"P" document published prior to the international filing date but later than the priority date claimed

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"&" document member of the same patent family

Date of the actual completion of the international search

10 August 2017

Date of mailing of the international search report

28 August 2017

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2017/088966

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	105874587	A	17 August 2016	TW	201535516	A	16 September 2015
				US	9640422	B2	02 May 2017
				KR	20160111364	A	26 September 2016
				WO	2015112277	A1	30 July 2015
				US	2015206796	A1	23 July 2015
				EP	3097583	A1	30 November 2016
				TW	I539521	B	21 June 2016
CN	105655383	A	08 June 2016	None			
CN	104282548	A	14 January 2015	None			
CN	103794498	A	14 May 2014	CN	103794498	B	21 December 2016
US	2012138568	A1	07 June 2012	US	8437585	B2	07 May 2013