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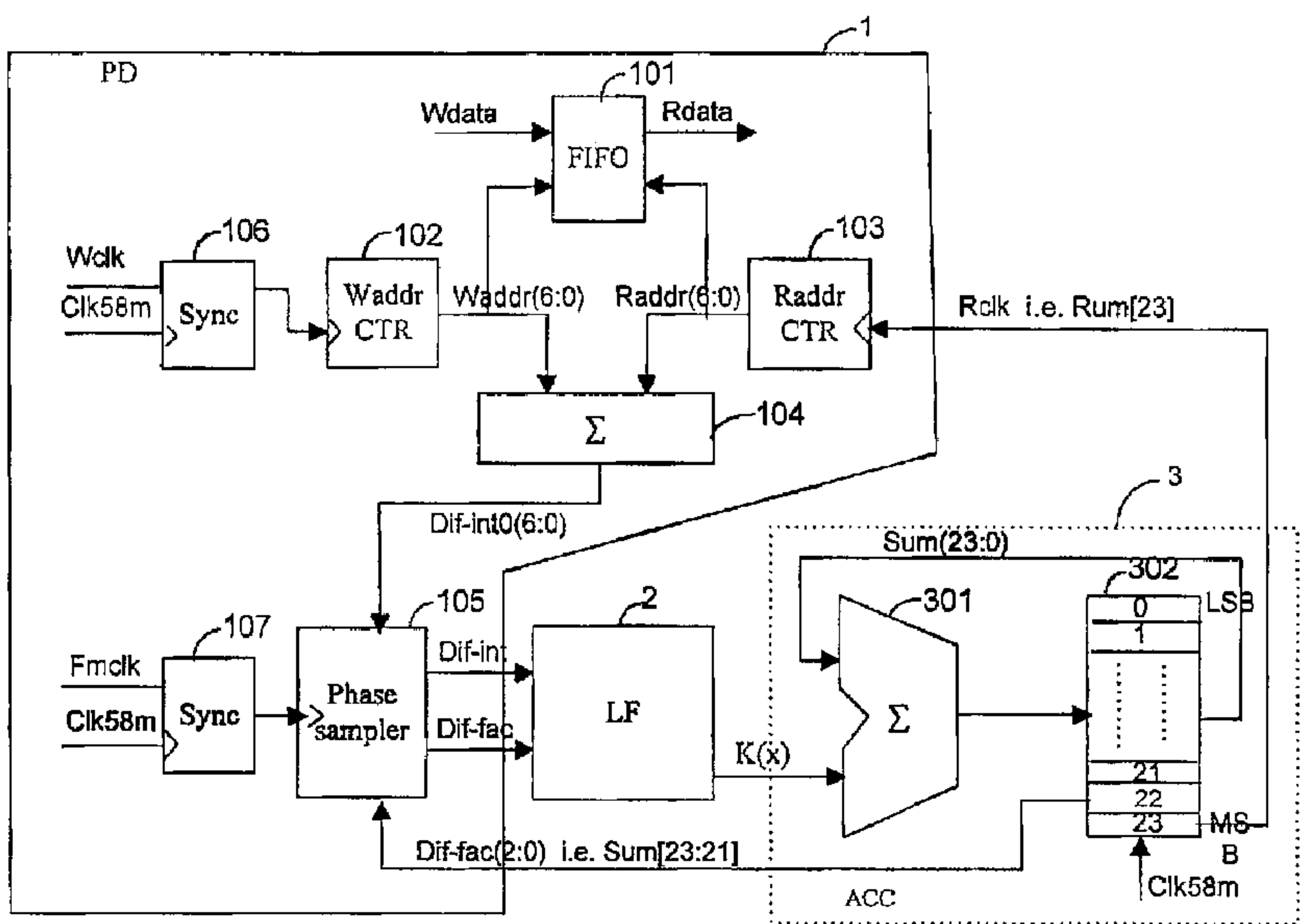
(54) **Titre :** PROCEDE DE FILTRAGE DANS UNE BOUCLE A VERROUILLAGE DE PHASE NUMERIQUE

(54) **Title:** A FILTERING METHOD FOR DIGITAL PHASE LOCK LOOP



(57) **Abrégé/Abstract:**

A filtering method for digital Phase Lock Loop, comprises: defining a phase difference value representing a nominal value of the difference between the phase of an input clock signal and the phase of a local recovery clock signal by setting an address difference reference offset representative of said phase difference reference value to half the bit depth of a first-in-first-out memory; calculating a read/write address difference which denotes a bit position difference in a data stream of content data between an input data pointer and an output data pointer indicating the starting addresses of contents data written to and contents data read from the first-in-first-out memory, respectively, said read/write address difference being representative of a detected phase difference between the input clock signal and the local recovery clock signal; comparing the detected phase difference with the phase difference reference value; and adjusting the local recovery clock signal in segments to the phase difference reference value, wherein a correction signal used for adjusting the local recovery clock signal, said correction signal being representative of a change in the detected phase difference, is increased or decreased segment by segment depending on the magnitude and the algebraic sign of a detected deviation of the detected phase difference from the phase difference reference value. The invention concerns non-error code and vibration minimization at the same time, so vibration tolerance is better raised, vibration transfer characteristic is very good, and net output vibration indicator at low band and high band parts is improved.

Abstract

A filtering method for digital Phase Lock Loop, comprises: defining a phase difference value representing a nominal value of the difference between the phase of an input clock signal and the phase of a local recovery clock signal by setting an address difference reference offset representative of said phase difference reference value to half the bit depth of a first-in-first-out memory; calculating a read/write address difference which denotes a bit position difference in a data stream of content data between an input data pointer and an output data pointer indicating the starting addresses of contents data written to and contents data read from the first-in-first-out memory, respectively, said read/write address difference being representative of a detected phase difference between the input clock signal and the local recovery clock signal; comparing the detected phase difference with the phase difference reference value; and adjusting the local recovery clock signal in segments to the phase difference reference value, wherein a correction signal used for adjusting the local recovery clock signal, said correction signal being representative of a change in the detected phase difference, is increased or decreased segment by segment depending on the magnitude and the algebraic sign of a detected deviation of the detected phase difference from the phase difference reference value. The invention concerns non-error code and vibration minimization at the same time, so vibration tolerance is better raised, vibration transfer characteristic is very good, and net output vibration indicator at low band and high band parts is improved.

A Filtering Method for Digital Phase Lock Loop

Field of the Technology

The present invention relates generally to digital Phase Lock Loop technology , and more particularly to a filtering method used in digital Phase Lock Loop.

Background of the Invention

Phase Lock Loop (PLL) is a closed loop tracking system which can track phase and frequency of a input signal. When PLL tracks a input signal with constant frequency, there is no frequency difference. When PLL tracks an input signal with variable frequency, the tracking accuracy is very high also.

There are two kinds of PLL: Analog Phase Lock Loop (APLL) and Digital Phase Lock Loop (DPLL). An APLL is consisted of a Phase Detector (PD), a Loop Filter (LF) and a Voltage-Controlled Oscillator (VCO). APLL has better vibration suppression performance, but has discreteness in technology, and has higher manufacture cost and lower stability.

If part of a DPLL is a digital circuit, it is called partial DPLL. The principle is similar to APLL, and as it frequency control still applies analog circuit, so disadvantage, such as high discreteness, high manufacture difficulty and high cost, exist. DPPL is consisted of all digital circuit. A newer implementation method of DPPL is proposed by the US patent (US5033064). The DPPL implemented by the method has better vibration transfer characteristic and net vibration output characteristic, but there is no effective loop filtering method and vibration filter performance at lower band frequency is not ideal enough.

Summary of the Invention

The invention provides a filtering method for DPLL to make the DPPL vibration tolerance, vibration transfer and net vibration output performances, at lower band frequency and higher band frequency, are excellent.

A filtering method for DPLL comprises following steps:

defining a phase difference value $\Delta\varphi_{ref}$ representing a nominal value of the difference $\Delta\varphi$ between the phase φ_{ref} of an input clock signal (*Wclk*) and the phase φ_{rec} of a local recovery clock signal *Rclk* by setting an address difference reference offset x_0 representative of said phase difference reference value $\Delta\varphi_{ref}$ to half the bit depth L of a first-in-first-out memory;

calculating a read/write address difference Dif-int0 which denotes a bit position difference in a data stream of content data between an input data pointer P_W and an output data pointer P_R indicating the starting addresses of contents data Wdata written to and contents data Rdata read from the first-in-first-out memory, respectively, said read/write address difference Dif-int0 being representative of a detected phase difference $\Delta\varphi$ between the input clock signal *Wclk* and the local recovery clock signal *Rclk*;

comparing the detected phase difference $\Delta\varphi$ with the phase difference reference value $\Delta\varphi_{ref}$; and

adjusting the local recovery clock signal *Rclk* in segments to the phase difference reference value $\Delta\varphi_{ref}$, wherein a correction signal $K(x)$ used for adjusting the local recovery clock signal *Rclk*, said correction signal $K(x)$ being representative of a change in the detected phase difference $\Delta\varphi$, is increased or decreased segment by segment depending on the magnitude and the algebric sign of a detected deviation of the detected phase difference $\Delta\varphi$ from the phase difference reference value $\Delta\varphi_{ref}$;

wherein said correction signal $K(x)$ is calculated based on a digital signal x which, compared with said read/write address difference Dif-int0, is representative of a more precise representation of the detected phase difference $\Delta\varphi$, said digital signal x being a function of two futher digital signals Dif-int and Dif-frac representing an integer part and a fractional part of the detected phase difference $\Delta\varphi$, respectively.

As the invention is based on DPLL, it can overcome weaknesses of APLL: large dispersion, high cost and low stability. The very important point is the local recovery clock signal frequency f_{rec}, outputted from the digital frequency divider, can be adaptively adjusted according to detected phase difference $\Delta\varphi$.

The invention thereby concerns non-error code and vibration minimization at the same time, which has the advantage that vibration tolerance is better raised, vibration transfer characteristic are enhanced and net output vibration indicators at low-band frequency and high-band frequency are improved.

Brief Description of the Drawings

Figure 1 is a block diagram of Phase Lock Loop circuitry according to the present invention.

Figure 2 is a more detailed view of the block diagram depicted in Figure 1.

Figure 3 is a filtering operational function diagram showing the input signal $K(x)$ of the phase accumulator as a function of a digital signal x represented by a function of the integer part and the fractional part of the detected phase difference $\Delta\varphi$.

Embodiments of the Invention

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout.

Figure 1 shows that a DPLL is consisted of a phase detector 1, a loop filter (LF) 2 and a phase accumulator 3. The phase detector 1 receives an input clock signal (*Wclk*) and a local recovery clock signal (*Rclk*), and makes frequency detection and phase detection, then outputs a phase difference $\Delta\varphi$ to the LF 2. The LF 2 calculates an accumulated frequency signal $K(x)$ according to a signal x representing the phase difference $\Delta\varphi$. The phase accumulator 3 is consisted of an adder 301 and a register 302. The adder 301 adds output data S of the register 302 and output data *K* of the LF 2, and the register 302 stores the current adding result at every rising clock pulse edge of a local high-speed crystal oscillator signal. Wherein the register has a bit length that equals the adder bit length, and only stores a sum without carry bit. The register 302 outputs to the adder 301 an accumulated value $S(n:0)$, e.g. the result of last adding, so a accumulative function is implemented. Wherein n is the adder bit length , and most significant bit (MSB) of the accumulative value is a local recovery clock signal frequency f_{rec} recovered by the phase accumulator 3 whose output is provided to the phase detector 1 for phase detection. The clock frequency of the phase accumulator 3 is provided by the local high-speed crystal oscillator's frequency f_{LO}.

Figure 2 is a circuit block diagram of an embodiment of the invention. The circuit applies a local high-speed crystal oscillator providing an oscillator frequency of 58.32MHz to recover a ideal 2.048MHz clock with minimized vibration, and the phase accumulator 3 applies a 24-bit adder. The digital phase detector 1 performs frequency detection and phase detection of PLL, and includes: a first-in-first-out memory (FIFO) 101 with a bit depth of L=128 bit, a read address counter 103, a write address counter 102, a subtracter module 104, a phase sampling circuit 105 and two synchronization circuits 106 and 107. The subtracter module 104 calculates a read/write address difference Dif-int0 which is representative of a digital signal Dif-int representing an integer part of the detected phase difference $\Delta\varphi$, wherein *Dif-int* is given by the read/write address difference Dif-int0(6:0) := Waddr(6:0)-Raddr(6:0) after being sampled by a sampling clock signal *Fmclk*. The digital signal Dig-int representing the integer part of the detected phase difference $\Delta\varphi$ is then inputted to the LF 2.

A digital signal *Dif-fac* representing the fractional part of the detected phase difference $\Delta\varphi$ which is inputted to the LF 2 is given by the signal *Sum*(23:21), which represents the sum of accumulated phase values stored in the three most significant bits of the digital signal supplied by the phase accumulator 3. The LF 2 calculates, according to a method described in detail below, the input signal $K(x)$ of the phase accumulator 3 of the phase accumulator 3 based on a digital signal x represented by a function of two further digital signals Dif-int and Dif-frac representing the integer part and the fractional part of the detected phase difference $\Delta\varphi$, respectively, and outputs the calculating data to the phase accumulator 3 to implement accumulation. The clock frequency of the phase sampling circuit 105 is the frequency of the clock signal *Fmclk* synchronized by a local high-speed crystal oscillator *Clk*58m. *Fmclk* is a sampling clock signal which appears at a specific position of the frame head for each frame. The phase accumulator 3 accumulates the output signal $K(x)$ of the LF 2 on each rising clock edge of the clock signal *Clk*58m supplied by the local high-speed crystal oscillator. Carry bit of addition is overflow automatically. Addition sum is stored to the register group variable *Sum*(23:0) at each rising clock edge of *Clk*58m. The accumulated phase values stored in the most significant bit *Sum*(23) of the digital signal supplied by the phase accumulator 3 represents the local recovery clock signal *Rclk*.

The LF 2, i.e. a filtering operational module of a PLL, implements operational function for calculating the accumulated signal $K(x)$ and adjusts the local recovery clock signal frequency f_{rec} at the output port of the phase accumulator 3. The operational method is as follow.

First, an address difference reference offset x_0 representative of said phase difference reference value $\Delta\varphi_{ref}$ is set to half the bit depth L of the first-in-first-out memory (FIFO) for defining a phase difference reference value $\Delta\varphi_{ref}$ representing a nominal value of the difference $\Delta\varphi$ between the phase φ_{ref} of the input clock signal Wclk and the phase φ_{rec} of the local recovery clock signal Rclk . In this embodiment, bit depth L of the FIFO is 128bit, so the address difference reference offset x_0 can be set to x_0 :=L/2=128 bit /2= 64bit.

The subtracter module 104 calculates the phase difference $\Delta\varphi$ between the input clock signal phase φ_{ref} and the local recovery clock signal phase φ_{rec} according to output signal Waddr(6:0)of the write address counter 102 and output signal Raddr(6:0) of the read address counter 103, and the calculating result *Dif-int*0, after being submitted to a sampling procedure with the clock signal Fmclk, is sent to the LF 2 as a digital signal *Dif-int* representing an integer part of the phase difference $\Delta\varphi$. Write clock of the FIFO 101 is the input clock signal *Wclk* having been synchronized by the local high-speed crystal oscillator clock signal *Clk*58m, and read clock of the FIFO 101 is the local recovery clock signal *Rclk*. The phase accumulator 3 outputs to the phase sample circuit 105 a digital signal *Dif-fac*(2:0) constituted by the *Sum*(23:21) of the digital values stored in the three most significant bits of 24-bit register 302. The digital signal *Dif-fac*(2:0), after being submitted to a phase sampling procedure, is fed to the LF 2 as a fraction part of the phase difference representing signal x.

The LF 2, i.e. filtering operational module, calculates the accumulated signal $K(x)$ in segments according to a deviation of the detected phase reference $\Delta\varphi$ represented by the digital signal x (in bit) and a phase difference reference value φ_{ref} represented by an address difference reference offset x_0 of 64bit. when the deviation $|x - x_0|$ is large, the accumulated signal $K(x)$ follows x with a larger increment ΔK_m; when said deviation is small, the accumulated signal $K(x)$ follows x with a smaller increment ΔK_m. The accumulated signal $K(x)$ is outputted to the phase accumulator 3 for accumulation. Therefore, when the $|x - x_0|$ increases, the frequency of the local recovery clock signal *Rclk*, i.e. the most significant bit *Sum*(23), is changed towards the nominal ideal frequency 2.048MHz with a higher rate; otherwise, when $|x - x_0|$ decreases, the frequency of the local recovery clock signal *Rclk* is changed towards the nominal ideal frequency 2.048MHz with a lower rate.

In the embodiment, the LF 2 applies seven increments Δk_1 to Δk_7 and four coefficients α_1 to α_4 to an algorithm used for calculating the phase accumulator input signal $K(x)$ according to the magnitude and the algebraic sign of a measured deviation $(x - x_0)$ representing a deviation of the detected phase difference $\Delta\varphi$ from the phase difference reference value $\Delta\varphi_{ref}$, wherein said algorithm with seven increments and four coefficients can be given by the following function:

$$K(x) := K_0 + \Delta S_m(x) = K_0 + \sum_{\mu=1}^{m} \Delta K_\mu(x) \quad [bit] \quad for \quad m \in \{1,2,\cdots,7\} \quad (1a)$$

with $K_0 = K(x = x_0) \quad [bit] \quad (1b)$

and

$$\Delta S_m(x) := \begin{cases} -\Delta x \cdot \sum_{\mu=0}^{3-m} \alpha_\mu - (m \cdot \Delta x - x) \cdot \alpha_{3-m+1}, & (m-1) \cdot \Delta x < x \le m \cdot \Delta x, \quad m \in \{1,2,3\} \\ (x - x_0) \cdot \alpha_0, & (m-1) \cdot \Delta x < x \le (m+1) \cdot \Delta x, \quad m = 4 \\ \Delta x \cdot \sum_{\mu=0}^{m-5} \alpha_\mu + (x - m \cdot \Delta x) \cdot \alpha_{m-5+1}, & m \cdot \Delta x < x \le (m+1) \cdot \Delta x, \quad m \in \{5,6,7\} \end{cases}$$

$$= \begin{cases} -16 \cdot \sum_{\mu=0}^{2} \alpha_\mu - (16 - x) \cdot \alpha_3 & \text{for} \quad 0 < x \le 16 \\ -16 \cdot \sum_{\mu=0}^{1} \alpha_\mu - (32 - x) \cdot \alpha_2 & \text{for} \quad 16 < x \le 32 \\ -16 \cdot \alpha_0 - (48 - x) \cdot \alpha_1 & \text{for} \quad 32 < x \le 48 \\ (x - 64) \cdot \alpha_0 & \text{for} \quad 48 < x \le 80 \\ 16 \cdot \alpha_0 + (x - 80) \cdot \alpha_1 & \text{for} \quad 80 < x \le 96 \\ 16 \cdot \sum_{\mu=0}^{1} \alpha_\mu + (x - 96) \cdot \alpha_2 & \text{for} \quad 96 < x \le 112 \\ 16 \cdot \sum_{\mu=0}^{2} \alpha_\mu + (x - 112) \cdot \alpha_3 & \text{for} \quad 112 < x \le 128 \end{cases} \quad [bit] \quad (1c)$$

with $\Delta x := 16 bit$ and $x_0 = 4 \cdot \Delta x = 64 bit$, wherein

$$x(n \cdot T_S) := \beta_1 \cdot \underbrace{\Delta A_{WR}(n \cdot T_S)}_{=:Dif-\mathrm{int}} + \beta_2 \underbrace{\sum_{\substack{l=L_S \\ (c \neq 0)}}^{L_{REG}-1} K(x((n-l) \cdot T_S)) \cdot c_l^{-1}}_{=:Dif-frac} + x_0 \quad [bit] \quad (1d)$$

with $\Delta A_{WR}(n \cdot T_S)$ being address difference Dif-int0, β_1 and β_2 being real-valued spreading factors used for spreading the obtained values for Dif-int and Dif-frac (here: $\beta_1 = \beta_2 := 1$),

$$c_l := b_l \cdot 2^l \quad \forall \quad l \in \{0,1,2,\cdots,L_{reg}-1\} \quad (1e)$$

being the respective frequency divider coefficient given by the binary value ('0' or '1') stored in the l-th bit cell of register 302, which follows from the fact that a digital value represented by a bit sequence $B := (b_0, b_1, \cdots, b_l, \cdots, b_{L_{reg}})$ which is stored in said register 302 is representative of a sequence of frequency divider coefficients c_l which can be written in the form

$$C := (c_0, c_1, \cdots, c_l, \cdots, c_{L_{reg}}) = (b_0, b_1 \cdot 2^1, \cdots, b_l \cdot 2^l \cdots, b_{L_{reg}} \cdot 2^{L_{reg}}), \quad (1f)$$

$L_{reg} := 24\, bit$ being the bit depth of register 302, L_s being the index of the L_s-th bit cell of said register 302,

$$x_0 := \frac{L}{2} \quad [bit] \quad (1g)$$

being the address difference reference offset and, finally, L being the bit depth of first-in-first out memory 101 denotes a digital signal being a function of two further digital signals Dif-int and Dif-frac which are representative of the integer part and the fractional part of the detected phase difference $\Delta\varphi$, respectively, said function containing a shift of the obtained address difference signal by the address difference reference offset x_0, K_0 is a digital reference value of phase accumulator input signal $K(x)$ supplied by the LP 2 when the detected phase difference $\Delta\varphi$ is equal to the phase difference reference value $\Delta\varphi_{ref}$, K_0 being calculated dependent on the frequency f_{rec} of the local recovery clock signal *Rclk*, the frequency f_{LO} of the local crystal oscillator signal and the bit depth L_{reg} of register 302, which is obtained when x is equal to x_0, and m is the index of said increments ΔK_m. The accumulated input signal $K(x)$ in each segment follows the detected phase difference $\Delta\varphi$ with a continuous, piecewise linear and strictly monotonously rising function, said function featuring the four segment slope factors $\alpha_0, \alpha_1, \alpha_2, \alpha_3 \in R$, respectively, and α_0, α_1, α_2 and α_3 obeying the inequation

$$\alpha_0 < \alpha_1 < \alpha_2 < \alpha_3 \quad (2)$$

Thereby, said segment slope factors α_0, α_1, α_2 and α_3 are respectively set to the following values: $\alpha_0 = 1$, $\alpha_1 = 2$, $\alpha_2 = 3$, $\alpha_3 = 4$.

According to the above-described embodiment of the present invention, the phase accumulator input value K_0 supplied by LF 2 in case x is equal to x_0 is given by the following equation:

$$K_0 := \left\lceil \frac{f_{rec}}{f_{LO}} \cdot 2^{L_{reg}} \right\rceil = \left\lceil \frac{2.048MHz}{58.32MHz} \right\rceil \cdot 2^{24} = 589{,}159 \quad (3)$$

Because in the embodiment the bit depth L of the FIFO 101 is 128bit, x can take values from a range between 0 and 128 bit.

Figure 3 shows that the accumulated input signal $K(x)$ is a continuous, piecewise linear and strictly monotonously rising function of digital x. At segments where x deviates farthest from x_0=64bit, such as 0~16bit and 112~128bit segments, having the steepest slope factor of the segments, the accumulated signal $K(x)$ follows x with largest increments ΔK_m, from which it follows that frequency f_{rec} of the local recovery clock signal Rclk is adjusted to a nominal frequency given by the clock frequency f_{ref}=2.048MHz of input clock signal Wclk with the fastest changing rate. At segments where x deviates largely from x_0=64bit, such as 16~32bit and 96~112bit, where the slope factors of the segments is relatively steep, the accumulated signal $K(x)$ follows x with relatively large increments ΔK_m, compared with the increment values at other segments, which implies that the f_{rec} is adjusted to f_{ref}= 2.048MHz with a relatively fast changing rate. By contrast, at segments where x deviates less from x_0=64bit, such as 32~48bit and 80~96bit, where the slope factors of the segments are relatively small, the accumulated signal $K(x)$ follows x with relatively small increments ΔK_m, compared with the increment values at other segments, which leads to the fact that the f_{rec} is adjusted to f_{ref}=2.048MHz with a relatively slow changing rate. Finally, at segment where the magnitude of the deviation $(x-x_0)$ is features a minimum, such as 48~80 bit having the smallest slope factor of all segments, the accumulated signal $K(x)$ follows x with the smallest increment ΔK_m, from which it follows that the f_{rec} is adjusted to f_{ref}=2.048MHz with slowest changing rate. In this way, $K(x)$ is implemented without error code, and at the same time, vibration minimization is also concerned, so DPLL vibration tolerance is better raised, vibration transfer characteristic is enhanced and net output vibration indicators at low-band and high-band frequencies are improved. In the embodiment, when reference clock frequency is 20Hz, vibration tolerance is 60UI (unit of issue) and vibration suppression characteristic is higher than -30db; when reference clock frequency is 2018KHz, net output vibration is less than 0.1UI; and when reference clock frequency is 18100KHz, net output vibration is 0.035UI in general.

Any revision, equivalence replacement and improvement etc. within the spirit and principle of the invention must be all included in the appended Claims of the invention.

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CLAIMS:

1. A filtering method for digital Phase Lock Loop, comprising:

defining a phase difference value ($\Delta\varphi_{\text{ref}}$) representing a nominal value of the difference ($\Delta\varphi$) between the phase (φ_{ref}) of an input clock signal (*Wclk*) and the phase (φ_{rec}) of a local recovery clock signal (*Rclk*) by setting an address difference reference offset (x_0) representative of said phase difference reference value ($\Delta\varphi_{\text{ref}}$) to half the bit depth (L) of a first-in-first-out memory (101);

calculating a read/write address difference (Dif-int0) which denotes a bit position difference in a data stream of content data between an input data pointer (P_W) and an output data pointer (P_R) indicating the starting addresses of contents data (Wdata) written to and contents data (Rdata) read from the first-in-first-out memory (101), respectively, said read/write address difference (Dif-int0) being representative of a detected phase difference ($\Delta\varphi$) between the input clock signal (*Wclk*) and the local recovery clock signal (*Rclk*);

comparing the detected phase difference ($\Delta\varphi$) with the phase difference reference value ($\Delta\varphi_{\text{ref}}$); and

adjusting the local recovery clock signal (*Rclk*) in segments to the phase difference reference value ($\Delta\varphi_{\text{ref}}$), wherein a correction signal ($K(x)$) used for adjusting the local recovery clock signal (*Rclk*), said correction signal ($K(x)$) being representative of a change in the detected phase difference ($\Delta\varphi$), is increased or decreased segment by segment depending on the magnitude and the algebric sign of a detected deviation of the detected phase difference ($\Delta\varphi$) from the phase difference reference value ($\Delta\varphi_{\text{ref}}$),

wherein

said correction signal ($K(x)$) is calculated based on a digital signal (x) which, compared with said read/write address difference (Dif-int0), is representative of a more precise representation of the detected phase difference ($\Delta\varphi$), said digital signal (x) being a function of two futher digital signals (Dif-int and Dif-frac) representing an integer part and a fractional part of the detected phase difference ($\Delta\varphi$), respectively.

2. The method according to Claim 1, wherein the digital signal (Dif-int) representing the integer part of the detected phase difference ($\Delta\varphi$) is given by the read/write address difference (Dif-int0) and the digital signal (Dif-frac) representing the fractional part of the detected phase difference ($\Delta\varphi$) is given by a particular increment (ΔK_m) of said correction signal ($K(x)$) or by a partial sum of said increments (ΔK_m).

3. The method according to Claim 2, wherein the first-in-first-out memory (101) receives a write address signal (*Waddr*) and a read address signal (*Raddr*), the write address signal (*Waddr*) being a counter output value which is representative of the clock frequency of the input clock signal (*Wclk*) synchronized with a local crystal oscillator clock signal (*Clk58m*) and the read address signal (*Raddr*) being a further counter output value which is representative of the clock frequency (f_{rec}) of the local recovery clock signal (*Rclk*).

4. The method according to Claim 3, wherein the step of adjusting the local recovery clock signal (*Rclk*) in segments comprises:

sampling (105) the detected phase difference ($\Delta\varphi$);

calculating (2) the increments (ΔK_m) of a phase accumulator input signal ($K(x)$) which is used for adjusting the phase (φ_{rec}) of the local recovery clock (*Rclk*) based on a deviation of a sampled time-domain signal representing the detected phase difference ($\Delta\varphi$) from the phase difference reference value ($\Delta\varphi_{ref}$) such that in case said deviation increases the step size of said increments (ΔK_m) is set to a larger value, wheeas in case said deviation decreases the step size of said increments (ΔK_m) is set to a smaller value, said increments (ΔK_m) being a function of the sampled time-domain signal representing the detected phase difference ($\Delta\varphi$);

accumulating (301) the increments (ΔK_m); and

calculating (302) the local recovery clock signal (*Rclk*) by controlling the divider coefficient of a digital frequency divider (302) used for dividing a frequency (f_{LO}) of the local crystal oscillator clock signal (*Clk58m*) such that in case said deviation increases an offset rate used for adjusting the phase (φ_{rec}) of the local recovery clock signal (*Rclk*) to the phase (φ_{ref}) of the input clock signal (*Wclk*) is set to a larger value, whereas in case said deviation decreases said offset rate is set to a smaller value, said offset rate being a cumulative function of digital signals which are representative of the frequency (f_{LO}) of said local crystal oscillator clock signal (*Clk58m*) divided by different divider coefficients stored in the digital frequency divider (302).

5. The method according to claim 4, wherein the steps of accumulating (301) said increments (ΔK_m) and calculating (302) said local recovery clock signal (*Rclk*) are performed by means of a phase accumulator (3) comprising an adder (301) and a register (302) supplied with a signal being representative of the frequency (f_{LO}) of the local crystal oscillator clock signal (*Clk58m*).

6. The method according to Claim 5, wherein the step of sampling (105) the detected phase difference ($\Delta\varphi$) is performed by means of a phase sampling circuit (105) supplied with a sampling clock signal (*Fmclk*) which is synchronized by the local crystal oscillator clock signal (*Clk58m*).

7. The method according to Claim 6, wherein the phase accumulator input signal ($K(x)$) is a continuous, piecewise linear and strictly monotonously rising function of the digital signal (x) which is representative of the more precise representation of the detected phase difference ($\Delta\varphi$).

8. The method according to Claim 7, wherein the bit depth (L) of the first-in-first-out memory (101) is 128bit and the phase difference reference value ($\Delta\varphi_{\text{ref}}$) is represented by an address difference offset (x_0) of 64bit.

9. The method according to Claim 8, wherein in the step of calculating (2) increments of a phase accumulator input signal, applying seven segments Δk_1 to Δk_7 and four coefficients α_1 to α_4 to an algorithm used for calculating the phase accumulator input signal ($K(x)$) according to the deviation of the sampled time-domain signal representing the phase difference ($\Delta\varphi$) from the phase difference reference value ($\Delta\varphi_{\text{ref}}$), it is represented with function:

$$K(x) := K_0 + \Delta S_m(x) = K_0 + \sum_{\mu=1}^{m} \Delta K_\mu(x) \quad [bit] \quad for \quad m \in \{1,2,\cdots,7\}$$

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with $K_0 = K(x = x_0)$ $[bit]$ and

$$\Delta S_m(x) := \begin{cases} -\Delta x \cdot \sum_{\mu=0}^{3-m} \alpha_\mu - (m \cdot \Delta x - x) \cdot \alpha_{3=m+1}, & (m-1) \cdot \Delta x < x \leq m \cdot \Delta x, \quad m \in \{1,2,3\} \\ (x - x_0) \cdot \alpha_0, & (m-1) \cdot \Delta x < x \leq (m+1) \cdot \Delta x, \quad m = 4 \\ \Delta x \cdot \sum_{\mu=0}^{m-5} \alpha_\mu + (x - m \cdot \Delta x) \cdot \alpha_{m-5+1}, & m \cdot \Delta x < x \leq (m+1) \cdot \Delta x, \quad m \in \{5,6,7\} \end{cases}$$

$$= \begin{cases} -16 \cdot \sum_{\mu=0}^{2} \alpha_\mu - (16 - x) \cdot \alpha_3 & \text{for} \quad 0 < x \leq 16 \\ -16 \cdot \sum_{\mu=0}^{1} \alpha_\mu - (32 - x) \cdot \alpha_2 & \text{for} \quad 16 < x \leq 32 \\ -16 \cdot \alpha_0 - (48 - x) \cdot \alpha_1 & \text{for} \quad 32 < x \leq 48 \\ (x - 64) \cdot \alpha_0 & \text{for} \quad 48 < x \leq 80 \quad [bit] \\ 16 \cdot \alpha_0 + (x - 80) \cdot \alpha_1 & \text{for} \quad 80 < x \leq 96 \\ 16 \cdot \sum_{\mu=0}^{1} \alpha_\mu + (x - 96) \cdot \alpha_2 & \text{for} \quad 96 < x \leq 112 \\ 16 \cdot \sum_{\mu=0}^{2} \alpha_\mu + (x - 112) \cdot \alpha_3 & \text{for} \quad 112 < x \leq 128 \end{cases}$$

$\Delta x := 16bit$ and $x_0 = 4 \cdot \Delta x = 64bit$, wherein, x (in bit) is a digital signal which is represented by a function of two further digital signals (Dif-int and Dif-frac) which are representative of the integer part and the fractional part of the detected phase difference ($\Delta\varphi$), K_0 denotes a digital reference value of the phase accumulator input signal ($K(x)$) which is obtained when the detected phase difference ($\Delta\varphi$) is equal to the phase difference reference value ($\Delta\varphi_{ref}$), K_0 being calculated dependent on the frequency (f_{rec}) of the local recovery clock signal (*Rclk*), the frequency (f_{LO}) of the local crystal oscillator signal (*Clk58m*) and the bit depth (L_{reg}) of said register (302), and m is the index of said increments (ΔK_m), and wherein the accumulated input signal ($K(x)$) in each segment follows the detected phase difference ($\Delta\varphi$) with a continuous, piecewise linear and strictly monotonously rising function, said function having the segment slope factors $\alpha_0, \alpha_1, \alpha_2, \alpha_3 \in R$, respectively, with α_0, α_1, α_2 and α_3 obeying the inequation $\alpha_0 < \alpha_1 < \alpha_2 < \alpha_3$.

10. The method according to Claim 9, wherein $\alpha_0 = 1$, $\alpha_1 = 2$, $\alpha_2 = 3$, $\alpha_3 = 4$.

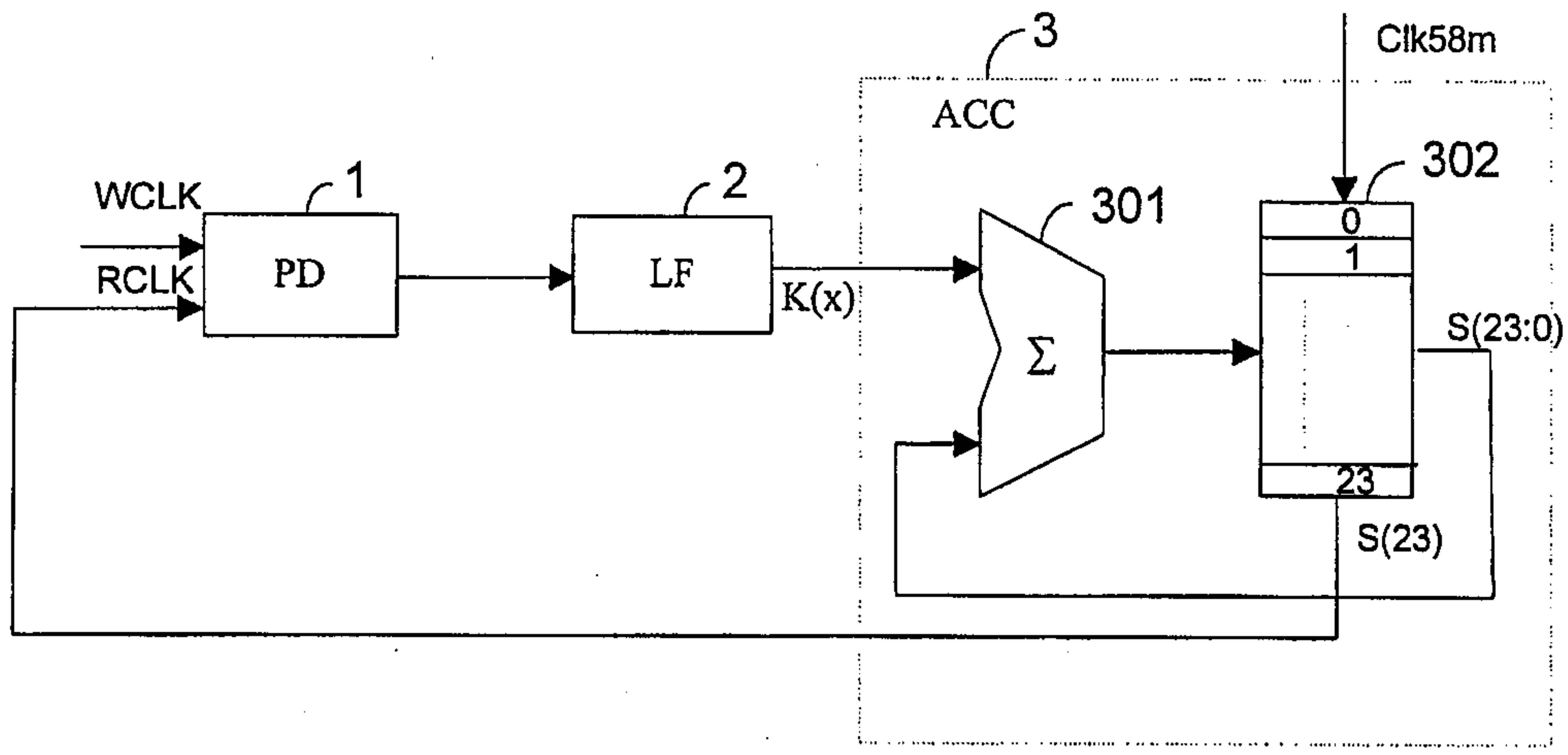


Figure 1

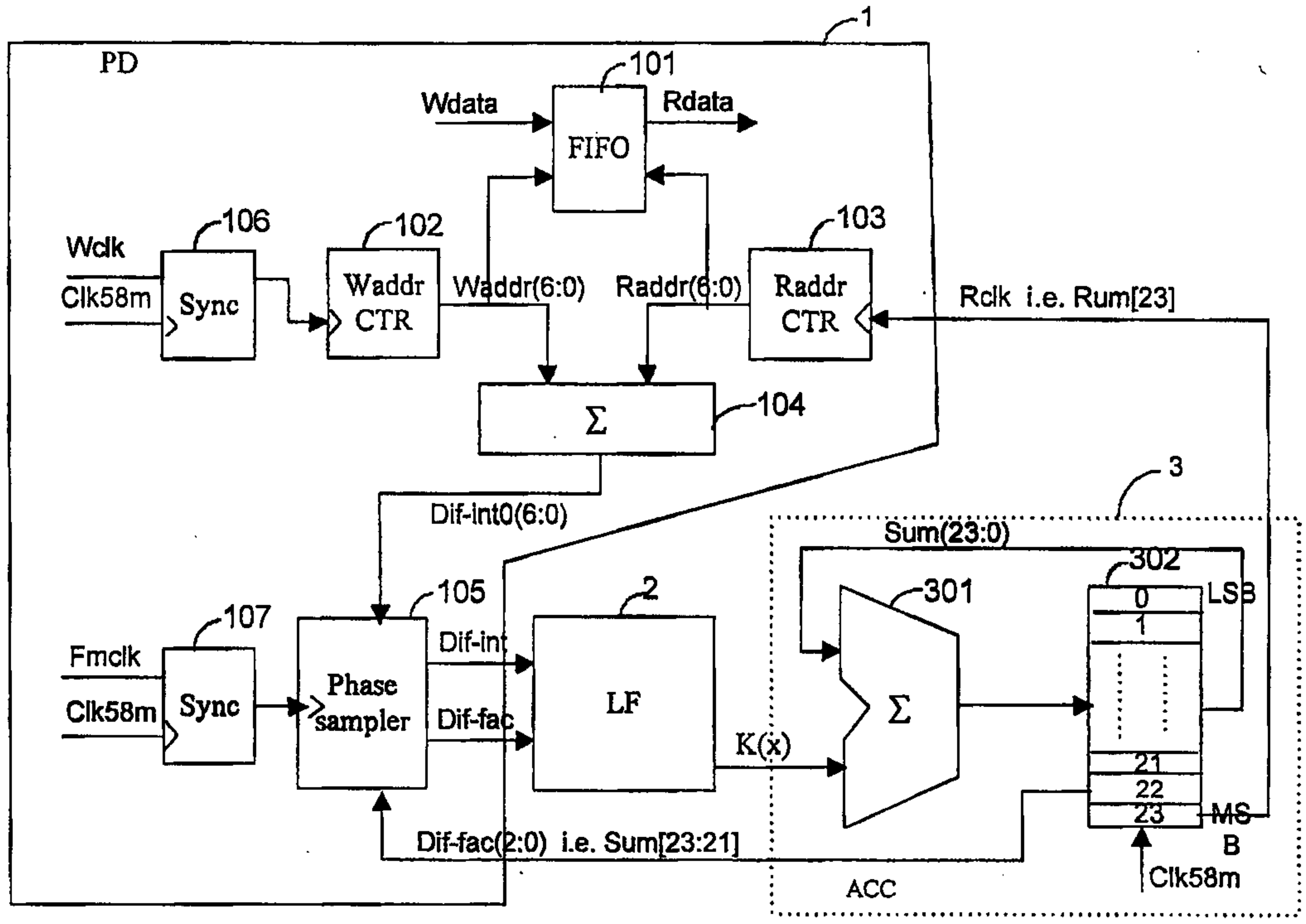

1
PD
101
Wdata
FIFO
Rdata
106
102
103
Wclk
Clk58m
Sync
Waddr CTR
Waddr(6:0)
Raddr(6:0)
Raddr CTR
Rclk i.e. Rum[23]
Σ
104
Dif-int0(6:0)
3
Sum(23:0)
302
105
2
301
107
0
LSB
1
Fmclk
Clk58m
Sync
Phase sampler
Dif-int
Dif-fac
LF
Σ
K(x)
21
22
23
MSB
Dif-fac(2:0) i.e. Sum[23:21]
ACC
Clk58m

Figure 2

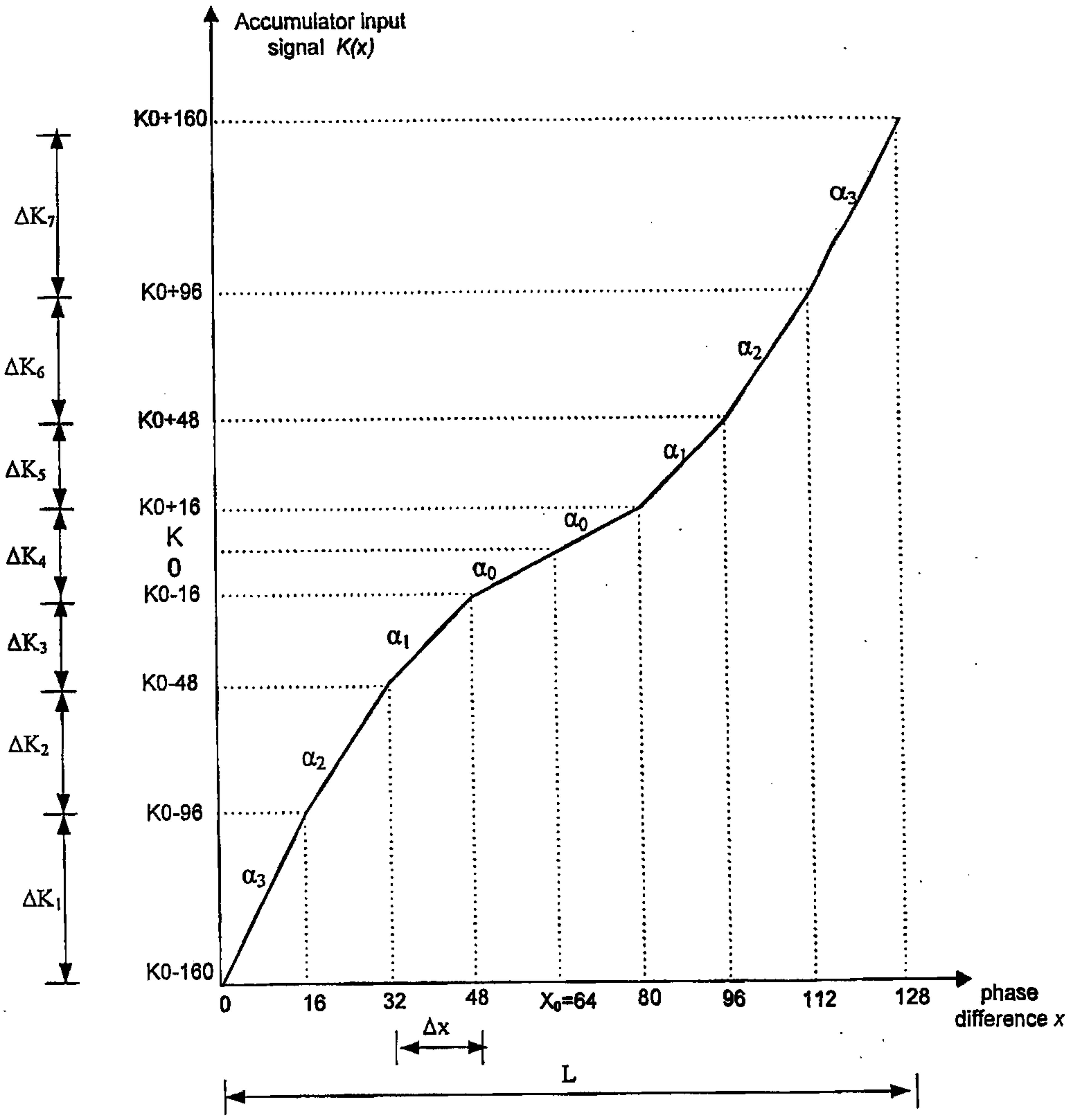
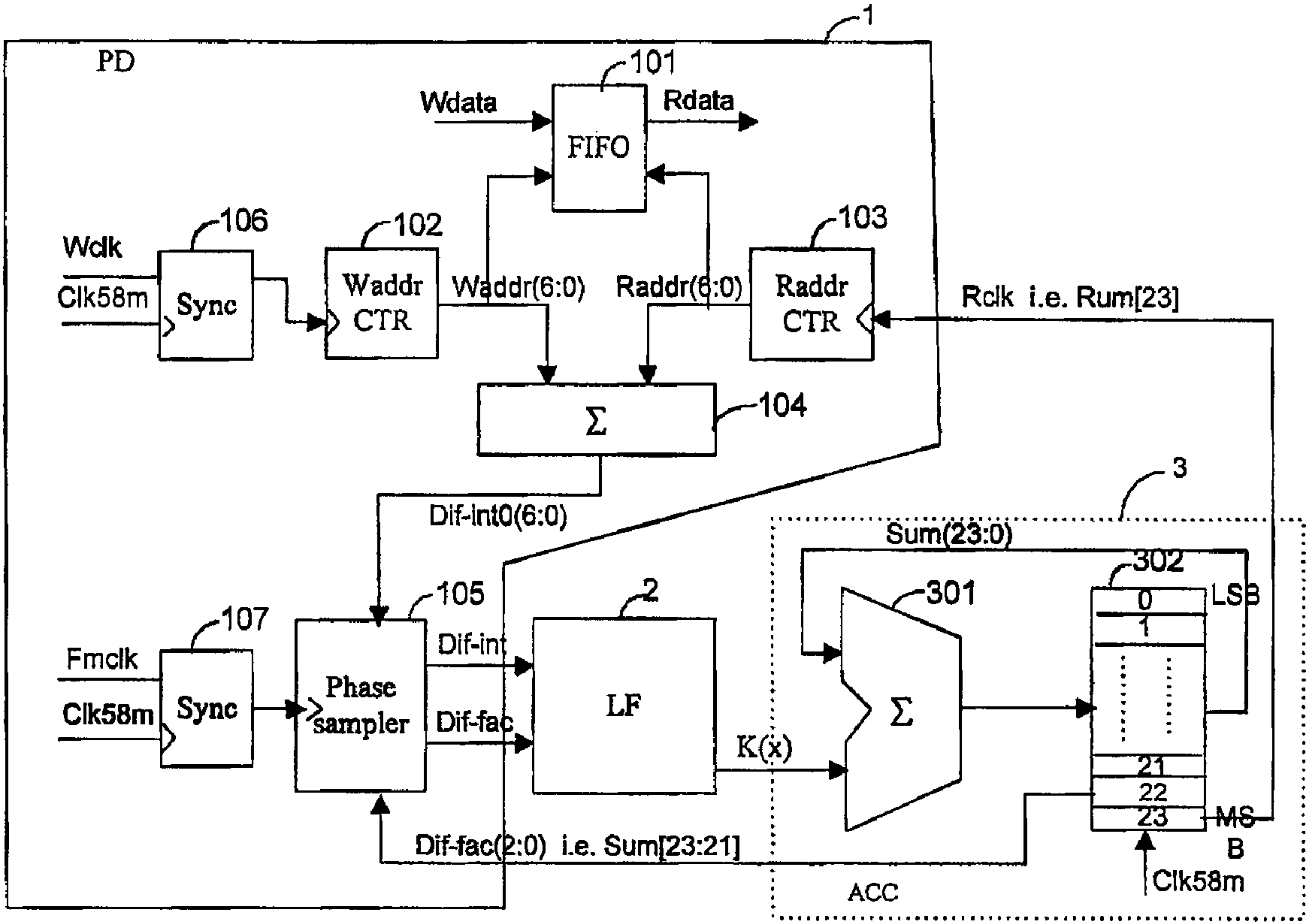

Accumulator input
signal K(x)
K0+160
K0+96
K0+48
K0+16
K
0
K0-16
K0-48
K0-96
K0-160
ΔK7
ΔK6
ΔK5
ΔK4
ΔK3
ΔK2
ΔK1
α3
α2
α1
α0
α0
α1
α2
α3
0
16
32
48
X0=64
80
96
112
128
phase
difference x
Δx
L

Figure 3


1
PD
101
Wdata
Rdata
FIFO
106
102
103
Wclk
Clk58m
Sync
Waddr
CTR
Waddr(6:0)
Raddr(6:0)
Raddr
CTR
Rclk i.e. Rum[23]
Σ
104
Dif-int0(6:0)
3
Sum(23:0)
302
301
105
2
0
LSB
1
107
Fmclk
Clk58m
Sync
Phase
sampler
Dif-int
Dif-fac
LF
K(x)
Σ
21
22
23
MSB
Dif-fac(2:0) i.e. Sum[23:21]
ACC
Clk58m