

GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ,
UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ,
TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK,
EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV,
MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,
TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW,
KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

AMBIPOLAR LAYER BASED ACCESS TRANSISTORS FOR MEMORY APPLICATIONS AND METHODS OF FABRICATION

5 TECHNICAL FIELD

[0001] Embodiments of the invention are in the field of integrated circuit fabrication and, in particular, ambipolar layer based transistors for memory applications and their methods of fabrication.

10 BACKGROUND

[0002] For the past several decades, the scaling of features in integrated circuits has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor chips. For example, shrinking transistor size allows for the incorporation of an
15 increased number of memory devices on a chip, lending to the fabrication of products with increased functionality. The drive for ever-more functionality, however, is not without issue. It has become increasingly significant to rely heavily on innovative fabrication techniques to meet the exceedingly tight tolerance requirements imposed by scaling.

[0003] Non-volatile embedded resistive memory integrated with transistors (1T-1R), for
20 example, on-chip embedded memory with non-volatility can enable energy and computational efficiency. Typically, a 1T-1R cell includes a transistor whose drain terminal is connected in series with a memory device. By biasing the transistor and the memory device appropriately, the resistance state of the memory device is toggled between high resistance state and low resistance state or vice versa enabling memory operation. However, inherent voltage losses due to
25 dedicated channel type in single MOS transistors creates inefficiencies during 1T-1R operations. Such inefficiencies can present formidable roadblocks to commercialization of this technology as devices continue to scale in size as well as with respect to voltage and current requirements. Thus, furthering development in the areas of integrating novel transistors that overcome limitations imposed by dedicated single MOS transistors is an integral part of the non-volatile
30 memory roadmap.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Figure 1 illustrates a cross-sectional view of a transistor with an ambipolar layer

and a resistive random access memory device formed on the drain contact of the transistor.

[0005] Figures 2A-2I illustrate cross-sectional views representing various operations in a method of fabricating a transistor with an ambipolar layer and an RRAM coupled to the drain of the transistor in accordance with embodiments of the present invention.

5 [0006] Figure 2A illustrates a cross-sectional view of an ambipolar layer formed on an insulator layer formed above a substrate.

[0007] Figure 2B illustrates the structure of Figure 2A following the formation of a gate dielectric layer on the ambipolar layer and a gate electrode on the gate dielectric layer. Figure 2A illustrates a conductive interconnect surrounded by a first dielectric layer.

10 [0008] Figure 2C illustrates the structure of Figure 2B following the deposition of a dielectric layer.

[0009] Figure 2D illustrates the structure of Figure 2C following the formation of a drain contact in the drain region.

[0010] Figure 2E illustrates the structure of Figure 2D following the deposition of various materials layers to form an RRAM device on the drain contact.

15 [0011] Figure 2F illustrates the structure of Figure 2E following the formation of an RRAM device on the drain contact.

[0012] Figure 2G illustrates the structure of Figure 2F following the deposition of a second dielectric layer and a planarization process.

20 [0013] Figure 2H illustrates the structure of Figure 2G following the formation of a contact on the RRAM device.

[0014] Figure 2I illustrates the structure of Figure 2H following the formation of a source contact on the source region and a gate contact on the gate electrode of the transistor. Figure 3H

[0015] Figure 3A-3D illustrates an ambipolar layer based transistor fabricated by a replacement gate process in accordance with an embodiment of the present invention.

25 [0016] Figure 3A illustrates the structure of Figure 2C following an extended planarization process that exposes the hardmask and a subsequent process to remove the hardmask and the dummy gate stack.

[0017] Figure 3B illustrates the structure of Figure 3A following a deposition of a functional gate dielectric layer and a functional gate electrode.

30 [0018] Figure 3C illustrates the structure of Figure 3B following the deposition of an interlayer dielectric film (ILD) followed by the formation of source contact, a drain contact.

[0019] Figure 3D illustrates the structure of Figure 3C following the process operations described in connection with Figures 2E – 2I to form an RRAM device, dielectric spacers, a contact electrode, a gate contact and a source electrode.

[0020] Figure 4A-4C illustrate various biasing schemes on the source region, on the gate electrode, and on the RRAM top electrode to cycle the RRAM device and associated current-voltage traces of the RRAM device resulting from such biasing.

[0021] Figure 4A illustrates biasing conditions to perform a RESET event in the RRAM device and associated current-voltage trace.

[0022] Figure 4B illustrates biasing conditions to perform a SET event in the RRAM device and associated current-voltage trace.

[0023] Figure 4C illustrates biasing conditions to perform a READ event in the RRAM device and associated current-voltage trace.

[0024] Figure 5 illustrates a block diagram of an electronic system, in accordance with embodiments of the present invention.

[0025] Figure 6 illustrates a computing device in accordance with embodiments of the present invention.

DESCRIPTION OF THE EMBODIMENTS

[0026] An ambipolar layer based access transistor for memory applications and their methods of fabrication are described. In the following description, numerous specific details are set forth, such as novel structural schemes and detailed fabrication methods in order to provide a thorough understanding of embodiments of the present invention. It will be apparent to one skilled in the art that embodiments of the present invention may be practiced without these specific details. In other instances, well-known features, such as transistor operations and switching operations associated with embedded memory, are described in lesser detail in order to not unnecessarily obscure embodiments of the present invention. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

[0027] Integrating a memory array with low voltage logic circuitry, such as logic circuitry operational at a voltage less than or equal to 1 Volt, may be advantageous since it enables higher operation speeds compared to having physically separate logic and memory chips. As transistor operating voltages are scaled down in an effort to become energy efficient, a memory device that is connected in series with a transistor, to form a 1T-1R cell, is also required to function at lower voltages and currents. A 1T-1R cell typically utilizes a conventional metal oxide semiconductor (MOS) transistor. By appropriately biasing the gate, source and drain terminals of the MOS transistor, the resistance state of the memory device is toggled between high resistance state and low resistance state or vice versa, in a process known as resistance switching. By switching direction of the current flow through the transistor and the

memory cell resistance switching is accomplished in a memory device. This in turn is accomplished by changing the bias on the respective terminals of the 1T-1R cell. Depending on the biasing condition the memory device is sometimes effectively connected to the drain end of a transistor and at other times connected to the source end. When the memory device is connected to the source end of the transistor the 1T-1R cell is said to be in a source follower configuration. In a source follower configuration, the gate to source voltage, V_{GS} , is effectively decreased from the power supply voltage because of the presence of the load resistor. Reduction in V_{GS} , therefore, reduces the effective transistor drive current, I_D . In the non-source follower configuration, the gate to source voltage, V_{GS} , is the same as the power supply voltage as there is no load in series at the source terminal. As a result, an asymmetry in current in the 1T-R cell results when the memory device is cycled. Typically, since resistance changes in a memory device are voltage driven during one part of the switching cycle and current driven in another, reduction in current during cycling is highly undesirable. One way to mitigate this effect is to increase the power supply voltage, V_{cc} , of the transistor during a portion of the cycling until that the current threshold required to switch the memory device is met. However, increasing V_{cc} , also increases power requirement. For a given channel type (N or P), the asymmetry in the gate to source voltage, V_{GS} , during resistance switching is a fundamental problem in both NMOS or PMOS transistors. Because of the fixed majority charge carrier in each MOS type, it is not possible to reverse the voltage polarity on the gate to avoid a source follower configuration during a portion of the switching cycle. However, by implementing a 2-dimensional (2D) material such as an ambipolar layer, a transistor channel may be able to conduct both electrons and holes enabling direction of the current flow in the 1T-1R cell to be reversed in a single switching cycle. In one such transistor, the sign of the majority carrier can be dictated by changing the polarity of the applied voltage on the gate and on the drain terminals of the transistor as will be discussed further below. A 1T-1R cell fashioned with one such transistor including an ambipolar layer may be able to operate in non-source follower mode during the entire switching cycle with no appreciable reduction in current flow. Adverse effects arising from reduction in available current flow in the 1T-1R cell may be avoided.

[0028] In accordance with embodiments of the present invention, a 1T-1R memory cell includes a transistor structure where an ambipolar layer is disposed on an insulator layer formed on a substrate. The ambipolar layer may include a material such as but not limited to transition metal dichalcogenide (TMDC) layer, a carbon nanotube (CNT) or a pentacene layer. Similar to a traditional FET, the transistor further includes a gate dielectric layer that is disposed on the ambipolar layer and a gate electrode disposed on the gate dielectric layer. A source region and a drain region are disposed on the ambipolar layer. The source region is separated from the drain

region by the gate electrode. A source contact is disposed on the source region and a drain contact disposed on the drain region. In an embodiment, the source contact and the drain contact include an adhesion layer that can also improve the contact resistance and improve carrier conduction by reducing the Schottky barrier height. A transistor fashioned from an ambipolar layer exhibits several properties that makes it highly desirable for low power transistor applications, namely (a) large ON-OFF current ratio ($>10^8$) resulting in significantly reduced off-state leakage and (b) lack of mobility dependence at high gate fields.

[0029] The 1T-1R cell further includes a memory device that is disposed above the drain contact of the transistor. The memory device belongs to a class of memory devices that is based on resistive switching. That is, the state of the memory device corresponds to state where the device is in a high resistance state or a low resistance state. Some examples of memory devices that exhibit resistive switching include metal oxide resistive random access memory (RRAM), conductive bridge resistive random access memory (CBRAM) and spin transfer torque memory (STTM). Additionally, depending on embodiments, the memory device may be directly disposed on the drain contact or connected to the drain contact by a series of copper interconnects having negligible line resistance.

[0030] Figure 1 illustrates a 1T-1R cell 100 in accordance with an embodiment of the present invention. The 1T-1R cell 100 includes a transistor 101 disposed on a semiconductor substrate 102 and a memory device 124 coupled with the transistor 101. The transistor 101 includes an ambipolar layer 104 disposed on an insulator layer 106. The insulator layer 106 is disposed on the substrate 102. A portion of the ambipolar layer 104 forms a channel of the device. A gate dielectric layer 108 is disposed on the channel portion of the ambipolar layer 104. A gate electrode 110 is disposed on the gate dielectric layer 108. A source region 112 and a drain region 114 are disposed on the ambipolar layer 104. The source 112 region is separated from the drain region 114 by the gate electrode 110. A source contact 116 is disposed on the ambipolar layer 104 in the source region 112 and a drain contact 118 is disposed on the ambipolar layer 104 in the drain region 114. A gate contact 120 is disposed on the gate electrode 110.

[0031] The ambipolar layer 104 may include a material such as but not limited to transition metal dichalcogenide (TMDC) layer, a carbon nanotube (CNT) or a pentacene layer. In an embodiment, the ambipolar layer 104 is a TMDC layer. In one such embodiment, the TMDC layer has a chemical composition, MX_2 , where M is a transition metal and X is a chalcogen. In an embodiment, the transition metal, M, is selected from a group consisting of molybdenum, tungsten and chromium, and the chalcogen, X, is selected from a group consisting of sulfur, selenium and tellurium. In an embodiment the TMDC layer is WSe_2 . The TMDC is typically an atomically uniform film having a thickness ranging between 0.2 – 2nm. In an

embodiment, the TMDC layer has a thickness that is 0.5nm. The TMDC layer has a direct bandgap that is at least 1.8 eV and facilitates transport of both holes and electrons. Depending on the material composition of the TMDC layer, the electron and hole mobility can range from approximately 30-200 cm² V⁻¹ s⁻¹. Such a range is within an order of magnitude of the maximum electron and hole mobility in silicon.

[0032] In an embodiment, the gate dielectric layer 108 includes a material such as, but not limited to silicon oxide, silicon dioxide (SiO₂), silicon nitride or a high-k dielectric material. The high-k dielectric material may include oxides such as but not limited to hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide or titanium oxide. Another example of TMDC compatible gate dielectric layer 108 includes a material such as hexagonal boron nitride. In an embodiment, the gate dielectric layer 108 has a thickness that ranges between 0.5nm – 2nm.

[0033] In an embodiment, the transistor 101 includes a gate electrode 110 with a workfunction in the range of 3.8 eV -4.5 eV. Similar to traditional MOSFET, the workfunction of gate electrode 110 in transistor 101 is tuned to optimize threshold voltage. For an ambipolar layer 104, gate workfunction optimization includes having to optimize for both electron and hole transport to accomplish current flow in directions from drain to source and vice versa. In an embodiment, the gate electrode 110 includes metals such as palladium or gold or a metal alloy such as TiN. In some implementations, the gate electrode 110 may consist of a stack of two or more conductive layers, where a first conductive layer that is directly disposed on the ambipolar layer 104 sets the workfunction of the gate electrode 110, and the remaining one or more conductive layers include fill layers.

[0034] In an embodiment, the source contact 116 and drain contact 118 includes a material such as but not limited to tungsten, titanium, gold, scandium or graphene. In some implementations, the source contact 116 and drain contact 118 may include a contact adhesion layer. In some implementations, the contact adhesion layer is chosen to minimize barrier height for optimizing electron and hole conduction between source and drain contacts 116 and 118 and the source and drain regions 112 and 114, respectively, of the ambipolar layer 104. Examples of such adhesion layers include Ti or Ni. The thickness of the adhesion layer can range from 3-10nm.

[0035] In an embodiment, the substrate 102 includes a semiconductor material such as but not limited to silicon, silicon germanium (Ge) or silicon carbide (SiC). In an embodiment, insulator layer 106 includes a material such as, but not limited to silicon dioxide (SiO₂), carbon doped oxide (CDO), silicon nitride. In an embodiment, the insulator layer 106 has a thickness in the range of 30nm-200nm. In an embodiment, the dielectric layer 122 includes a material such

as but not limited to silicon dioxide, silicon carbide or carbon-doped silicon oxide.

A memory device 124 is disposed on the drain contact 118 of the transistor 101. The memory device may include a metal oxide resistive random access memory (RRAM) element, a conductive bridge resistive random access memory (CBRAM) element or a spin transfer torque memory (STTM) element. In an embodiment, the memory device 124 is a resistive random access memory (RRAM) device as is illustrated in Figure 1. In one such embodiment, the RRAM device includes a bottom electrode 126 disposed on the drain contact 118, a metal oxide switching layer 128 disposed above the bottom electrode 126 and a top electrode 132 disposed above the switching layer 128. In an embodiment, the RRAM device includes an oxygen exchange layer 130. The oxygen exchange layer 130 may be disposed between the bottom electrode 126 and the metal oxide switching layer 128, as is illustrated in Figure 1, or between the metal oxide switching layer 128 and the top electrode 132 in a different embodiment. In an embodiment, a dielectric spacer 134 is disposed laterally adjacent and on sidewalls of the RRAM device and on the dielectric layer 122. The dielectric spacer 134 extends from the bottom of the bottom electrode layer 126 to an upper most surface of the top electrode 132 and is designed to prevent oxidation of the oxygen exchange layer 130. A contact electrode 136 is disposed in the dielectric layer 122 and on a portion of the top electrode 132. The RRAM device may have a width that is larger or smaller than the width of the drain contact 118.

[0036] In an embodiment, the bottom electrode 126 includes a material such as but not limited to titanium nitride, tantalum, tantalum nitride, tungsten or ruthenium. In an embodiment, the bottom electrode 126 has a thickness in the range of 40 to 100 nanometers (nm). Typically for RRAM applications the composition and thickness of the bottom electrode 126 are tuned to meet specific device attributes such as series resistance, programming voltage and current. In an embodiment, a monolayer portion of the bottom electrode 126 at an interface between the bottom electrode 126 and the metal oxide switching layer 128 is oxidized but remains conductive. In one such embodiment, the bottom electrode 126 includes tungsten or ruthenium.

[0037] In an embodiment, the metal oxide switching layer 128 is composed of a metal (M), such as but not limited to, hafnium, tantalum or titanium. In the case of titanium or hafnium, or tantalum with an oxidation state +4, the metal oxide switching layer 128 has a chemical composition, MO_X , where O is oxygen and X is or is substantially close to 2. In the case of tantalum with an oxidation state +5, the metal oxide switching layer 128 has a chemical composition, M_2O_X , where O is oxygen and X is or is substantially close to 5. In an embodiment, the metal oxide layer 128 has a thickness in the range of 1-5 nm.

[0038] In an embodiment, the oxygen exchange layer 130 acts as a source of oxygen vacancy or as a sink for O^{2-} . In an embodiment the oxygen exchange layer 130 is composed of a

metal such as but not limited to, hafnium, tantalum or titanium. In an embodiment, oxygen exchange layer 130 has a thickness in the range of 5-20nm. In an embodiment, the thickness of the oxygen exchange layer 130 is at least twice the thickness of the metal oxide switching layer 126. In another embodiment, the thickness of the oxygen exchange layer 130 is at least twice the thickness of the metal oxide switching layer 128.

[0039] In an embodiment, the top electrode 132 is composed of a material such as, but not limited to, titanium nitride, tantalum nitride, tungsten and ruthenium. In an embodiment, the bottom electrode 126 and the top electrode 132 are composed of the same material. In an embodiment, the top electrode has a thickness approximately in the range of 30 to 100 nm. In an embodiment, the composition and thickness of the top electrode 132 are tuned to meet specific device attributes such as series resistance, programming voltage and current.

[0040] In an embodiment, the dielectric spacer 134 may be any suitable dielectric material such as but not limited to carbon doped silicon nitride or silicon nitride. Typically, a non-oxygen-containing material is preferred for the dielectric spacer 134 to minimize oxidation of sidewalls of the oxygen exchange layer 130. In an embodiment, the dielectric spacer 134 has a thickness that ranges from 30-60nm.

[0041] Figures 2A-2I illustrate cross-sectional views representing various operations in a method of fabricating a transistor 200 with an ambipolar layer 206 and an RRAM device 240 coupled to the drain contact 224 of the transistor 200 in accordance with embodiments of the present invention.

[0042] Figure 2A illustrates a cross-sectional view of a patterned ambipolar layer 206 formed on an insulator layer 204 formed above a substrate 202. In an embodiment, an insulator layer 204 is formed on the substrate 202. The insulator layer 204 includes a material such as but not limited to silicon dioxide, silicon carbide or carbon-doped silicon oxide. In an embodiment, the insulator layer 204 is blanket deposited on the substrate 202 by a chemical vapor deposition (CVD) process or plasma enhanced chemical vapor deposition (PECVD) process. In an embodiment, the thickness of the insulator layer 204 ranges from 50-200 nm.

[0043] In an embodiment, the ambipolar layer 206 is deposited on the insulator layer 204. In an embodiment, the ambipolar layer 206 includes a material such as but not limited to transition metal dichalcogenide (TMDC), a carbon nanotube or a pentacene. In one specific embodiment, the ambipolar layer 206 is a TMDC layer. In one such embodiment, the TMDC layer has a chemical composition, MX_2 , where M is a transition metal and X is a chalcogen. In an embodiment, the transition metal, M, is selected from a group consisting of molybdenum, tungsten and chromium, and the chalcogen, X, is selected from a group consisting of sulfur, selenium and tellurium. In an embodiment the TMDC layer is WSe_2 . In an embodiment,

ambipolar layer 206 is deposited by a process such as an atomic layer deposition (ALD) process, a thermally assisted growth process, or an exfoliation process that is well known in the art. In an embodiment, for the purposes of meeting operational requirements of a 1T1R cell, the ambipolar layer 206 is highly uniform and atomically thin. In an embodiment, the ambipolar layer 206 has a thickness that ranges between 0.5nm-2nm. The uniformity of such thin layers dictates the quality of the accumulation or depletion regions that will be formed during transistor operation.

[0044] The transistor 200 is built on a foundation of the ambipolar layer 206. To define a source, a drain and a gate region of the transistor 200, the ambipolar layer 206 is first patterned and then subsequently etched as is depicted by the dashed box 208 in the illustration of Figure 2A. In other embodiments, desired portions of the ambipolar layer 206 where the transistor is to be fabricated is formed by masking a region and subsequently treating the exposed areas to an O₂ containing plasma ash process. The O₂ plasma ash process is an example of an oxidizing process that can convert the exposed portions of ambipolar layer 206 into a dielectric layer. Such a process may avoid etch and exposure of ultrathin sidewalls of the ambipolar layer 206.

[0045] Figure 2B illustrates the structure of Figure 2A following the formation of a gate stack 210 on the ambipolar layer 206. In an embodiment, the gate stack 210 includes a gate dielectric layer 212 and a gate electrode layer 214. In an embodiment, the gate dielectric layer 212 includes a material such as gate dielectric layer 108. In an embodiment, a gate dielectric layer 212 having a thickness ranging from 0.5nm -2nm, is formed on the ambipolar layer 206 using an atomic layer deposition (ALD) technique. In an embodiment, the gate electrode layer 214 includes a layer such as a gate electrode 110 and is formed on the surface of the gate dielectric layer 212 using a PVD or an ALD process. In an embodiment, thickness of the gate electrode layer 214 ranges from 20-100nm.

[0046] In an embodiment, hardmask layer 216 is formed on the gate electrode layer 214 to enable patterning of the gate stack 210. In an embodiment, the hardmask layer 216 includes a material such as silicon nitride, silicon oxynitride or carbon doped silicon nitride as is blanket deposited on the gate electrode layer 214. In an embodiment, the thickness of the hardmask layer 216 ranges from 10-50nm. In an embodiment, a photoresist pattern is formed on the hardmask layer 216. In an embodiment, the hardmask layer 216 and the gate stack 210 is subtractively etched by a plasma etch process. A gate electrode layer 214 having a thickness of approximately 30nm or less may also be patterned using a wet etch technique. In an embodiment, the gate length, L_G, of the gate stack 210 ranges from 10-30nm.

[0047] Figure 2C illustrates the structure of Figure 2B following the deposition and planarization of a dielectric layer 218. In an embodiment, a dielectric layer 218 is blanket deposited using a PECVD process. In an embodiment, the dielectric layer 218 is deposited to a

thickness of at least 2.5 times the combined thickness of the patterned gate stack 210 and the hardmask layer 216 to provide sufficient material to form a planarized dielectric layer 218. In an embodiment, the planarization process is a chemical mechanical polish (CMP) process.

[0048] Figure 2D illustrates the structure of Figure 2C following the formation of a drain

5 contact 224 in the dielectric layer 218 in the drain region 220 and the formation of a source contact 225 in the dielectric layer 218 in the source region 221. In an embodiment, a drain opening 219A and a source opening 219B are formed in the dielectric layer 218 by a combination of a plasma etch process followed by a wet etch process. The wet etch process exposes the ambipolar layer 206 and may prevent damage to the ambipolar layer 206.

10 A contact material 222 is deposited on the surface of the ambipolar layer 206 and fills the drain opening 219A and the source opening 219B. In an embodiment, the contact material may include an adhesion layer 222A and a conductive cap layer 222B as is illustrated in Figure 2D. The adhesion layer 222A is first deposited on surface of the ambipolar layer 206, and the conductive cap layer 222B is deposited on the adhesion layer 222A. The adhesion layer 222A
15 may include a material such as Ti, Ni, Sc or graphene. A strong Vander Walls interaction between the adhesion layer 222A and the uppermost surface of the ambipolar layer 206 can help form a robust contact. In an embodiment, the adhesion layer 222A forms a Schottky or an ohmic contact with the ambipolar layer 206 to minimize contact resistance between the ambipolar layer 206 and an RRAM device that will eventually be formed on the drain contact 224. The
20 conductive cap layer includes a material having a low electrical resistance such as tungsten, ruthenium or copper. By minimizing the overall contact resistance of the source contact 225 and the drain contact 224, the amount of current that can flow through the RRAM device can be optimized. After deposition of the adhesion layer 222A and the conductive cap 222 a planarization process may be carried out to form the drain contact 224 and source contact 225.
25 In some instances, a forming gas anneal employing a H₂/N₂ mixture (5% H₂/ 95% N₂) may be carried out at 200-250 degrees C to improve the interface between the drain and source contacts 224 and 225, respectively and the ambipolar layer 206.

[0049] In a different embodiment, the plasma etch process that forms the drain opening 219A in the drain region 220 and the source opening 219B in the source region 221 also etches
30 through the ambipolar layer 206 (denoted by dashed lines 223). In such an instance, the contact material 222 is formed adjacent to the exposed sidewalls of the ultrathin ambipolar layer 206. Contacts formed adjacent to the sidewalls of the ambipolar layer 206 may offer electrostatic advantages such as enhanced carrier injection into the drain and source regions 220 and 221, respectively. In yet another embodiment, a wet etch process is carried out after the plasma etch
35 process etches through the ambipolar layer 206 in each of the drain and source openings 219A

and 219B, respectively. In one such embodiment, the wet etch process widens the drain and source openings 219A and 219B, respectively, and exposes a portion of an uppermost surface of the ambipolar layer 206 in the drain and source openings 219A and 219B, respectively. The contact material 222 which is subsequently deposited in the drain opening 219A and source opening 219B, has portions that are in contact with the sidewalls and portions that are in contact with the uppermost surface of the ambipolar layer 206 in the drain opening 219A and source opening 219B.

[0050] The fabrication of a memory device on the drain contact 224 is described next. In an embodiment, the memory device is an RRAM device which includes a switching layer that is a metal oxide.

[0051] Figure 2E illustrates the structure of Figure 2D following the deposition of an RRAM material layer stack 238 on the drain contact 224 and on the uppermost surface of the dielectric layer 218. In an embodiment, the deposition of the RRAM material layer stack 238 includes a sequential deposition of a bottom electrode layer 226, a metal oxide switching layer 228, an oxygen exchange layer 230 and a top electrode layer 232 on the uppermost surface of the drain contact 222 and on the uppermost surface of the dielectric layer 218. The top electrode is capped by a dielectric hardmask layer 236.

[0052] In an embodiment, the bottom electrode layer 226 is a material having a composition and a thickness similar to the material composition and thickness of the bottom electrode layer 126. In an embodiment the bottom electrode layer 226 includes a material that is deposited by a physical vapor deposition (PVD) process. The PVD deposition method may further include a pre-deposition in-situ sputter cleans to first remove any oxide residue from an uppermost surface of the drain contact 224. In an embodiment, the sputter cleans process may include a gas containing Ar to energetically bombard the upper most surface of the drain contact 224 in order to remove any native oxide.

[0053] The metal oxide switching layer 228 is formed on the bottom electrode layer 226. In an embodiment, the metal oxide switching layer 228 is composed of a material having a composition and a thickness similar to the material composition and thickness of the metal oxide switching material 128. In an embodiment, the metal oxide switching layer 228 is formed using an ALD process. The ALD process may be characterized by a slow and a highly controlled metal oxide deposition rate. The ALD process may also be highly uniform (e.g., approximately 0.1nm level variation). In an embodiment, a pre-clean of the surface of the bottom electrode layer 226 is performed immediately prior to deposition of the metal oxide switching layer 228. In another embodiment, the metal oxide switching layer 228 is formed using a PVD process. In an embodiment, a pre-clean of the surface of the bottom electrode layer 226 is performed using

an Ar sputter clean immediately prior to deposition of the metal oxide switching layer 228.

[0054] The oxygen exchange layer 230 is formed on the metal oxide switching layer 228. In an embodiment, the oxygen exchange layer 230 is a material having a composition and a thickness similar to the material composition and thickness of the oxygen exchange material 130.

5 In an embodiment, the oxygen exchange layer 230 is formed using a PVD process. In one such embodiment, the metal oxide switching layer 228 and the oxygen exchange layer 230 are deposited sequentially in a same chamber or in a same tool without breaking vacuum.

[0055] The top electrode layer 232 is formed on the oxygen exchange material 230. In an embodiment, the top electrode layer 232 is a material having a composition and a thickness
10 similar to the material composition and thickness of the top electrode 132. In an embodiment, the top electrode layer 232 is formed using a PVD process. In an embodiment, the top electrode layer 232 and the oxygen exchange layer 230 are deposited sequentially in a same chamber or in a same tool without breaking vacuum. By doing so, the oxygen exchange layer 230 does not become oxidized. In an embodiment the top electrode layer 232 has a same composition as the
15 bottom electrode layer 226. The dielectric hardmask layer 236 is blanket deposited on the top electrode 232 using a PECVD process. The dielectric hardmask layer 236 may include a silicon nitride or a carbon doped silicon nitride layer.

[0056] Figure 2F illustrates the structure of Figure 2E following the formation of an RRAM device 240 on the drain contact 224 and a formation of a dielectric spacer 242
20 surrounding the RRAM device 240. In an embodiment, the dielectric hardmask layer 236 and the RRAM material layer stack 238 are patterned by a plasma etch process to form a patterned dielectric hardmask layer 236 and an RRAM device 240. Subsequently, a dielectric spacer 242 is blanket deposited on the patterned dielectric hardmask layer 236, on sidewalls of the RRAM device 240 and on the dielectric layer 218 and then etched back to form a dielectric spacer 242.
25 In an embodiment, deposition of the dielectric spacer layer 242 is performed immediately post formation of the RRAM device 240, but prior to breaking vacuum in the same tool or chamber used for the etch process. Such a procedure, known in the art as in-situ deposition, may hermetically seal the device and potentially decrease oxidation of the perimeter of the sensitive oxygen exchange layer 230. In an embodiment, the dielectric spacer layer is a material such as,
30 but not limited to, silicon nitride, silicon carbide, carbon-doped silicon nitride, or any suitable non-oxygen containing material. In an embodiment, the dielectric spacer layer has a thickness approximately in the range of 20-50nm. In an embodiment, the dielectric spacer layer may be plasma etched to form dielectric spacer 242. The plasma etch process removes all of the dielectric spacer layer 242 from the uppermost surface of the hardmask layer 236 and from the
35 uppermost surface of the dielectric layer 218.

[0057] Figure 2G illustrates the structure of Figure 2F following the deposition of a second dielectric layer 244 followed by a planarization process. The second dielectric layer 244 is blanket deposited on the memory device 240, on the dielectric spacer 242, on the first dielectric layer 218 and on the source contact 225. In an embodiment, the second dielectric layer 244 is compositionally similar to the dielectric layer 218. In an embodiment, the planarization process removes the excess portions of the second dielectric layer 244 deposited above the dielectric hardmask layer 236. The planarization process is further extended to remove the entire hardmask layer 236 and removes top portions of the top electrode 232 and top portions of the dielectric spacer 242. In an embodiment, the planarization process results in the second dielectric layer 244, the top electrode layer 232 and the dielectric spacer 242 having uppermost surfaces that are substantially coplanar as is illustrated in Figure 2G.

[0058] Figure 2H illustrates the structure of Figure 2G following the formation of a contact electrode 250 on the RRAM device 240. In an embodiment, a third dielectric layer 246 is blanket deposited on the structure of Figure 2G. An electrode opening 249 is formed in the third dielectric layer 246 and exposes a portion of the top electrode 232. A contact electrode 250 is formed by a contact electrode material deposition process and a planarization process. The contact electrode material may include a metal such as tungsten, ruthenium or copper. In an embodiment, a Ta liner is used to form a liner in the opening 249 prior to deposition of the contact electrode material.

[0059] Figure 2I illustrates the structure of Figure 2H following the formation of a source electrode 252 on the source contact 225 and the formation of a gate contact 254 on the gate electrode layer 214. In an embodiment, an opening 251 is formed in the third and second dielectric layers 246 and 244 respectively. The opening 251 exposes the source contact 225. The opening 251 may be filled with a contact electrode material such as tungsten, ruthenium or copper and then planarized to form a source electrode 252. Subsequently, a gate electrode opening 253 is formed in the dielectric layer 218, and in the second and third dielectric layers 244 and 246 respectively and in a portion of the hardmask layer 216 to expose the gate electrode layer 214. The gate electrode opening 253 may be filled with a metal such as tungsten and subsequently planarized. In a variation of the present embodiment, the gate contact 254 may be formed before the formation of the source electrode 252. In another embodiment, the source electrode 252, the contact electrode 250 and the gate contact 254 may be all formed at the same time.

[0060] Figure 3A-3D illustrates an ambipolar layer based transistor 300 fabricated by a replacement gate process in an accordance with an embodiment of the present invention.

[0061] Figure 3A illustrates the structure of Figure 2C following an extended

planarization process to expose the hardmask 216 and a subsequent etch process to remove the hardmask 216 and the gate stack 210. In an embodiment, the gate stack 210 is a replaceable dummy gate stack which includes a gate dielectric layer 212 that is silicon dioxide and a gate electrode layer 214 that is polysilicon. Removal of the gate stack 210 creates an opening 310.

5 [0062] Figure 3B illustrates the structure of Figure 3A following a deposition of a functional gate dielectric layer 312 and a functional gate electrode 314 followed by a planarization process. In an embodiment, the functional gate dielectric layer 312 and the functional gate electrode 314 include materials similar to the materials used to fabricate gate dielectric layer 108 and gate electrode 110, respectively. The functional gate dielectric layer 312 and the functional gate electrode 314 may be deposited by an ALD process to ensure conformal deposition in the opening 310. The excess functional gate dielectric layer 312 and the excess functional gate electrode 314 deposited over the uppermost surface of the dielectric layer 218 may be removed by a planarization process such as a CMP process.

15 [0063] Figure 3C illustrates the structure of Figure 3B following the deposition of an interlayer dielectric film (ILD) 344 followed by the formation of source contact 225, a drain contact 224 in the source region 221 and drain region 220. The materials and methods utilized to form source contact 225 and drain contact 224 are as described above.

[0064] Figure 3D illustrates the structure of Figure 3C following the process steps described in connection with Figures 2E – 2I to form an RRAM device 240, dielectric spacers 242, a contact electrode 250, a gate contact 254 and a source electrode 252.

20 [0065] The various embodiments of the 1T-1R cell 100 typically undergo a high temperature anneal process at the end of the fabrication process. In an embodiment, annealing is carried out at temperatures in the range of 350 degrees C - 450 degrees C and last for a time period ranging from 30-60 minutes. Annealing offers an additional advantage such as lowering the voltage required to “voltage - form” (or initialize) the RRAM device 240.

25 [0066] Figure 4A-4C illustrate various biasing schemes on the source region 112, on the gate electrode 110, and on the RRAM top electrode 132 to cycle the RRAM device 124 and associated current-voltage traces of the RRAM device 124 resulting from such biasing. The operation of the 1T-1R circuit in the Figures 4A-4B highlights some advantages of ambipolar layer 104 in the 1T-1R cell 100.

30 [0067] Figure 4A illustrates biasing conditions to perform a RESET event in the RRAM device 124 and the associated current voltage trace of the RRAM device 124. Referring to the I-V trace in Figure 4A, at point A, the RRAM device 124 is in a low resistance state after having undergone a “forming event” (dashed line 1). The forming event is associated with the creation of a conductive filament in the metal oxide switching layer 128. Referring to the circuit diagram

of the 1T-1R cell 100 in Figure 4A, the source voltage, V_S , is set to ground or 0, and the voltage, V_D , on the top electrode 132, and the voltage, V_G , on the gate electrode 110 are slowly changed from a positive value to a negative value as indicated in the circuit diagram. The corresponding $I-V_{DS}$ trace for the RRAM device 124 illustrates the current – voltage relationship during this portion of the switching cycle. From point A, the voltage V_{DS} , gradually decreases in magnitude to 0 (at point O) and then reverses polarity and increases in magnitude (from point O to point B). At point B, the voltage, V_D , on the top electrode 132 (with respect to the source), reaches a critical negative value, V_{RESET} . At point B, the gate voltage, V_G , is also negative with respect to the source. As the magnitude of the voltage, V_D , on the top electrode 132 continues to increase (point B to point C), the RRAM device 124 undergoes a transition from a low resistance state (LRS) at point B to a high resistance state (HRS) at point C. The transition from LRS to HRS is termed RESET. The direction of the current through the transistor changes when the “gate voltage”, V_G , “and” the top electrode voltage, V_D , change from a positive value to a negative value (around point O). It is to be appreciated that the polarity of the gate voltage and the polarity of the drain voltage must be in sync to enable current flow in the desired direction. The change in direction of the current (around point O) is made possible by the presence of the ambipolar layer 104 which enables electron and hole transport. The direction of the current shown in the circuit diagram in Figure 4A represents the direction of hole transport during any moment from point O to point C. Typical SET voltages for an RRAM device 124 can range from 0.8V to 1.2V.

[0068] Figure 4B illustrates biasing conditions to perform a SET event in the RRAM device 124 and the associated current voltage trace of the RRAM device 124. At point C the RRAM device 124 is in HRS state. Referring to the circuit diagram of the 1T-1R cell 100 in Figure 4B, the source voltage, V_S , is set to ground or 0, and the voltage, V_D , on the top electrode 132, and the voltage, V_G , on the gate electrode 110 are slowly changed from a negative value to a positive value as indicated in the circuit diagram. The corresponding $I-V_{DS}$ trace in the RRAM device 124 illustrates the current – voltage relationship during this portion of the switching cycle. From point C, the magnitude of the voltage V_{DS} , gradually decreases in magnitude to 0 (at point O) and then reverses polarity and increases in magnitude (from point O to point D). At point D, the voltage, V_D , (with respect to the source), on the top electrode 132 reaches a critical positive value, V_{SET} . At point D, the gate voltage, V_G , is also positive with respect to the source. As the magnitude of the voltage, V_D , on the top electrode 132 continues to increase (point D to point A), the RRAM device 124 undergoes a transition from HRS at point D to a LRS at point A. The transition from HRS to LRS is termed SET. The direction of the current through the transistor changes when the “gate voltage”, V_G , “and” the top electrode voltage, V_D , change from a

negative value to a positive value (around point O). The change in direction in the current (about point O) is made possible by the presence of the ambipolar layer 104 which now enables hole transport in an opposite direction as compared to the direction indicated in Figure 4A. The direction of the current shown in the circuit diagram in Figure 4B represents the direction of hole transport during any moment from point O to point A. Typical SET voltages for an RRAM device 124 can range from 0.8-1.2V.

[0069] Figure 4C represents the transistor biasing condition to perform a read event. The READ operation of a memory cell is often more important for memory applications than SET or RESET. In practice, a memory cell is more often programmed into a certain state once but read back repeatedly. Typically read operation is performed over a voltage range of 0.1 - 0.2V. In one specific example a finite small positive voltage V_D , and V_G , are applied to the contact electrode and the gate electrode, respectively. The I-V plot in Figure 4C, drawn at a magnified scale, illustrates current – voltage trace for two read events in the RRAM device 124. Read event 1 corresponds to reading of the RRAM device 124 in the LRS state and read event 2 corresponds to reading of the RRAM device 124 in the HRS state. The magnitude of the READ voltage is too small to cause any perturbation in the RRAM device 124 and does not enable a resistance change. The relative magnitude of the READ voltage and READ current is very small compared to the magnitude of the SET voltage and SET current.

[0070] Figure 5 illustrates a block diagram of an electronic system 500, in accordance with an embodiment of the present invention. The electronic system 500 can correspond to, for example, a portable system, a computer system, a process control system, or any other system that utilizes a processor and an associated memory. The electronic system 500 may include a microprocessor 502 (having a processor 504 and control unit 506), a memory device 124, transistor with an ambipolar layer 104 and an input/output device 530 (it is to be appreciated that the electronic system 500 may have a plurality of processors, control units, memory device units and/or input/output devices in various embodiments). In one embodiment, the electronic system 500 has a set of instructions that define operations which are to be performed on data by the processor 504, as well as, other transactions between the processor 504, the memory device 508, and the input/output device 510. The control unit 506 coordinates the operations of the processor 504, the memory device 508 and the input/output device 510 by cycling through a set of operations that cause instructions to be retrieved from the memory device 508 and executed. The memory device 508 can include a memory device having a conductive oxide and electrode stack as described in the present description. In an embodiment, the memory device 508 is embedded in the microprocessor 502, as depicted in Figure 5. In an embodiment, the processor 504, or another component of electronic system 500, includes an array of RRAM devices 124.

[0071] Figure 6 illustrates a computing device 600 in accordance with one embodiment of the invention. The computing device 600 houses a board 602. The board 602 may include a number of components, including but not limited to a processor 604 and at least one communication chip 606. The processor 604 is physically and electrically coupled to the board 602. In some implementations the at least one communication chip 606 is also physically and electrically coupled to the board 602. In further implementations, the communication chip 606 is part of the processor 604.

[0072] Depending on its applications, computing device 600 may include other components that may or may not be physically and electrically coupled to the board 602. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

[0073] The communication chip 606 enables wireless communications for the transfer of data to and from the computing device 600. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 606 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 600 may include a plurality of communication chips 606. For instance, a first communication chip 606 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 506 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0074] The processor 604 of the computing device 600 includes an integrated circuit die packaged within the processor 604. In some implementations of embodiments of the invention, the integrated circuit die of the processor includes one or more arrays, such as an array of 1T-1R cell 100, built in accordance with embodiments of the present invention. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or

memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0075] The communication chip 606 also includes an integrated circuit die packaged within the communication chip 606. In accordance with another implementation of an
5 embodiment of the invention, the integrated circuit die of the communication chip includes RRAM memory arrays integrated into a logic processor, built in accordance with embodiments of the present invention.

[0076] In further implementations, another component housed within the computing device 600 may contain a stand-alone integrated circuit memory die that includes one or more
10 arrays of 1T-1R cells 100, built in accordance with embodiments of the present invention.

[0077] In various implementations, the computing device 600 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra-mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital
15 video recorder. In further implementations, the computing device 600 may be any other electronic device that processes data.

[0078] Accordingly, one or more embodiments of the present invention relate generally to the fabrication of embedded microelectronic memory. The microelectronic memory may be non-volatile, wherein the memory can retain stored information even when not powered. One or
20 more embodiments of the present invention relate to the fabrication of a 1T-1R cell 100. Such a 1T-1R cell 100 may be used in an embedded non-volatile memory.

[0079] Thus, embodiments of the present invention include an ambipolar layer based transistors for memory applications and methods of fabrication.

[0080] Example 1: A semiconductor device includes a transistor structure. The
25 transistor structure further includes a semiconductor substrate. An insulator disposed above the substrate. An ambipolar layer is disposed on the insulator layer. A gate dielectric layer is disposed on the ambipolar layer. A gate electrode is disposed on the gate dielectric layer. A source region and a drain region are disposed on the ambipolar conductive layer. The source region is separated from the drain region by the gate electrode. A source contact is disposed on
30 the source region and a drain contact is disposed on the drain region. A memory device is disposed on the drain contact.

[0081] Example 2: The semiconductor device of example 1, wherein the ambipolar layer includes a material selected from the group consisting of transition metal dichalcogenide, a carbon nanotube and a pentacene.

[0082] Example 3: The semiconductor device structure of example 1 or 2, wherein the

ambipolar layer has a thickness between 0.2nm - 0.5nm.

[0083] Example 4: The semiconductor device structure of example 1, wherein the source contact and the drain contact further include an adhesion layer on the ambipolar layer and a conductive fill layer on the adhesion layer.

5 [0084] Example 5: The semiconductor device structure of example 1, wherein the gate dielectric layer is a high-K gate dielectric layer.

[0085] Example 6: The semiconductor device structure of example 1 or 5, wherein the gate dielectric layer has a portion disposed on the sidewall of the gate electrode.

[0086] Example 7: A semiconductor device includes a transistor structure. The
10 transistor structure includes a semiconductor substrate. An insulator is disposed on the substrate. A transition metal dichalcogenide (TMDC) layer is disposed on the insulator layer. A gate dielectric layer is disposed on the TMDC layer. A gate electrode is disposed on the gate dielectric layer. A source region and a drain region are disposed on the TMDC layer. The source region is separated from the drain region by the gate electrode. A source contact is disposed on
15 the source region and a drain contact is disposed on the drain region. A resistive random access memory (RRAM) element is disposed on the drain contact. The RRAM device includes a bottom electrode. A switching layer is disposed above the bottom electrode and a top electrode is disposed above the switching layer.

[0087] Example 8: The semiconductor device of example 7, wherein the TMDC layer
20 has a chemical composition, MX_2 , where M is a transition metal and X is a chalcogen.

[0088] Example 9: The semiconductor device of example 8, wherein the transition metal, M, is selected from a group consisting of molybdenum, tungsten and chromium, and the chalcogen, X, is selected from a group consisting of sulfur, selenium and tellurium.

[0089] Example 10: The semiconductor device of example 7, wherein the TMDC layer
25 has a thickness between 0.2 – 5nm.

[0090] Example 11: The semiconductor device of example 7, wherein the gate dielectric layer is a high K gate dielectric layer.

[0091] Example 12: The semiconductor device of example 7 or 11, wherein the gate dielectric layer has a portion is disposed on sidewalls of the gate electrode.

30 [0092] Example 13: The semiconductor device of example 7, wherein the switching layer has a chemical composition, MO_{2-x} , where M is a metal and O is an oxide, where X is approximately in the range from 0 to 0.05.

[0093] Example 14: The semiconductor device of example 7 or 13, wherein the switching layer has a thickness approximately in the range of 1-5 nm and the oxygen exchange
35 layer has a thickness approximately in the range of 5-20 nanometers.

[0094] Example 15: The semiconductor device of example 7, wherein the bottom electrode and the top electrode comprise a material selected from the group consisting of titanium nitride, tantalum nitride, tungsten and ruthenium.

[0095] Example 16: The semiconductor device of example 7, 13 or 14, wherein the oxygen exchange layer is disposed on the switching layer and below the top electrode.

[0096] Example 17: The semiconductor device of example 7, 13, 15 or 16, wherein the oxygen exchange layer is disposed on the bottom electrode and below the switching layer.

[0097] Example 18: A method of fabricating semiconductor structure includes providing a substrate. The method includes forming an insulator layer on the substrate. The method includes forming an ambipolar layer on the insulator layer. The method includes forming a gate dielectric layer on the ambipolar layer. A gate electrode is formed on the gate dielectric layer. A source region and a drain region are formed on the ambipolar layer. A source contact is formed on the source region and a drain contact is formed on the drain region. The source region is separated from the drain region by the gate electrode. The method further includes forming a resistive random access memory (RRAM) element on the drain contact. Forming the RRAM device includes forming a bottom electrode and forming a switching layer above the bottom electrode. A top electrode is disposed above the switching layer.

[0098] Example 19: The method of example 18, wherein the forming the ambipolar layer includes a process selected from the group consisting of an atomic layer deposition process, a thermally assisted growth process, and an exfoliation process.

[0099] Example 20: The method of example 18, wherein, forming the RRAM device further comprises forming an oxygen exchange layer on the switching layer.

[00100] Example 21: The method of example 18 or 20, wherein forming the RRAM device further includes forming a dielectric spacer laterally surrounding the switching layer and the top electrode.

[00101] Example 22: The method of example 18, 20 or 21, wherein, forming the RRAM device further comprises forming an oxygen exchange layer on the bottom electrode.

[00102] Example 23: The method of example 20, wherein the top electrode layer is formed on the oxygen exchange layer without an air break post deposition of the oxygen exchange layer.

CLAIMS

What is claimed is:

1. A semiconductor device comprising:

a transistor structure, the transistor structure comprising:

- 5 a semiconductor substrate;
 an insulator disposed above the substrate;
 an ambipolar layer disposed on the insulator layer;
 a gate dielectric layer disposed on the ambipolar layer;
 a gate electrode disposed on the gate dielectric layer;
10 a source region and a drain region disposed on the ambipolar conductive layer, the
 source region separated from the drain region by the gate electrode;
 a source contact disposed on the source region and a drain contact disposed on the
 drain region; and
 a memory device disposed on the drain contact.

15

2. The semiconductor device of claim 1, wherein the ambipolar layer includes a material selected from the group consisting of transition metal dichalcogenide, a carbon nanotube and a pentacene.

20

3. The semiconductor device structure of claim 1, wherein the ambipolar layer has a thickness between 0.2nm - 0.5nm.

4. The semiconductor device structure of claim 1, wherein the source contact and the drain contact further include an adhesion layer on the ambipolar layer and a conductive fill layer on
25 the adhesion layer.

5. The semiconductor device structure of claim 1, wherein the gate dielectric layer is a high-K gate dielectric layer.

30 6. The semiconductor device structure of claim 1, wherein the gate dielectric layer has a portion disposed on the sidewall of the gate electrode.

7. A semiconductor device comprising:

a transistor structure comprising:

- 35 a semiconductor substrate;

- an insulator disposed on the substrate;
a transition metal dichalcogenide (TMDC) layer disposed on the insulator layer;
a gate dielectric layer disposed on the TMDC layer;
a gate electrode disposed on the gate dielectric layer,
5 a source region and a drain region disposed on the TMDC layer, the source region separated from the drain region by the gate electrode;
a source contact disposed on the source region and a drain contact disposed on the drain region;
a resistive random access memory (RRAM) element disposed on the drain contact, the
10 RRAM device comprising:
a bottom electrode;
a switching layer disposed above the bottom electrode; and
a top electrode disposed above the switching layer.
- 15 8. The semiconductor device of claim 7, wherein the TMDC layer has a chemical composition, MX_2 , where M is a transition metal and X is a chalcogen.
9. The semiconductor device of claim 8 where the transition metal, M, is selected from a group consisting of molybdenum, tungsten and chromium, and the chalcogen, X, is selected from a
20 group consisting of sulfur, selenium and tellurium.
10. The semiconductor device of claim 7, wherein the TMDC layer has a thickness between 0.2 – 5nm.
- 25 11. The semiconductor device of claim 7, wherein the gate dielectric layer is a high K gate dielectric layer.
12. The semiconductor device of claim 7, wherein the gate dielectric layer has a portion disposed on sidewalls of the gate electrode.
- 30 13. The semiconductor device of claim 7, wherein the switching layer has a chemical composition, MO_{2-X} , where M is a metal and O is an oxide, where X is approximately in the range from 0 to 0.05.
- 35 14. The semiconductor device of claim 7, wherein the switching layer has a thickness

approximately in the range of 1-5 nm and the oxygen exchange layer has a thickness approximately in the range of 5-20 nanometers.

15. The semiconductor device of claim 7, wherein the bottom electrode and the top electrode
5 comprise a material selected from the group consisting of titanium nitride, tantalum nitride, tungsten and ruthenium.

16. The semiconductor device of claim 7, wherein an oxygen exchange layer is disposed on the switching layer and below the top electrode.

10 17. The semiconductor device of claim 7, wherein the oxygen exchange layer is disposed on the bottom electrode and below the switching layer.

18. A method of fabricating semiconductor structure, the method comprising:

15 providing a substrate;

forming an insulator layer on the substrate;

forming an ambipolar layer on the insulator layer;

forming a gate dielectric layer on the ambipolar layer;

forming a gate electrode on the gate dielectric layer;

20 forming a source region and a drain region on the ambipolar layer;

forming a source contact on the source region and forming a drain contact on the drain region, the source region separated from the drain region by the gate electrode;

forming a resistive random access memory (RRAM) element on the drain contact, the forming the RRAM device comprising:

25 forming a bottom electrode;

forming a switching layer above the bottom electrode; and

a top electrode disposed above the switching layer.

19. The method of claim 18, wherein the forming the ambipolar layer comprises a process
30 selected from the group consisting of an atomic layer deposition process, a thermally assisted growth process, and an exfoliation process.

20. The method of claim 18, wherein, forming the RRAM device further comprises forming an

oxygen exchange layer on the switching layer.

21. The method of claim 18, wherein, forming the RRAM device further comprises forming an oxygen exchange layer on the bottom electrode.

5

22. The method of claim 18, wherein forming the RRAM device further comprises forming a dielectric spacer laterally surrounding the switching layer and the top electrode.

23. The method of claim 20, wherein the top electrode layer is formed on the oxygen exchange
10 layer without an air break post deposition of the oxygen exchange layer.

1/8

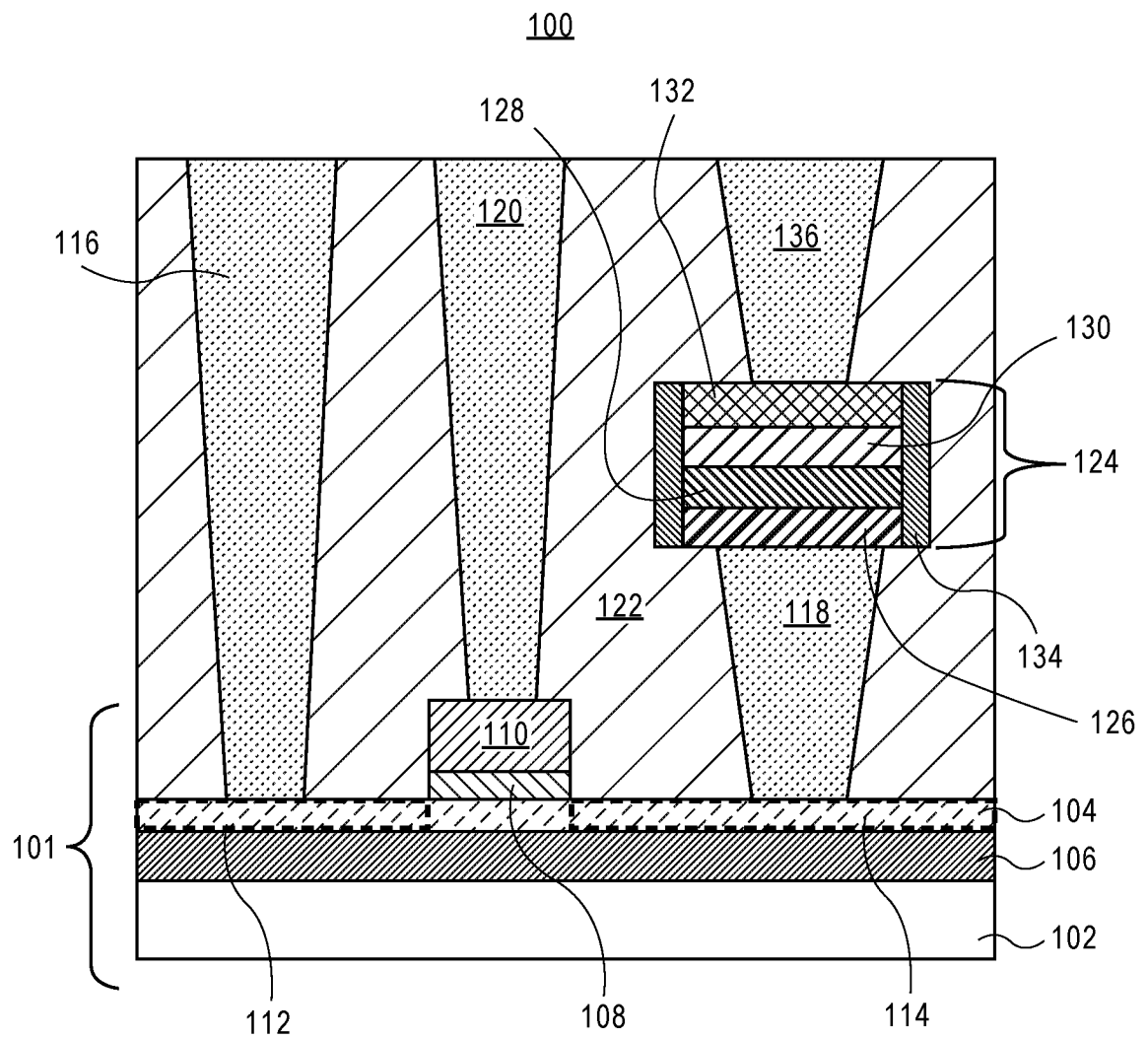


FIG. 1

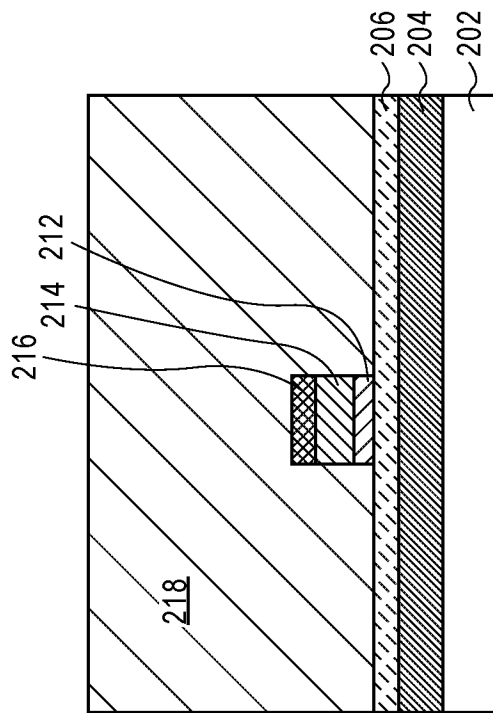


FIG. 2C

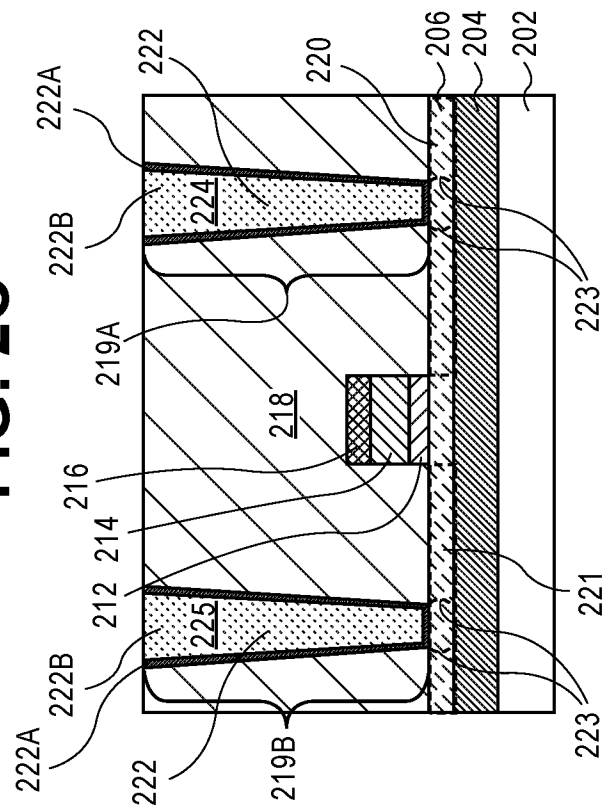


FIG. 2D

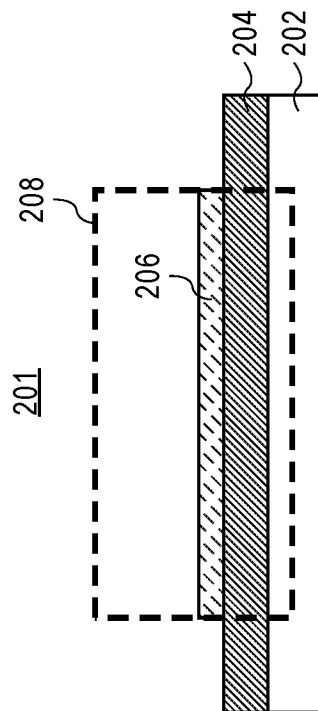


FIG. 2A

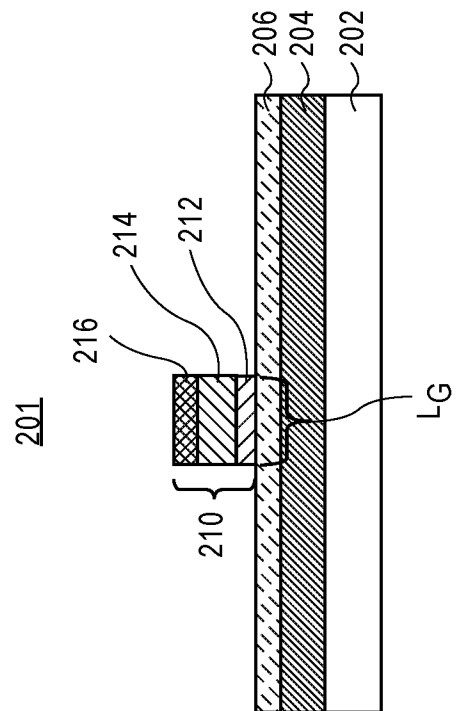


FIG. 2B

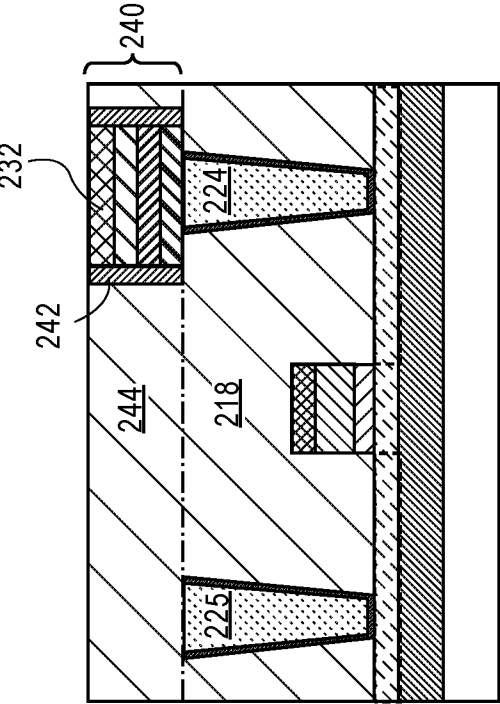


FIG. 2G

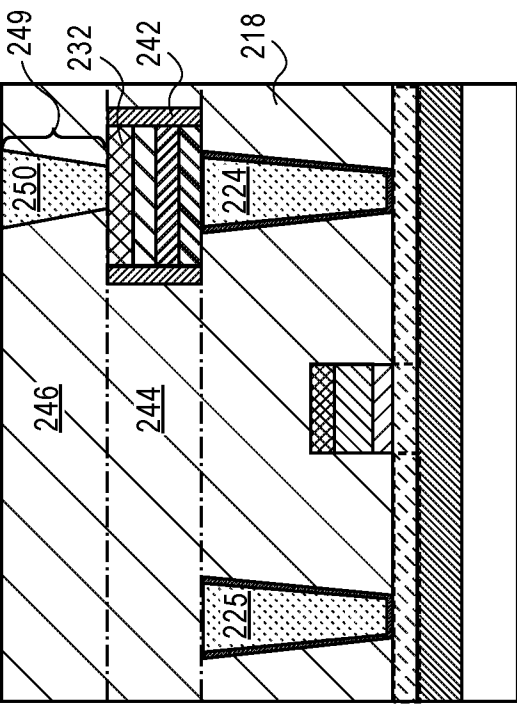


FIG. 2H

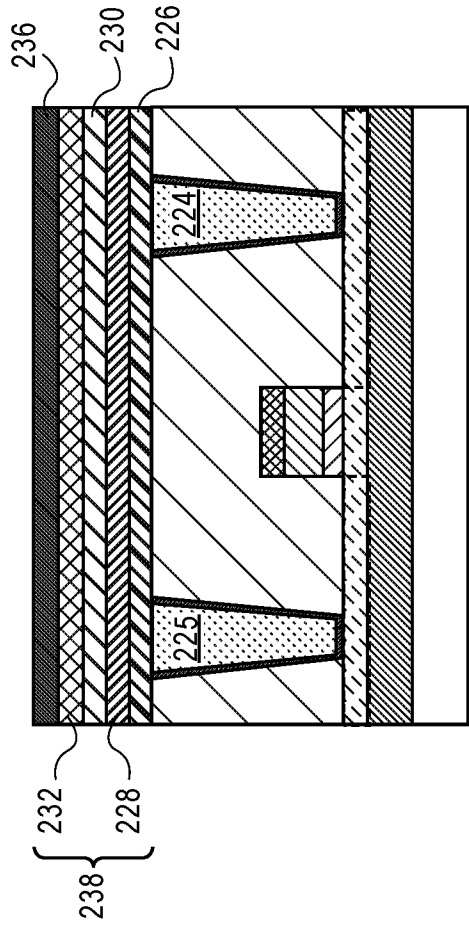


FIG. 2E

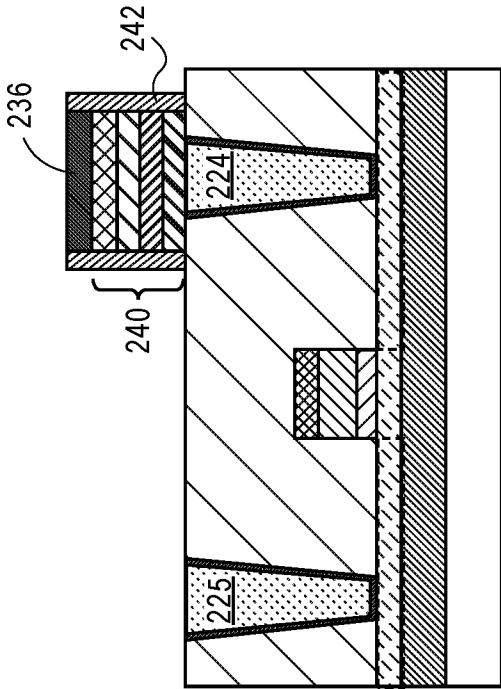


FIG. 2F

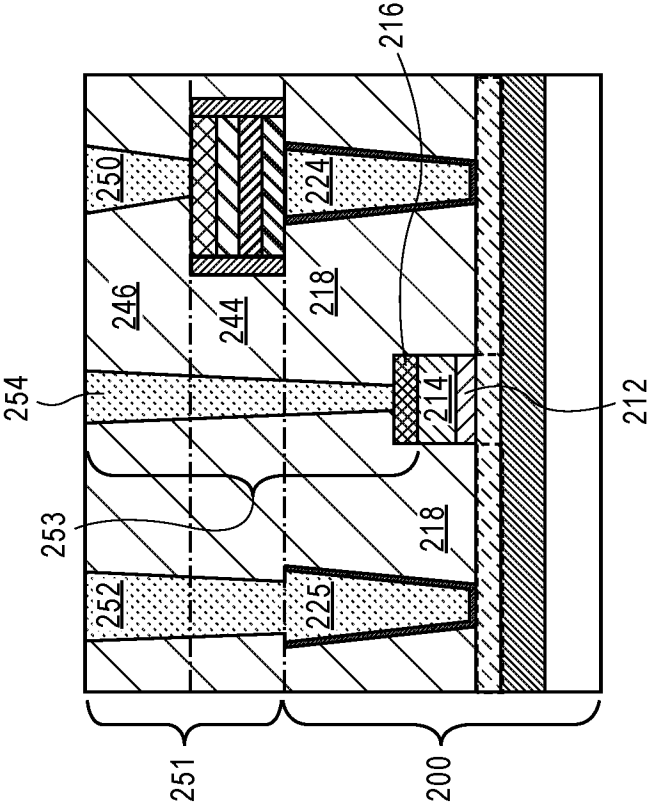


FIG. 2I

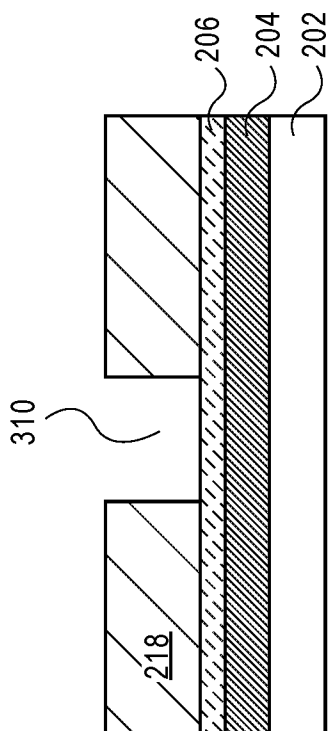


FIG. 3A

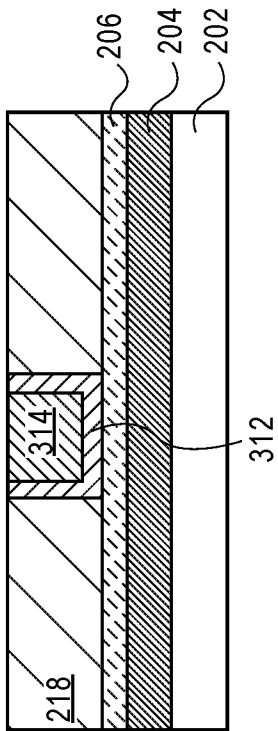


FIG. 3B

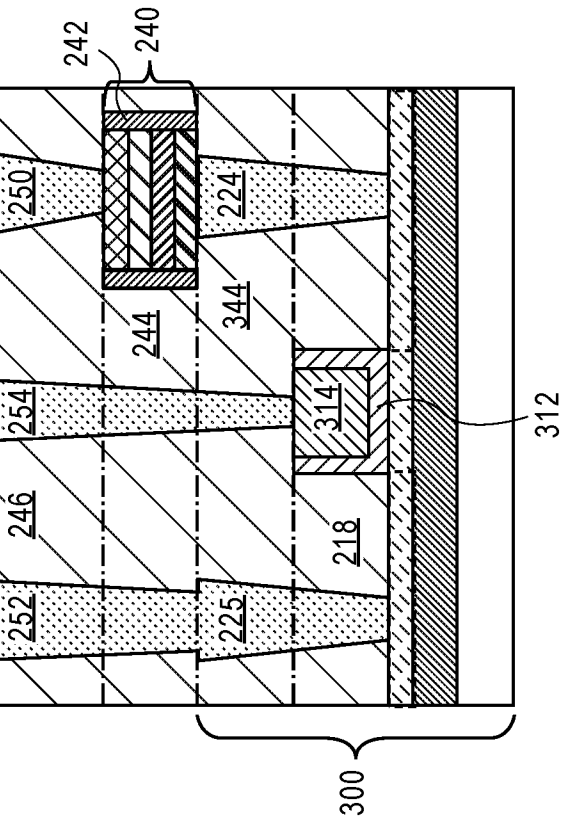


FIG. 3D

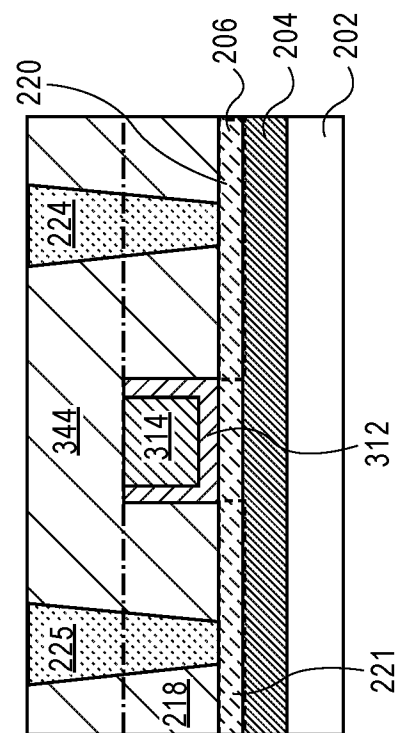


FIG. 3C

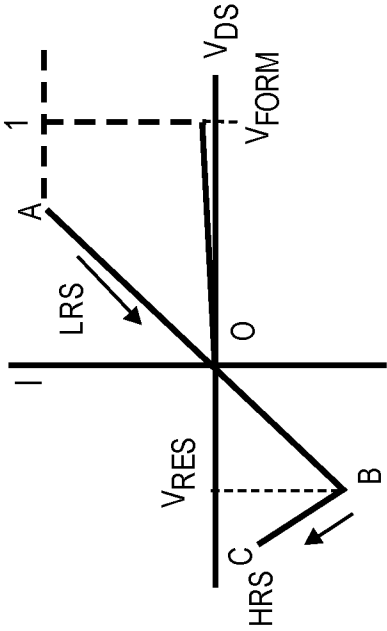


FIG. 4A

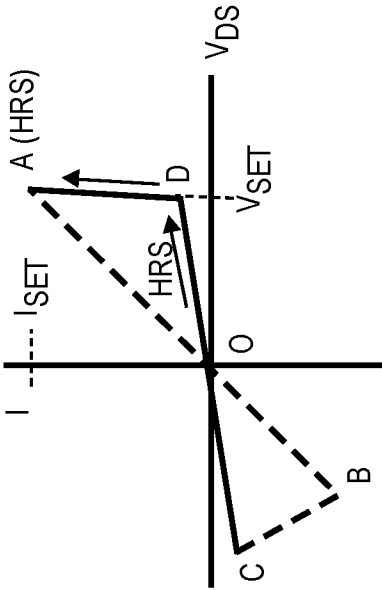


FIG. 4B

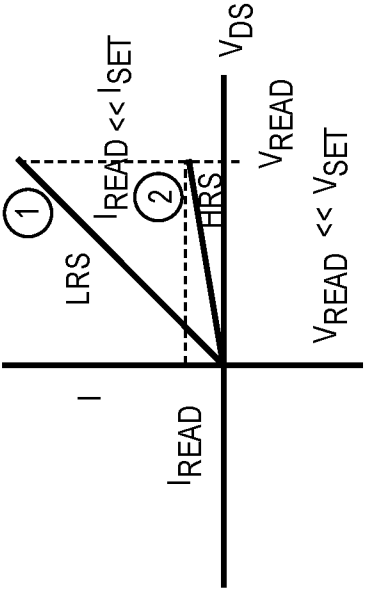
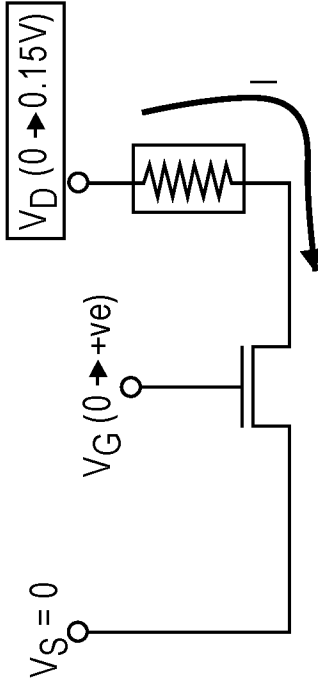
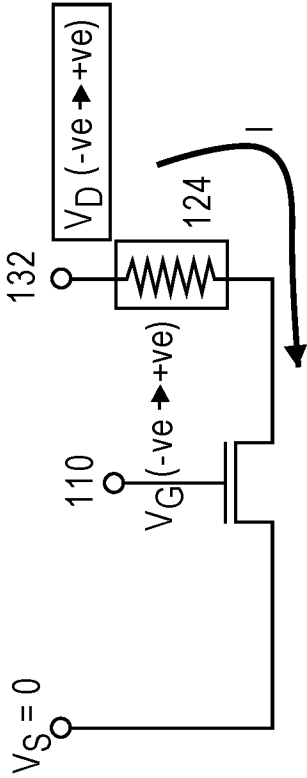
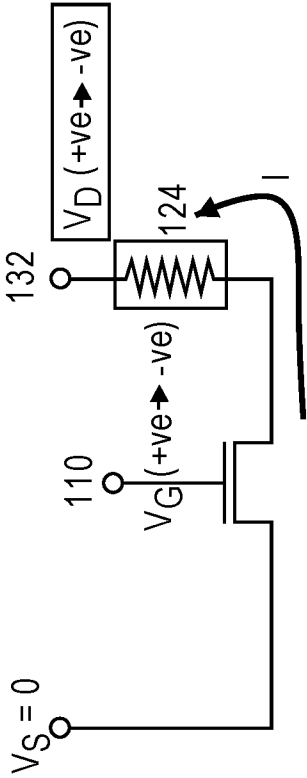
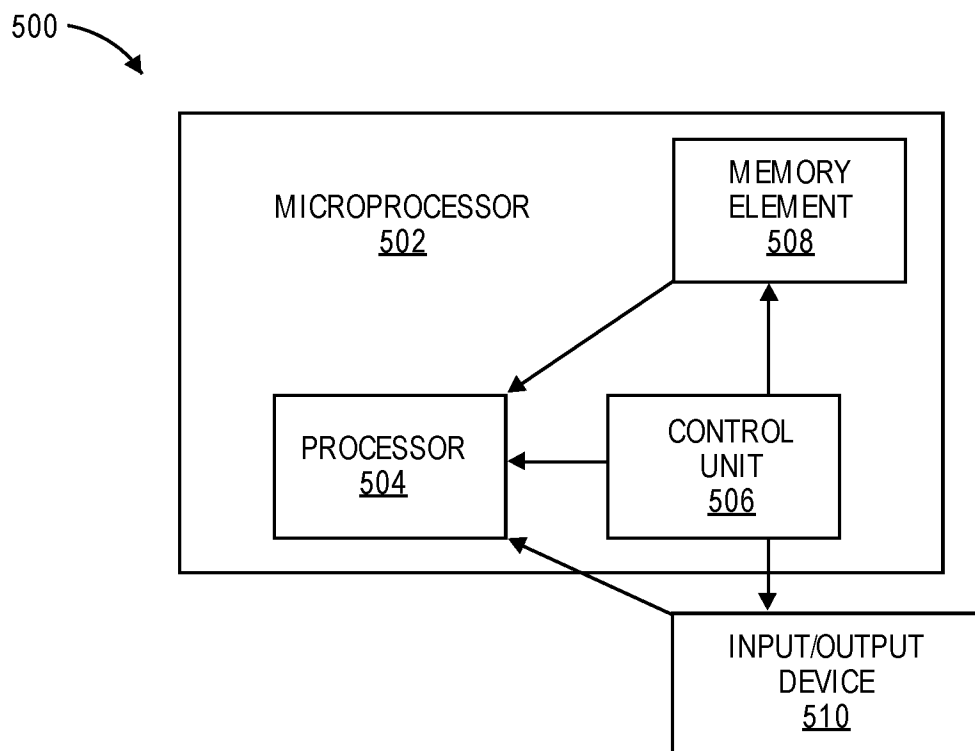


FIG. 4C



7/8

**FIG. 5**

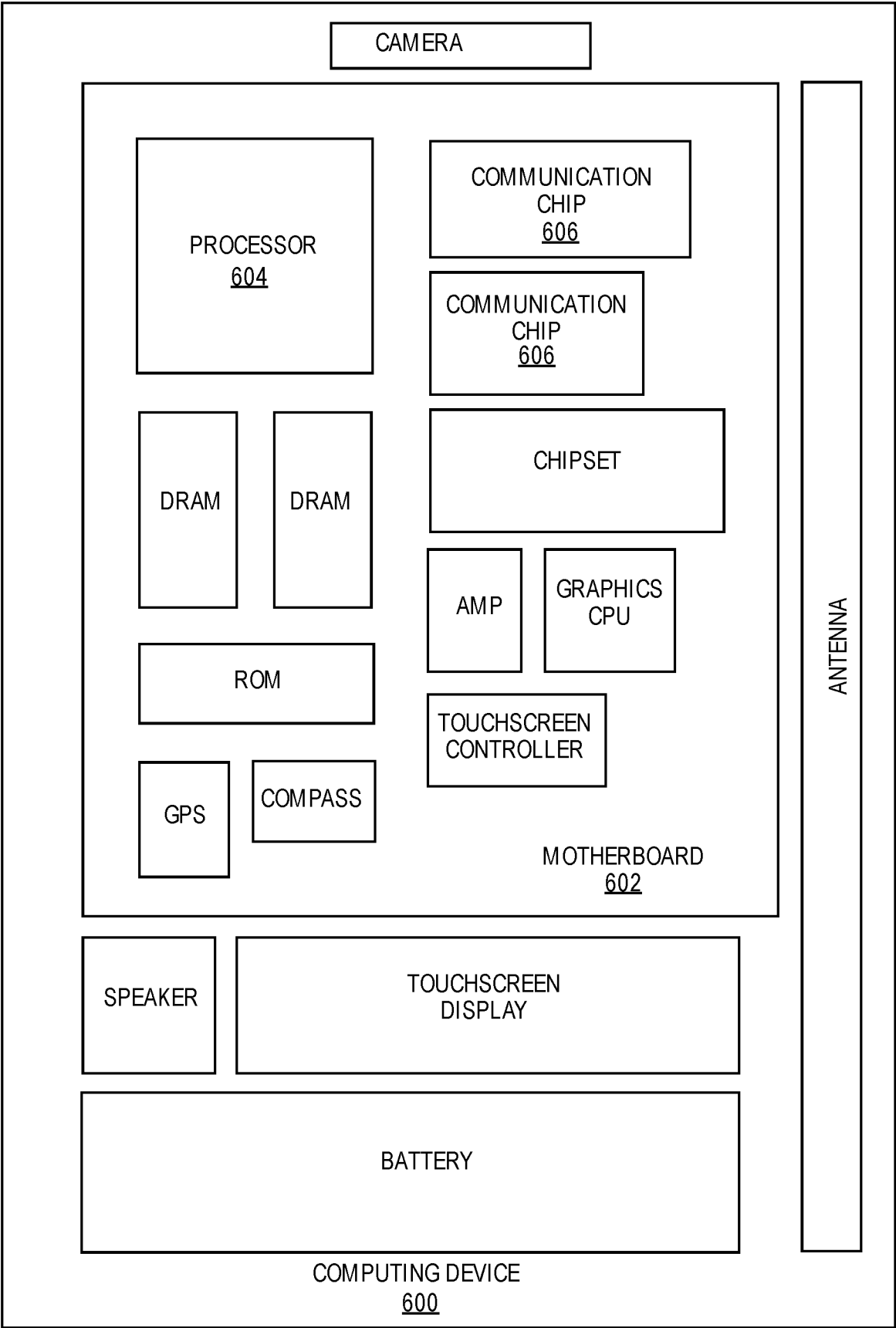


FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/069477**A. CLASSIFICATION OF SUBJECT MATTER****H01L 29/73(2006.01)i, H01L 29/66(2006.01)i, H01L 29/78(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/73; H01L 21/84; H01L 21/336; H01L 45/00; H01L 29/16; H01L 29/775; H01L 29/24; H01L 27/11; H01L 27/24; H01L 29/66; H01L 29/78

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: memory, transistor, ambipolar, layer, source, drain

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2014-0319452 A1 (UNIVERSITY OF NOTRE DAME DU LAC) 30 October 2014 See paragraphs [0016]-[0019], claim 1 and figures 2-3.	1-23
Y	US 2016-0351806 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.) 01 December 2016 See paragraphs [0016]-[0024], [0054]-[0057] and figures 2, 9.	1-23
A	US 2008-0312088 A1 (CHUNG et al.) 18 December 2008 See claims 1-8 and figures 1-2.	1-23
A	US 2011-0204332 A1 (LEE et al.) 25 August 2011 See claims 1-7 and figures 1-3.	1-23
A	US 2015-0325788 A1 (INTERMOLECULAR INC.) 12 November 2015 See claims 1-5 and figures 1A-5E.	1-23



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

18 September 2017 (18.09.2017)

Date of mailing of the international search report

19 September 2017 (19.09.2017)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

KANG, Sung Chul

Telephone No. +82-42-481-8405



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/069477

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2014-0319452 A1	30/10/2014	None	
US 2016-0351806 A1	01/12/2016	CN 106159086 A US 9431603 B1	23/11/2016 30/08/2016
US 2008-0312088 A1	18/12/2008	CN 101325218 A CN 101325218 B JP 2008-311643 A JP 5456987 B2 KR 10-1443215 B1 KR 10-2008-0109549 A US 8274098 B2	17/12/2008 13/02/2013 25/12/2008 02/04/2014 24/09/2014 17/12/2008 25/09/2012
US 2011-0204332 A1	25/08/2011	KR 10-1659816 B1 KR 10-2011-0097444 A US 8823077 B2	26/09/2016 31/08/2011 02/09/2014
US 2015-0325788 A1	12/11/2015	KR 10-2015-0056842 A US 2014-0078808 A1 US 9129894 B2 US 9444047 B2 WO 2014-043630 A1	27/05/2015 20/03/2014 08/09/2015 13/09/2016 20/03/2014