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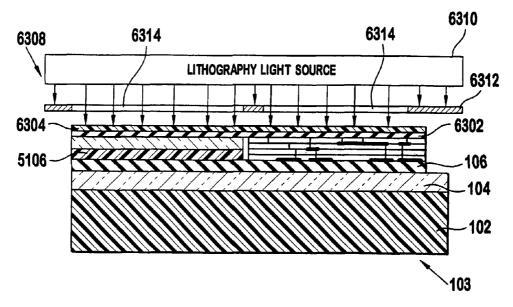
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(54) Title: INTEGRATED OPTICAL/ELECTRONIC CIRCUITS AND ASSOCIATED METHODS OF SIMULTANEOUS GEN-**ERATION THEREOF**

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(57) Abstract: A method for forming a hybrid active electronic and optical circuit (103) using a lithography mask (6312) is disclosed. The hybrid active electronic and optical circuit (103) includes an active electronic device and at least one optical device on a Silicon-On-Insulator, SOI, wafer (102). The SOI wafer (102) includes an insulator layer (104) and an upper silicon layer (106). The upper silicon layer (106) includes at least one component of the active electronic device and at least one component of the optical device. The method includes projecting the lithography mask (6312) onto the SOI wafer (102) in order to simultaneously pattern the component of the active electronic device and the component of the optical device on the SOI wafer (102).



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	2 0 21 0 5 0 27 15 1 10						
A. CLASSIFICATION OF SUBJECT MATTER IPC(7) : H01L 21/00; G02B 6/26, 6/42; G06G 7/48 US CL : 438/69; 385/30; 703/4, 6 According to International Patent Classification (IPC) or to both national classification and IPC							
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Minimum documentation searched (classification system followed by classification symbols) U.S.: 438/69, 29; 385/30, 33, 36, 37, 43, 45, 49; 703/4, 6							
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched							
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) Please See Continuation Sheet							
C. DOCUMENTS CONSIDERED TO BE RELEVANT							
Category * Citation of document, with indication, where a		Relevant to claim No.					
X US 5,838,870 A (Soref) 17 November 1998 (17.11.9	98), Abstract, cols 4-6, Figs. 2-4.	1-4, 6, 10, 11, 33, 36, 37, 39, 43-46, 56, 57, 60, 63, 65, 66, 67, 96-100, 102, 103					
		5, 7-9, 31, 32, 34, 35, 41, 42, 58, 59, 61, 64, 70-74, 90-95, 101, 104-118					
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Y		9, 31, 32, 34, 35, 42, 69, 90-95					
Further documents are listed in the continuation of Box C.	See patent family annex.						
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"P" document published prior to the international filing date but later than the priority date claimed	"&" document member of the same patent	family					
Date of the actual completion of the international search 06 November 2002 (06.11.2002)	Date of mailing of the international sear	ch report					
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C. (Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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INTERNATIONAL SEARCH REPORT	
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Continuation of B. FIELDS SEARCHED Item 3:	
EAST: optoelectronic, optical, electronic, SOI, silicon-on-insulator, semiconduct	or-on-insulator, lithography, patterning, waveguide,
Fabry-Perot cavity, multiplexer, demultiplexer, mirror, lens, deflector, evanescen	it, coupler, photonic band gap, photonic crystal,
photonic waveguide, topography, simulation, carrier, etch	