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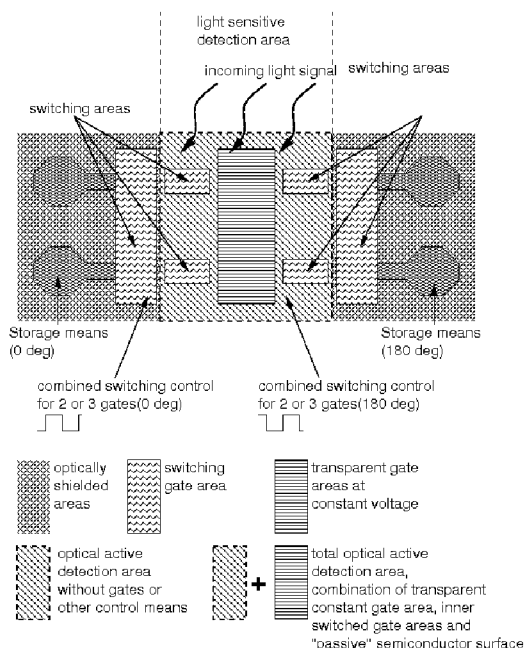
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(54) Title: SWITCH AND GATE TOPOLOGIES FOR IMPROVED DEMODULATION PERFORMANCE OF TIME OF FLIGHT PIXELS

Fig. 11



(57) Abstract: A pixel for detection and demodulation of intensity-modulated light comprises a central light-sensitive region, in which charge carriers are generated in response to light impinging thereon; at least a first and a second storage cells arranged opposite one another with respect to the light-sensitive region, the storage cells being shielded against incident light; at least a first and a second transfer path for transferring the charge carriers generated in the central light-sensitive region alternately to the first and the second storage cell, respectively; wherein each of the first and second transfer paths comprises (a) at least two switching gates arranged in series between the light-sensitive region and the first and second storage cell, respectively, and/or (b) at least one switching gate implemented as a stripe gate.



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SWITCH AND GATE TOPOLOGIES FOR IMPROVED DEMODULATION PERFORMANCE OF TIME OF FLIGHT PIXELS

Technical field

[0001] The present invention relates to “Time of Flight” sensors or cameras, in
5 general: semiconductor sensors for the detection of electromagnetic waves,
demodulation and switching demodulators.

Introduction

[0002] The time-of-flight measurement principle is well known in the field of 3D
imaging. 3D cameras (or range cameras) are known that acquire range images in
10 real time based on the time-of-flight (TOF) principle. Such camera generally
comprises a light source emitting sinusoidally modulated light into the scene to be
imaged in 3D and a sensor pixel array on which the scene is imaged by an optical
system. Sensor pixels will hereinafter be referred to as “pixels” for conciseness.
The camera then correlates the light detected in the pixels with the light emitted
15 and determines, for each pixel, the phase difference between emitted and
received light. This phase difference is proportional to the radial distance between
the camera and the part of the scene that is imaged onto the pixel concerned. As
the demodulation is synchronously performed for all pixels of the pixel array, the
camera provides an array of distance values associated each to a particular pixel
20 and thus to a particular part of the scene. In the following, we will also use “phase”
instead of “phase difference”; it is understood that the phase of the emitted light or
a clock signal, used for modulating the emitted light or derived from the modulation
of the emitted light, then serves as a reference phase. It should also be noted that,
as used herein, “phase” and “phase difference” always refer to the phase of the
25 modulation, not to the phase of the carrier wave that is modulated.

[0003] The demodulation process, which leads to the determination of the phase
of the light impinging on the pixels, can be carried out in different ways.
EP 0 792 555 discloses a 3D camera with a one- or two-dimensional pixel array,
each pixel thereof comprising a light-sensitive part, in which charge carriers are
30 generated in response to light impinging thereon, and a light-insensitive part with a
plurality of electrical switches and storage cells associated with a respective one of

these switches. The charges that are integrated in the light-sensitive part are transferred to the storage cells by sequential actuation of the electrical switches. The electrical switches are controlled in such a way that the charges transferred to a particular storage cell belong to a time interval or time intervals at a known phase of the emitted light. The charges accumulated in the different storage cells are then used to determine the phase of the light having impinged on the pixel, its amplitude and a background light level. More details on that principle of measurement can be found in T. Spirig's doctoral thesis "Smart CDD/CMOS Based Image Sensors with Programmable Real-Time, Temporal and Spatial Convolution Capabilities for Applications in Machine Vision and Optical Metrology" (Diss ETH 11993, 1997), especially in section 4.3.

[0004] This invention targets to the area of semiconductor sensors for the detection of phase information from received modulated electromagnetic waves by demodulation. The smallest unit of such a sensor is a pixel. In such a pixel, RF-modulated electromagnetic waves reflected in a scene are received and the separated charges demodulated and guided to two or more storage elements. Since the demodulation is done at RF frequencies, the charge transport and the shutter for the storage elements has to be very fast.

[0005] German patent application DE 197 04 496 A1 discloses a process and a device for determining phase and/or amplitude information of an electromagnetic wave. This application describes pixels with large-area gate structures, which are simultaneously used for detection and demodulation. A pixel with only one modulated/switched gate between or inside the detection region is described. The gates are transparent.

[0006] EP 1 624 490 A1 discloses a large-area pixel for use in an image sensor. The application describes various gate topologies. The gates have at least two terminals and are traversed by currents to generate voltage gradients in the gates and thus potential gradients in the semiconductor substrate below.

General Description of the Invention

[0007] In order to improve the optical-electrical performance of such a pixel and simultaneously reduce the requirements for the RF pixel control electronics stripe

gate topologies can be used as switches and constant voltage gates. On one hand, these stripe gates may help to reduce the gate capacitances to be switched and thus reducing the RF current during demodulation. On the other hand these topologies may improve the optical performance by enlarging the optical active area due to less pixel areas with optical cover and more areas without poly-silicon gates. Moreover, this approach allows the series connection of more than one switch between the detection area and the storage element without too much loss of optical active area. These multi stage switch topologies may further improve the pixel demodulation performance. Using such pixels, it is possible to construct single pixels, row sensors or area sensor. Pixel Operation: Charges separated in the semiconductor sensor by received electromagnetic waves are collected and transported to either of two or more storage means by electrical controlled switches.

[0008] The invention has two basic aspects, which are described below:

[0009] (a) Series connected multi stage switches: for the performance of a demodulating pixel it may be advantageous to have a demodulator, which comprises of more than one switch in each path from the detector to the storage element. Therefore the idea is to add one or more switching stages on the path between the detection region and the major demodulation switch. These additional switches are added in every path to the storage elements. The additional switches may improve the shutter performance in comparison with a single switch and thus improve the demodulation contrast. Moreover these additional shutters may additionally accelerate charges on their way to the storage element.

[0010] A Pixel for detection and demodulation of intensity-modulated light according to the first aspect of the invention preferably comprises:

- a central light-sensitive region, in which charge carriers are generated in response to light impinging thereon;
- at least a first and a second storage cells, possibly arranged opposite one another with respect to the light-sensitive region, the storage cells being shielded against incident light;

- at least a first and a second transfer path for transferring the charge carriers generated in the central light-sensitive region alternately to the first and the second storage cell, respectively, and wherein

each of the first and second transfer paths comprises at least two switching gates arranged in series between the light-sensitive region and the first and second storage cell, respectively.

[0011] (b) Stripe and area switch gate topologies: If the sensor is produced in CMOS or CCD technology, switching and constant voltage gates are made from poly-silicon. Thus each gate in the optical active area adds more boundary surfaces, which possibly corrupt the optical response. Moreover, it might be necessary to produce gates from opaque materials or cover them with opaque material (e.g. salicided poly-silicon). This, in turn reduces the optical active area of the pixel, the optical fill factor and the sensitivity. Therefore, the idea is to layout the gates as a repeated or single stripe topology rather than a full area topology.

The idea includes combinations of full area gates with stripe gates. The choice of stripe or area gates depends on the influence of the gate topology on the pixel performance. Whenever it is advantageous for the pixel performance, stripe gates should be chosen. Another benefit of stripe gates is the reduced RF demodulation power or current due to reduced gate capacitances. The stripe gates may be considered as switches. The gates have only one terminal are not flown through by currents and have no voltage gradient.

[0012] A Pixel for detection and demodulation of intensity-modulated light according to the second aspect of the invention preferably comprises:

- a central light-sensitive region, in which charge carriers are generated in response to light impinging thereon;
- at least a first and a second storage cells, possibly arranged opposite one another with respect to the light-sensitive region, the storage cells being shielded against incident light;
- at least a first and a second transfer path for transferring the charge carriers generated in the central light-sensitive region alternately to the first and the second storage cell, respectively, and wherein

each of the first and second transfer paths comprises at least one switching gate configured as a stripe gate, i.e. a switching gate, the width of which is substantially less than the width of the light-sensitive region, or the overall width of the storage cells.

5 [0013] Aspects (a) and (b) may be combined in embodiments of the invention.

Brief Description of the Drawings

[0014] Preferred embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings in which:

Fig. 1 is a schematic cross sectional view of a conventional ToF (time-of-flight) pixel with a combined detection and demodulation region;

10

Fig. 2 is a schematic cross sectional view of a conventional ToF pixel with separated detection and switching (demodulation) regions;

Fig. 3 is a schematic cross sectional view of a two-stage version of a ToF pixel with combined detection and demodulation region according to the first aspect of the invention;

15

Fig. 4 is a schematic cross sectional view of a two-stage version of a ToF Pixel with separated detection and switching (demodulation) regions according to the first aspect of the invention

Fig. 5 is a schematic illustrating parallel connection of multi stage demodulators with a combined detection and demodulation area in one pixel;

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Fig. 6 is a schematic illustrating parallel connection of multi stage switches with separated detection and demodulation area in one pixel;

Fig. 7 is a top schematic view of a CMOS or CCD implementation of a conventional ToF pixel with combined detection and demodulation region as in Fig. 1;

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Fig. 8 is a top schematic view of a CMOS or CCD implementation of a conventional ToF pixel with separated detection and demodulation regions;

Fig. 9 is a top schematic view of a CMOS or CCD implementation of a ToF pixel according to the present invention, separated detection and two-stage demodulation regions, two stage switches, inner switches as stripes;

Fig. 10 is an illustration of the optically active and the covered areas of the pixel in Figure 9;

Fig. 11 is a top schematic view of a CMOS or CCD implementation of a ToF pixel according to the present invention, combined detection and demodulation region and an additional separated switch gate, inner switches as stripes;

Fig. 12 is an illustration of optically active and covered areas of the pixel in Figure 11;

Fig. 13 is a schematic top view of a CMOS or CCD implementation of an example ToF pixel according to the present invention, separated detection and demodulation region, 2-stage parallel switches, all switches as stripe gates;

Fig. 14 is a schematic top view of a CMOS or CCD implementation of an example ToF pixel according to the present invention, separated detection and demodulation region, 2-stage parallel switches, all switch gates and constant gates as stripes;

Fig. 15 is a schematic top view of a CMOS or CCD implementation of an example of a ToF pixel according to the present invention, separated detection and demodulation region, 2-stage switches, inner switch gates as single stripes.

Description of Preferred Embodiments

Aspect (a)

[0015] Conventional demodulator pixels implemented in CMOS or CCD technology comprise of an optical active area for detection and charge separation, demodulation means (gates, switches) and storage means (storage cells). Fig. 1 shows such a pixel with a combined detection and demodulation means ("modulation photo gates"). The pixel structure of Fig. 1 is e.g. known from DE 197 04 496 A1. A similar pixel is shown in Fig 2. However, here the detection means is strictly separated from the demodulation or switching means. The switches are optically shielded. Both structures have in common that there is only

one controlled switching or demodulation means from the detection area to each storage means. The pixel structure of Fig. 2 is e.g. known from EP 0 792 555.

[0016] In contrast, according to the first aspect of the invention, a pixel has more than one controlled switching or demodulation means (switching or demodulation gate) on the transfer path from the light-sensitive region to each storage means (storage cell). Examples of pixels according to the first aspect of the invention are illustrated in Figs. 3 and 4. These drawings illustrate such pixels with multi-stage switches or demodulators having two gates on each path. However, this aspect of the invention is not restricted to two stages. Indeed, any number of stages greater than 1 may be used. The pixel of Fig. 3 has a combined detection and demodulation region with two switched stages on each path to a storage cell. The inner switches are 1a and 1b, the outer switches are 2a and 2b and 0 is a static (remaining at constant potential) part of the detection region, which is not necessarily present in such a pixel type. The pixel of Fig. 4 has separate detection and demodulation regions: the detection region (light-sensitive region in which the charge carriers are generated when light impinges thereon) is exposed to incoming light, whereas the demodulation regions (the switching or demodulation gates) are covered with an opaque shield.

[0017] The first aspect of the invention includes the parallel connection of multi-stage switches or demodulators in a single pixel. Figs. 5 and 6 illustrate examples of such parallel connections for the pixel types of Figs. 3 and 4, respectively. The number of parallel connected multi stage structures is not restricted to three as in the drawings but can be any number greater than or equal to 1. The invention is intended to cover also all possible combinations of parallel-connected stages and single path stages as well as connections of the parallel paths between the stages.

[0018] The switching or demodulation means on the path to a storage cell can be either controlled by the same signal or by different signals with any possible timing and shape but with the same basic frequency.

[0019] To all gate stages, special static or dynamic signals can be applied in order to improve the pixel behaviour during hold (shut) time and during reset.

Aspect (b)

[0020] If a ToF pixel is implemented in CMOS or CCD technology, the common approach is to use “area gates”, i.e. switching or demodulation gates, the width of which corresponds to the entire width of the paths to the storage cells associated with the pixel, or to the width of the optical active area (the light-sensitive region). Examples of conventional pixels are depicted in Figs 7 and 8. Fig. 7 shows a schematic top view of the pixel with combined detection and demodulation area of Fig. 1. There is no optical shield on top of the RF controlled demodulation gates. Fig. 8 shows a comparable pixel structure but here with separate detection and demodulation regions. The demodulator gates are entirely covered with an optical shielding.

[0021] According to the second aspect of the invention some or all switching or demodulation gates in the transfer paths to the storage cells are configured as “stripe gates”, i.e. switching or demodulation gates, the width of which is substantially less than the width of the light-sensitive region, or the overall width of the storage cells. The width of the stripe gates preferably amounts to at most 50%, more preferably to at most 30%, possibly to at most 25% and possibly even to at most 20% of the width of the light-sensitive region. The stripe gates can be either connected in a metal layer or in the same poly-silicon layer over field oxide. The second aspect of the invention is intended to cover any combination of stripe and area gates, if at least one switching or demodulation gate is arranged as a stripe gate. A gate, which consists of one stripe only and whose stripe width is significantly smaller than that of a neighbouring area gate is considered to be a stripe gate in the context of the present description, too. The switching or demodulation gates implemented as stripe gates may be part of the light-sensitive region, or, alternatively, be covered by an optical shield.

[0022] Fig. 9 shows an example of a pixel structure according to both aspects of the present invention. The light-sensitive inner constant voltage gate and the outer switching gates are implemented as area gates. The inner switching gates are implemented as stripe gates. In Fig. 9, the pixel comprises four storage cells and four transfer paths associated with one of the storage cells, respectively. Each transfer path includes at least one switching or demodulation gate implemented as

a stripe gate. However, the number of stripe gates and the orientation of the stripe gates is not limited to the illustrated examples. In the example of Fig. 9, all switching gates are covered with an optical shield. The shown pixel thus has strictly separated detection and demodulation areas. Figure 10 illustrates the optical active and optically covered areas of the pixel of Fig. 9.

[0023] Fig. 11 shows the same gate structure as in Fig. 9 but with different optical cover. Here, the inner stripe gates are without optical cover. The pixel thus comprises a combined detection and demodulation area (consisting here of the central constant-voltage gate and the inner transparent stripe gates) and optically shielded outer area switching gates. Fig. 12 illustrates the optical active and the optically shielded areas of the pixel of Fig. 11.

[0024] More examples of possible gate configurations using multi-stage switching or demodulating gates, at least some of which are implemented as stripe gates, are depicted in Figs. 13-15. All examples could be modified by changing the area of the optical shielding.

[0025] It should also be noted that the second aspect of the invention is not limited to multi-stage switches or demodulators on the transfer paths. In order to keep this description simple, examples with single-stage switches or multi-stage-switches with three or more stages have not been illustrated in the drawings.

[0026] The area between the stripe gates may be filled with the standard isolation and passivation stack of the used technology or with a special optical window stack in order to improve the response of the pixel to the impinging light.

Claims

1. Pixel for detection and demodulation of intensity-modulated light, comprising
a central light-sensitive region, in which charge carriers are generated in response to light impinging thereon;
at least a first and a second storage cells, preferably arranged opposite one another with respect to said light-sensitive region, said storage cells being shielded against incident light;
at least a first and a second transfer path for transferring said charge carriers generated in said central light-sensitive region alternately to said first and said second storage cell, respectively,
characterized in that each of said first and second transfer paths comprises at least two switching gates arranged in series between said light-sensitive region and said first and second storage cell, respectively.
2. Pixel as claimed in claim 1, wherein at least one of said least two switching gates arranged in series between said light-sensitive region and said first and second storage cell, respectively, is configured as a stripe gate.
3. Pixel for detection and demodulation of intensity-modulated light, comprising
a central light-sensitive region, in which charge carriers are generated in response to light impinging thereon;
at least a first and a second storage cells, preferably arranged opposite one another with respect to said light-sensitive region, said storage cells being shielded against incident light;
at least a first and a second transfer path for transferring said charge carriers generated in said central light-sensitive region alternately to said first and said second storage cell, respectively,
characterized in that each of said first and second transfer paths comprises at least one switching gate configured as a stripe gate.
4. Pixel as claimed in claim 3, wherein each of said first and second transfer paths comprises at least two switching gates arranged in series between said light-sensitive region and said first and second storage cell, respectively.

5. Pixel as claimed in claim 2 or 4, wherein said at least one switching gate configured as a stripe gate is closer, on said first or second transfer path, to said light-sensitive region than to the respective storage cell.
6. Pixel as claimed in any one of claims 1 to 5, wherein each of said first and second transfer paths comprises at least one switching gate configured as an area gate.
7. Pixel as claimed in any one of claims 2 to 6, wherein the width of the stripe gates preferably amounts to at most 50%, more preferably to at most 30%, possibly to at most 25% and possibly even to at most 20% of the width of the light-sensitive region.
8. Pixel as claimed in any one of claims 1 to 7, wherein at least part of said switching gates form or are part of a peripheral light-sensitive region in which charge carriers are generated in response to light impinging thereon.
9. Pixel as claimed in any one of claims 1 to 8, wherein at least part of said switching gates are shielded against incident light.
10. Pixel as claimed in any one of claims 1 to 9, wherein at least part of said switching gates are transparent to incident light.

Fig. 1 (Related Art)

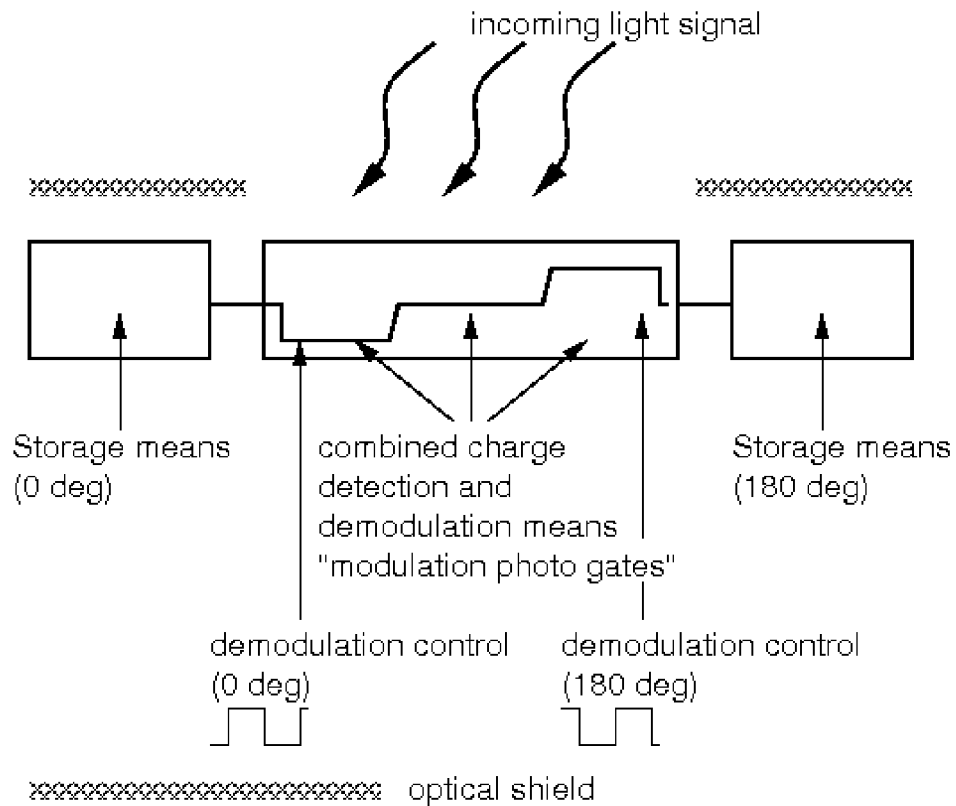


Fig. 2 (Related Art)

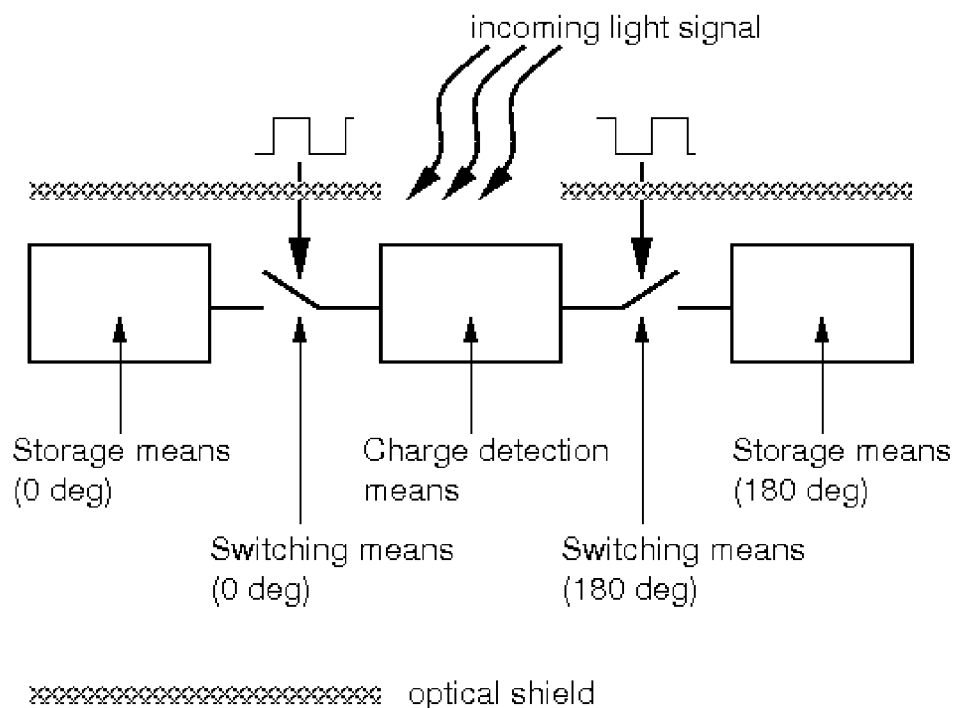


Fig. 3

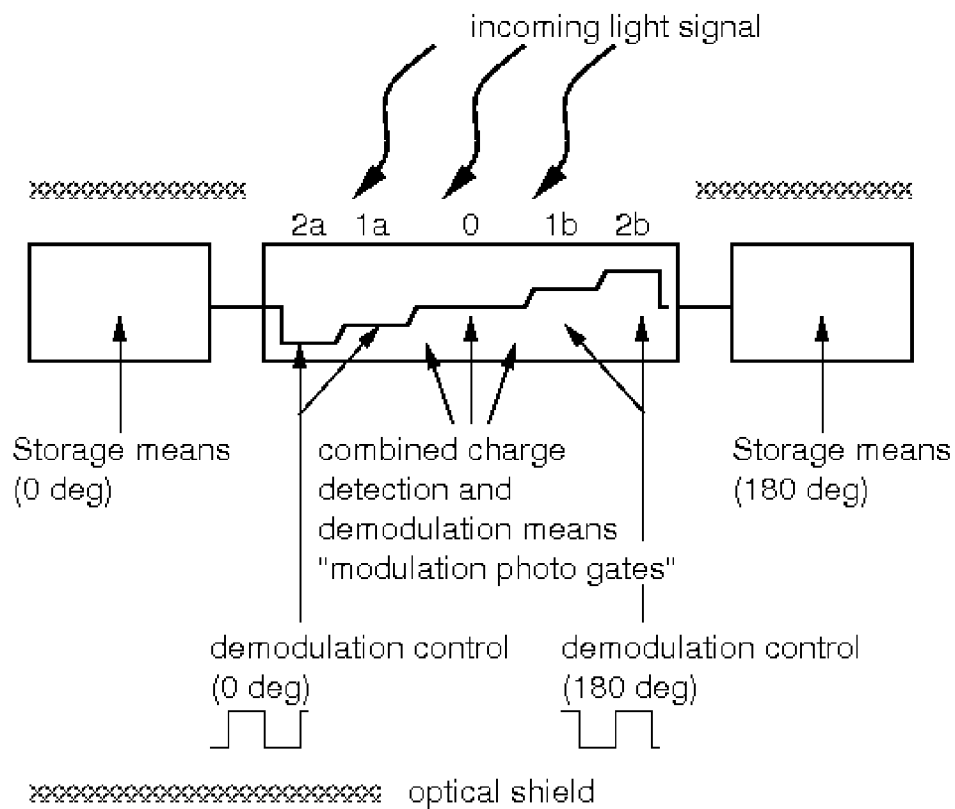


Fig. 4

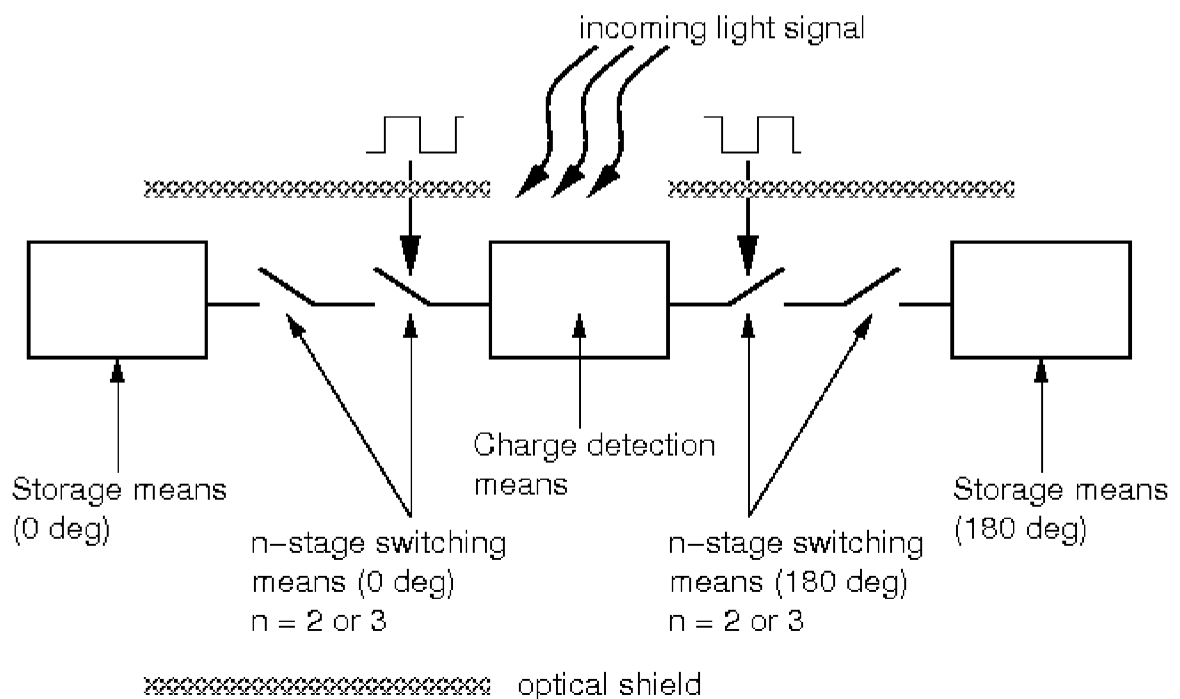


Fig. 5

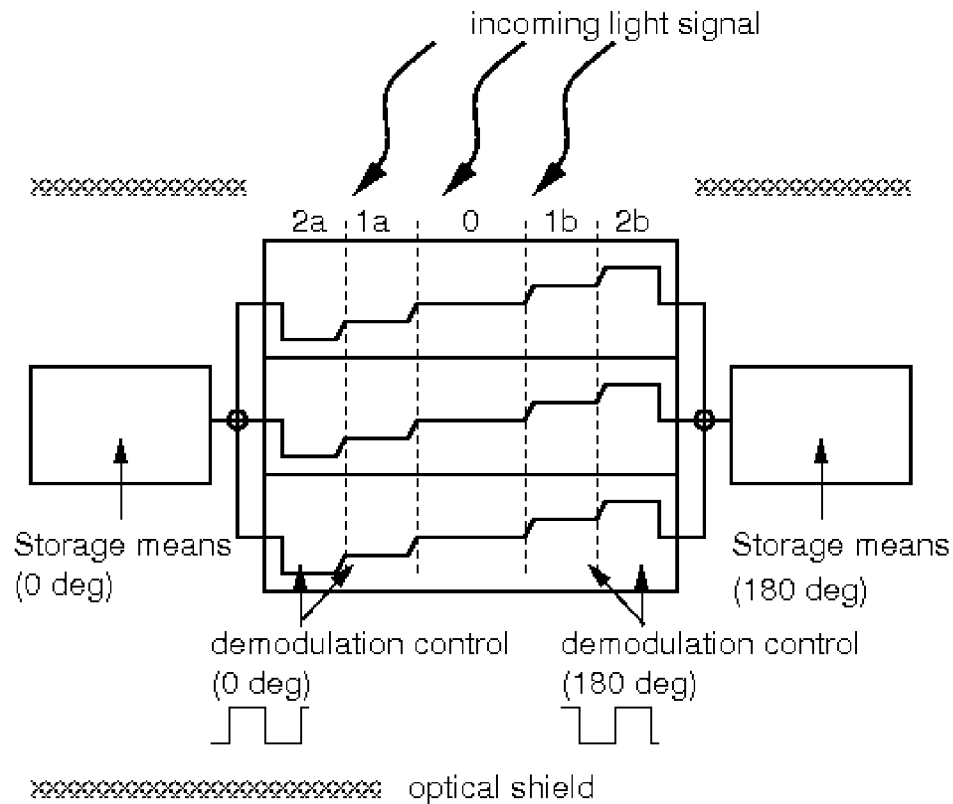


Fig. 6

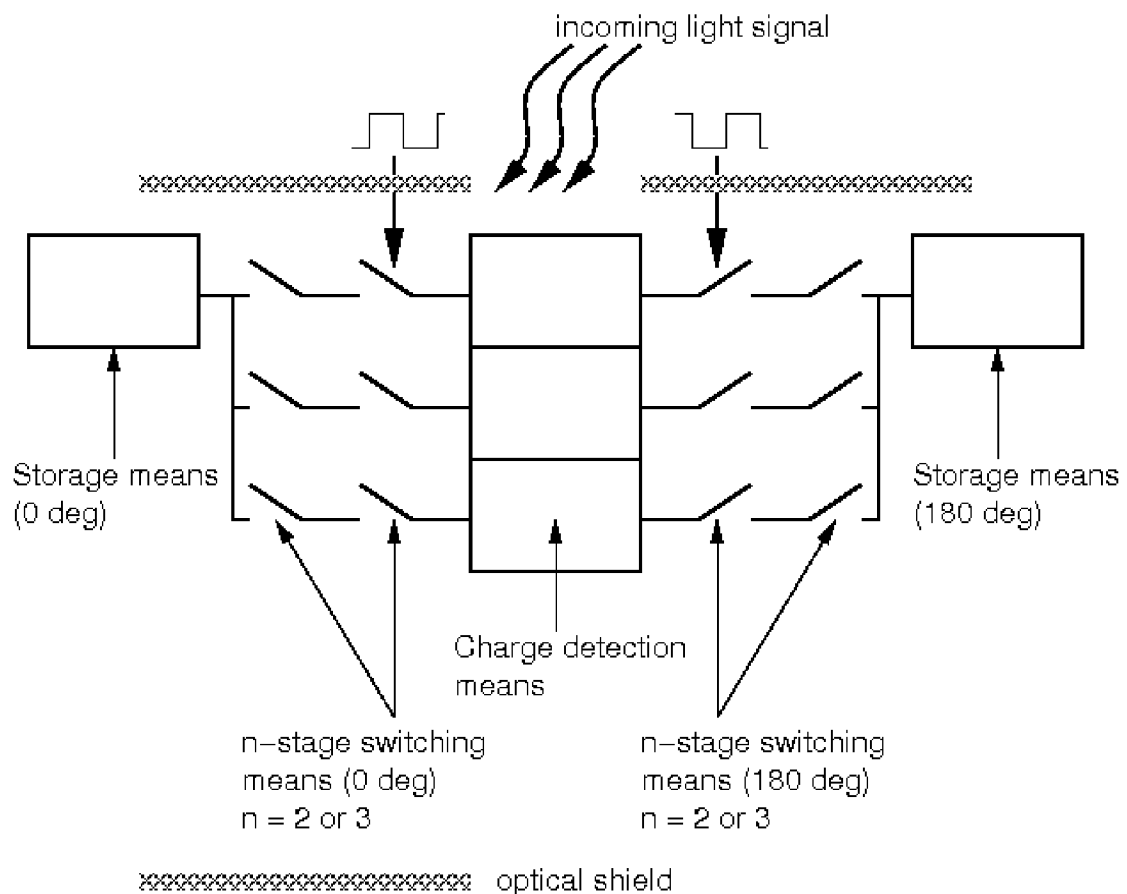


Fig. 7 (Related Art)

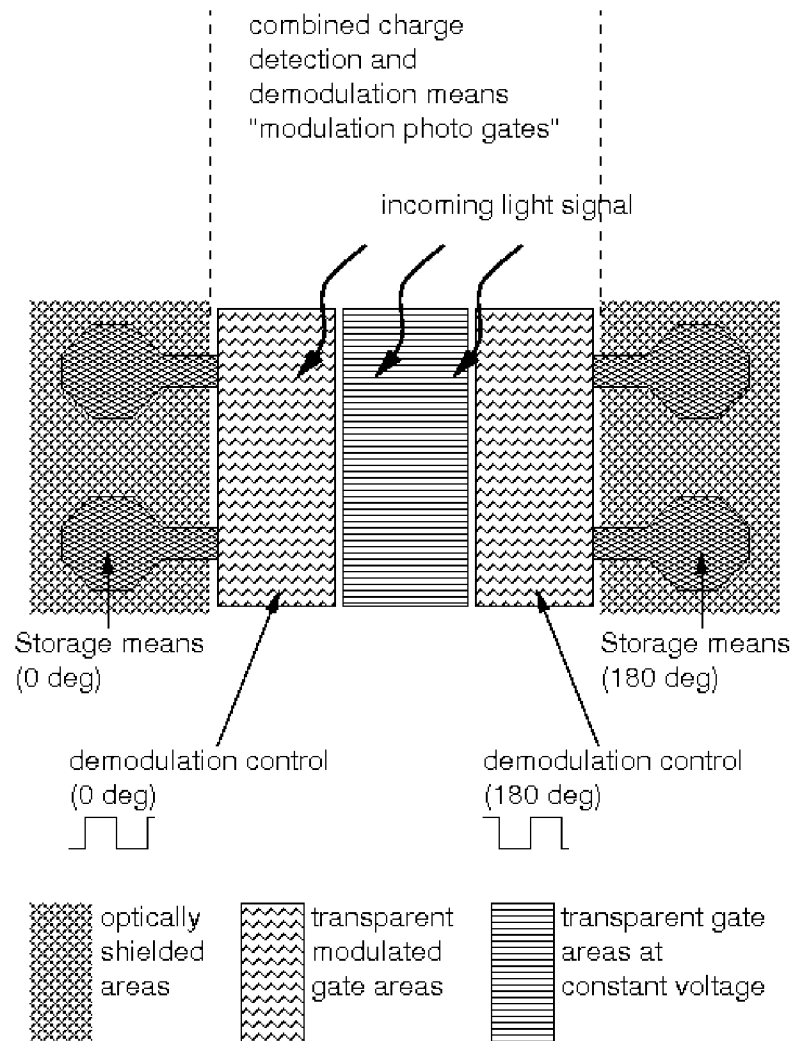


Fig. 8 (Related Art)

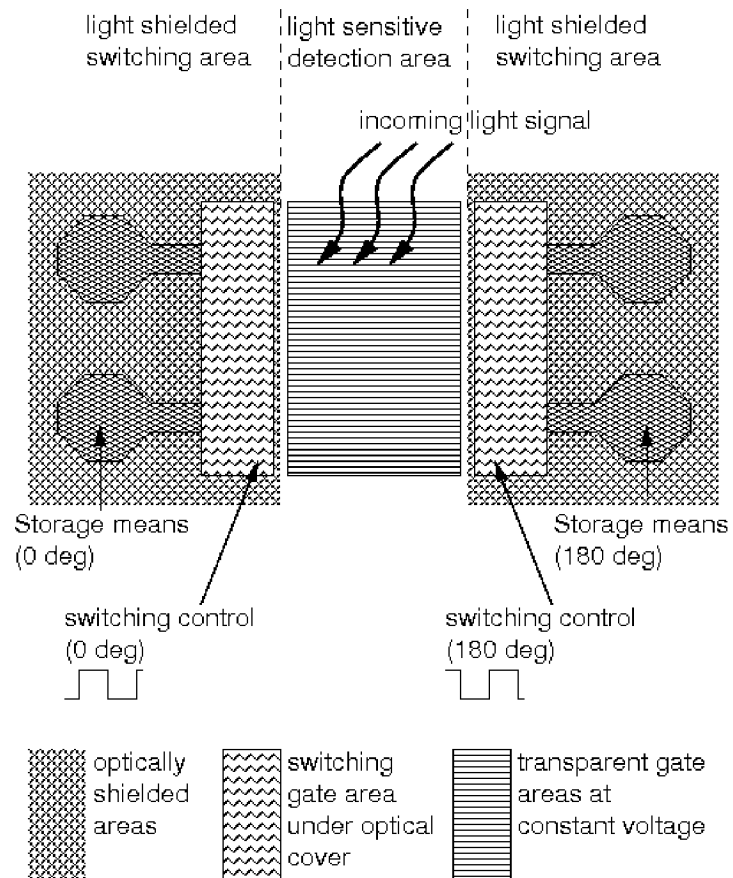


Fig. 9

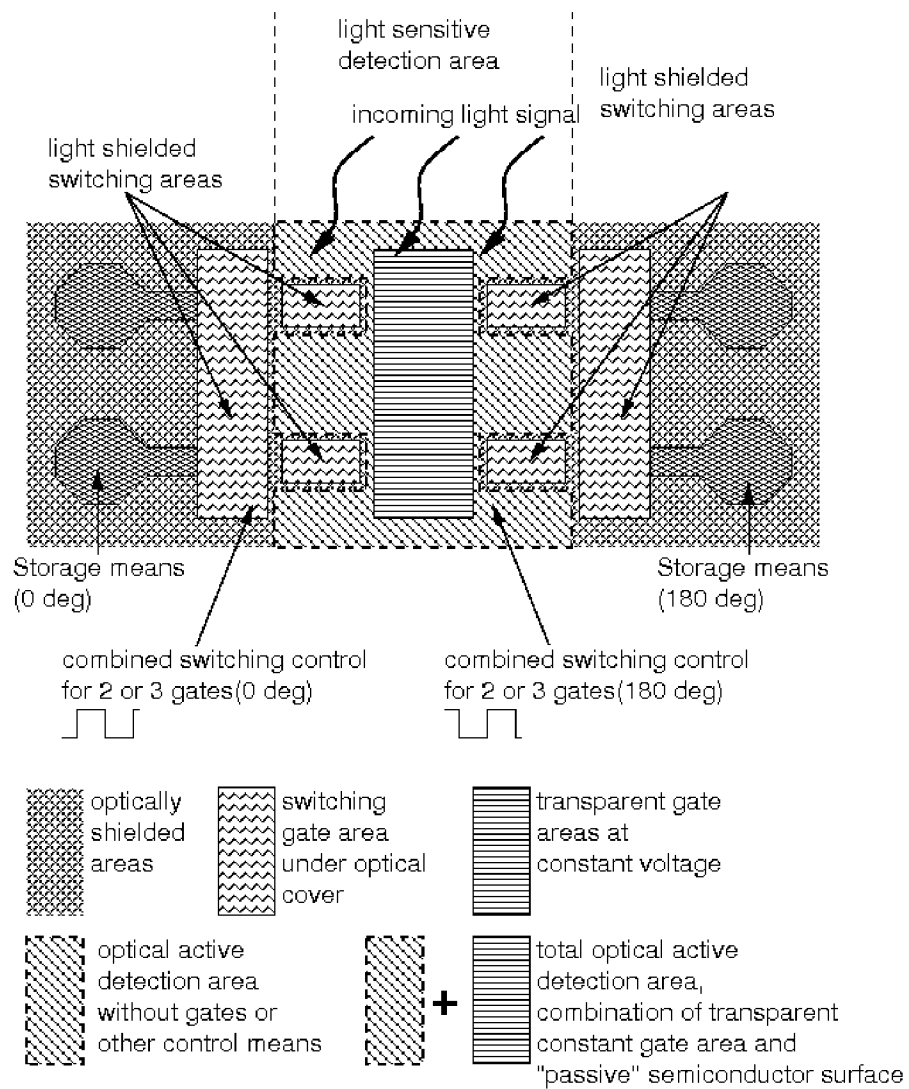


Fig. 10

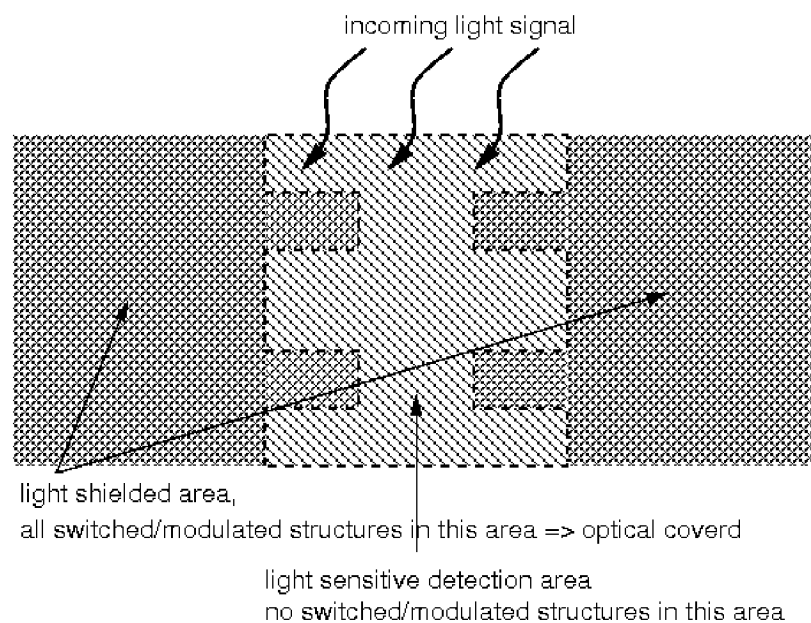


Fig. 11

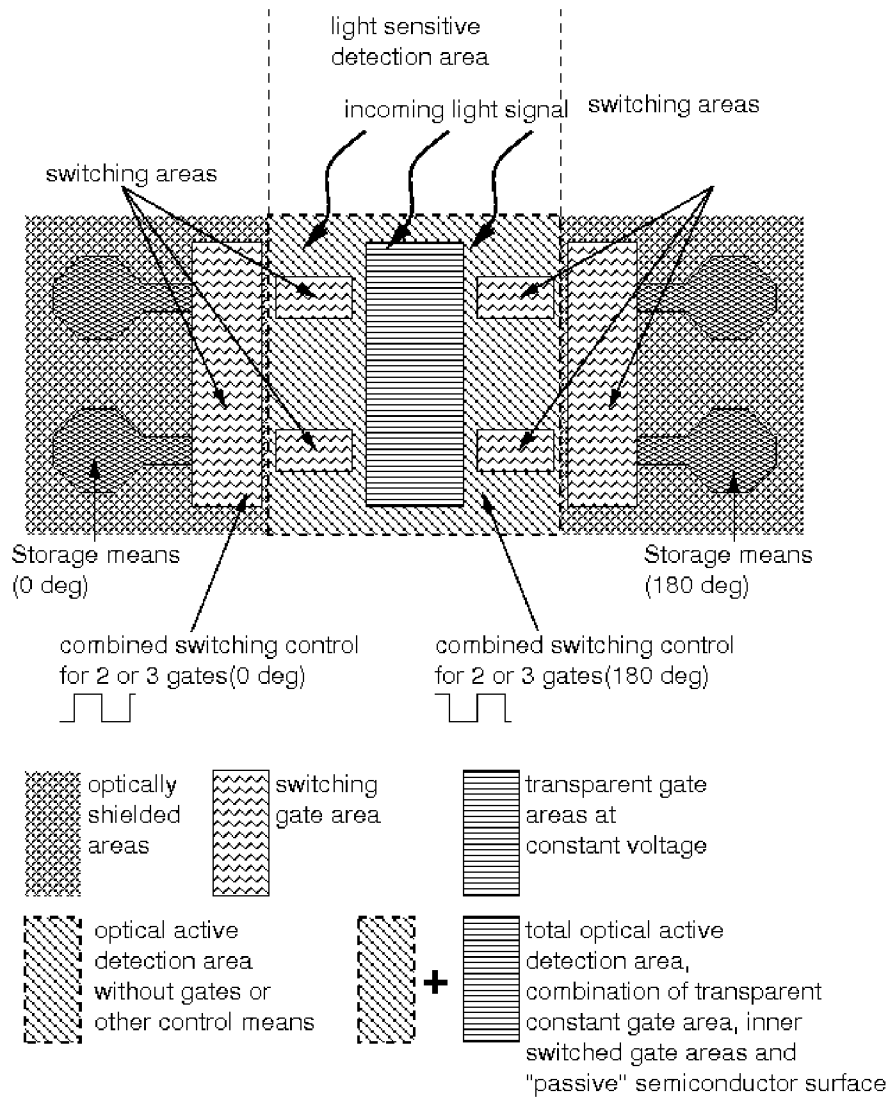


Fig. 12

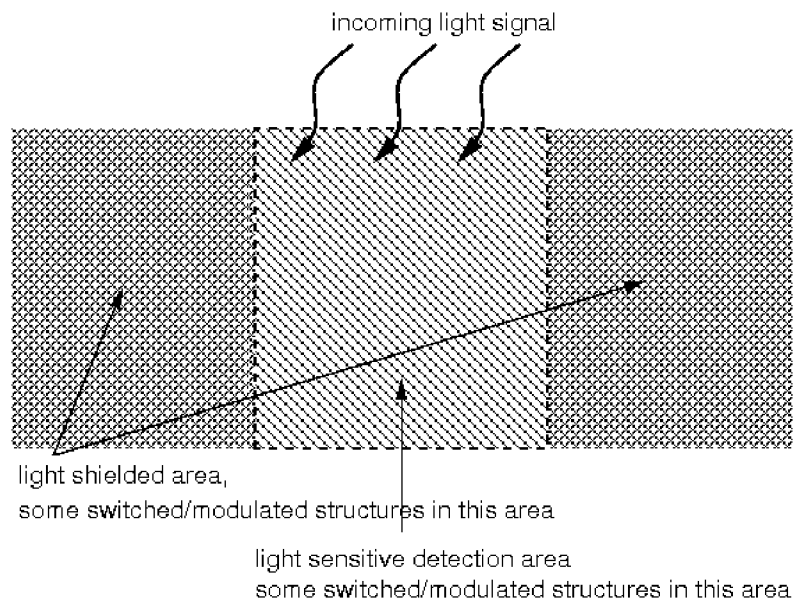


Fig. 13

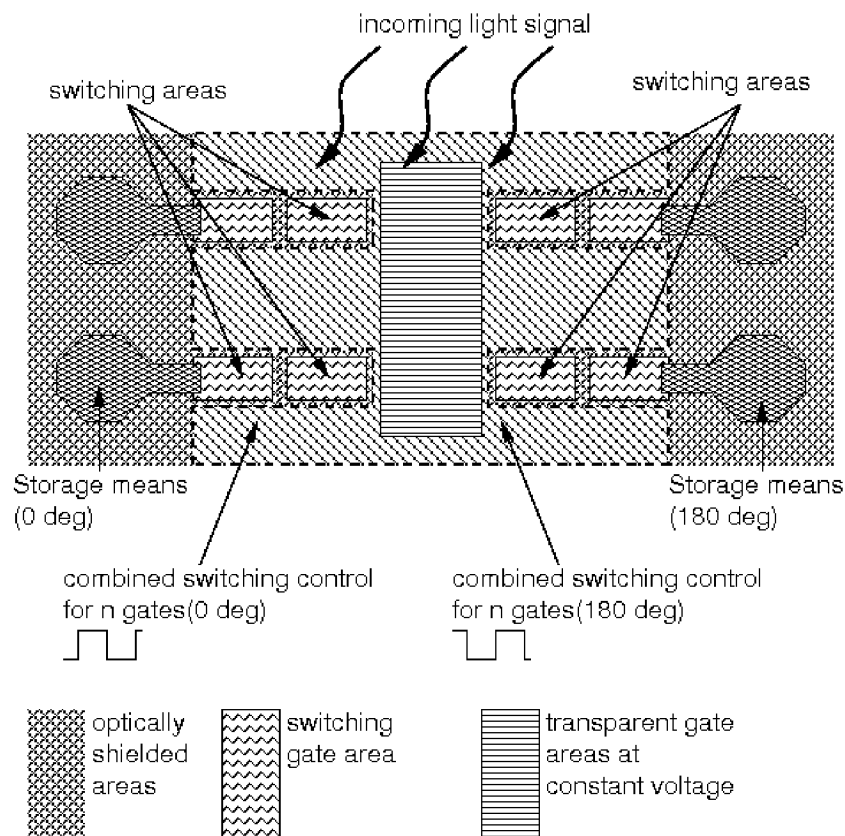


Fig. 14

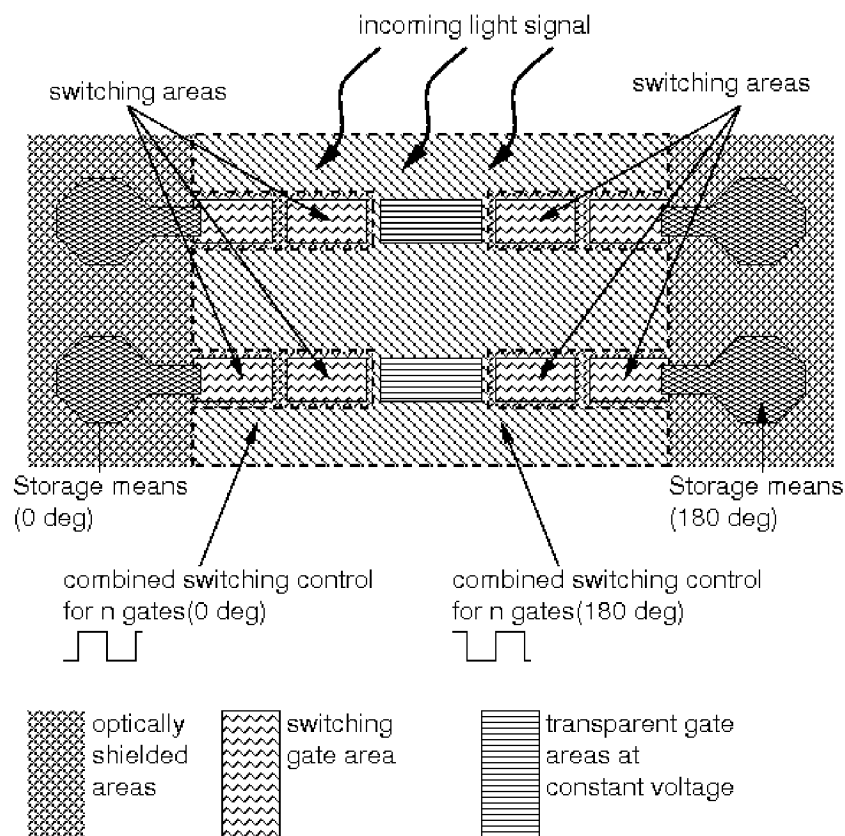
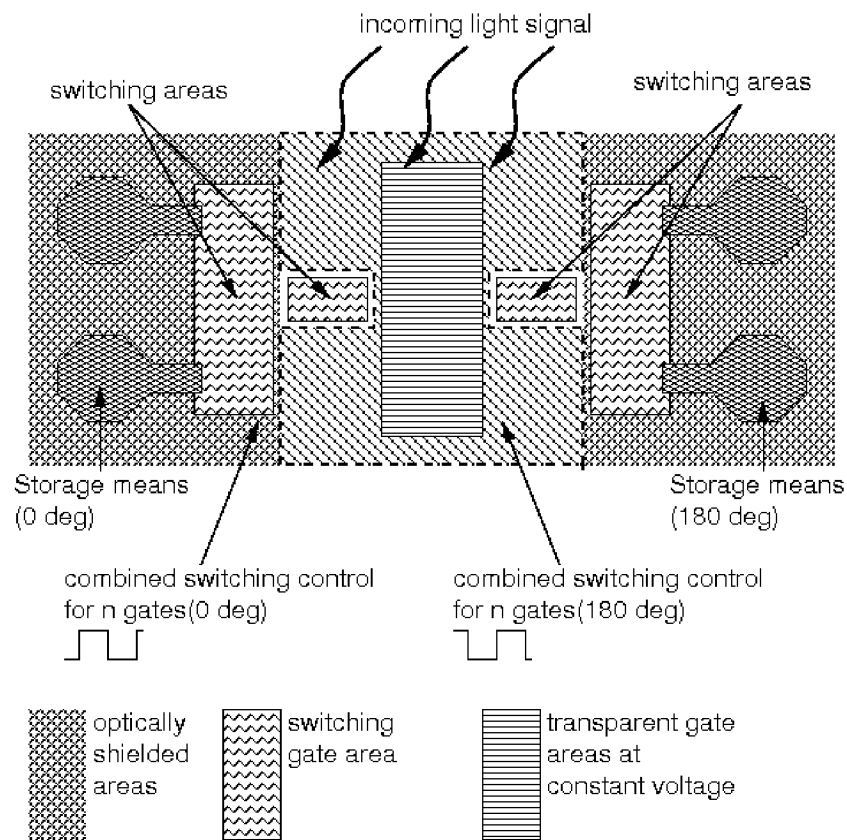


Fig. 15



INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2011/059878

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L27/144
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L G01S H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009/134396 A1 (KAWAHITO SHOJI [JP] ET AL) 28 May 2009 (2009-05-28) paragraphs [0030] - [0042]; figures 2-5 -----	1-10
X	US 2007/158770 A1 (KAWAHITO SHOJI [JP]) 12 July 2007 (2007-07-12) paragraphs [0029] - [0053]; figures 1-2,5,7 -----	1-10



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

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Date of the actual completion of the international search

16 November 2011

Date of mailing of the international search report

22/11/2011

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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