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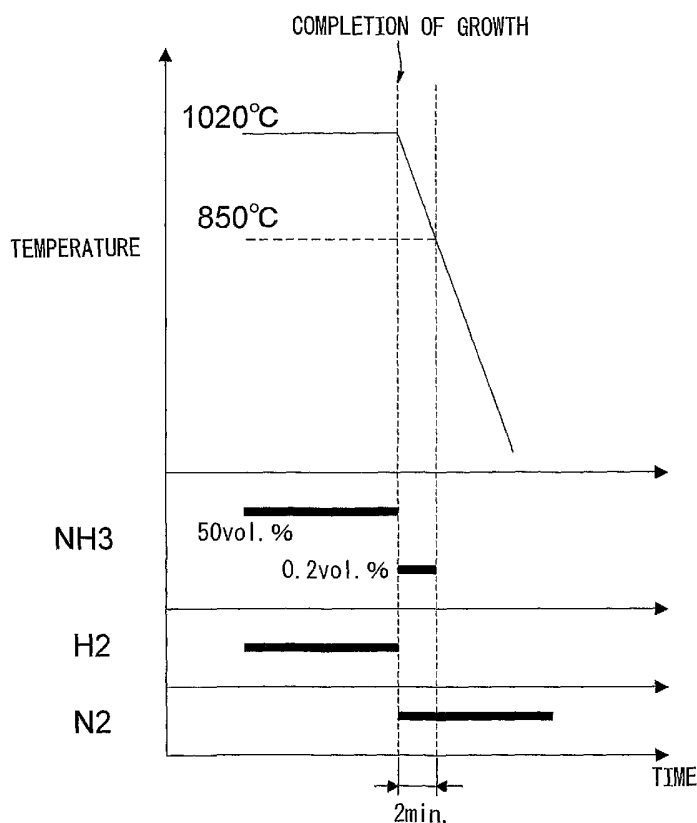
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(54) Title: P-TYPE GROUP III NITRIDE SEMICONDUCTOR AND PRODUCTION METHOD THEREOF



(57) Abstract: An object of the present invention is to provide a method for producing a p-type Group III nitride semiconductor which can be used to produce a light-emitting device exhibiting a low operation voltage and a sufficiently high reverse voltage. The inventive method for producing a p-type Group III nitride semiconductor comprises, during lowering temperature after completion of growth of a Group III nitride semiconductor containing a p-type dopant, immediately after completion of the growth, starting, at a temperature at which the growth has been completed, supply of a carrier gas composed of an inert gas and reduction of the flow rate of a nitrogen source; and stopping supply of the nitrogen source at a time in the course of lowering the temperature.



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DESCRIPTION

P-TYPE GROUP III NITRIDE SEMICONDUCTOR AND PRODUCTION
METHOD THEREOF

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Cross Reference to Related Application

This application is an application filed under 35 U.S.C. §111(a) claiming benefit, pursuant to 35 U.S.C. §119(e)(1), of the filing date of the Provisional Application No.60/572,269 filed on May 19, 2004, pursuant to 35 U.S.C. §111(b).

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Technical Field

The present invention relates to a method for producing a p-type Group III nitride semiconductor and to a Group III nitride semiconductor light-emitting device produced by the method. More particularly, the present invention relates to a method for producing a p-type Group III nitride semiconductor, the method being capable of producing a light-emitting device exhibiting a low forward voltage (V_f) and a sufficiently high reverse voltage (V_r) at a high yield.

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Background Art

In recent years, Group III nitride semiconductor materials have become of interest as materials for producing light-emitting devices which emit light of a short wavelength. Generally, a Group III nitride semiconductor material is grown on a substrate made of an oxide crystal such as a sapphire single crystal, or a Group III-V compound single crystal, through a method such as metal-organic chemical vapor deposition (MOCVD), molecular-beam epitaxy (MBE), or hydride vapor phase epitaxy (HVPE).

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For a long time, a p-type Group III nitride semiconductor having a sufficient carrier concentration was difficult to produce. However, recent studies have

revealed that a p-type Group III nitride semiconductor having a sufficient carrier concentration can be produced through, for example, irradiating an Mg-doped gallium nitride (GaN) with a low-energy electron beam (see
5 Japanese Laid-Open Patent Application (*kokai*) No. 2-257679) or heating an Mg-doped gallium nitride in a hydrogen-free atmosphere (see Japanese Laid-Open Patent Application (*kokai*) No. 5-183189). One conceivable mechanism for yielding a p-type Group III nitride
10 semiconductor having a sufficient carrier concentration is that a p-type dopant which is contained in the semiconductor and which has been passivated with hydrogen is activated through dehydrogenation on the basis of the aforementioned techniques. Actually, in Mg-doped gallium
15 nitride semiconductor which was activated by an annealing, the concentration of hydrogen atoms is about 1/10 of the concentration of Mg atoms.

Generally, a Group III nitride semiconductor having high crystallinity is grown through metal-organic
20 chemical vapor deposition (MOCVD). However, in a crystal growth apparatus employed in MOCVD, hydrogen molecules, hydrogen radicals, and atomic hydrogen, which are formed through decomposition of hydrogen gas (serving as a carrier gas for conveying source compounds to a
25 substrate) or ammonia (NH₃) serving as a nitrogen source, are present at high concentrations. These hydrogen species are incorporated into a Group III nitride semiconductor crystal layer, during the growth thereof, and bond to a p-type dopant added to the crystal during
30 cooling of the crystal layer from a growth temperature. The p-type dopant thus passivated with hydrogen is no longer active and does not provide holes. However, when the semiconductor sample is irradiated with an electron beam or heated, bonds between hydrogen and the p-type
35 dopant are cleaved, thereby removing hydrogen from the crystal, whereby the p-type dopant can be activated.

Of the above two approaches, irradiation with an

electron beam can be applied to only a limited area for one operation, and treating the entire area of the semiconductor requires a long time. Thus, this approach is not commonly employed in the industry.

5 When a p-type Group III nitride semiconductor produced through the other approach; i.e., heat treatment is used to fabricate light-emitting device wafers, some (a certain percentage of) chips have been found to exhibit a low voltage (V_r), which is a voltage generated
10 upon passing a predetermined current in a reverse direction with respect to the pn junction and which is one of the electric characteristics determined after providing electrodes for the chips. Such low V_r values indicate leakage of current with respect to the pn
15 junction, which is not desired for device products. When such failure chips are removed, productivity drops considerably. In general, when hydrogen is removed from a Group III nitride semiconductor through heat treatment, nitrogen is known to be removed simultaneously, thereby
20 reducing crystallinity. This phenomenon may be a cause of lowering V_r .

 Meanwhile, a technique for reducing the resistance of a semiconductor layer doped with a p-type impurity element has been disclosed (see Japanese Laid-Open Patent
25 Application (*kokai*) No. 8-115880). In the technique, during the course of cooling a gallium-nitride-based compound semiconductor doped with a p-type impurity element, an atmosphere containing ammonia gas is changed to a hydrogen or nitrogen atmosphere at 400°C or higher.
30 The document discloses an example in which an Mg-doped layer whose growth has been completed is cooled to 600°C under $\text{NH}_3\text{-H}_2$ mixture and, at 600°C, the supply of NH_3 is stopped and the atmosphere becomes only hydrogen.

 The experiments conducted previously by the present
35 inventors revealed that device operation voltage cannot be reduced when cooling to 600°C is performed under an NH_3

flow. Particularly, when a positive electrode is formed from a metallic material (e.g., Pt), the operation voltage before bonding, which has been sufficiently lowered, is elevated through the heating, at about 300°C, carried out during bonding.

It has also been reported that a sufficient carrier concentration is attained by cooling a Group III nitride semiconductor from a growth temperature to room temperature in an atmosphere of inert gas instead of H₂ gas or NH₃ gas (see Japanese Laid-Open Patent Application (*kokai*) No. 8-125222). In an example disclosed in the document, a p-type semiconductor is produced by substituting the growth atmosphere by nitrogen gas or inert gas via vacuum as a transition state.

However, even when a grown semiconductor was cooled in an atmosphere of inert gas instead of H₂ gas or NH₃ gas, semiconductor chips exhibiting low device operation voltage cannot be produced unconditionally at high yield. In other words, semiconductor chips exhibiting excellent characteristics cannot be produced at high yield and high reproducibility, even when the conditions as stipulated in the document are controlled. In addition, when a positive electrode material such as Pt is employed, the operation voltage increases due to the heat applied during bonding.

There has been disclosed another technique including, immediately after completion of a growth of a nitride semiconductor, changing the growth atmosphere to an inert gas atmosphere at 1,100°C (i.e., growth temperature) (see Japanese Laid-Open Patent Application (*kokai*) No. 9-129929). This technique requires 2 to 3 hours for lowering the temperature to room temperature from the time of changing the atmosphere to inert gas.

The present inventors previously confirmed, through experiments, that V_r of the produced chips was lowered according to the above technique in which the atmosphere was changed to inert gas immediately after growth, and

that lowering temperature over a long period of time lowered V_r .

Finally, there has been disclosed a technique, for growing a low-resistance p-type gallium-nitride-based semiconductor, including cooling (to $\leq 700^\circ\text{C}$) a semiconductor crystal grown at a 700°C or higher, in an atmosphere of a carrier gas other than hydrogen (see Japanese Laid-Open Patent Application (*kokai*) No. 9-199758). In an example described in the document, a p-type gallium-nitride-based semiconductor grown at $1,030^\circ\text{C}$ is cooled in an atmosphere composed of hydrogen and ammonia, and the atmosphere is changed to nitrogen at 700°C .

The present inventors examined the above growth technique. Even when a grown semiconductor was cooled (to $\leq 700^\circ\text{C}$) in a gas atmosphere other than hydrogen, semiconductor chips exhibiting low device operation voltage could not be produced at high yield. In other words, semiconductor chips exhibiting excellent characteristics cannot be produced at high yield and high reproducibility, even when the conditions as stipulated in the document are controlled. In addition, when a positive electrode material such as Pt is employed, the operation voltage increases due to the heat applied during bonding.

As described above, according to the methods disclosed in Japanese Laid-Open Patent Applications (*kokai*) No. 5-183189 and No. 9-129929, chips exhibiting leakage are produced, due to a low V_r . According to the methods disclosed in Japanese Laid-Open Patent Applications (*kokai*) No. 8-115880, No. 8-125222, and No. 9-199758, an operation voltage increases. Particularly when a positive electrode material such as Pt is employed, the operation voltage increases due to the heat applied during bonding.

Thus, hitherto, there has never been proposed a

problem-free method for forming a semiconductor layer
containing a p-type dopant for fabrication of a Group III
nitride semiconductor device, which method attains both
satisfactory device characteristics and satisfactory
5 yield.

The aforementioned documents disclose the
requirement for reducing the resistance of a layer
containing a p-type dopant, and a low-resistive p-type
semiconductor layer is provided through any of the
10 disclosed techniques.

Disclosure of Invention

The present invention has been conceived with the
aim of solving the problems involved in the
15 aforementioned conventional techniques. Thus, an object
of the present invention is to provide a method for
producing a p-type Group III nitride semiconductor which
can be used to produce a light-emitting device exhibiting
a low operation voltage and a sufficiently high reverse
20 voltage.

The present invention provides the following.

(1) A method for producing a p-type Group III
nitride semiconductor, wherein the method comprises,
during lowering temperature after completion of growth of
25 a Group III nitride semiconductor containing a p-type
dopant,

immediately after completion of the growth,
starting, at a temperature at which the growth has been
completed, supply of a carrier gas composed of an inert
30 gas and reduction of the flow rate of a nitrogen source;
and

stopping supply of the nitrogen source at a time in
the course of lowering temperature.

(2) A production method according to (1) above,
35 wherein the temperature when the growth has been
completed is 900°C or higher.

(3) A production method according to (1) or (2)

above, wherein the nitrogen source is ammonia gas.

(4) A production method according to any one of (1) to (3) above, wherein the carrier gas employed during growth of the semiconductor contains hydrogen gas.

5 (5) A production method according to any one of (1) to (4) above, wherein the flow rate of the nitrogen source after the reduction is 0.001 to 10% with respect to the flow rate of the total volume of gas.

10 (6) A production method according to any one of (1) to (5) above, wherein supply of nitrogen source is stopped at 700 to 950°C.

(7) A p-type Group III nitride semiconductor containing hydrogen atom in an amount which is more than 1/5 the p-type dopant concentration and which is less
15 than the p-type dopant concentration.

(8) A p-type Group III nitride semiconductor having a resistivity of 20 $\Omega\cdot\text{cm}$ to 10,000 $\Omega\cdot\text{cm}$.

(9) A Group III nitride semiconductor light-emitting device comprising a substrate; an n-type layer, a light-emitting layer, and a p-type layer, the layers being
20 provided atop the substrate and being formed of a Group III nitride semiconductor; a negative electrode provided on the n-type layer; and a positive electrode provided on the p-type layer, wherein the p-type layer is produced
25 through a production method according to any one of (1) to (6) above.

(10) A Group III nitride semiconductor light-emitting device comprising a substrate; an n-type layer, a light-emitting layer, and a p-type layer, the layers
30 being provided atop the substrate and being formed of a Group III nitride semiconductor; a negative electrode provided on the n-type layer; and a positive electrode provided on the p-type layer, wherein the p-type layer is composed of a p-type Group III nitride semiconductor
35 according to (7) or (8) above.

(11) A light-emitting device according to (9) or (10) above, wherein the positive electrode is formed of a

platinum group metal selected from among Pd, Pt, Rh, Os, Ir, and Ru.

(12) A light-emitting device according to any one of (9) to (11) above, which is of a flip-chip type.

5 (13) A light-emitting device according to any one of (9) to (11) above, which is of a face-up type.

According to the present invention, a p-type Group III nitride semiconductor exhibiting satisfactory characteristics for use in semiconductor devices can be produced. Thus, a Group III nitride semiconductor light-emitting device exhibiting no increase in operation voltage caused by heat and high Vr can be effectively produced from the p-type Group III nitride semiconductor.

15 Brief Description of Drawings

Fig. 1 is a schematic illustration of a Group III nitride semiconductor light-emitting device of the present invention.

20 Fig. 2 is a schematic cross-sectional view showing the stacked structure fabricated in Example 1.

Fig. 3 is a schematic plan view of the LED fabricated in Example 1.

Fig. 4 is a chart schematically showing a temperature lowering profile employed in Example 1.

25 Fig. 5 is a chart schematically showing a temperature lowering profile employed in Comparative Example 1.

Fig. 6 is a chart schematically showing a temperature lowering profile employed in Comparative Example 2.

30 Fig. 7 is a schematic plan view of the LED fabricated in Example 2.

Best Modes for Carrying Out the Invention

35 Examples of the Group III nitride semiconductor to which the method of the present invention for producing a p-type semiconductor can be applied include 2-component

mixed crystals such as GaN, InN and AlN; 3-component mixed crystals such as InGa_{1-x}N and AlGa_{1-x}N; and 4-component mixed crystals such as InAlGa_{1-x-y}N. In the present invention, examples of the Group III nitride semiconductor further include 3-component mixed crystals containing a non-nitrogen Group V element such as GaPN and GaNAs; 4-component mixed crystals further containing In or Al such as InGaPN, InGaAsN, AlGaPN, and AlGaAsN; 5-component mixed crystals further containing In and Al such as AlInGaPN and AlInGaAsN; 5-component mixed crystals further containing P and As such as AlGaPAsN and InGaPAsN; and 6-component mixed crystals containing all the elements such as AlInGaPAsN.

Particularly, the method of the present invention is preferably applied to produce, among the above semiconductors, Group III nitride semiconductors containing sole N as a Group V element such as 2-component mixed crystals such as GaN, InN, and AlN; 3-component mixed crystals such as InGa_{1-x}N and AlGa_{1-x}N; and 4-component mixed crystals such as InAlGa_{1-x-y}N, which can be readily produced and are resistive to decomposition. When these semiconductors are represented by formula $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ ($0 \leq X + Y \leq 1$), X is preferably 0 to 0.5, and Y is preferably 0 to 0.1.

Examples of the p-type dopant which can be employed in the present invention include Mg, Ca, Zn, Cd, and Hg, which are reported or considered to impart p-type conductivity to Group III nitride semiconductors. Among these dopants, Mg is particularly preferred as a p-type dopant, because Mg exhibits high doping activity when heat treatment is performed. The amount of dopant is preferably 1×10^{18} to $1 \times 10^{21} \text{ cm}^{-3}$. When the amount is less than $1 \times 10^{18} \text{ cm}^{-3}$, emission intensity decreases, whereas when the amount is more than $1 \times 10^{21} \text{ cm}^{-3}$, crystallinity is impaired. Both cases are not preferred. More preferably, the amount of dopant is 1×10^{19} to $1 \times$

10^{20} cm^{-3} .

The p-type semiconductor layer fabricated through the method of the present invention may contain hydrogen atoms in the crystal. In some cases, hydrogen atoms
5 contained in the semiconductor crystal are preferable for fabricating devices exhibiting high reverse voltage (V_r). The amount of hydrogen atoms contained in the crystal is preferably smaller than the amount of p-type dopant. This is because, when the hydrogen atom amount is equal
10 to or higher than the p-type dopant amount, electric contact of the p-type electrode becomes difficult to attain. The hydrogen atom amount is more preferably $9/10$ or less the p-type dopant amount, particularly preferably $7/8$ or less the p-type dopant amount. However, when the
15 hydrogen atom amount is $1/5$ or less the p-type dopant amount, release of nitrogen also occurs. Thus, the hydrogen atom amount is preferably more than $1/5$, more preferably $1/3$ or more, still more preferably $1/2$ or more. The Mg atom concentration and the hydrogen atom
20 concentration of a p-type semiconductor layer are quantified through conventional SIMS (Secondary Ion Mass Spectroscopy).

Presence of hydrogen in the crystal does not reduce electrical resistance of the p-type layer. However, such
25 a high resistance is not detrimental to device characteristics. In semiconductor devices including a Group III nitride semiconductor, the formed p-type layer is usually thinner as compared to other semiconductor layer. Therefore, resistance of the p-type layer *per se*
30 does not greatly affect device operation voltage (V_f). High resistivity of the p-type layer is rather preferable for maintaining V_r high.

The p-type layer preferably has a resistivity about $20 \Omega \cdot \text{cm}$ to about $10,000 \Omega \cdot \text{cm}$. When the resistivity is
35 higher than $10,000 \Omega \cdot \text{cm}$, emission intensity may decrease, whereas when the resistivity is lower than $20 \Omega \cdot \text{cm}$, V_r

may decrease. More preferably, the resistivity is 50 $\Omega \cdot \text{cm}$ to 2,000 $\Omega \cdot \text{cm}$, with 100 $\Omega \cdot \text{cm}$ to 1,000 $\Omega \cdot \text{cm}$ being further more preferred. Resistivity is determined through conventional TLM (Transfer Length Measurement).

5 No particular limitation is imposed on the method for growing the p-type Group III nitride semiconductor to which the present invention is applied, and there may be employed any known method for growing a Group III nitride semiconductor, such as MOCVD (metal-organic chemical
10 vapor deposition), HVPE (hydride vapor phase epitaxy), or MBE (molecular beam epitaxy). From the viewpoints of layer thickness controllability and mass productivity, MOCVD is preferably employed.

 In the case of MOCVD, hydrogen (H_2) or nitrogen (N_2)
15 is employed as a carrier gas, trimethylgallium (TMG) or triethylgallium (TEG) is employed as a Ga (Group III element) source, trimethylaluminum (TMA) or triethylaluminum (TEA) is employed as an Al source, trimethylindium (TMI) or triethylindium (TEI) is employed
20 as an In source, and ammonia (NH_3), hydrazine (N_2H_4), or the like is employed as a nitrogen source. Bis(cyclopentadienyl)magnesium (Cp_2Mg) or bis(ethylcyclopentadienyl)magnesium ($(\text{EtCp})_2\text{Mg}$) serving as an Mg source or dimethylzinc ($\text{Zn}(\text{CH}_3)_2$) serving as a Zn
25 source is employed as a p-type dopant.

 When the carrier gas contains hydrogen and/or the nitrogen source is composed of NH_3 , the effects of the present invention can fully be attained.

 The growth temperature is preferably 900°C or higher
30 so as to attain excellent crystallinity and contact resistance, more preferably 1,000°C to 1,250°C.

 Next, the procedure of cooling a semiconductor stacked structure to room temperature after completion of growth of a Group III nitride semiconductor containing a
35 p-type dopant and removing it from a growth apparatus will be described. When the carrier gas during growth

contains hydrogen, the carrier gas must be altered to a hydrogen-free inert gas at the growth temperature immediately after completion of the growth. The acceptable time lag required for changing the carrier gas is shorter than about one minute. If hydrogen gas flow is continued for one minute or longer, a sufficiently low operation voltage cannot be attained. The inert gas replacing hydrogen is preferably nitrogen. Alternatively, argon, helium, or a mixture thereof may also be employed.

Simultaneously when the carrier gas is changed, the flow rate of the nitrogen source is reduced, which is a key issue. The flow rate of the nitrogen source during growth is generally 20% to 70% with respect to the flow rate of the total volume of gas. After reduction of the flow rate, the flow rate is preferably 10% or less with respect to the flow rate of the total volume of gas, more preferably 1% or less. When the amount of the nitrogen source is excessively high, device operation voltage cannot be lowered as intended. However, if the flow of the nitrogen source is stopped (i.e., controlled to 0), nitrogen is released from the p-type layer crystal, thereby lowering V_r of produced devices. The flow rate of the nitrogen source is preferably controlled to 0.001% or higher with respect to the flow rate of the total volume of gas, more preferably 0.01% or higher.

Lowering of the temperature is preferably started immediately after changing of the flow rate of the nitrogen source and changing of the carrier gas. When the retention period at the growth temperature after completion of growth is long, crystallinity is impaired, and heat-induced damage is accumulated in the light-emitting layer, leading to decrease in emission intensity.

In addition, the reduced flow rate of the nitrogen source is required to be adjusted to 0 in the course of temperature lowering. When devices are fabricated

through a cooling step (for example to 300°C) without stopping flow of the nitrogen source, an operation voltage of the devices is increased by the heat applied during bonding.

5 Controlling of the nitrogen source flow to 0 in the course of lowering temperature is preferably performed at 700°C to 950°C. When the control of the nitrogen source flow to 0 is performed at a temperature higher than 950°C, Vr of the devices is lowered, whereas when the nitrogen
10 source is continued to flow to a temperature lower than 700°C, an operation voltage increases due to heat.

 The time from the completion of growth to control the nitrogen flow rate to 0, which depends on the temperature lowering rate, is about 30 seconds to about
15 eight minutes.

 The p-type Group III nitride semiconductor of the present invention and the production method of the invention can be applied to production of any of a variety of semiconductor devices, so long as the devices
20 require a p-type Group III nitride semiconductor. Examples of the semiconductor devices include light-emitting devices such as light-emitting diodes and laser diodes; high-speed transistors; and photo detectors. Among these semiconductor devices, the present invention
25 is particularly preferably applied to production of semiconductor light-emitting devices which require formation of a pn junction and a positive electrode exhibiting excellent characteristics.

 Fig. 1 is a schematic illustration of a p-type Group
30 III nitride semiconductor light-emitting device produced from the p-type Group III nitride semiconductor of the invention and through the production method of the invention. In Fig. 1, an n-type semiconductor layer 3, light-emitting layer 4, and p-type semiconductor layer 5, which are composed of a group III nitride semiconductor,
35 are layered in this order on the substrate 1 via a buffer

layer 2 as needed. A negative electrode 6 and a positive electrode 7 are provided on the n-type semiconductor layer 3 and the p-type semiconductor layer 5, respectively.

5 No particular limitation is imposed on the material of the substrate 1, and any known substrate, such as sapphire, SiC, GaN, AlN, Si, ZnO, and other oxides, may be employed. Of these, sapphire is preferred. The buffer layer 2 is provided, in accordance with needs, so
10 as to adjust lattice-mismatch between the substrate and the n-type semiconductor layer 3 grown thereon. The buffer layer is formed through a conventionally known technique in accordance with needs.

 The n-type semiconductor layer 3 may be formed so as
15 to have a desired structure and composition through a technique well known in the art. Generally, the n-type semiconductor layer is composed of a contact layer and a cladding layer, the contact layer attaining excellent Ohmic contact with the negative electrode 6 and the
20 cladding layer having a bandgap wider than that of the light-emitting layer. The negative electrode may be formed so as to have a desired structure and composition through a technique well known in the art.

 No particular limitation is imposed on the
25 composition and structure of the light-emitting layer 4, and any known structure, such as a single quantum well (SQW) structure and a multiple quantum well (MQW) structure, may be employed.

 The p-type semiconductor layer 5 is formed through
30 the production method of the present invention. The composition and structure of the semiconductor layer may be controlled as desired through a technique well known in the art. Similar to the n-type semiconductor layer, the p-type semiconductor layer is composed of a contact
35 layer and a cladding layer, the contact layer attaining excellent Ohmic contact with the positive negative electrode and the cladding layer having a bandgap wider

than that of the light-emitting layer.

5 The positive electrode 7 which is to be in contact with the p-type layer produced through the method of the invention may be formed from a metal such as Au, Ni, Co, Cu, Pd, Pt, Rh, Os, Ir, or Ru. The positive electrode may contain a transparent oxide such as ITO, NiO, or CoO. The transparent oxide may be incorporated into the metal film in the form of aggregates. Alternatively, the transparent oxide film may be laminated on the metal film.

10 Particularly when the positive electrode is formed from a platinum-group metal such as Pd, Pt, Rh, Os, Ir, or Ru, the semiconductor light-emitting device fully attains the effects of the present invention; i.e., is prevented from an elevation of an operation voltage caused by heat during bonding. Among these metal elements, Pd, Pt, and Rh are useful as high purity materials are comparatively readily available.

15 The positive electrode may be formed on virtually the entire surface or formed in the lattice-like or dendritic form. After formation of the positive electrode, thermal annealing may be performed so as to alloy or make the electrode to be transparent. This annealing is optional.

20 The semiconductor device may be a face-up (FU) type in which light is emitted from the semiconductor side through a transparent positive electrode. Alternatively, a flip-chip (FC) type in which light is emitted from the substrate side through employment of a reflecting-type positive electrode may also be employed.

Examples

25 The present invention will next be described in detail by way of examples, which should not be construed as limiting the invention thereto.

35 <Example 1>

Fig. 2 is a schematic cross-sectional view showing a

stacked structure 11 employed for producing an LED 10 described in Example 1. Fig. 3 is a schematic plan view of the LED 10.

5 The stacked structure 11 included a substrate 101 formed of sapphire having a c-plane ((0001) crystal plane). On the substrate, via an AlN buffer layer (not illustrated), the following layers were sequentially formed: an undoped GaN layer (thickness: 8 μm) 102; a
10 silicon (Si)-doped n-type GaN layer (thickness: 2 μm , carrier concentration: $1 \times 10^{19} \text{ cm}^{-3}$) 103; an Si-doped n-type $\text{Al}_{0.07}\text{Ga}_{0.93}\text{N}$ cladding layer (thickness: 25 nm, carrier concentration: $1 \times 10^{18} \text{ cm}^{-3}$) 104; a light-emitting layer
105 of a multiple quantum well structure including Si-doped GaN barrier layers (6 layers, thickness: 14.0 nm, carrier concentration: $1 \times 10^{18} \text{ cm}^{-3}$) and undoped
15 $\text{In}_{0.20}\text{Ga}_{0.80}\text{N}$ well layers (5 layers, thickness: 2.5 nm); an Mg-doped p-type $\text{Al}_{0.07}\text{Ga}_{0.93}\text{N}$ cladding layer 106 (thickness: 10 nm); and an Mg-doped p-type $\text{Al}_{0.02}\text{Ga}_{0.98}\text{N}$ contact layer 107 (thickness: 150 nm). These layers 102 to 107 of the
20 stacked structure 11 were grown through a conventional reduced-pressure MOCVD means.

Among them, the Mg-doped p-type AlGaN contact layer 107 was grown through the following procedure.

(1) After completion of the growth of the Mg-doped
25 p-type $\text{Al}_{0.07}\text{Ga}_{0.93}\text{N}$ cladding layer 106, the pressure inside the growth reactor furnace was adjusted to $2 \times 10^4 \text{ Pa}$. Hydrogen was employed as a carrier gas.

(2) Growth of an Mg-doped p-type AlGaN layer from trimethylgallium, trimethylaluminum, and ammonia serving
30 as sources and biscyclopentamagnesium serving as an Mg-dopant was started at $1,020^\circ\text{C}$.

(3) Trimethylgallium, trimethylaluminum, ammonia, and biscyclopentamagnesium were continuously supplied to a growth reaction furnace for four minutes, whereby an
35 Mg-doped p-type $\text{Al}_{0.02}\text{Ga}_{0.98}\text{N}$ layer having a thickness of 0.15 μm was formed.

(4) Supply of trimethylgallium, trimethylaluminum, and biscyclopentamagnesium to the growth reactor furnace was stopped, to thereby terminate the growth of the Mg-doped p-type $\text{Al}_{0.02}\text{Ga}_{0.98}\text{N}$ layer.

5 Immediately after completion of vapor-phase growth of the Mg-doped p-type AlGa_N layer serving as the contact layer 107, the carrier gas was changed from hydrogen to nitrogen, and the flow rate of ammonia was reduced. The amount of reduced gas was compensated for with nitrogen
10 serving as a carrier gas. Specifically, a flow rate of ammonia during growth of 50% with respect to the flow rate of the total volume of gas was reduced to 0.2%, and simultaneously operation of a high-frequency induction heater that had been employed for heating the substrate
15 101 was stopped.

Under these conditions, the stacked structure was maintained for two minutes, and then flow of ammonia was stopped. The substrate temperature at the instance was 850°C. Fig. 4 is a chart schematically showing a
20 temperature lowering profile.

After cooling to room temperature, the stacked structure 11 was removed from the growth reactor furnace, and the magnesium atom concentration and the hydrogen atom concentration of the contact layer 107 were
25 quantitatively determined through conventional SIMS. The Mg atom concentration was found to be $7 \times 10^{19} \text{ cm}^{-3}$, and the concentration was virtually uniform from the top to the bottom in the depth direction. The hydrogen atom concentration was found to be $6 \times 10^{19} \text{ cm}^{-3}$ and almost
30 uniformly distributed. The resistivity of the contact layer 107 was estimated to be about 150 Ωcm through conventional TLM.

The LED 10 was fabricated from the stacked structure 11 having the aforementioned p-type contact layer.
35 Firstly, the region of the structure where a negative electrode 108 was to be formed was dry-etched in a

typical manner, whereby the above region of the Si-doped GaN layer 103 was exclusively exposed. On the exposed surface, the negative electrode 108 (titanium (Ti)/aluminum (Al)) was formed.

5 On virtually the entire remaining surface of the contact layer 107, a positive electrode 109 was formed. The positive electrode had a multilayer structure of platinum (Pt) film/rhodium (Rh) film/gold (Au) film and a function of reflecting light emitted from the light-
10 emitting layer to the sapphire substrate 101. The Pt film was in contact with the surface of the p-type contact layer 107.

 After formation of the negative electrode 108 and the positive electrode 109, the back of the sapphire
15 substrate 101 was polished by use of abrasive grains such as diamond particles, to thereby form a mirror-finished surface. Then, the stacked structure 11 was cut into square ($350\ \mu\text{m} \times 350\ \mu\text{m}$) LED 10 pieces. Each piece was sub-mounted via the negative electrode and the positive
20 electrode, thereby forming a flip type chip. The chip was placed on a lead frame and wire-bonded to the lead frame with gold (Au) wire.

 Electric characteristics and emission characteristics of the flip-chip type LEDs were evaluated
25 when forward current was caused to flow between the negative electrode 108 and the positive electrode 109. The forward voltage (V_f) at a forward current of 20 mA was found to be 3.2 V. The reverse voltage (V_r) at a reverse current of 10 μA was found to be 20 V or higher.
30 Thus, an elevation of the forward voltage (V_f) by heat during bonding was not found.

 The light emitted through the sapphire substrate 101 to the outside had a wavelength of 455 nm. The output of the emitted light, as determined through a typical
35 integrating sphere, was 10 mW. Such characteristics were attained with uniformity from LED to LED among about 10,000 LEDs (products with defective appearance were not

included as such had been rejected in advance) produced from a wafer (diameter: 5.1 cm (2 inches)).

<Example 2>

5 A stacked structure formed in this Example was as follows:

10 In Fig. 2, the stacked structure 11 included a substrate 101 formed of sapphire having a c-plane ((0001) crystal plane). On the substrate, via an AlN buffer layer (not illustrated), the following layers were sequentially formed: an undoped GaN layer (thickness: 8 μm) 102; a Ge-doped n-type GaN layer (thickness: 2 μm , carrier concentration: $7 \times 10^{18} \text{ cm}^{-3}$) 103; an Si-doped n-type $\text{In}_{0.01}\text{Ga}_{0.99}\text{N}$ cladding layer (thickness: 18 nm, carrier concentration: $1 \times 10^{18} \text{ cm}^{-3}$) 104; a light-emitting layer 15 105 of a multiple quantum well structure including Si-doped GaN barrier layers (6 layers, thickness: 14.0 nm, carrier concentration: $1 \times 10^{17} \text{ cm}^{-3}$) and undoped $\text{In}_{0.20}\text{Ga}_{0.80}\text{N}$ well layers (5 layers, thickness: 2.5 nm); an Mg-doped p-type $\text{Al}_{0.07}\text{Ga}_{0.93}\text{N}$ cladding layer 106 (thickness: 20 12 nm); and an Mg-doped p-type $\text{Al}_{0.02}\text{Ga}_{0.98}\text{N}$ contact layer 107 (thickness: 175 nm). These layers 102 to 107 of the stacked structure 11 were grown through a conventional reduced-pressure MOCVD means.

25 The Mg-doped p-type AlGaN contact layer 107 was grown through the same procedure as Example 1 and, after completion of vapor-phase growth of the contact layer 107, the stacked structure 11 was cooled to room temperature through the same procedure as Example 1.

30 After cooling to room temperature, the stacked structure 11 was removed from the growth reactor furnace, and the magnesium atom concentration and the hydrogen atom concentration of the contact layer 107 were quantitatively determined through conventional SIMS. The Mg atom concentration was found to be $1.5 \times 10^{20} \text{ cm}^{-3}$, and 35 the concentration was virtually uniform from the top to the bottom in the depth direction. The hydrogen atom

concentration was found to be $8 \times 10^{19} \text{ cm}^{-3}$ and was almost uniformly distributed. The resistivity of the contact layer 107 was estimated to be about $180 \Omega \cdot \text{cm}$ through conventional TLM.

5 The LED 10 was fabricated from the stacked structure 11 having the aforementioned p-type contact layer. The procedure of fabrication and the structure of electrodes were similar to Example 1.

 Electric characteristics and emission
10 characteristics of the flip-chip type LEDs were evaluated when a forward current was caused to flow between the negative electrode 108 and the positive electrode 109. The forward voltage (V_f) at a forward current of 20 mA was found to be 3.3 V. The reverse voltage (V_r) at a
15 reverse current of $10 \mu\text{A}$ was found to be 20 V or higher. Thus, an elevation of the forward voltage (V_f) by heat during bonding was not found.

 The light emitted through the sapphire substrate 101 to the outside had a wavelength of 455 nm. The output of
20 the emitted light, as determined through a typical integrating sphere, was 12 mW. Such characteristics were attained with uniformity from LED to LED among about 10,000 LEDs (products with defective appearance were not included as such had been rejected in advance) produced
25 from a wafer (diameter: 5.1 cm (2 inches)).
<Comparative Example 1>

 The procedure of Example 1 was repeated, except that treatment after completion of the growth of p-type contact layer was performed under different conditions,
30 to thereby form flip-chip type LEDs. In Comparative Example 1, a stacked structure as described in Example 1 was formed under the same conditions and through the same procedure as employed in Example 1. Subsequently, the carrier gas employed during growth was changed from
35 hydrogen to nitrogen, and the flow rate of ammonia was reduced to 0.2%. However, the ammonia continued to flow

until temperature was lowered to 350°C. Fig. 5 is a chart schematically showing a temperature lowering profile.

Similar to Example 1, the magnesium atom concentration and the hydrogen atom concentration of the p-type contact layer of the semiconductor sample fabricated in Comparative Example 1 were quantitatively determined through SIMS. The Mg atom concentration was found to be $7 \times 10^{19} \text{ cm}^{-3}$, which is equivalent to the concentration obtained in Example 1. The hydrogen atom concentration was found to be $7 \times 10^{19} \text{ cm}^{-3}$. The resistivity of the p-type contact layer was estimated 15,000 $\Omega \cdot \text{cm}$ through TLM similar to Example 1.

FC-type device chips were fabricated in a manner similar to Example 1, and each chip was placed on a lead frame. Electric characteristics and emission characteristics of the FC-type device chips were evaluated when forward current was caused to flow between the negative electrode 108 and the positive electrode 109. The forward voltage (V_f) at a forward current of 20 mA was found to be 4.0 V, which is higher than that obtained in Example 1. The output of the emitted light was found to be 8 mW.

<Comparative Example 2>

The procedure of Example 1 was repeated, except that treatment after completion of the growth of p-type contact layer was performed under different conditions, to thereby form flip-chip type LEDs. In Comparative Example 2, a stacked structure as described in Example 1 was formed under the same conditions and through the same procedure as employed in Example 1. Subsequently, immediately after completion of vapor-phase growth of the p-type contact layer, the carrier gas employed during growth was changed from hydrogen to nitrogen and, at the same time flow of ammonia was stopped. The temperature was lowered to 350°C under these conditions. Fig. 6 is a chart schematically showing a temperature lowering

profile.

Similar to Example 1, the magnesium atom concentration and the hydrogen atom concentration of the p-type contact layer of the semiconductor sample
5 fabricated in Comparative Example 2 were quantitatively determined through SIMS. The Mg atom concentration was found to be $7 \times 10^{19} \text{ cm}^{-3}$, which is equivalent to the concentration obtained in Example 1. The hydrogen atom
10 concentration was found to be $1 \times 10^{19} \text{ cm}^{-3}$. The resistivity of the p-type contact layer was estimated $10 \text{ } \Omega \cdot \text{cm}$ through TLM similar to Example 1.

FC-type device chips were fabricated in a manner similar to Example 1, and each chip was placed on a lead frame. Electric characteristics and emission
15 characteristics of the FC-type device chips were evaluated when forward current was caused to flow between the negative electrode 108 and the positive electrode 109. The forward voltage (V_f) at a forward current of 20 mA was found to be 3.0 V, and the output of the emitted
20 light was found to be 10 mW. The reverse voltage (V_r) at a reverse current of 10 μA was found to be 5 V.

<Example 3>

In Example 3, electrodes were provided, in an FU manner, on the same stacked structure 11 as employed in
25 Example 1, to thereby fabricate LEDs. Fig. 7 is a schematic plan view of the electrodes formed in Example 3.

In a manner similar to that of Example 1, a negative electrode 108 as shown in Fig. 7 was formed. On
30 virtually the entire remaining surface of the contact layer 107, a positive electrode 109, which had a multilayer structure of platinum (Pt) film/gold (Au) film and exhibited transparency for extracting light emitted from the light-emitting layer to the outside from the
35 semiconductor layer side, was formed. The Pt film was in contact with the surface of the p-type contact layer 107.

On the transparent electrode 109, a bonding pad 110 having an outermost surface of Au was formed. Thereafter, in a manner similar to that of Example 1, the stacked structure was cut into square (350 μm $\times$ 350 μm) LED 20 pieces.

Electric characteristics and emission characteristics of the LEDs were evaluated when forward current was caused to flow between the negative electrode 108 and the positive electrode 109 of each FU-type chip. The forward voltage (V_f) at a forward current of 20 mA was found to be 3.0 V. The reverse voltage (V_r) at a reverse current of 10 μA was found to be 20 V or higher. The light emitted from the semiconductor layer side to the outside had a wavelength of 455 nm. The output of the emitted light, as determined through a typical integrating sphere, was 6 mW. Such characteristics were attained with uniformity from LED to LED among about 10,000 LEDs (products with defective appearance were not included as such had been rejected in advance) produced from a wafer (diameter: 5.1 cm (2 inches)).

Industrial Applicability

The method of the present invention for producing a p-type Group III nitride semiconductor is capable of producing a light-emitting device exhibiting both high V_r and low operation voltage. Thus, the production method is remarkably useful for producing a p-type Group III nitride semiconductor light-emitting device.

CLAIMS

1. A method for producing a p-type Group III nitride semiconductor wherein the method comprises, during lowering temperature after completion of growth of a Group III nitride semiconductor containing a p-type dopant,

immediately after the completion of the growth, starting, at a temperature at which the growth has been completed, supply of a carrier gas composed of an inert gas and reduction of the flow rate of a nitrogen source; and

stopping supply of the nitrogen source at a time in the course of lowering temperature.

2. A production method according to claim 1, wherein the temperature when the growth has been completed is 900°C or higher.

3. A production method according to claim 1 or 2, wherein the nitrogen source is ammonia gas.

4. A production method according to any one of claims 1 to 3, wherein the carrier gas employed during growth of the semiconductor contains hydrogen gas.

5. A production method according to any one of claims 1 to 4, wherein the flow rate of the nitrogen source after the reduction is 0.001 to 10% with respect to the flow rate of the total volume of gas.

6. A production method according to any one of claims 1 to 5, wherein supply of nitrogen source is stopped at 700 to 950°C.

7. A p-type Group III nitride semiconductor containing hydrogen atom in an amount which is more than 1/5 the p-type dopant concentration and which is less than the p-type dopant concentration.

8. A p-type Group III nitride semiconductor having a resistivity of 20 $\Omega \cdot \text{cm}$ to 10,000 $\Omega \cdot \text{cm}$.

9. A Group III nitride semiconductor light-emitting device comprising a substrate; an n-type layer,

a light-emitting layer, and a p-type layer, the layers being provided atop the substrate and being formed of a Group III nitride semiconductor; a negative electrode provided on the n-type layer; and a positive electrode provided on the p-type layer, wherein the p-type layer is produced through a production method according to any one of claims 1 to 6.

10. A Group III nitride semiconductor light-emitting device comprising a substrate; an n-type layer, a light-emitting layer, and a p-type layer, the layers being provided atop the substrate and being formed of a Group III nitride semiconductor; a negative electrode provided on the n-type layer; and a positive electrode provided on the p-type layer, wherein the p-type layer is composed of a p-type Group III nitride semiconductor according to claim 7 or 8.

11. A light-emitting device according to claim 9 or 10, wherein the positive electrode is formed of a platinum group metal selected from among Pd, Pt, Rh, Os, Ir, and Ru.

12. A light-emitting device according to any one of claims 9 to 11, which is of a flip-chip type.

13. A light-emitting device according to any one of claims 9 to 11, which is of a face-up type.

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Fig.1

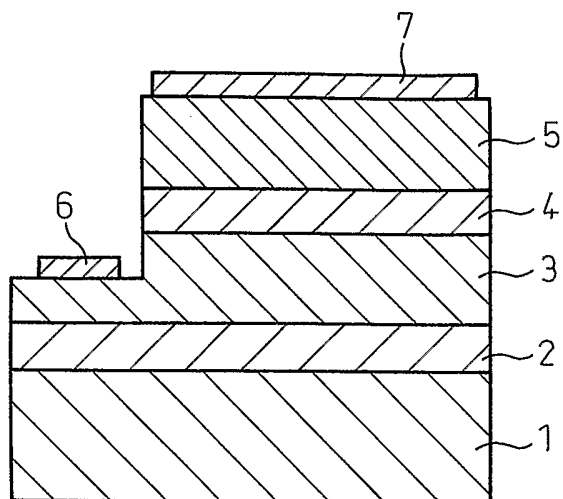
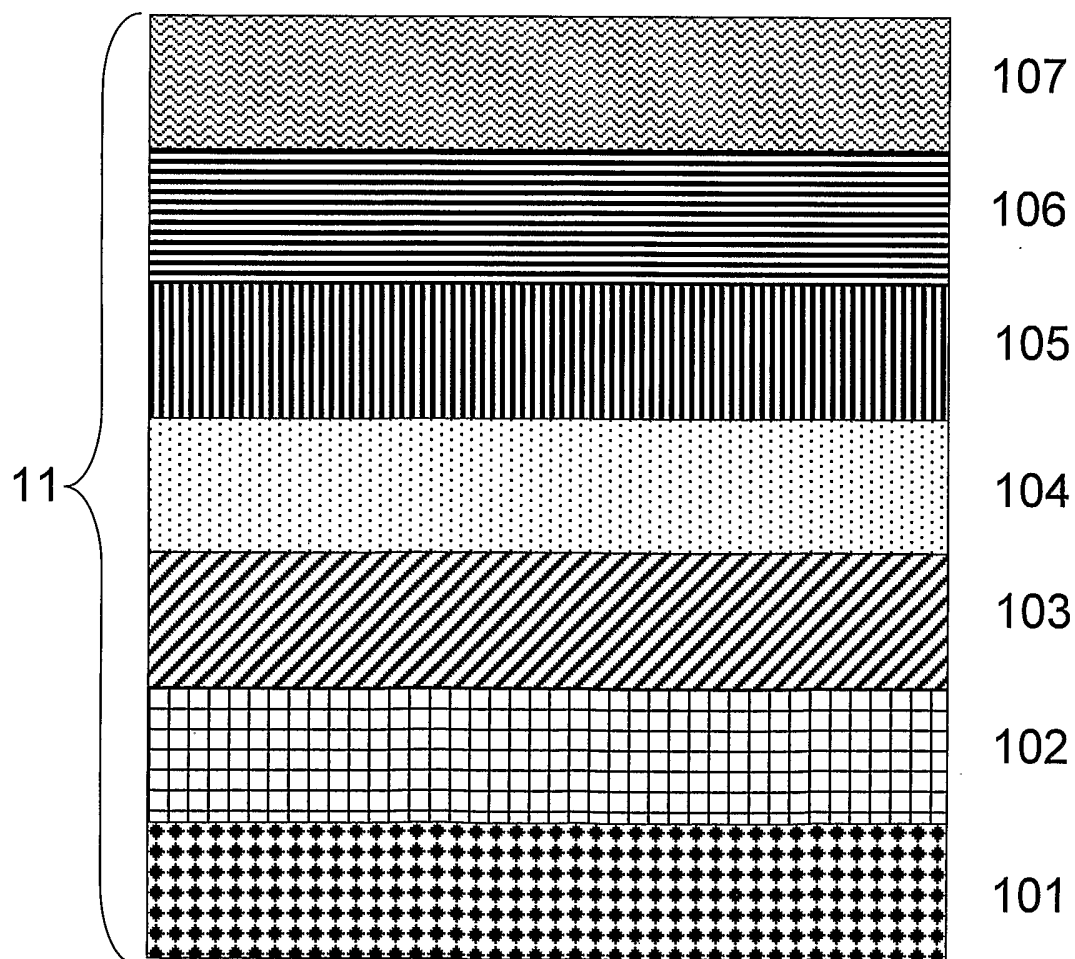
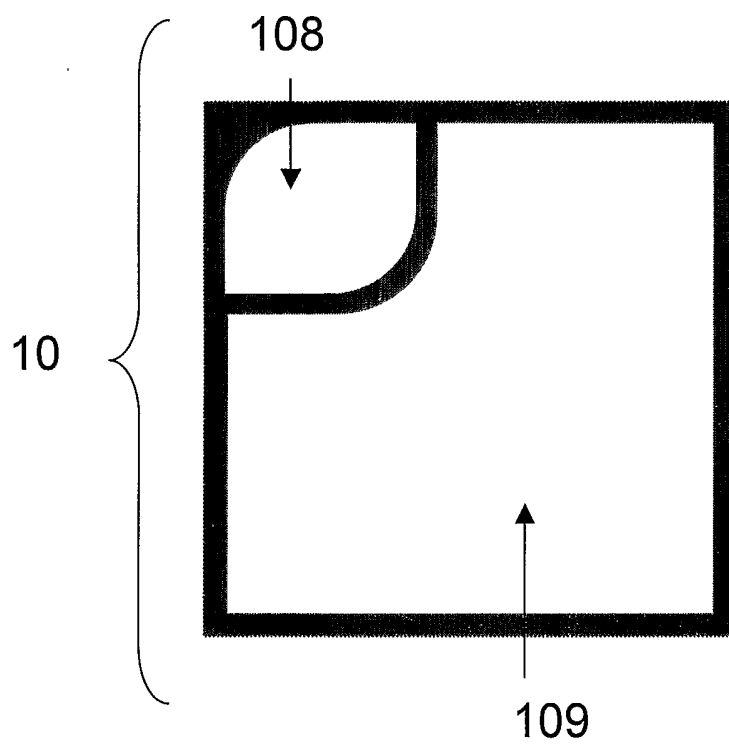


Fig.2



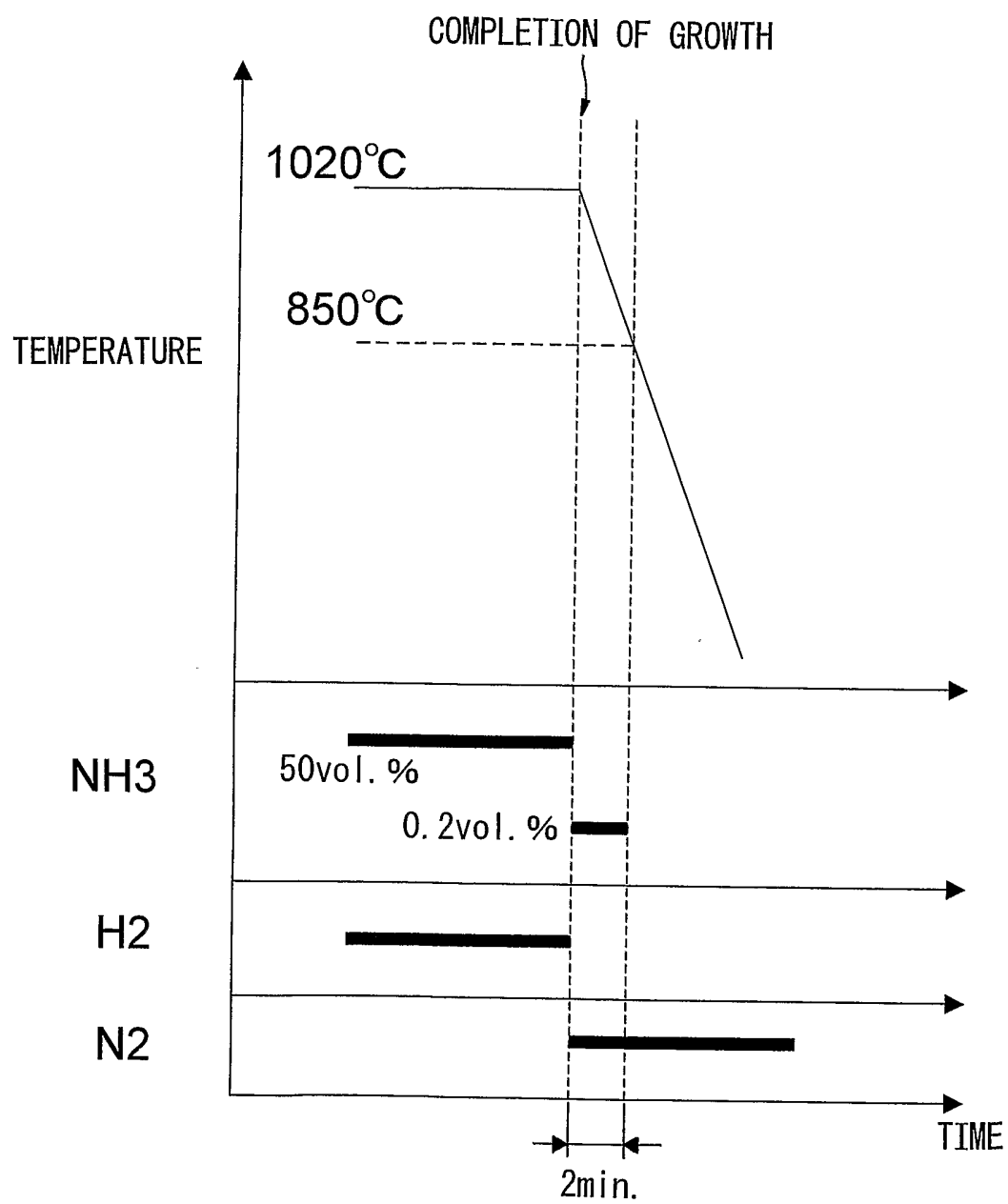
2/6

Fig.3



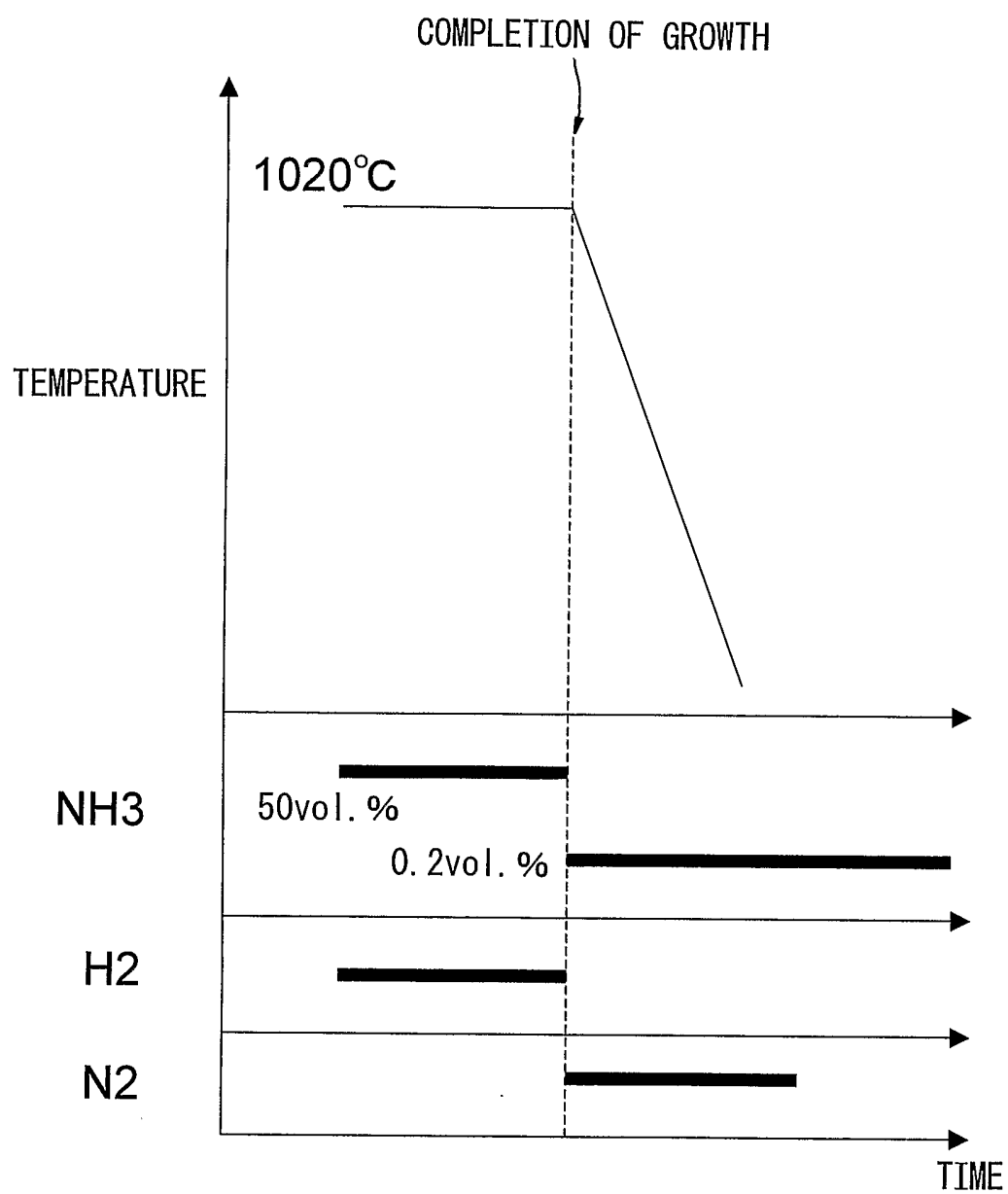
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Fig.4



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Fig. 5



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Fig.6

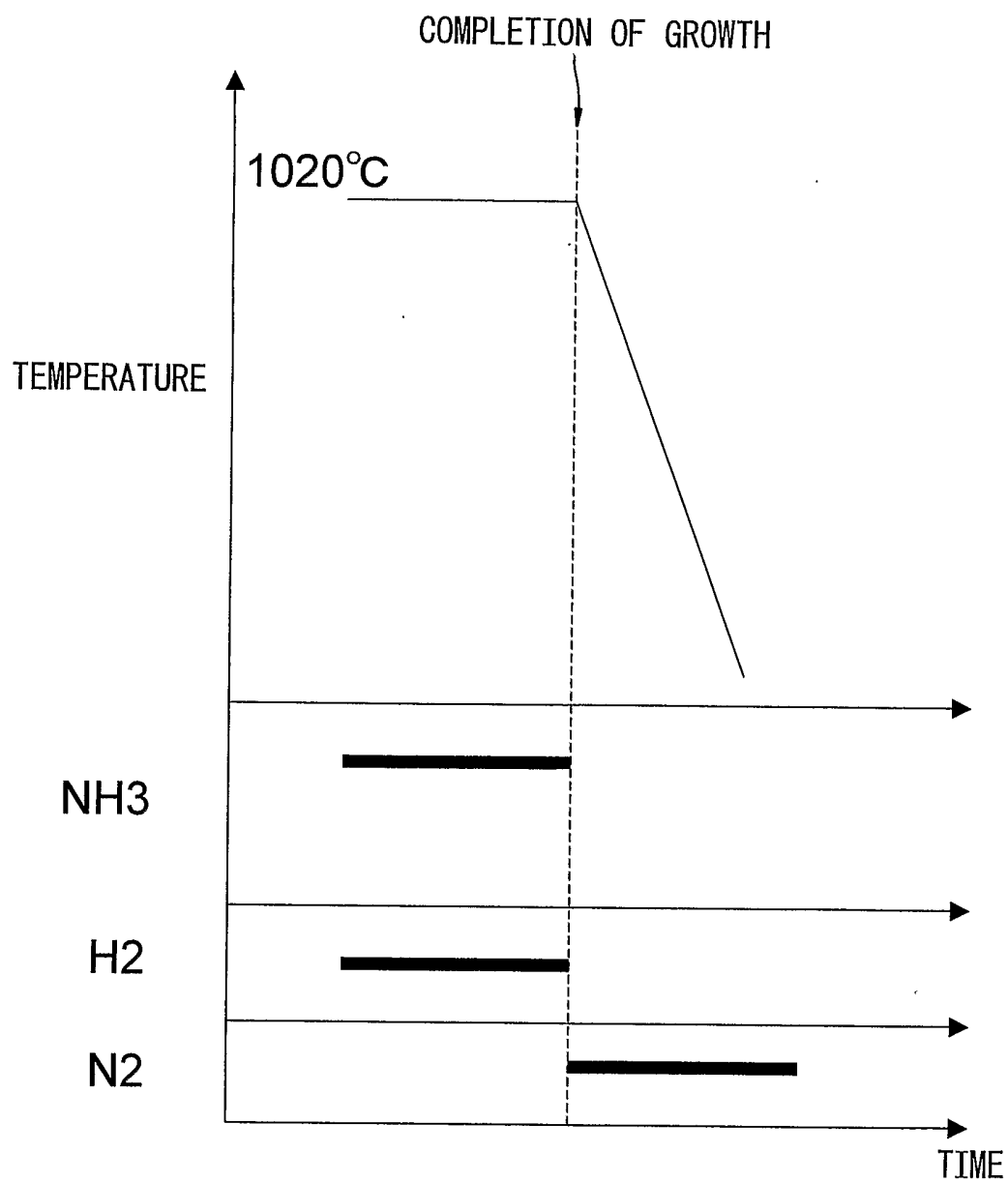
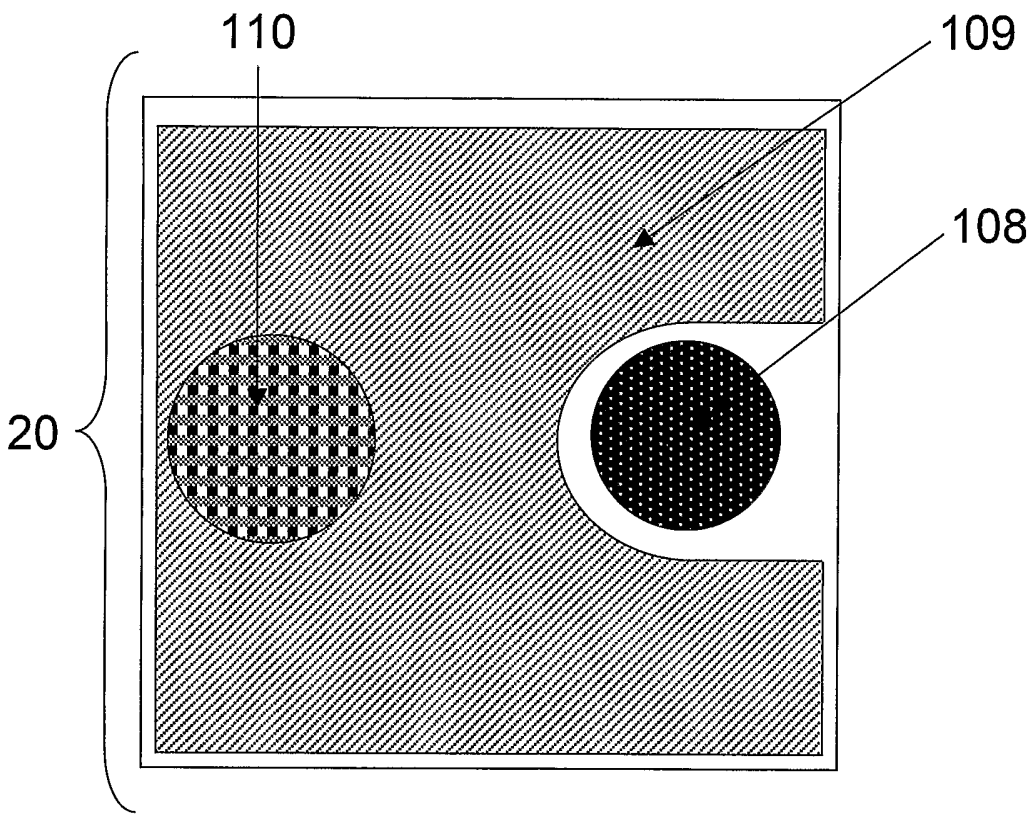


Fig.7



INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2005/009008

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl.⁷ H01L21/205, C23C16/34

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl.⁷ H01L21/205, C23C16/34

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
 Published unexamined utility model applications of Japan 1971-2005
 Registered utility model specifications of Japan 1996-2005
 Published registered utility model applications of Japan 1994-2005

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	JP 2003-243302 A (SHOWA DENKO K.K.) 2003.08.29, paragraph[0074]-[0076] & WO 2003/068699 A1	1-5, 9, 12, 13 6, 11 7
X A	JP 2004-096021 A (SHOWA DENKO K.K.) 2004.03.25, paragraph[0068]-[0071] (Family: none)	1-5, 9 7
Y	JP 2003-133649 A (SHARP CORPORATION) 2003.05.09, paragraph[0058] & US 2005/042787 A1	6
X	JP 2004-080047 A (TOYODA GOSEI CO. LTD.) 2004.03.11, paragraph[0019], FIG1 (Family: none)	8, 10
Y	JP 2002-057161 A (SONY CORPORATION) 2002.02.22, paragraph[0051] & EP 1179859 A2	11

☐ Further documents are listed in the continuation of Box C.☐ See patent family annex.

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