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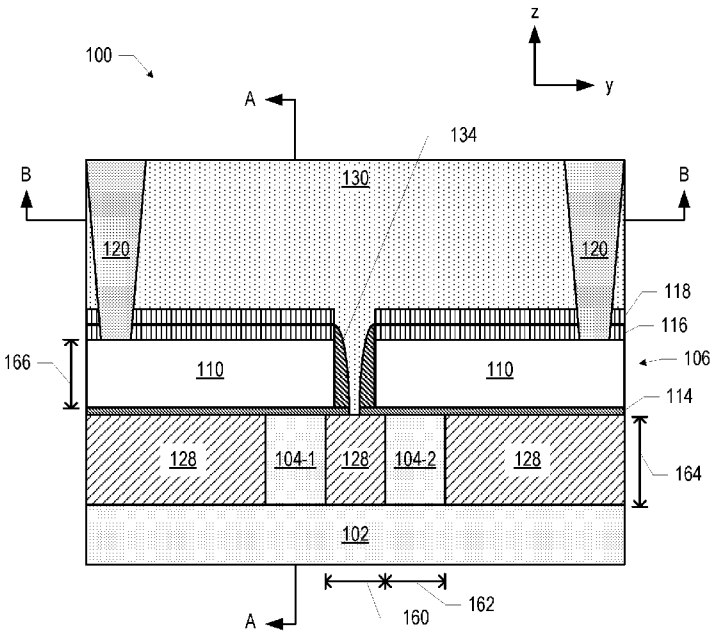

FIG. 1

(57) Abstract: Disclosed herein are quantum dot devices, as well as related computing devices and methods. For example, in some embodiments, a quantum dot device may include: a gate disposed on a quantum well stack; an insulating material disposed on the gate; and a conductive via extending through the insulating material and in conductive contact with the gate.

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INTERCONNECTS FOR QUANTUM DOT DEVICES

Background

[0001] Quantum computing refers to the field of research related to computation systems that use quantum mechanical phenomena to manipulate data. These quantum mechanical phenomena, such as superposition (in which a quantum variable can simultaneously exist in multiple different states) and entanglement (in which multiple quantum variables have related states irrespective of the distance between them in space or time), do not have analogs in the world of classical computing, and thus cannot be implemented with classical computing devices.

Brief Description of the Drawings

[0002] Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0003] FIGS. 1-3 are cross-sectional views of a quantum dot device, in accordance with various embodiments.

[0004] FIGS. 4-25 illustrate various example stages in the manufacture of a quantum dot device, in accordance with various embodiments.

[0005] FIGS. 26-28 are cross-sectional views of various examples of quantum well stacks that may be used in a quantum dot device, in accordance with various embodiments.

[0006] FIGS. 29-35 illustrate example base/fin arrangements that may be used in a quantum dot device, in accordance with various embodiments.

[0007] FIGS. 36-38 illustrate various example stages in the manufacture of alternative gate arrangements that may be included in a quantum dot device, in accordance with various embodiments.

[0008] FIG. 39 illustrates an embodiment of a quantum dot device having multiple groups of gates on a single fin, in accordance with various embodiments.

[0009] FIGS. 40-44 illustrate various alternative stages in the manufacture of a quantum dot device, in accordance with various embodiments.

[0010] FIG. 45 illustrates an example alternative stage in the manufacture of a quantum dot device, in accordance with various embodiments.

[0011] FIGS. 46-47 illustrate detail views of various embodiments of a doped region in a quantum dot device.

[0012] FIGS. 48-67 illustrate various example stages in the formation of interconnects in a quantum dot device, in accordance with various embodiments.

[0013] FIGS. 68-71 illustrate various alternative example stages in the formation of interconnects in a quantum dot device, in accordance with various embodiments.

[0014] FIG. 72 is a flow diagram of an illustrative method of manufacturing a quantum dot device, in accordance with various embodiments.

[0015] FIGS. 73-74 are flow diagrams of illustrative methods of operating a quantum dot device, in accordance with various embodiments.

[0016] FIG. 75 is a block diagram of an example quantum computing device that may include any of the quantum dot devices disclosed herein, in accordance with various embodiments.

Detailed Description

[0017] Disclosed herein are quantum dot devices, as well as related computing devices and methods. For example, in some embodiments, a quantum dot device may include: a gate disposed on a quantum well stack; an insulating material disposed on the gate; and a conductive via extending through the insulating material and in conductive contact with the gate.

[0018] The quantum dot devices disclosed herein may enable the formation of quantum dots to serve as quantum bits ("qubits") in a quantum computing device, as well as the control of these quantum dots to perform quantum logic operations. Unlike previous approaches to quantum dot formation and manipulation, various embodiments of the quantum dot devices disclosed herein provide strong spatial localization of the quantum dots (and therefore good control over quantum dot interactions and manipulation), good scalability in the number of quantum dots included in the device, and/or design flexibility in making electrical connections to the quantum dot devices to integrate the quantum dot devices in larger computing devices.

[0019] In the following detailed description, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, embodiments that may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense.

[0020] Various operations may be described as multiple discrete actions or operations in turn in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different order from the described embodiment. Various additional operations may be performed, and/or described operations may be omitted in additional embodiments.

[0021] For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B, and C). The term "between," when used with reference to measurement ranges, is inclusive of the ends of the measurement ranges. As used herein, the notation "A/B/C" means (A), (B), and/or (C).

[0022] The description uses the phrases "in an embodiment" or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous. The disclosure may use perspective-based descriptions such as "above," "below," "top," "bottom," and "side"; such descriptions are used to facilitate the discussion and are not intended to restrict the application of disclosed embodiments. The accompanying drawings are not necessarily drawn to scale. As used herein, a "high-k dielectric" refers to a material having a higher dielectric constant than silicon oxide.

[0023] FIGS. 1-3 are cross-sectional views of a quantum dot device 100, in accordance with various embodiments. In particular, FIG. 2 illustrates the quantum dot device 100 taken along the section A-A of FIG. 1 (while FIG. 1 illustrates the quantum dot device 100 taken along the section C-C of FIG. 2), and FIG. 3 illustrates the quantum dot device 100 taken along the section B-B of FIG. 1 with a number of components not shown to more readily illustrate how the gates 106/108 may be patterned (while FIG. 1 illustrates a quantum dot device 100 taken along the section D-D of FIG. 3). Although FIG. 1 indicates that the cross section illustrated in FIG. 2 is taken through the fin 104-1, an analogous cross section taken through the fin 104-2 may be identical, and thus the discussion of FIG. 2 refers generally to the "fin 104."

[0024] The quantum dot device 100 may include a base 102 and multiple fins 104 extending away from the base 102. The base 102 and the fins 104 may include a substrate and a quantum well stack (not shown in FIGS. 1-3, but discussed below with reference to the substrate 144 and the quantum well stack 146), distributed in any of a number of ways between the base 102 and the fins 104. The base 102 may include at least some of the substrate, and the fins 104 may each include a quantum well layer of the quantum well stack (discussed below with reference to the quantum well layer 152). Examples of base/fin arrangements are discussed below with reference to the base/fin arrangements 158 of FIGS. 29-35.

[0025] Although only two fins, 104-1 and 104-2, are shown in FIGS. 1-3, this is simply for ease of illustration, and more than two fins 104 may be included in the quantum dot device 100. In some embodiments, the total number of fins 104 included in the quantum dot device 100 is an even number, with the fins 104 organized into pairs including one active fin 104 and one read fin 104, as

discussed in detail below. When the quantum dot device 100 includes more than two fins 104, the fins 104 may be arranged in pairs in a line (e.g., 2N fins total may be arranged in a 1x2N line, or a 2xN line) or in pairs in a larger array (e.g., 2N fins total may be arranged as a 4xN/2 array, a 6xN/3 array, etc.). The discussion herein will largely focus on a single pair of fins 104 for ease of illustration, but all the teachings of the present disclosure apply to quantum dot devices 100 with more fins 104.

[0026] As noted above, each of the fins 104 may include a quantum well layer (not shown in FIGS. 1-3, but discussed below with reference to the quantum well layer 152). The quantum well layer included in the fins 104 may be arranged normal to the z-direction, and may provide a layer in which a two-dimensional electron gas (2DEG) may form to enable the generation of a quantum dot during operation of the quantum dot device 100, as discussed in further detail below. The quantum well layer itself may provide a geometric constraint on the z-location of quantum dots in the fins 104, and the limited extent of the fins 104 (and therefore the quantum well layer) in the y-direction may provide a geometric constraint on the y-location of quantum dots in the fins 104. To control the x-location of quantum dots in the fins 104, voltages may be applied to gates disposed on the fins 104 to adjust the energy profile along the fins 104 in the x-direction and thereby constrain the x-location of quantum dots within quantum wells (discussed in detail below with reference to the gates 106/108). The dimensions of the fins 104 may take any suitable values. For example, in some embodiments, the fins 104 may each have a width 162 between 10 and 30 nanometers. In some embodiments, the fins 104 may each have a height 164 between 200 and 400 nanometers (e.g., between 250 and 350 nanometers, or equal to 300 nanometers).

[0027] The fins 104 may be arranged in parallel, as illustrated in FIGS. 1 and 3, and may be spaced apart by an insulating material 128, which may be disposed on opposite faces of the fins 104. The insulating material 128 may be a dielectric material, such as silicon oxide. For example, in some embodiments, the fins 104 may be spaced apart by a distance 160 between 100 and 250 microns.

[0028] Multiple gates may be disposed on each of the fins 104. In the embodiment illustrated in FIG. 2, three gates 106 and two gates 108 are shown as distributed on the top of the fin 104. This particular number of gates is simply illustrative, and any suitable number of gates may be used. Additionally, as discussed below with reference to FIG. 39, multiple groups of gates (like the gates illustrated in FIG. 2) may be disposed on the fin 104.

[0029] As shown in FIG. 2, the gate 108-1 may be disposed between the gates 106-1 and 106-2, and the gate 108-2 may be disposed between the gates 106-2 and 106-3. Each of the gates 106/108 may include a gate dielectric 114; in the embodiment illustrated in FIG. 2, the gate dielectric 114 for all of the gates 106/108 is provided by a common layer of gate dielectric material. In other embodiments, the gate dielectric 114 for each of the gates 106/108 may be provided by separate portions of gate

dielectric 114 (e.g., as discussed below with reference to FIGS. 40-44). In some embodiments, the gate dielectric 114 may be a multilayer gate dielectric (e.g., with multiple materials used to improve the interface between the fin 104 and the corresponding gate metal). The gate dielectric 114 may be, for example, silicon oxide, aluminum oxide, or a high-k dielectric, such as hafnium oxide. More generally, the gate dielectric 114 may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of materials that may be used in the gate dielectric 114 may include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, tantalum oxide, tantalum silicon oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric 114 to improve the quality of the gate dielectric 114.

[0030] Each of the gates 106 may include a gate metal 110 and a hardmask 116. The hardmask 116 may be formed of silicon nitride, silicon carbide, or another suitable material. The gate metal 110 may be disposed between the hardmask 116 and the gate dielectric 114, and the gate dielectric 114 may be disposed between the gate metal 110 and the fin 104. Only one portion of the hardmask 116 is labeled in FIG. 2 for ease of illustration. In some embodiments, the gate metal 110 may be a superconductor, such as aluminum, titanium nitride (e.g., deposited via atomic layer deposition), or niobium titanium nitride. In some embodiments, the hardmask 116 may not be present in the quantum dot device 100 (e.g., a hardmask like the hardmask 116 may be removed during processing, as discussed below). The sides of the gate metal 110 may be substantially parallel, as shown in FIG. 2, and insulating spacers 134 may be disposed on the sides of the gate metal 110 and the hardmask 116. As illustrated in FIG. 2, the spacers 134 may be thicker closer to the fin 104 and thinner farther away from the fin 104. In some embodiments, the spacers 134 may have a convex shape. The spacers 134 may be formed of any suitable material, such as a carbon-doped oxide, silicon nitride, silicon oxide, or other carbides or nitrides (e.g., silicon carbide, silicon nitride doped with carbon, and silicon oxynitride). The gate metal 110 may be any suitable metal, such as titanium nitride.

[0031] Each of the gates 108 may include a gate metal 112 and a hardmask 118. The hardmask 118 may be formed of silicon nitride, silicon carbide, or another suitable material. The gate metal 112 may be disposed between the hardmask 118 and the gate dielectric 114, and the gate dielectric 114 may be disposed between the gate metal 112 and the fin 104. In the embodiment illustrated in FIG. 2, the hardmask 118 may extend over the hardmask 116 (and over the gate metal 110 of the gates

106), while in other embodiments, the hardmask 118 may not extend over the gate metal 110 (e.g., as discussed below with reference to FIG. 45). In some embodiments, the gate metal 112 may be a different metal from the gate metal 110; in other embodiments, the gate metal 112 and the gate metal 110 may have the same material composition. In some embodiments, the gate metal 112 may be a superconductor, such as aluminum, titanium nitride (e.g., deposited via atomic layer deposition), or niobium titanium nitride. In some embodiments, the hardmask 118 may not be present in the quantum dot device 100 (e.g., a hardmask like the hardmask 118 may be removed during processing, as discussed below).

[0032] The gate 108-1 may extend between the proximate spacers 134 on the sides of the gate 106-1 and the gate 106-2, as shown in FIG. 2. In some embodiments, the gate metal 112 of the gate 108-1 may extend between the spacers 134 on the sides of the gate 106-1 and the gate 106-2. Thus, the gate metal 112 of the gate 108-1 may have a shape that is substantially complementary to the shape of the spacers 134, as shown. Similarly, the gate 108-2 may extend between the proximate spacers 134 on the sides of the gate 106-2 and the gate 106-3. In some embodiments in which the gate dielectric 114 is not a layer shared commonly between the gates 108 and 106, but instead is separately deposited on the fin 104 between the spacers 134 (e.g., as discussed below with reference to FIGS. 40-44), the gate dielectric 114 may extend at least partially up the sides of the spacers 134, and the gate metal 112 may extend between the portions of gate dielectric 114 on the spacers 134. The gate metal 112, like the gate metal 110, may be any suitable metal, such as titanium nitride.

[0033] The dimensions of the gates 106/108 may take any suitable values. For example, in some embodiments, the z-height 166 of the gate metal 110 may be between 40 and 75 nanometers (e.g., approximately 50 nanometers); the z-height of the gate metal 112 may be in the same range. In embodiments like the ones illustrated in FIGS. 2, 38, and 45, the z-height of the gate metal 112 may be greater than the z-height of the gate metal 110. In some embodiments, the length 168 of the gate metal 110 (i.e., in the x-direction) may be between 20 and 40 nanometers (e.g., 30 nanometers). In some embodiments, the distance 170 between adjacent ones of the gates 106 (e.g., as measured from the gate metal 110 of one gate 106 to the gate metal 110 of an adjacent gate 106 in the x-direction, as illustrated in FIG. 2) may be between 40 and 60 nanometers (e.g., 50 nanometers). In some embodiments, the thickness 172 of the spacers 134 may be between 1 and 10 nanometers (e.g., between 3 and 5 nanometers, between 4 and 6 nanometers, or between 4 and 7 nanometers). The length of the gate metal 112 (i.e., in the x-direction) may depend on the dimensions of the gates 106 and the spacers 134, as illustrated in FIG. 2. As indicated in FIG. 1, the gates 106/108 on one fin 104 may extend over the insulating material 128 beyond their respective

fins 104 and towards the other fin 104, but may be isolated from their counterpart gates by the intervening insulating material 130 and spacers 134.

[0034] As shown in FIG. 2, the gates 106 and 108 may be alternatingly arranged along the fin 104 in the x-direction. During operation of the quantum dot device 100, voltages may be applied to the gates 106/108 to adjust the potential energy in the quantum well layer (not shown) in the fin 104 to create quantum wells of varying depths in which quantum dots 142 may form. Only one quantum dot 142 is labeled with a reference numeral in FIGS. 2 and 3 for ease of illustration, but five are indicated as dotted circles in each fin 104. The location of the quantum dots 142 in FIG. 2 is not intended to indicate a particular geometric positioning of the quantum dots 142. The spacers 134 may themselves provide "passive" barriers between quantum wells under the gates 106/108 in the quantum well layer, and the voltages applied to different ones of the gates 106/108 may adjust the potential energy under the gates 106/108 in the quantum well layer; decreasing the potential energy may form quantum wells, while increasing the potential energy may form quantum barriers.

[0035] The fins 104 may include doped regions 140 that may serve as a reservoir of charge carriers for the quantum dot device 100. For example, an n-type doped region 140 may supply electrons for electron-type quantum dots 142, and a p-type doped region 140 may supply holes for hole-type quantum dots 142. In some embodiments, an interface material 141 may be disposed at a surface of a doped region 140, as shown. The interface material 141 may facilitate electrical coupling between a conductive contact (e.g., a conductive via 136, as discussed below) and the doped region 140. The interface material 141 may be any suitable metal-semiconductor ohmic contact material; for example, in embodiments in which the doped region 140 includes silicon, the interface material 141 may include nickel silicide, aluminum silicide, titanium silicide, molybdenum silicide, cobalt silicide, tungsten silicide, or platinum silicide (e.g., as discussed below with reference to FIGS. 22-23). In some embodiments, the interface material 141 may be a non-silicide compound, such as titanium nitride. In some embodiments, the interface material 141 may be a metal (e.g., aluminum, tungsten, or indium).

[0036] The quantum dot devices 100 disclosed herein may be used to form electron-type or hole-type quantum dots 142. Note that the polarity of the voltages applied to the gates 106/108 to form quantum wells/barriers depend on the charge carriers used in the quantum dot device 100. In embodiments in which the charge carriers are electrons (and thus the quantum dots 142 are electron-type quantum dots), amply negative voltages applied to a gate 106/108 may increase the potential barrier under the gate 106/108, and amply positive voltages applied to a gate 106/108 may decrease the potential barrier under the gate 106/108 (thereby forming a potential well in which an electron-type quantum dot 142 may form). In embodiments in which the charge carriers are holes

(and thus the quantum dots 142 are hole-type quantum dots), amply positive voltages applied to a gate 106/108 may increase the potential barrier under the gate 106/108, and amply negative voltages applied to a gate 106 and 108 may decrease the potential barrier under the gate 106/108 (thereby forming a potential well in which a hole-type quantum dot 142 may form). The quantum dot devices 100 disclosed herein may be used to form electron-type or hole-type quantum dots.

[0037] Voltages may be applied to each of the gates 106 and 108 separately to adjust the potential energy in the quantum well layer under the gates 106 and 108, and thereby control the formation of quantum dots 142 under each of the gates 106 and 108. Additionally, the relative potential energy profiles under different ones of the gates 106 and 108 allow the quantum dot device 100 to tune the potential interaction between quantum dots 142 under adjacent gates. For example, if two adjacent quantum dots 142 (e.g., one quantum dot 142 under a gate 106 and another quantum dot 142 under a gate 108) are separated by only a short potential barrier, the two quantum dots 142 may interact more strongly than if they were separated by a taller potential barrier. Since the depth of the potential wells/height of the potential barriers under each gate 106/108 may be adjusted by adjusting the voltages on the respective gates 106/108, the differences in potential between adjacent gates 106/108 may be adjusted, and thus the interaction tuned.

[0038] In some applications, the gates 108 may be used as plunger gates to enable the formation of quantum dots 142 under the gates 108, while the gates 106 may be used as barrier gates to adjust the potential barrier between quantum dots 142 formed under adjacent gates 108. In other applications, the gates 108 may be used as barrier gates, while the gates 106 are used as plunger gates. In other applications, quantum dots 142 may be formed under all of the gates 106 and 108, or under any desired subset of the gates 106 and 108.

[0039] Conductive vias and lines may make contact with the gates 106/108, and to the doped regions 140, to enable electrical connection to the gates 106/108 and the doped regions 140 to be made in desired locations. As shown in FIGS. 1-3, the gates 106 may extend away from the fins 104, and conductive vias 120 may contact the gates 106 (and are drawn in dashed lines in FIG. 2 to indicate their location behind the plane of the drawing). The conductive vias 120 may extend through the hardmask 116 and the hardmask 118 to contact the gate metal 110 of the gates 106. The gates 108 may extend away from the fins 104, and conductive vias 122 may contact the gates 108 (also drawn in dashed lines in FIG. 2 to indicate their location behind the plane of the drawing). The conductive vias 122 may extend through the hardmask 118 to contact the gate metal 112 of the gates 108. Conductive vias 136 may contact the interface material 141 and may thereby make electrical contact with the doped regions 140. The quantum dot device 100 may include further conductive vias and/or lines (not shown) to make electrical contact to the gates 106/108 and/or the

doped regions 140, as desired. Example techniques for forming conductive vias 120/122/136 (as well as conductive lines and further interconnect structures to contact the conductive vias 120/122/136) are discussed below with reference to FIGS. 48-71. The conductive vias and lines included in a quantum dot device 100 may include any suitable materials, such as copper, tungsten (deposited, e.g., by CVD), or a superconductor (e.g., aluminum, tin, titanium nitride, niobium titanium nitride, tantalum, niobium, or other niobium compounds such as niobium tin and niobium germanium).

[0040] During operation, a bias voltage may be applied to the doped regions 140 (e.g., via the conductive vias 136 and the interface material 141) to cause current to flow through the doped regions 140. When the doped regions 140 are doped with an n-type material, this voltage may be positive; when the doped regions 140 are doped with a p-type material, this voltage may be negative. The magnitude of this bias voltage may take any suitable value (e.g., between 0.25 volts and 2 volts).

[0041] The conductive vias 120, 122, and 136 may be electrically isolated from each other by an insulating material 130. The insulating material 130 may be any suitable material, such as an interlayer dielectric (ILD). Examples of the insulating material 130 may include silicon oxide, silicon nitride, aluminum oxide, carbon-doped oxide, and/or silicon oxynitride. As known in the art of integrated circuit manufacturing, conductive vias and lines may be formed in an iterative process in which layers of structures are formed on top of each other. In some embodiments, the conductive vias 120/122/136 may have a width that is 20 nanometers or greater at their widest point (e.g., 30 nanometers), and a pitch of 80 nanometers or greater (e.g., 100 nanometers). In some embodiments, conductive lines (not shown) included in the quantum dot device 100 may have a width that is 100 nanometers or greater, and a pitch of 100 nanometers or greater. The particular arrangement of conductive vias shown in FIGS. 1-3 is simply illustrative, and any electrical routing arrangement may be implemented.

[0042] As discussed above, the structure of the fin 104-1 may be the same as the structure of the fin 104-2; similarly, the construction of gates 106/108 on the fin 104-1 may be the same as the construction of gates 106/108 on the fin 104-2. The gates 106/108 on the fin 104-1 may be mirrored by corresponding gates 106/108 on the parallel fin 104-2, and the insulating material 130 may separate the gates 106/108 on the different fins 104-1 and 104-2. In particular, quantum dots 142 formed in the fin 104-1 (under the gates 106/108) may have counterpart quantum dots 142 in the fin 104-2 (under the corresponding gates 106/108). In some embodiments, the quantum dots 142 in the fin 104-1 may be used as "active" quantum dots in the sense that these quantum dots 142 act as qubits and are controlled (e.g., by voltages applied to the gates 106/108 of the fin 104-1) to perform

quantum computations. The quantum dots 142 in the fin 104-2 may be used as "read" quantum dots in the sense that these quantum dots 142 may sense the quantum state of the quantum dots 142 in the fin 104-1 by detecting the electric field generated by the charge in the quantum dots 142 in the fin 104-1, and may convert the quantum state of the quantum dots 142 in the fin 104-1 into electrical signals that may be detected by the gates 106/108 on the fin 104-2. Each quantum dot 142 in the fin 104-1 may be read by its corresponding quantum dot 142 in the fin 104-2. Thus, the quantum dot device 100 enables both quantum computation and the ability to read the results of a quantum computation.

[0043] The quantum dot devices 100 disclosed herein may be manufactured using any suitable techniques. FIGS. 4-25 illustrate various example stages in the manufacture of the quantum dot device 100 of FIGS. 1-3, in accordance with various embodiments. Although the particular manufacturing operations discussed below with reference to FIGS. 4-25 are illustrated as manufacturing a particular embodiment of the quantum dot device 100, these operations may be applied to manufacture many different embodiments of the quantum dot device 100, as discussed herein. Any of the elements discussed below with reference to FIGS. 4-25 may take the form of any of the embodiments of those elements discussed above (or otherwise disclosed herein).

[0044] FIG. 4 illustrates a cross-sectional view of an assembly 200 including a substrate 144. The substrate 144 may include any suitable semiconductor material or materials. In some embodiments, the substrate 144 may include a semiconductor material. For example, the substrate 144 may include silicon (e.g., may be formed from a silicon wafer).

[0045] FIG. 5 illustrates a cross-sectional view of an assembly 202 subsequent to providing a quantum well stack 146 on the substrate 144 of the assembly 200 (FIG. 4). The quantum well stack 146 may include a quantum well layer (not shown) in which a 2DEG may form during operation of the quantum dot device 100. Various embodiments of the quantum well stack 146 are discussed below with reference to FIGS. 26-28.

[0046] FIG. 6 illustrates a cross-sectional view of an assembly 204 subsequent to forming fins 104 in the assembly 202 (FIG. 5). The fins 104 may extend from a base 102, and may be formed in the assembly 202 by patterning and then etching the assembly 202, as known in the art. For example, a combination of dry and wet etch chemistry may be used to form the fins 104, and the appropriate chemistry may depend on the materials included in the assembly 202, as known in the art. At least some of the substrate 144 may be included in the base 102, and at least some of the quantum well stack 146 may be included in the fins 104. In particular, the quantum well layer (not shown) of the quantum well stack 146 may be included in the fins 104. Example arrangements in which the

quantum well stack 146 and the substrate 144 are differently included in the base 102 and the fins 104 are discussed below with reference to FIGS. 29-35.

[0047] FIG. 7 illustrates a cross-sectional view of an assembly 206 subsequent to providing an insulating material 128 to the assembly 204 (FIG. 6). Any suitable material may be used as the insulating material 128 to electrically insulate the fins 104 from each other. As noted above, in some embodiments, the insulating material 128 may be a dielectric material, such as silicon oxide.

[0048] FIG. 8 illustrates a cross-sectional view of an assembly 208 subsequent to planarizing the assembly 206 (FIG. 7) to remove the insulating material 128 above the fins 104. In some embodiments, the assembly 206 may be planarized using a chemical mechanical polishing (CMP) technique.

[0049] FIG. 9 is a perspective view of at least a portion of the assembly 208, showing the fins 104 extending from the base 102 and separated by the insulating material 128. The cross-sectional views of FIGS. 4-8 are taken parallel to the plane of the page of the perspective view of FIG. 9. FIG. 10 is another cross-sectional view of the assembly 208, taken along the dashed line along the fin 104-1 in FIG. 9. The cross-sectional views illustrated in FIGS. 11-25 are taken along the same cross-section as FIG. 10.

[0050] FIG. 11 is a cross-sectional view of an assembly 210 subsequent to forming a gate stack 174 on the fins 104 of the assembly 208 (FIGS. 8-10). The gate stack 174 may include the gate dielectric 114, the gate metal 110, and a hardmask 116. The hardmask 116 may be formed of an electrically insulating material, such as silicon nitride or carbon-doped nitride.

[0051] FIG. 12 is a cross-sectional view of an assembly 212 subsequent to patterning the hardmask 116 of the assembly 210 (FIG. 11). The pattern applied to the hardmask 116 may correspond to the locations for the gates 106, as discussed below. The hardmask 116 may be patterned by applying a resist, patterning the resist using lithography, and then etching the hardmask (using dry etching or any appropriate technique).

[0052] FIG. 13 is a cross-sectional view of an assembly 214 subsequent to etching the assembly 212 (FIG. 12) to remove the gate metal 110 that is not protected by the patterned hardmask 116 to form the gates 106. In some embodiments, as illustrated in FIG. 13, the gate dielectric 114 may remain after the etched gate metal 110 is etched away; in other embodiments, the gate dielectric 114 may also be etched during the etching of the gate metal 110. Examples of such embodiments are discussed below with reference to FIGS. 40-44.

[0053] FIG. 14 is a cross-sectional view of an assembly 216 subsequent to providing spacer material 132 on the assembly 214 (FIG. 13). The spacer material 132 may include any of the materials discussed above with reference to the spacers 134, for example, and may be deposited using any

suitable technique. For example, the spacer material 132 may be a nitride material (e.g., silicon nitride) deposited by sputtering.

[0054] FIG. 15 is a cross-sectional view of an assembly 218 subsequent to etching the spacer material 132 of the assembly 216 (FIG. 14), leaving spacers 134 formed of the spacer material 132 on the sides of the gates 106 (e.g., on the sides of the hardmask 116 and the gate metal 110). The etching of the spacer material 132 may be an anisotropic etch, etching the spacer material 132 "downward" to remove the spacer material 132 on top of the gates 106 and in some of the area between the gates 106, while leaving the spacers 134 on the sides of the gates 106. In some embodiments, the anisotropic etch may be a dry etch.

[0055] FIG. 16 is a cross-sectional view of an assembly 220 subsequent to providing the gate metal 112 on the assembly 218 (FIG. 15). The gate metal 112 may fill the areas between adjacent ones of the gates 106, and may extend over the tops of the gates 106.

[0056] FIG. 17 is a cross-sectional view of an assembly 222 subsequent to planarizing the assembly 220 (FIG. 16) to remove the gate metal 112 above the gates 106. In some embodiments, the assembly 220 may be planarized using a CMP technique. Some of the remaining gate metal 112 may fill the areas between adjacent ones of the gates 106, while other portions 150 of the remaining gate metal 112 may be located "outside" of the gates 106.

[0057] FIG. 18 is a cross-sectional view of an assembly 224 subsequent to providing a hardmask 118 on the planarized surface of the assembly 222 (FIG. 17). The hardmask 118 may be formed of any of the materials discussed above with reference to the hardmask 116, for example.

[0058] FIG. 19 is a cross-sectional view of an assembly 226 subsequent to patterning the hardmask 118 of the assembly 224 (FIG. 18). The pattern applied to the hardmask 118 may extend over the hardmask 116 (and over the gate metal 110 of the gates 106, as well as over the locations for the gates 108 (as illustrated in FIG. 2). The hardmask 118 may be non-coplanar with the hardmask 116, as illustrated in FIG. 19. The hardmask 118 illustrated in FIG. 19 may thus be a common, continuous portion of hardmask 118 that extends over all of the hardmask 116. Examples of embodiments in which the hardmask 118 is not disposed over the entirety of the hardmask 116 are discussed below with reference to FIGS. 36-38 and 45. The hardmask 118 may be patterned using any of the techniques discussed above with reference to the patterning of the hardmask 116, for example.

[0059] FIG. 20 is a cross-sectional view of an assembly 228 subsequent to etching the assembly 226 (FIG. 19) to remove the portions 150 that are not protected by the patterned hardmask 118 to form the gates 108. Portions of the hardmask 118 may remain on top of the hardmask 116, as shown. The operations performed on the assembly 226 may include removing any gate dielectric 114 that is

"exposed" on the fin 104, as shown. The excess gate dielectric 114 may be removed using any suitable technique, such as chemical etching or silicon bombardment.

[0060] FIG. 21 is a cross-sectional view of an assembly 230 subsequent to doping the fins 104 of the assembly 228 (FIG. 20) to form doped regions 140 in the portions of the fins 104 "outside" of the gates 106/108. The type of dopant used to form the doped regions 140 may depend on the type of quantum dot desired, as discussed above. In some embodiments, the doping may be performed by ion implantation. For example, when the quantum dot 142 is to be an electron-type quantum dot 142, the doped regions 140 may be formed by ion implantation of phosphorous, arsenic, or another n-type material. When the quantum dot 142 is to be a hole-type quantum dot 142, the doped regions 140 may be formed by ion implantation of boron or another p-type material. An annealing process that activates the dopants and causes them to diffuse farther into the fins 104 may follow the ion implantation process. The depth of the doped regions 140 may take any suitable value; for example, in some embodiments, the doped regions 140 may extend into the fin 104 to a depth 115 between 500 and 1000 Angstroms.

[0061] The outer spacers 134 on the outer gates 106 may provide a doping boundary, limiting diffusion of the dopant from the doped regions 140 into the area under the gates 106/108. As shown, the doped regions 140 may extend under the adjacent outer spacers 134. In some embodiments, the doped regions 140 may extend past the outer spacers 134 and under the gate metal 110 of the outer gates 106, may extend only to the boundary between the outer spacers 134 and the adjacent gate metal 110, or may terminate under the outer spacers 134 and not reach the boundary between the outer spacers 134 and the adjacent gate metal 110. Examples of such embodiments are discussed below with reference to FIGS. 46 and 47. The doping concentration of the doped regions 140 may, in some embodiments, be between $10^{17}/cm^3$ and $10^{20}/cm^3$.

[0062] FIG. 22 is a cross-sectional side view of an assembly 232 subsequent to providing a layer of nickel or other material 143 over the assembly 230 (FIG. 21). The nickel or other material 143 may be deposited on the assembly 230 using any suitable technique (e.g., a plating technique, chemical vapor deposition, or atomic layer deposition).

[0063] FIG. 23 is a cross-sectional side view of an assembly 234 subsequent to annealing the assembly 232 (FIG. 22) to cause the material 143 to interact with the doped regions 140 to form the interface material 141, then removing the unreacted material 143. When the doped regions 140 include silicon and the material 143 includes nickel, for example, the interface material 141 may be nickel silicide. Materials other than nickel may be deposited in the operations discussed above with reference to FIG. 22 in order to form other interface materials 141, including titanium, aluminum, molybdenum, cobalt, tungsten, or platinum, for example. More generally, the interface material 141

of the assembly 234 may include any of the materials discussed herein with reference to the interface material 141.

[0064] FIG. 24 is a cross-sectional view of an assembly 236 subsequent to providing an insulating material 130 on the assembly 234 (FIG. 23). The insulating material 130 may take any of the forms discussed above. For example, the insulating material 130 may be a dielectric material, such as silicon oxide. The insulating material 130 may be provided on the assembly 234 using any suitable technique, such as spin coating, chemical vapor deposition (CVD), or plasma-enhanced CVD (PECVD). In some embodiments, the insulating material 130 may be polished back after deposition, and before further processing.

[0065] FIG. 25 is a cross-sectional view of an assembly 238 subsequent to forming, in the assembly 236 (FIG. 24), conductive vias 120 through the insulating material 130 (and the hardmasks 116 and 118) to contact the gate metal 110 of the gates 106, conductive vias 122 through the insulating material 130 (and the hardmask 118) to contact the gate metal 112 of the gates 108, and conductive vias 136 through the insulating material 130 to contact the interface material 141 of the doped regions 140. Further conductive vias and/or lines may be formed on the assembly 238 using conventional interconnect techniques, if desired. The resulting assembly 238 may take the form of the quantum dot device 100 discussed above with reference to FIGS. 1-3. In some embodiments, the assembly 236 may be planarized to remove the hardmasks 116 and 118, then additional insulating material 130 may be provided on the planarized surface before forming the conductive vias 120, 122, and 136; in such an embodiment, the hardmasks 116 and 118 would not be present in the quantum dot device 100.

[0066] As discussed above, the base 102 and the fin 104 of a quantum dot device 100 may be formed from a substrate 144 and a quantum well stack 146 disposed on the substrate 144. The quantum well stack 146 may include a quantum well layer in which a 2DEG may form during operation of the quantum dot device 100. The quantum well stack 146 may take any of a number of forms, several of which are illustrated in FIGS. 26-28. The various layers in the quantum well stacks 146 discussed below may be grown on the substrate 144 (e.g., using epitaxial processes).

[0067] FIG. 26 is a cross-sectional view of a quantum well stack 146 including only a quantum well layer 152. The quantum well layer 152 may be disposed on the substrate 144 (e.g., as discussed above with reference to FIG. 5), and may be formed of a material such that, during operation of the quantum dot device 100, a 2DEG may form in the quantum well layer 152 proximate to the upper surface of the quantum well layer 152. The gate dielectric 114 of the gates 106/108 may be disposed on the upper surface of the quantum well layer 152 (e.g., as discussed above with reference to FIG. 11). In some embodiments, the quantum well layer 152 of FIG. 26 may be formed

of intrinsic silicon, and the gate dielectric 114 may be formed of silicon oxide; in such an arrangement, during use of the quantum dot device 100, a 2DEG may form in the intrinsic silicon at the interface between the intrinsic silicon and the silicon oxide. Embodiments in which the quantum well layer 152 of FIG. 26 is formed of intrinsic silicon may be particularly advantageous for electron-type quantum dot devices 100. In some embodiments, the quantum well layer 152 of FIG. 26 may be formed of intrinsic germanium, and the gate dielectric 114 may be formed of germanium oxide; in such an arrangement, during use of the quantum dot device 100, a 2DEG may form in the intrinsic germanium at the interface between the intrinsic germanium and the germanium oxide. Such embodiments may be particularly advantageous for hole-type quantum dot devices 100. In some embodiments, the quantum well layer 152 may be strained, while in other embodiments, the quantum well layer 152 may not be strained. The thicknesses (i.e., z-heights) of the layers in the quantum well stack 146 of FIG. 26 may take any suitable values. For example, in some embodiments, the thickness of the quantum well layer 152 (e.g., intrinsic silicon or germanium) may be between 0.8 and 1.2 microns.

[0068] FIG. 27 is a cross-sectional view of a quantum well stack 146 including a quantum well layer 152 and a barrier layer 154. The quantum well stack 146 may be disposed on a substrate 144 (e.g., as discussed above with reference to FIG. 5) such that the barrier layer 154 is disposed between the quantum well layer 152 and the substrate 144. The barrier layer 154 may provide a potential barrier between the quantum well layer 152 and the substrate 144. As discussed above with reference to FIG. 26, the quantum well layer 152 of FIG. 27 may be formed of a material such that, during operation of the quantum dot device 100, a 2DEG may form in the quantum well layer 152 proximate to the upper surface of the quantum well layer 152. For example, in some embodiments in which the substrate 144 is formed of silicon, the quantum well layer 152 of FIG. 27 may be formed of silicon, and the barrier layer 154 may be formed of silicon germanium. The germanium content of this silicon germanium may be 20-80% (e.g., 30%). In some embodiments in which the quantum well layer 152 is formed of germanium, the barrier layer 154 may be formed of silicon germanium (with a germanium content of 20-80% (e.g., 70%)). The thicknesses (i.e., z-heights) of the layers in the quantum well stack 146 of FIG. 27 may take any suitable values. For example, in some embodiments, the thickness of the barrier layer 154 (e.g., silicon germanium) may be between 0 and 400 nanometers. In some embodiments, the thickness of the quantum well layer 152 (e.g., silicon or germanium) may be between 5 and 30 nanometers.

[0069] FIG. 28 is a cross-sectional view of a quantum well stack 146 including a quantum well layer 152 and a barrier layer 154-1, as well as a buffer layer 176 and an additional barrier layer 154-2. The quantum well stack 146 may be disposed on the substrate 144 (e.g., as discussed above with

reference to FIG. 5) such that the buffer layer 176 is disposed between the barrier layer 154-1 and the substrate 144. The buffer layer 176 may be formed of the same material as the barrier layer 154, and may be present to trap defects that form in this material as it is grown on the substrate 144. In some embodiments, the buffer layer 176 may be grown under different conditions (e.g., deposition temperature or growth rate) from the barrier layer 154-1. In particular, the barrier layer 154-1 may be grown under conditions that achieve fewer defects than the buffer layer 176. In some embodiments in which the buffer layer 176 includes silicon germanium, the silicon germanium of the buffer layer 176 may have a germanium content that varies from the substrate 144 to the barrier layer 154-1; for example, the silicon germanium of the buffer layer 176 may have a germanium content that varies from zero percent at the silicon substrate 144 to a nonzero percent (e.g., 30%) at the barrier layer 154-1. The thicknesses (i.e., z-heights) of the layers in the quantum well stack 146 of FIG. 28 may take any suitable values. For example, in some embodiments, the thickness of the buffer layer 176 (e.g., silicon germanium) may be between 0.3 and 4 microns (e.g., 0.3-2 microns, or 0.5 microns). In some embodiments, the thickness of the barrier layer 154-1 (e.g., silicon germanium) may be between 0 and 400 nanometers. In some embodiments, the thickness of the quantum well layer 152 (e.g., silicon or germanium) may be between 5 and 30 nanometers (e.g., 10 nanometers). The barrier layer 154-2, like the barrier layer 154-1, may provide a potential energy barrier around the quantum well layer 152, and may take the form of any of the embodiments of the barrier layer 154-1. In some embodiments, the thickness of the barrier layer 154-2 (e.g., silicon germanium) may be between 25 and 75 nanometers (e.g., 32 nanometers).

[0070] As discussed above with reference to FIG. 27, the quantum well layer 152 of FIG. 28 may be formed of a material such that, during operation of the quantum dot device 100, a 2DEG may form in the quantum well layer 152 proximate to the upper surface of the quantum well layer 152. For example, in some embodiments in which the substrate 144 is formed of silicon, the quantum well layer 152 of FIG. 28 may be formed of silicon, and the barrier layer 154-1 and the buffer layer 176 may be formed of silicon germanium. In some such embodiments, the silicon germanium of the buffer layer 176 may have a germanium content that varies from the substrate 144 to the barrier layer 154-1; for example, the silicon germanium of the buffer layer 176 may have a germanium content that varies from zero percent at the silicon substrate 144 to a nonzero percent (e.g., 30%) at the barrier layer 154-1. The barrier layer 154-1 may in turn have a germanium content equal to the nonzero percent. In other embodiments, the buffer layer 176 may have a germanium content equal to the germanium content of the barrier layer 154-1 but may be thicker than the barrier layer 154-1 so as to absorb the defects that arise during growth.

[0071] In some embodiments, the quantum well layer 152 of FIG. 28 may be formed of germanium, and the buffer layer 176 and the barrier layer 154-1 may be formed of silicon germanium. In some such embodiments, the silicon germanium of the buffer layer 176 may have a germanium content that varies from the substrate 144 to the barrier layer 154-1; for example, the silicon germanium of the buffer layer 176 may have a germanium content that varies from zero percent at the substrate 144 to a nonzero percent (e.g., 70%) at the barrier layer 154-1. The barrier layer 154-1 may in turn have a germanium content equal to the nonzero percent. In other embodiments, the buffer layer 176 may have a germanium content equal to the germanium content of the barrier layer 154-1 but may be thicker than the barrier layer 154-1 so as to absorb the defects that arise during growth. In some embodiments of the quantum well stack 146 of FIG. 28, the buffer layer 176 and/or the barrier layer 154-2 may be omitted.

[0072] The substrate 144 and the quantum well stack 146 may be distributed between the base 102 and the fins 104 of the quantum dot device 100, as discussed above. This distribution may occur in any of a number of ways. For example, FIGS. 29-35 illustrate example base/fin arrangements 158 that may be used in a quantum dot device 100, in accordance with various embodiments.

[0073] In the base/fin arrangement 158 of FIG. 29, the quantum well stack 146 may be included in the fins 104, but not in the base 102. The substrate 144 may be included in the base 102, but not in the fins 104. When the base/fin arrangement 158 of FIG. 29 is used in the manufacturing operations discussed with reference to FIGS. 5-6, the fin etching may etch through the quantum well stack 146, and stop when the substrate 144 is reached.

[0074] In the base/fin arrangement 158 of FIG. 30, the quantum well stack 146 may be included in the fins 104, as well as in a portion of the base 102. A substrate 144 may be included in the base 102 as well, but not in the fins 104. When the base/fin arrangement 158 of FIG. 30 is used in the manufacturing operations discussed with reference to FIGS. 5-6, the fin etching may etch partially through the quantum well stack 146, and stop before the substrate 144 is reached. FIG. 31 illustrates a particular embodiment of the base/fin arrangement 158 of FIG. 30. In the embodiment of FIG. 31, the quantum well stack 146 of FIG. 28 is used; the fins 104 include the barrier layer 154-1, the quantum well layer 152, and the barrier layer 154-2, while the base 102 includes the buffer layer 176 and the substrate 144.

[0075] In the base/fin arrangement 158 of FIG. 32, the quantum well stack 146 may be included in the fins 104, but not the base 102. The substrate 144 may be partially included in the fins 104, as well as in the base 102. When the base/fin arrangement 158 of FIG. 32 is used in the manufacturing operations discussed with reference to FIGS. 5-6, the fin etching may etch through the quantum well stack 146 and into the substrate 144 before stopping. FIG. 33 illustrates a particular embodiment of

the base/fin arrangement 158 of FIG. 32. In the embodiment of FIG. 33, the quantum well stack 146 of FIG. 28 is used; the fins 104 include the quantum well stack 146 and a portion of the substrate 144, while the base 102 includes the remainder of the substrate 144.

[0076] Although the fins 104 have been illustrated in many of the preceding figures as substantially rectangular with parallel sidewalls, this is simply for ease of illustration, and the fins 104 may have any suitable shape (e.g., shape appropriate to the manufacturing processes used to form the fins 104). For example, as illustrated in the base/fin arrangement 158 of FIG. 34, in some embodiments, the fins 104 may be tapered. In some embodiments, the fins 104 may taper by 3-10 nanometers in x-width for every 100 nanometers in z-height (e.g., 5 nanometers in x-width for every 100 nanometers in z-height). When the fins 104 are tapered, the wider end of the fins 104 may be the end closest to the base 102, as illustrated in FIG. 34. FIG. 35 illustrates a particular embodiment of the base/fin arrangement 158 of FIG. 34. In FIG. 35, the quantum well stack 146 is included in the tapered fins 104 while a portion of the substrate 144 is included in the tapered fins and a portion of the substrate 144 provides the base 102.

[0077] In the embodiment of the quantum dot device 100 illustrated in FIG. 2, the z-height of the gate metal 112 of the gates 108 may be approximately equal to the sum of the z-height of the gate metal 110 and the z-height of the hardmask 116, as shown. Also in the embodiment of FIG. 2, the gate metal 112 of the gates 108 may not extend in the x-direction beyond the adjacent spacers 134. In other embodiments, the z-height of the gate metal 112 of the gates 108 may be greater than the sum of the z-height of the gate metal 110 and the z-height of the hardmask 116, and in some such embodiments, the gate metal 112 of the gates may extend beyond the spacers 134 in the x-direction. FIGS. 36-38 illustrate various example stages in the manufacture of alternative gate arrangements that may be included in a quantum dot device 100, in accordance with various embodiments.

[0078] FIG. 36 illustrates an assembly 242 subsequent to providing the gate metal 112 and a hardmask 118 on the assembly 218 (FIG. 15). The assembly 242 may be similar to the assembly 224 of FIG. 18 (and may be formed using any of the techniques discussed above with reference to FIGS. 16-18), but may include additional gate metal 112 between the hardmask 116 and the hardmask 118, of any desired thickness. In some embodiments, the gate metal 112 may be planarized prior to provision of the hardmask 118, but the hardmask 118 may still be spaced away from the hardmask 116 in the z-direction by the gate metal 112, as shown in FIG. 36.

[0079] FIG. 37 illustrates an assembly 244 subsequent to patterning the hardmask 118 of the assembly 242 (FIG. 36). The pattern applied to the hardmask 118 may include the locations for the gates 108, as discussed below. The hardmask 118 may be non-coplanar with the hardmask 116, as

illustrated in FIG. 36, and may extend "over" at least a portion of the hardmask 116 (and thus over the gate metal 110 of the gates 106).

[0080] FIG. 38 illustrates an assembly 246 subsequent to etching the assembly 244 (FIG. 37) to remove the portions 150 that are not protected by the patterned hardmask 118 to form the gates 108. The gate metal 112 of the gates 106 may extend "over" the hardmask 116 of the gates 108, and may be electrically insulated from the gate metal 110 by the hardmask 116. In the embodiment illustrated in FIG. 38, the z-height of the gate metal 112 of the gates 108 may be greater than the sum of the z-height of the gate metal 110 and the z-height of the hardmask 116 of the gates 106. Additionally, the gate metal 112 of the gates 108 may extend beyond the spacers 134 in the x-direction, as shown. Further manufacturing operations may be performed on the assembly 246, as discussed above with reference to FIGS. 21-25.

[0081] As noted above, a single fin 104 may include multiple groups of gates 106/108, spaced apart along the fin by a doped region 140. FIG. 39 is a cross-sectional view of an example of such a quantum dot device 100 having multiple groups of gates 180 on a single fin 104, in accordance with various embodiments. Each of the groups 180 may include gates 106/108 (not labeled in FIG. 39 for ease of illustration) that may take the form of any of the embodiments of the gates 106/108 discussed herein. A doped region 140 (and its interface material 141) may be disposed between two adjacent groups 180 (labeled in FIG. 39 as groups 180-1 and 180-2), and may provide a common reservoir for both groups 180. In some embodiments, this "common" doped region 140 may be electrically contacted by a single conductive via 136. The particular number of gates 106/108 illustrated in FIG. 39, and the particular number of groups 180, is simply illustrative, and a fin 104 may include any suitable number of gates 106/108 arranged in any suitable number of groups 180.

[0082] As discussed above with reference to FIGS. 1-3, in some embodiments in which the gate dielectric 114 is not a layer shared commonly between the gates 108 and 106, but instead is separately deposited on the fin 104 between the spacers 134, the gate dielectric 114 may extend at least partially up the sides of the spacers 134, and the gate metal 112 may extend between the portions of gate dielectric 114 on the spacers 134. FIGS. 40-44 illustrate various alternative stages in the manufacture of such an embodiment of a quantum dot device 100, in accordance with various embodiments. In particular, the operations illustrated in FIGS. 40-44 may take the place of the operations illustrated in FIGS. 13-15.

[0083] FIG. 40 is a cross-sectional view of an assembly 248 subsequent to etching the assembly 212 (FIG. 12) to remove the gate metal 110, and the gate dielectric 114 that is not protected by the patterned hardmask 116, to form the gates 106.

[0084] FIG. 41 is a cross-sectional view of an assembly 250 subsequent to providing spacer material 132 on the assembly 248 (FIG. 40). The deposition of the spacer material 132 may take any of the forms discussed above with reference to FIG. 14, for example.

[0085] FIG. 42 is a cross-sectional view of an assembly 252 subsequent to etching the spacer material 132 of the assembly 250 (FIG. 41), leaving spacers 134 formed of the spacer material 132 on the sides of the gates 106 (e.g., on the sides of the hardmask 116, the gate metal 110, and the gate dielectric 114). The etching of the spacer material 132 may take any of the forms discussed above with reference to FIG. 15, for example.

[0086] FIG. 43 is a cross-sectional view of an assembly 254 subsequent to providing a gate dielectric 114 on the fin 104 between the gates 106 of the assembly 252 (FIG. 42). In some embodiments, the gate dielectric 114 provided between the gates 106 of the assembly 252 may be formed by atomic layer deposition (ALD) and, as illustrated in FIG. 43, may cover the exposed fin 104 between the gates 106, and may extend onto the adjacent spacers 134.

[0087] FIG. 44 is a cross-sectional view of an assembly 256 subsequent to providing the gate metal 112 on the assembly 254 (FIG. 43). The gate metal 112 may fill the areas between adjacent ones of the gates 106, and may extend over the tops of the gates 106, as shown. The provision of the gate metal 112 may take any of the forms discussed above with reference to FIG. 16, for example. The assembly 256 may be further processed as discussed above with reference to FIGS. 17-25.

[0088] As discussed above with reference to FIG. 19, in some embodiments, the pattern applied to the hardmask 118 (used for patterning the gates 108) may not result in a common, continuous portion of hardmask 118 that extends over all of the hardmask 116. One such example was discussed above with reference to FIGS. 36-38, and another example of such an embodiment is illustrated in FIG. 45. In particular, FIG. 45 is a cross-sectional view of an assembly 258 in which the hardmask 118 of the assembly 224 (FIG. 18) is not patterned to extend over the gates 106, but instead is patterned so as not to extend over the gate metal 110. The assembly 258 may be further processed as discussed above with reference to FIGS. 20-25 (e.g., etching away the excess portions 150, etc.). In some embodiments, the hardmasks 116 and 118 may remain in the quantum dot device 100 as part of the gates 106/108, while in other embodiments, the hardmasks 116 and 118 may be removed.

[0089] As discussed above with reference to FIGS. 2 and 21, the outer spacers 134 on the outer gates 106 may provide a doping boundary, limiting diffusion of the dopant from the doped regions 140 into the area under the gates 106/108. In some embodiments, the doped regions 140 may extend past the outer spacers 134 and under the outer gates 106. For example, as illustrated in FIG. 46, the doped region 140 may extend past the outer spacers 134 and under the outer gates 106 by a

distance 182 between 0 and 10 nanometers. In some embodiments, the doped regions 140 may not extend past the outer spacers 134 toward the outer gates 106, but may instead "terminate" under the outer spacers 134. For example, as illustrated in FIG. 47, the doped regions 140 may be spaced away from the interface between the outer spacers 134 and the outer gates 106 by a distance 184 between 0 and 10 nanometers. The interface material 141 is omitted from FIGS. 46 and 47 for ease of illustration.

[0090] As discussed above, conductive vias and/or lines may be used to provide electrical interconnects to the gates 106/108 and to the doped regions 140. FIGS. 48-67 illustrate various example stages in the formation of interconnects in a quantum dot device 100, in accordance with various embodiments. In particular, FIGS. 48-67 illustrate techniques that may be used to form the conductive vias 120/122/136, as well as conductive lines and additional conductive vias to create electrical pathways to the gates 106/108 and the doped regions 140. In particular, FIGS. 48-53 illustrate operations that may be used to form the conductive vias 136 of the assembly 238 of FIG. 25, and FIGS. 54-67 illustrate operations that may be used to form additional conductive vias and lines in conductive contact with the conductive vias 136.

[0091] Although FIGS. 48-67 explicitly depict the formation of the conductive vias 136 (and additional interconnect structures) to the doped regions 140 (for consistency with the particular cross-sections illustrated in FIGS. 2 and 4-25), this is simply for ease of illustration, and the structure of the interconnects formed in FIGS. 48-67 may be used for interconnects to any of the gates 106/108 (including the conductive vias 120 and 122). Similarly, the manufacturing techniques discussed with reference to the interconnects to the doped regions 140 formed in FIGS. 48-67 may be used to form interconnects to the gates 106/108, as readily recognized.

[0092] FIG. 48 is a cross-sectional view of an assembly 260 subsequent to providing a resist material 185 on the insulating material 130 of the assembly 236 (FIG. 24). The resist material 185 may be any suitable resist for patterning the insulating material 130, as discussed below with reference to FIG. 50 (e.g., a photoresist).

[0093] FIG. 49 is a cross-sectional view of an assembly 262 subsequent to patterning the resist material 185 of the assembly 260 (FIG. 48). The patterned resist material 185 may include cavities 186 that extend down to and expose portions of the insulating material 130. The patterning of the resist material 185 may be performed in accordance with any suitable technique (e.g., a photolithography technique).

[0094] FIG. 50 is a cross-sectional view of an assembly 264 subsequent to etching the insulating material 130 in accordance with the pattern provided by the patterned resist material 185 of the assembly 262 (FIG. 49), and removing the remaining resist material 185. In particular, cavities 187

may be formed in the insulating material 130 at locations corresponding to the locations of the cavities 186 in the resist material 185. The cavities 187 may extend down to the interface material 141 of the doped regions 140. In some embodiments, the cavities 187 may have a taper, and may be narrower closer to the doped regions 140, as illustrated. When the manufacturing techniques of FIGS. 48-50 are used to form cavities that extend down to the gate metal 110 of the gates 106 (i.e., to form the conductive vias 120), the intervening material of the hardmask 118 and the intervening material of the hardmask 116 may also be removed so that the gate metal 110 is exposed at the bottom of the cavities. Similarly, when the manufacturing techniques of FIGS. 48-50 are used to form cavities that extend down to the gate metal 112 of the gates 108 (i.e., to form the conductive vias 122), the intervening material of the hardmask 118 may also be removed so that the gate metal 112 is exposed at the bottom of the cavities.

[0095] FIG. 51 is a cross-sectional view of an assembly 266 subsequent to providing an adhesion material 188 on the assembly 264 (FIG. 50). In particular, the adhesion material 188 may be provided on the exposed insulating material 130, as well as at the bottom of the cavities 187 (in FIG. 51, on the exposed interface material 141). The adhesion material 188 may be a conductive material that facilitates adhesion between the assembly 266 and the conductive material that will be subsequently provided (e.g., the conductive material 189 discussed below with reference to FIG. 52). In some embodiments, the adhesion material 188 may include a refractory metal or a refractory metal nitride, such as titanium, tantalum, titanium nitride, titanium zirconium nitride, ruthenium, doped ruthenium (e.g., ruthenium doped with phosphorous) or tantalum nitride. In some embodiments, the adhesion material 188 may include tantalum nitride/tantalum (TNT). In some embodiments, the adhesion material 188 may include titanium nitride, which may have any suitable thickness (e.g., between 10 and 70 Angstroms). The adhesion material 188 may be provided using any suitable technique, such as ALD.

[0096] FIG. 52 is a cross-sectional view of an assembly 268 subsequent to providing a conductive material 189 on the assembly 266 (FIG. 51) such that the conductive material 189 fills the cavities 187. Any suitable technique may be used to provide the conductive material 189 on the assembly 266 (e.g., sputtering). The conductive material 189 may be in contact with the adhesion material 188. In some embodiments (e.g., as illustrated in FIG. 52), the conductive material 189 may extend beyond the cavities 187 over the insulating material 130. In some embodiments, the conductive material 189 may be copper. In some embodiments, the conductive material 189 may be tungsten (and may be deposited by CVD, for example). In some embodiments, the conductive material 189 may be a superconductor, such as aluminum, tin, titanium nitride, niobium titanium nitride, tantalum, niobium, and other niobium compounds (e.g., niobium tin and niobium germanium).

[0097] FIG. 53 is a cross-sectional view of an assembly 270 subsequent to planarizing the assembly 268 (FIG. 52) to remove the conductive material 189 that extends beyond the cavities 187. The remaining conductive material 189 in the cavities 187 (and the adhesion material 188 in the cavities 187) may provide the conductive vias 136. As noted above, analogous operations may be performed to manufacture the conductive vias 120 and 122 to the gates 106 and 108, respectively.

[0098] FIG. 54 is a cross-sectional view of an assembly 272 subsequent to depositing an etch stop material 191 and an insulating material 190 on the assembly 270 (FIG. 53). The etch stop material 191 may be disposed between the insulating material 190 and the assembly 270, as shown. The etch stop material 191 may include any suitable material, such as a nitride, silicon carbide, silicon nitride, carbon-doped silicon nitride, or silicon oxycarbide. In some embodiments, the etch stop material 191 may be deposited using CVD. The etch stop material 191 may have any suitable thickness. In some embodiments, the etch stop material 191 may have a thickness that is less than 20 nanometers (e.g., 8-12 nanometers). The insulating material 190 may be a dielectric material, such as any suitable ILD. In some embodiments, the insulating material 190 may be an oxide material, silicon oxide, carbon-doped oxide, silicon oxynitride, and/or a polymer material. In some embodiments, the insulating material 190 may be deposited using CVD. The insulating material 190 may have any suitable thickness. In some embodiments, the insulating material 190 may have a thickness between 10 and 30 nanometers (e.g., between 10 and 20 nanometers).

[0099] FIG. 55 is a cross-sectional view of an assembly 274 subsequent to providing a resist material 185 on the assembly 272 (FIG. 54) and patterning the resist material 171. The provision and patterning of the resist material 171 may take any suitable form (e.g., as discussed above with reference to FIGS. 48 and 49). In some embodiments, the resist material 171 may have the same material composition as the resist material 185; in other embodiments, the resist material 171 and the resist material 185 may have different material compositions. The patterned resist material 171 may include cavities 173 that extend down to and expose portions of the insulating material 190.

[0100] FIG. 56 is a cross-sectional view of an assembly 276 subsequent to etching the insulating material 190 and the etch stop material 191 in accordance with the pattern provided by the patterned resist material 171 of the assembly 274 (FIG. 55), and removing the remaining resist material 171. In particular, cavities 192 may be formed in the insulating material 190 and the etch stop material 191 at locations corresponding to the locations of the cavities 173 in the resist material 171. The cavities 173 (which may also be referred to as "trenches") may extend down to insulating material 130 and may expose the conductive material 189 of the conductive vias 136. In some embodiments, the formation of the cavities 192 may be a two-step process: first, the insulating material 190 may be etched (with the etch stop material 191 stopping that etch, and thus preventing

overetch into the insulating material 130), then the etch stop material 191 may be etched. In some embodiments, the cavities 192 may be tapered (e.g., as illustrated in FIG. 56).

[0101] FIG. 57 is a cross-sectional view of an assembly 278 subsequent to providing a seed layer 197 of conductive material on the assembly 276 (FIG. 56) such that the seed layer 197 extends over the walls and bottoms of the cavities 192 (as well as over the exposed top surfaces of the patterned insulating material 190). In particular, the seed layer 197 may be in conductive contact with the conductive material 189 of the conductive vias 136. The seed layer 197 may be formed of a same material as the conductive material 189, and as discussed below with reference to FIG. 58, may facilitate electroplating of additional such material. In some embodiments, the seed layer 197 may be formed of ruthenium, cobalt, or copper. In some embodiments, a liner material (not shown) may be provided on the assembly 278 before the seed layer 197 is provided. The liner material may serve one or more functions, including improving adhesion (e.g., as discussed above with reference to the adhesion material 188), providing a barrier against metal diffusion (e.g., between conductive lines/vias and proximate insulating material), and reducing electromigration between conductive lines and vias. In some embodiments, the liner material may take any of the forms discussed above with reference to the adhesion material 188 (e.g., to reduce electromigration and/or provide a diffusion barrier). In some embodiments, the liner material may include copper doped with aluminum, or copper doped with manganese (e.g., to reduce electromigration). The liner material may be provided by ALD, CVD, or sputtering, for example. The liner material may have any suitable thickness (e.g., between 2 and 70 Angstroms).

[0102] FIG. 58 is a cross-sectional view of an assembly 280 subsequent to providing additional conductive material 189 on the seed layer 197 of the assembly 278 (FIG. 57). In particular, the additional conductive material 189 may fill the cavities 192, and in some embodiments, may extend beyond the cavities 192 over the adjacent insulating material 190 (as shown). In some embodiments, the additional conductive material 189 may be electroplated onto the assembly 278 to form the assembly 280. The additional conductive material 189 may take the form of any of the embodiments of the conductive material 189 discussed herein (e.g., a superconducting material). In some embodiments, the additional conductive material 189 may not be provided by electroplating, but may instead be provide by electroless deposition (e.g., when the additional conductive material 189 includes copper or tin), ALD (e.g., when the additional conductive material includes titanium nitride), or sputtering, for example.

[0103] FIG. 59 is a cross-sectional view of an assembly 282 subsequent to planarizing the assembly 280 (FIG. 58) to remove the conductive material 189 that extended beyond the cavities 192 of the assembly 280. The resulting conductive material 189 that fills the cavities 192 may provide

conductive lines 193 in conductive contact with the conductive vias 136. The operations discussed above with reference to FIGS. 54-59 may represent a single Damascene process for forming the conductive lines 193; any suitable embodiments of such a process may be used to form interconnects in the quantum dot devices 100 disclosed herein. In some embodiments, the conductive lines 193 of the assembly 282 may extend into and out of the plane of the drawing, providing conductive pathways to route electrical signals to and/or from the doped regions 140. Analogous conductive lines may be formed to provide conductive contact to the conductive vias 120 and 122 for the gates 106 and 108, respectively.

[0104] FIG. 60 is a cross-sectional view of an assembly 284 subsequent to depositing additional etch stop material 191 and additional insulating material 190 on the assembly 282 (FIG. 59). The additional etch stop material 191 may be provided between the assembly 282 and the additional insulating material 190, as shown, and may be provided in accordance with any of the embodiments discussed above with reference to FIG. 54.

[0105] FIG. 61 is a cross-sectional view of an assembly 286 subsequent to providing a resist material 177 on the assembly 284 (FIG. 60) and patterning the resist material 177. The provision and patterning of the resist material 177 may take any suitable form (e.g., as discussed above with reference to FIGS. 48 and 49). In some embodiments, the resist material 177 may have the same material composition as the resist material 171; in other embodiments, the resist material 177 and the resist material 171 may have different material compositions. The patterned resist material 177 may include cavities 179 that extend down to and expose portions of the additional insulating material 190.

[0106] FIG. 62 is a cross-sectional view of an assembly 288 subsequent to etching the additional insulating material 190 in accordance with the pattern provided by the patterned resist material 177 of the assembly 286 (FIG. 61), and removing the remaining resist material 177. In particular, cavities 187 may be formed in the additional insulating material 190 at locations corresponding to the locations of the cavities 179 in the resist material 177. The cavities 187 may extend down to the additional etch stop material 191 (which may serve as an etch stop for the formation of the cavities 187). In some embodiments, the cavities 187 may be tapered, as shown.

[0107] FIG. 63 is a cross-sectional view of an assembly 290 subsequent to providing a resist material 175 on the assembly 288 (FIG. 62) and patterning the resist material 175. The provision and patterning of the resist material 175 may take any suitable form (e.g., as discussed above with reference to FIGS. 48 and 49). In some embodiments, the resist material 175 may have the same material composition as the resist material 177; in other embodiments, the resist material 175 and the resist material 177 may have different material compositions. The patterned resist material 175

may include cavities 181 that extend down to and expose portions of the additional insulating material 190, and also expose the cavities 187 in the additional insulating material 190.

[0108] FIG. 64 is a cross-sectional view of an assembly 292 subsequent to etching the additional insulating material 190 and the additional etch stop material 191 in accordance with the pattern provided by the patterned resist material 175 of the assembly 290 (FIG. 63), and removing the remaining resist material 175. In particular, a timed etch may be used to remove some of the additional oxide material 191 that was not protected by the resist material 175, leaving cavities 195 (which may also be referred to as "trenches"). After the timed etch, the additional etch stop material 191 at the bottom of the cavities 187 may be removed to form cavities 194 (e.g., as part of a two-step process, as discussed above with reference to FIGS. 56). The cavities 195 may extend over the cavities 194, as shown.

[0109] FIG. 65 is a cross-sectional view of an assembly 294 subsequent to providing a seed layer 117 of conductive material on the assembly 292 (FIG. 64) such that the seed layer 117 extends over the walls and bottoms of the cavities 194 and 195 (as well as over the exposed top surfaces of the additional insulating material 190). In particular, the seed layer 117 may be in conductive contact with the conductive lines 193. The seed layer 117 may take the form of any of the embodiments of the seed layer 197, discussed above.

[0110] FIG. 66 is a cross-sectional view of an assembly 296 subsequent to providing additional conductive material 189 on the seed layer 117 of the assembly 294 (FIG. 65). In particular, the additional conductive material 189 may fill the cavities 194 and 195, and in some embodiments, may extend beyond the cavities 194 and 195 over the adjacent insulating material 190 (as shown). In some embodiments, the additional conductive material 189 may be electroplated onto the assembly 294 to form the assembly 296.

[0111] FIG. 67 is a cross-sectional view of an assembly 298 subsequent to planarizing the assembly 296 (FIG. 66) to remove the conductive material 189 that extended beyond the cavities 194 and 195 of the assembly 296, forming conductive contacts 165 on the planarized surface, and providing a solder resist material 167 around the conductive contacts 165 on the planarized surface. The resulting conductive material 189 that fills the cavities 195 may provide conductive vias 198 in conductive contact with the conductive lines 193, and the conductive material 189 that fills the cavities 194 may provide conductive lines 196 in conductive contact with the conductive vias 198. The conductive contacts 165 may be in conductive contact with the conductive lines 196. In some embodiments, the conductive lines 196 of the assembly 298 may extend into and out of the plane of the drawing, providing conductive pathways to route electrical signals to and/or from the doped regions 140. Before providing the conductive contacts 165 and the solder resist material 167,

additional conductive vias and lines may be formed on the conductive lines 196 by repeating the operations discussed above with reference to FIGS. 60-67 to form any desired interconnect structures for electrical contact with the doped regions 140 (and, analogously, to form any desired interconnect structures for electrical contact with the gates 106 and 108). The operations discussed above with reference to FIGS. 60-67 may represent a dual Damascene process for forming conductive lines and vias; any suitable embodiments of such a process may be used to form interconnects in the quantum dot devices 100 disclosed herein.

[0112] During operation of the quantum dot device 100, electrical signals (such as power and/or input/output (I/O) signals) may be routed to and/or from the gates 106/108 and/or the doped regions 140 of the quantum dot device 100 through the interconnects provided by the conductive vias 120/122/136 and additional conductive vias and/or lines. The combination of the interconnect structures and the proximate insulating material (e.g., the insulating material 130, the insulating material 190, and the etch stop material 191) may provide an interlayer dielectric (ILD) stack of the quantum dot device 100. As noted above, interconnect structures may be arranged within the quantum dot device 100 to route electrical signals according to a wide variety of designs (in particular, the arrangement is not limited to the particular configuration of interconnect structures depicted in FIG. 67 or any of the other accompanying figures, and may include more or fewer interconnect structures).

[0113] The conductive vias 120/122/136 may be referred to as part of the "device layer" of the quantum dot device 100, which may also include the gates 106/108 and the doped regions 140. The conductive lines 193 may referred to as a Metal 1 or "M1" interconnect layer, and may couple the conductive vias 120/122/136 to other interconnect structures. The conductive vias 198 and the conductive lines 196 may be referred to as a Metal 2 or "M2" interconnect layer, and may be formed directly on the M1 interconnect layer. Although the different conductive vias and lines in FIG. 67 (and other figures herein) are not delineated with lines (and are instead illustrated as a continuous structure), conductive vias and lines that are in conductive contact may or may not be structurally and/or materially contiguous.

[0114] The solder resist material 167 (e.g., a polyimide or similar material) may be disposed around the conductive contacts 165, and in some embodiments, may extend onto the conductive contacts 165 (not shown). The conductive contacts 165 may provide the contacts to couple other components (e.g., a package substrate or other component) to the interconnect structures in the quantum dot device 100, and may be formed of any suitable conductive material (e.g., a superconducting material). For example, solder bonds may be formed on the one or more conductive contacts 165 to mechanically and/or electrically couple a chip including the quantum dot

device 100 with another component (e.g., a circuit board). The conductive contacts 165 illustrated in FIG. 67 take the form of bond pads, but other first level interconnect structures may be used (e.g., posts) to route electrical signals to/from the quantum dot device 100.

[0115] The manufacturing techniques illustrated in FIGS. 48-67 are illustrative examples of techniques that may be used to form some embodiments of the quantum dot devices 100 disclosed herein, but other techniques may be used instead of or in combination with the techniques discussed above. For example, FIGS. 68-71 illustrate various alternative manufacturing operations using subtractive techniques for forming various interconnect structures in a quantum dot device 100. In the example depicted in FIGS. 68-71, the conductive lines 193 (discussed above with reference to FIG. 59) may be formed using a subtractive process (e.g., instead of the additive process illustrated by FIGS. 54-59). In some embodiments, the operations discussed below with reference to FIGS. 68-71 may replace the operations discussed above with reference to FIGS. 54-59.

[0116] FIG. 68 is a cross-sectional view of an assembly 300 subsequent to providing a conductive material 189 on the assembly 270 (FIG. 53). The conductive material 189 may be provided using any suitable technique (e.g., sputtering), and may be in conductive contact with the conductive vias 136, as shown. The conductive material 189 may take the form of any of the conductive materials 189 disclosed herein (e.g., a superconducting material).

[0117] FIG. 69 is a cross-sectional view of an assembly 302 subsequent to providing a resist material 203 on the assembly 300 (FIG. 68) and patterning the resist material 203. The provision and patterning of the resist material 203 may take any suitable form (e.g., as discussed above with reference to FIGS. 48 and 49). The resist material 203 may be any resist material suitable for etching the conductive material 189, as discussed below. The patterned resist material 203 may include cavities 205 that extend down to and expose portions of the conductive material 189.

[0118] FIG. 70 is a cross-sectional view of an assembly 304 subsequent to etching the exposed conductive material 189, in accordance with the pattern provided by the patterned resist material 203 of the assembly 302 (FIG. 69), and removing the remaining resist material 203. The remaining patterned conductive material 189 (in conductive contact with the conductive vias 136) may provide the conductive lines 193.

[0119] FIG. 71 is a cross-sectional view of an assembly 306 subsequent to providing an insulating material 125 (e.g., a dielectric material) around the conductive lines 193. The insulating material 125 may be an insulating material (e.g., any of the materials discussed above with reference to the insulating material 190) or any other suitable material, and may be deposited using any suitable technique. In some embodiments, the insulating material 125 may be planarized subsequent to

deposition so as to provide a flat surface on which subsequent layers of conductive vias and lines may be built (e.g., using any of the techniques discussed herein).

[0120] Although particular patterning techniques are discussed herein, any suitable patterning techniques and materials may be used in the manufacture of the quantum dot devices 100 disclosed herein. For example, self-aligned double patterning techniques, hardmask lithography techniques, or antireflective coating (ARC) techniques may be used. In another example, air gap dielectrics may be included in any of the insulating materials, and air gap formation techniques may be incorporated into the process of manufacturing a quantum dot device 100, as suitable.

[0121] As noted above, any suitable techniques may be used to manufacture the quantum dot devices 100 disclosed herein. FIG. 72 is a flow diagram of an illustrative method 1000 of manufacturing a quantum dot device, in accordance with various embodiments. Although the operations discussed below with reference to the method 1000 are illustrated in a particular order and depicted once each, these operations may be repeated or performed in a different order (e.g., in parallel), as suitable. Additionally, various operations may be omitted, as suitable. Various operations of the method 1000 may be illustrated with reference to one or more of the embodiments discussed above, but the method 1000 may be used to manufacture any suitable quantum dot device (including any suitable ones of the embodiments disclosed herein).

[0122] At 1002, a quantum well stack may be provided on a substrate. For example, a quantum well stack 146 may be provided on a substrate 144 (e.g., as discussed above with reference to FIGS. 4-5 and 26-28).

[0123] At 1004, gates may be formed above the quantum well stack. For example, gates 106 and/or 108 may be formed on the fins 104 (e.g., as discussed above with reference to FIGS. 11-20 and 40).

[0124] At 1006, an insulating material may be provided above the gates. For example, hardmasks 116 and/or 118 may be provided on the gate metal 110 and/or 112 of the gates 106 and/or 108, respectively, and an insulating material 130 may be disposed on the gates 106 and/or 108 (e.g., as discussed above with reference to FIGS. 11-20 and 24).

[0125] At 1008, conductive vias may be formed through the insulating material to make electrical contact with the gates. For example, conductive vias 120 and/or 122 may be formed through the insulating material 130, the hardmask 116, and/or the hardmask 118 (e.g., as discussed above with reference to FIGS. 25 and 48-71).

[0126] A number of techniques are disclosed herein for operating a quantum dot device 100. FIGS. 73-74 are flow diagrams of particular illustrative methods 1020 and 1040, respectively, of operating a quantum dot device, in accordance with various embodiments. Although the operations discussed

below with reference to the methods 1020 and 1040 are illustrated in a particular order and depicted once each, these operations may be repeated or performed in a different order (e.g., in parallel), as suitable. Additionally, various operations may be omitted, as suitable. Various operations of the methods 1020 and 1040 may be illustrated with reference to one or more of the embodiments discussed above, but the methods 1020 and 1040 may be used to operate any suitable quantum dot device (including any suitable ones of the embodiments disclosed herein).

[0127] Turning to the method 1020 of FIG. 73, at 1022, voltages may be applied to a plurality of gates above a first quantum well stack region to cause a first quantum dot to form in the first quantum well stack region. The voltages may be applied to the plurality of gates above the first quantum well stack region through an associated plurality of conductive vias that extend through an insulating material to contact associated gates of the plurality of gates. For example, one or more voltages may be applied to the gates 106/108 on a fin 104-1 through the conductive vias 120/122 to cause at least one quantum dot 142 to form in the fin 104-1.

[0128] At 1024, voltages may be applied to a plurality of gates above a second quantum well stack region to cause a second quantum dot to form in the second quantum well stack region. For example, one or more voltages may be applied to the gates 106/108 on a fin 104-2 (e.g., through the conductive vias 120/122) to cause at least one quantum dot 142 to form in the fin 104-2.

[0129] At 1026, a quantum state of the first quantum dot may be sensed with the second quantum dot. For example, a quantum dot 142 in the fin 104-2 (the "read" fin) may sense the quantum state of a quantum dot 142 in the fin 104-1 (the "active" fin).

[0130] Turning to the method 1040 of FIG. 74, at 1042, a voltage may be applied to a first gate disposed above a quantum well stack region to cause a first quantum dot to form in a first quantum well in the quantum well stack region under the first gate. The voltage may be applied to the first gate through a conductive via in conductive contact with the first gate. For example, a voltage may be applied to the gate 108-1 disposed on a fin 104 (through a conductive via 122) to cause a first quantum dot 142 to form in the quantum well layer 152 in the fin 104 under the gate 108-1.

[0131] At 1044, a voltage may be applied to a second gate disposed above the quantum well stack region to cause a second quantum dot to form in a second quantum well in the quantum well stack region under the second gate. For example, a voltage may be applied to the gate 108-2 disposed on the fin 104 (e.g., through a conductive via 122) to cause a second quantum dot 142 to form in the quantum well layer 152 in the fin 104 under the gate 108-2.

[0132] At 1046, a voltage may be applied to a third gate disposed above the quantum well stack region to (1) cause a third quantum dot to form in a third quantum well in the quantum well stack region under the third gate or (2) provide a potential barrier between the first quantum well and the

second quantum well. For example, a voltage may be applied to the gate 106-2 (e.g., through a conductive via 120) to (1) cause a third quantum dot 142 to form in the quantum well layer 152 in the fin 104 (e.g., when the gate 106-2 acts as a "plunger" gate) or (2) provide a potential barrier between the first quantum well (under the gate 108-1) and the second quantum well (under the gate 108-2) (e.g., when the gate 106-2 acts as a "barrier" gate).

[0133] FIG. 75 is a block diagram of an example quantum computing device 2000 that may include any of the quantum dot devices disclosed herein. A number of components are illustrated in FIG. 75 as included in the quantum computing device 2000, but any one or more of these components may be omitted or duplicated, as suitable for the application. In some embodiments, some or all of the components included in the quantum computing device 2000 may be attached to one or more printed circuit boards (e.g., a motherboard). In some embodiments, various ones of these components may be fabricated onto a single system-on-a-chip (SoC) die. Additionally, in various embodiments, the quantum computing device 2000 may not include one or more of the components illustrated in FIG. 75, but the quantum computing device 2000 may include interface circuitry for coupling to the one or more components. For example, the quantum computing device 2000 may not include a display device 2006, but may include display device interface circuitry (e.g., a connector and driver circuitry) to which a display device 2006 may be coupled. In another set of examples, the quantum computing device 2000 may not include an audio input device 2024 or an audio output device 2008, but may include audio input or output device interface circuitry (e.g., connectors and supporting circuitry) to which an audio input device 2024 or audio output device 2008 may be coupled.

[0134] The quantum computing device 2000 may include a processing device 2002 (e.g., one or more processing devices). As used herein, the term "processing device" or "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. The processing device 2002 may include a quantum processing device 2026 (e.g., one or more quantum processing devices), and a non-quantum processing device 2028 (e.g., one or more non-quantum processing devices). The quantum processing device 2026 may include one or more of the quantum dot devices 100 disclosed herein, and may perform data processing by performing operations on the quantum dots that may be generated in the quantum dot devices 100, and monitoring the result of those operations. For example, as discussed above, different quantum dots may be allowed to interact, the quantum states of different quantum dots may be set or transformed, and the quantum states of quantum dots may be read (e.g., by another quantum dot). The quantum processing device 2026 may be a universal quantum processor, or specialized quantum

processor configured to run one or more particular quantum algorithms. In some embodiments, the quantum processing device 2026 may execute algorithms that are particularly suitable for quantum computers, such as cryptographic algorithms that utilize prime factorization, encryption/decryption, algorithms to optimize chemical reactions, algorithms to model protein folding, etc. The quantum processing device 2026 may also include support circuitry to support the processing capability of the quantum processing device 2026, such as input/output channels, multiplexers, signal mixers, quantum amplifiers, and analog-to-digital converters.

[0135] As noted above, the processing device 2002 may include a non-quantum processing device 2028. In some embodiments, the non-quantum processing device 2028 may provide peripheral logic to support the operation of the quantum processing device 2026. For example, the non-quantum processing device 2028 may control the performance of a read operation, control the performance of a write operation, control the clearing of quantum bits, etc. The non-quantum processing device 2028 may also perform conventional computing functions to supplement the computing functions provided by the quantum processing device 2026. For example, the non-quantum processing device 2028 may interface with one or more of the other components of the quantum computing device 2000 (e.g., the communication chip 2012 discussed below, the display device 2006 discussed below, etc.) in a conventional manner, and may serve as an interface between the quantum processing device 2026 and conventional components. The non-quantum processing device 2028 may include one or more digital signal processors (DSPs), application-specific integrated circuits (ASICs), central processing units (CPUs), graphics processing units (GPUs), cryptoprocessors (specialized processors that execute cryptographic algorithms within hardware), server processors, or any other suitable processing devices.

[0136] The quantum computing device 2000 may include a memory 2004, which may itself include one or more memory devices such as volatile memory (e.g., dynamic random access memory (DRAM)), nonvolatile memory (e.g., read-only memory (ROM)), flash memory, solid state memory, and/or a hard drive. In some embodiments, the states of qubits in the quantum processing device 2026 may be read and stored in the memory 2004. In some embodiments, the memory 2004 may include memory that shares a die with the non-quantum processing device 2028. This memory may be used as cache memory and may include embedded dynamic random access memory (eDRAM) or spin transfer torque magnetic random-access memory (STT-MRAM).

[0137] The quantum computing device 2000 may include a cooling apparatus 2030. The cooling apparatus 2030 may maintain the quantum processing device 2026 at a predetermined low temperature during operation to reduce the effects of scattering in the quantum processing device 2026. This predetermined low temperature may vary depending on the setting; in some

embodiments, the temperature may be 5 degrees Kelvin or less. In some embodiments, the non-quantum processing device 2028 (and various other components of the quantum computing device 2000) may not be cooled by the cooling apparatus 2030, and may instead operate at room temperature. The cooling apparatus 2030 may be, for example, a dilution refrigerator, a helium-3 refrigerator, or a liquid helium refrigerator.

[0138] In some embodiments, the quantum computing device 2000 may include a communication chip 2012 (e.g., one or more communication chips). For example, the communication chip 2012 may be configured for managing wireless communications for the transfer of data to and from the quantum computing device 2000. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a nonsolid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not.

[0139] The communication chip 2012 may implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 1402.11 family), IEEE 1402.16 standards (e.g., IEEE 1402.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., advanced LTE project, ultramobile broadband (UMB) project (also referred to as "3GPP2"), etc.). IEEE 1402.16 compatible Broadband Wireless Access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 1402.16 standards. The communication chip 2012 may operate in accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. The communication chip 2012 may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The communication chip 2012 may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), and derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The communication chip 2012 may operate in accordance with other wireless protocols in other embodiments. The quantum computing device 2000 may include an antenna 2022 to facilitate wireless communications and/or to receive other wireless communications (such as AM or FM radio transmissions).

[0140] In some embodiments, the communication chip 2012 may manage wired communications, such as electrical, optical, or any other suitable communication protocols (e.g., the Ethernet). As noted above, the communication chip 2012 may include multiple communication chips. For instance, a first communication chip 2012 may be dedicated to shorter-range wireless communications such as Wi-Fi or Bluetooth, and a second communication chip 2012 may be dedicated to longer-range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, or others. In some embodiments, a first communication chip 2012 may be dedicated to wireless communications, and a second communication chip 2012 may be dedicated to wired communications.

[0141] The quantum computing device 2000 may include battery/power circuitry 2014. The battery/power circuitry 2014 may include one or more energy storage devices (e.g., batteries or capacitors) and/or circuitry for coupling components of the quantum computing device 2000 to an energy source separate from the quantum computing device 2000 (e.g., AC line power).

[0142] The quantum computing device 2000 may include a display device 2006 (or corresponding interface circuitry, as discussed above). The display device 2006 may include any visual indicators, such as a heads-up display, a computer monitor, a projector, a touchscreen display, a liquid crystal display (LCD), a light-emitting diode display, or a flat panel display, for example.

[0143] The quantum computing device 2000 may include an audio output device 2008 (or corresponding interface circuitry, as discussed above). The audio output device 2008 may include any device that generates an audible indicator, such as speakers, headsets, or earbuds, for example.

[0144] The quantum computing device 2000 may include an audio input device 2024 (or corresponding interface circuitry, as discussed above). The audio input device 2024 may include any device that generates a signal representative of a sound, such as microphones, microphone arrays, or digital instruments (e.g., instruments having a musical instrument digital interface (MIDI) output).

[0145] The quantum computing device 2000 may include a global positioning system (GPS) device 2018 (or corresponding interface circuitry, as discussed above). The GPS device 2018 may be in communication with a satellite-based system and may receive a location of the quantum computing device 2000, as known in the art.

[0146] The quantum computing device 2000 may include an other output device 2010 (or corresponding interface circuitry, as discussed above). Examples of the other output device 2010 may include an audio codec, a video codec, a printer, a wired or wireless transmitter for providing information to other devices, or an additional storage device.

[0147] The quantum computing device 2000 may include an other input device 2020 (or corresponding interface circuitry, as discussed above). Examples of the other input device 2020 may

include an accelerometer, a gyroscope, a compass, an image capture device, a keyboard, a cursor control device such as a mouse, a stylus, a touchpad, a bar code reader, a Quick Response (QR) code reader, any sensor, or a radio frequency identification (RFID) reader.

[0148] The quantum computing device 2000, or a subset of its components, may have any appropriate form factor, such as a hand-held or mobile computing device (e.g., a cell phone, a smart phone, a mobile internet device, a music player, a tablet computer, a laptop computer, a netbook computer, an ultrabook computer, a personal digital assistant (PDA), an ultramobile personal computer, etc.), a desktop computing device, a server or other networked computing component, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a vehicle control unit, a digital camera, a digital video recorder, or a wearable computing device.

[0149] The following paragraphs provide examples of various ones of the embodiments disclosed herein.

[0150] Example 1 is a quantum dot device, including: a gate disposed above a quantum well stack; an insulating material disposed above the gate; and a conductive via extending through the insulating material and in conductive contact with the gate.

[0151] Example 2 may include the subject matter of Example 1, and may further specify that the conductive via has a taper that is narrower proximate to the gate.

[0152] Example 3 may include the subject matter of any of Examples 1-2, and may further specify that the conductive via is formed of a superconducting material.

[0153] Example 4 may include the subject matter of Example 3, and may further specify that the superconducting material includes tin.

[0154] Example 5 may include the subject matter of any of Examples 3-4, and may further specify that the superconducting material includes aluminum.

[0155] Example 6 may include the subject matter of any of Examples 1-5, and may further specify that the conductive via includes a conductive material and an adhesion material, and the adhesion material is disposed between the conductive material and the insulating material.

[0156] Example 7 may include the subject matter of any of Examples 1-6, and may further include a conductive line in contact with the conductive via.

[0157] Example 8 may include the subject matter of Example 7, and may further specify that a conductive line is adjacent to an etch stop material.

[0158] Example 9 may include the subject matter of any of Examples 1-8, and may further specify that the insulating material is an oxide material.

[0159] Example 10 may include the subject matter of any of Examples 1-9, and may further specify that the conductive via is a first conductive via, and the quantum dot device further includes: a

doped region in the quantum well stack, wherein the insulating material is also disposed above the quantum well stack; and a second conductive via extending through the insulating material and in conductive contact with the doped region.

[0160] Example 11 may include the subject matter of Example 10, and may further specify that a silicide material is disposed between the second conductive via and the doped region.

[0161] Example 12 may include the subject matter of any of Examples 1-11, and may further specify that the gate is one of a plurality of gates, the conductive via is one of a plurality of vias, and each of the conductive vias is in conductive contact with an associated gate of the plurality of gates.

[0162] Example 13 may include the subject matter of Example 12, and may further specify that the plurality of gates are arranged in an array on the quantum well stack and are spaced apart by spacer material.

[0163] Example 14 may include the subject matter of any of Examples 1-13, and may further specify that the quantum well stack is included in a fin extending away from a base.

[0164] Example 15 may include the subject matter of Example 14, and may further specify that the fin is a first fin, the gate is a first gate, the quantum well stack is a first quantum well stack, and the quantum dot device further includes: a second fin extending away from the base, wherein the second fin includes a second quantum well stack; and a second gate disposed on the second quantum well stack.

[0165] Example 16 may include the subject matter of Example 15, and may further specify that the first and second fins are parallel.

[0166] Example 17 may include the subject matter of any of Examples 15-16, and may further include an insulating material disposed between the first and second fins.

[0167] Example 18 is a method of operating a quantum dot device, including: applying voltages to a plurality of gates above a first quantum well stack region to cause a first quantum dot to form in the first quantum well stack region, wherein the voltages are applied to the plurality of gates above the first quantum well stack region through an associated plurality of conductive vias that extend through an insulating material to contact associated gates of the plurality of gates; applying voltages to a plurality of gates above a second quantum well stack region to cause a second quantum dot to form in the second quantum well stack region; and sensing a quantum state of the first quantum dot with the second quantum dot.

[0168] Example 19 may include the subject matter of Example 18, and may further specify that the first quantum well stack region is included in a first fin extending away from a base, the second quantum well stack region is included in a second fin extending away from the base, and an insulating material is disposed between the first and second fins.

[0169] Example 20 may include the subject matter of any of Examples 18-19, and may further specify that the voltages are applied to the plurality of gates above the first quantum well stack region through an associated plurality of conductive lines that extend through the insulating material to contact associated conductive vias of the plurality of conductive vias.

[0170] Example 21 may include the subject matter of any of Examples 18-20, and may further specify that applying the voltages to the plurality of gates above the first quantum well stack region comprises applying a voltage to a first gate of the plurality of gates to cause the first quantum dot to form in the first quantum well stack region under the first gate.

[0171] Example 22 may include the subject matter of any of Examples 18-21, and may further specify that sensing the quantum state of the first quantum dot with the second quantum dot comprises sensing a spin state of the first quantum dot with the second quantum dot.

[0172] Example 23 may include the subject matter of any of Examples 18-22, and may further include: applying the voltages to the plurality of gates above the first quantum well stack region to cause a third quantum dot to form in the first quantum well stack region; and prior to sensing the quantum state of the first quantum dot with the second quantum dot, allowing the first and third quantum dots to interact.

[0173] Example 24 may include the subject matter of Example 23, and may further specify that allowing the first and third quantum dots to interact comprises applying the voltages to the plurality of gates above the first quantum well stack region to control interaction between the first and third quantum dots.

[0174] Example 25 is a method of manufacturing a quantum dot device, including: providing a quantum well stack on a substrate; forming gates above the quantum well stack; providing an insulating material above the gates; and forming conductive vias through the insulating material to make electrical contact with the gates.

[0175] Example 26 may include the subject matter of Example 25, and may further specify that the insulating material includes an interlayer dielectric.

[0176] Example 27 may include the subject matter of any of Examples 25-26, and may further specify that the insulating material includes a hardmask disposed on gate metal of the gates.

[0177] Example 28 may include the subject matter of any of Examples 25-27, and may further specify that forming the conductive vias through the insulating material includes: etching cavities in the insulating material; providing an adhesion material in the cavities; and providing a conductive material in the cavities to form the conductive vias.

[0178] Example 29 may include the subject matter of Example 28, and may further include, after providing the conductive material in the cavities, planarizing the conductive material.

[0179] Example 30 may include the subject matter of any of Examples 25-27, and may further include forming conductive lines in conductive contact with the conductive vias.

[0180] Example 31 may include the subject matter of Example 30, and may further specify that forming conductive lines includes: providing an etch stop material on the insulating material; providing a second insulating material on the etch stop material; etching through the second insulating material and the etch stop material to form cavities; and providing a conductive material in the cavities to form the conductive lines.

[0181] Example 32 may include the subject matter of Example 30, and may further specify that forming the conductive lines includes: providing a etch stop material on the insulating material; providing a second insulating material on the etch stop material; etching through the second insulating material to form first cavities, wherein the bottom of the first cavities is provided by the etch stop material; after etching through the second insulating material to form the first cavities, removing additional second insulating material and the etch stop material to deepen the first cavities and form second cavities in the second insulating material; and providing a conductive material in the first and second cavities.

[0182] Example 33 may include the subject matter of Example 32, and may further specify that providing the conductive material in the first and second cavities includes electroplating the conductive material.

[0183] Example 34 is a quantum computing device, including: a quantum processing device, wherein the quantum processing device includes a first quantum well stack region including an active quantum well layer, a second quantum well stack region including a read quantum well layer, a first plurality of gates disposed on the first quantum well stack region, a second plurality of gates disposed on the second quantum well stack region, a first plurality of conductive vias in conductive contact with the first plurality of gates, and a second plurality of conductive vias in conductive contact with the second plurality of gates; a non-quantum processing device, coupled to the quantum processing device, to control voltages applied to the first and second pluralities of gates; and a memory device to store data generated by the read quantum well layer during operation of the quantum processing device.

[0184] Example 35 may include the subject matter of Example 34, and may further include a cooling apparatus to maintain a temperature of the quantum processing device below 5 degrees Kelvin.

[0185] Example 36 may include the subject matter of Example 35, and may further specify that the cooling apparatus includes a dilution refrigerator.

[0186] Example 37 may include the subject matter of Example 35, and may further specify that the cooling apparatus includes a liquid helium refrigerator.

[0187] Example 38 may include the subject matter of any of Examples 34-37, and may further specify that the memory device is to store instructions for a quantum computing algorithm to be executed by the quantum processing device.

[0188] Example 39 may include the subject matter of any of Examples 34-38, and may further specify that the first and second pluralities of conductive vias extend through an oxide insulating material disposed on the first and second pluralities of gates.

Claims:

1. A quantum dot device, comprising:

a gate disposed above a quantum well stack;

an insulating material disposed above the gate; and

a conductive via extending through the insulating material and in conductive contact with the gate.

2. The quantum dot device of claim 1, wherein the conductive via is formed of a superconducting material.

3. The quantum dot device of claim 2, wherein the superconducting material includes tin.

4. The quantum dot device of claim 2, wherein the superconducting material includes aluminum.

5. The quantum dot device of any of claims 1-4, wherein the insulating material is an oxide material.

6. The quantum dot device of any of claims 1-4, wherein the conductive via is a first conductive via, and the quantum dot device further comprises:

a doped region in the quantum well stack, wherein the insulating material is also disposed above the quantum well stack; and

a second conductive via extending through the insulating material and in conductive contact with the doped region.

7. The quantum dot device of any of claims 1-4, wherein the gate is one of a plurality of gates, the conductive via is one of a plurality of vias, and each of the conductive vias is in conductive contact with an associated gate of the plurality of gates.

8. The quantum dot device of claim 7, wherein the plurality of gates are arranged in an array on the quantum well stack and are spaced apart by spacer material.

9. The quantum dot device of any of claims 1-4, wherein the quantum well stack is included in a fin extending away from a base.

10. The quantum dot device of claim 9, wherein the fin is a first fin, the gate is a first gate, the quantum well stack is a first quantum well stack, and the quantum dot device further comprises:

a second fin extending away from the base, wherein the second fin includes a second quantum well stack; and

a second gate disposed on the second quantum well stack.

11. The quantum dot device of claim 10, further comprising:

an insulating material disposed between the first and second fins.

12. A method of operating a quantum dot device, comprising:

applying voltages to a plurality of gates above a first quantum well stack region to cause a first quantum dot to form in the first quantum well stack region, wherein the voltages are applied to the plurality of gates above the first quantum well stack region through an associated plurality of

conductive vias that extend through an insulating material to contact associated gates of the plurality of gates;

applying voltages to a plurality of gates above a second quantum well stack region to cause a second quantum dot to form in the second quantum well stack region; and

sensing a quantum state of the first quantum dot with the second quantum dot.

13. The method of claim 12, wherein the first quantum well stack region is included in a first fin extending away from a base, the second quantum well stack region is included in a second fin extending away from the base, and an insulating material is disposed between the first and second fins.

14. The method of claim 12, wherein the voltages are applied to the plurality of gates above the first quantum well stack region through an associated plurality of conductive lines that extend through the insulating material to contact associated conductive vias of the plurality of conductive vias.

15. The method of any of claims 12-14, wherein applying the voltages to the plurality of gates above the first quantum well stack region comprises applying a voltage to a first gate of the plurality of gates to cause the first quantum dot to form in the first quantum well stack region under the first gate.

16. The method of any of claims 12-14, wherein sensing the quantum state of the first quantum dot with the second quantum dot comprises sensing a spin state of the first quantum dot with the second quantum dot.

17. The method of any of claims 12-14, further comprising:

applying the voltages to the plurality of gates above the first quantum well stack region to cause a third quantum dot to form in the first quantum well stack region; and

prior to sensing the quantum state of the first quantum dot with the second quantum dot, allowing the first and third quantum dots to interact.

18. A method of manufacturing a quantum dot device, comprising:

providing a quantum well stack on a substrate;

forming gates above the quantum well stack;

providing an insulating material above the gates; and

forming conductive vias through the insulating material to make electrical contact with the gates.

19. The method of claim 18, wherein the insulating material includes a hardmask disposed on gate metal of the gates.

20. The method of any of claims 18-19, wherein forming the conductive vias through the insulating material comprises:

etching cavities in the insulating material;

providing an adhesion material in the cavities; and

providing a conductive material in the cavities to form the conductive vias.

21. The method of claim 20, further comprising:

after providing the conductive material in the cavities, planarizing the conductive material.

22. The method of any of claims 18-19, further comprising:

forming conductive lines in conductive contact with the conductive vias.

23. A quantum computing device, comprising:

a quantum processing device, wherein the quantum processing device includes a first quantum well stack region including an active quantum well layer, a second quantum well stack region including a read quantum well layer, a first plurality of gates disposed on the first quantum well stack region, a second plurality of gates disposed on the second quantum well stack region, a first plurality of conductive vias in conductive contact with the first plurality of gates, and a second plurality of conductive vias in conductive contact with the second plurality of gates;

a non-quantum processing device, coupled to the quantum processing device, to control voltages applied to the first and second pluralities of gates; and

a memory device to store data generated by the read quantum well layer during operation of the quantum processing device.

24. The quantum computing device of claim 23, wherein the memory device is to store instructions for a quantum computing algorithm to be executed by the quantum processing device.

25. The quantum computing device of any of claims 23-24, wherein the first and second pluralities of conductive vias extend through an insulating material disposed on the first and second pluralities of gates.

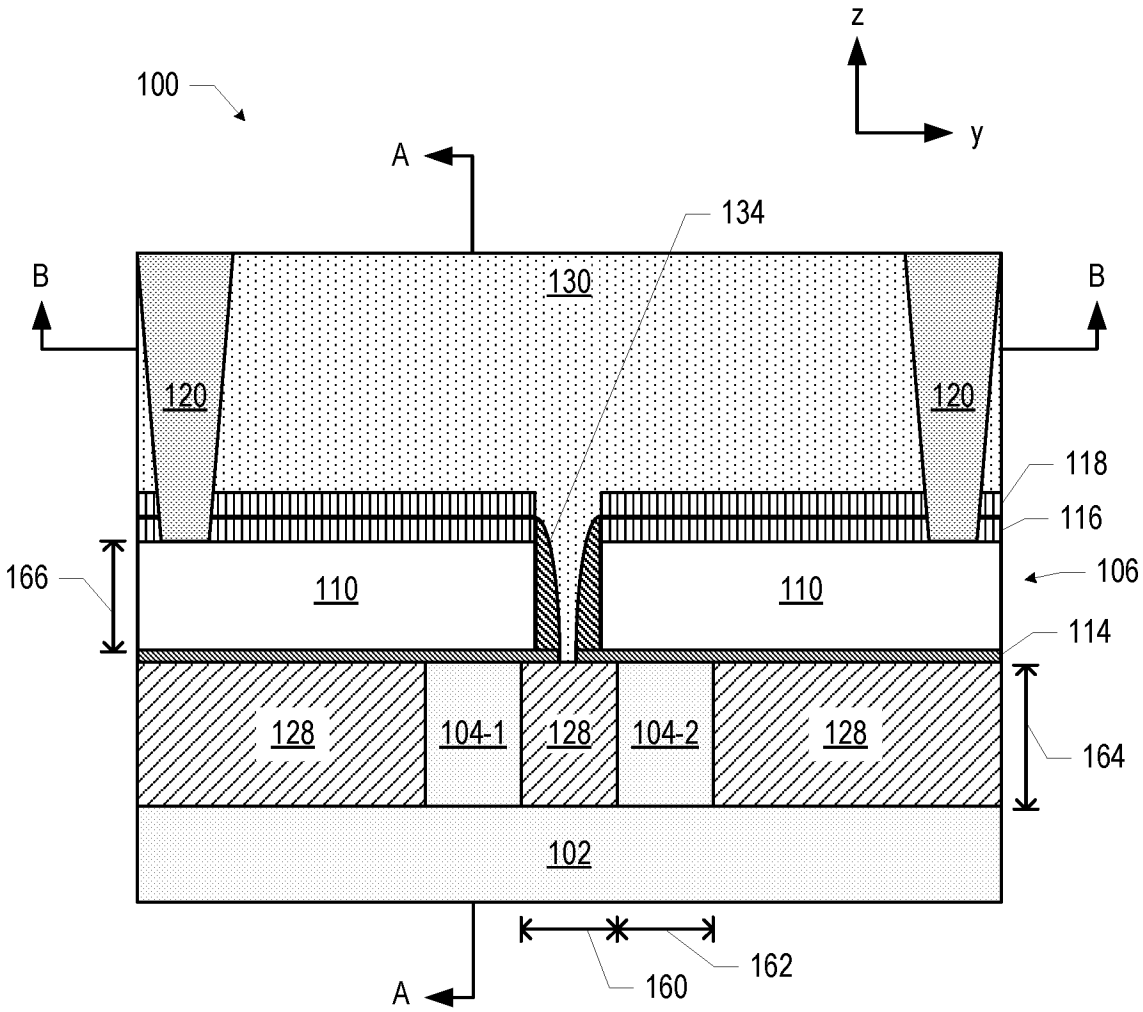
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FIG. 1

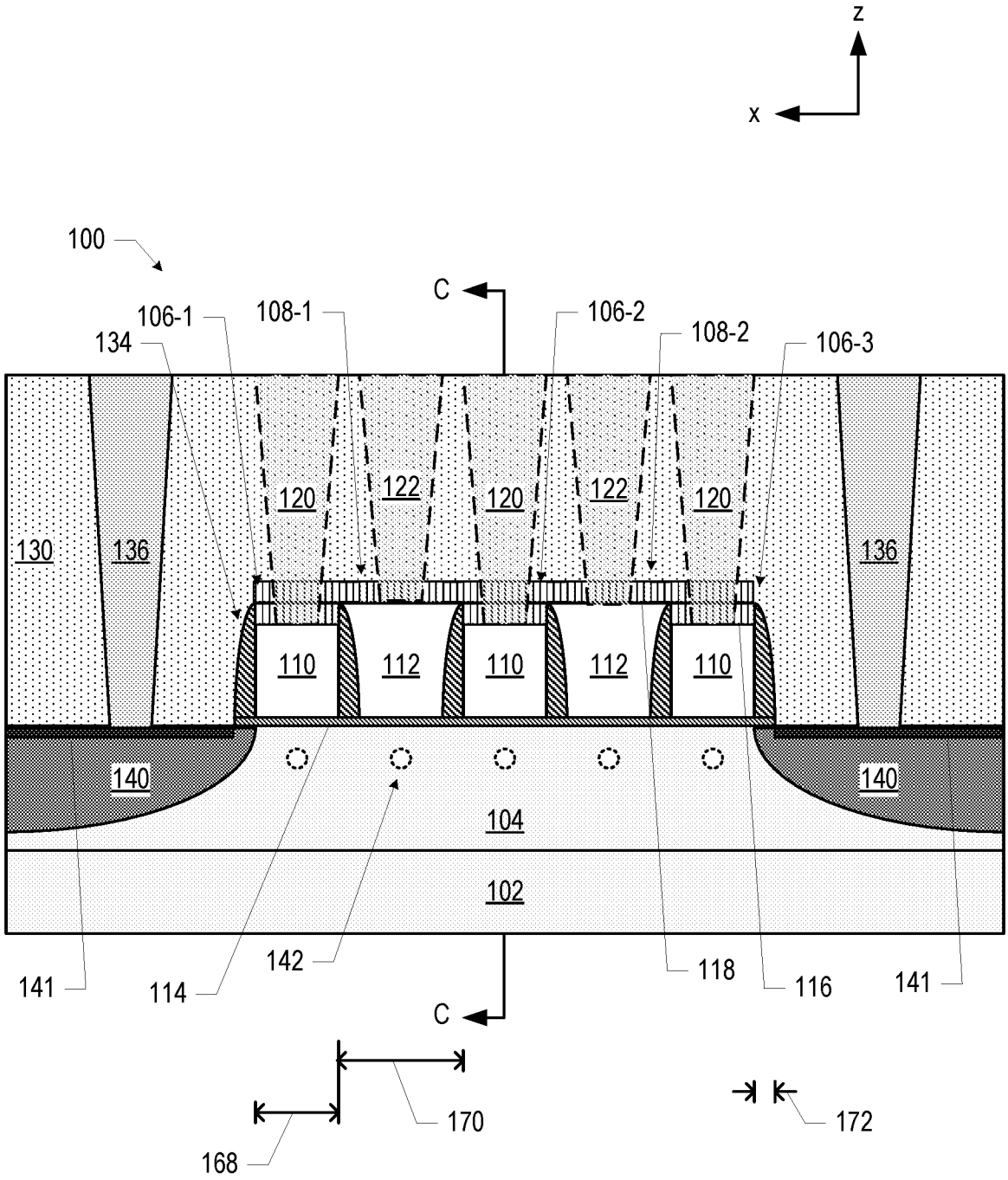
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FIG. 2

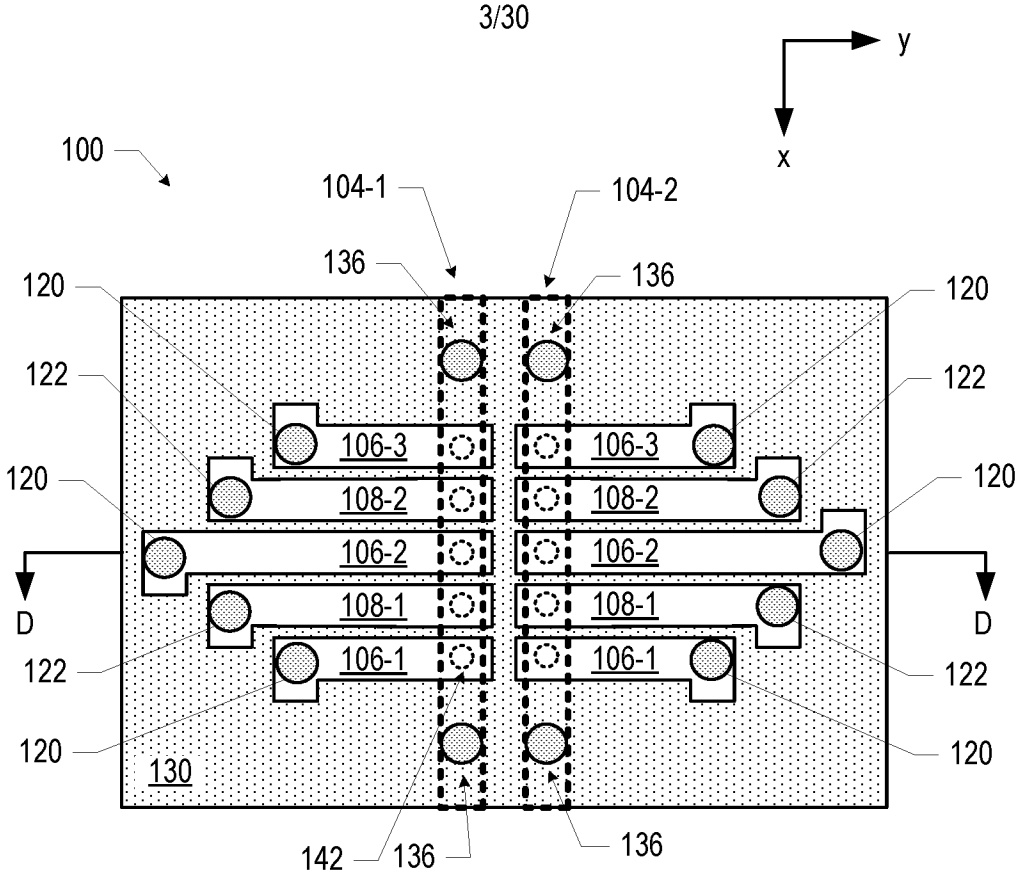

FIG. 3

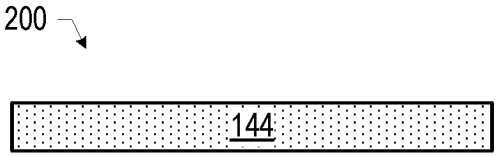

FIG. 4

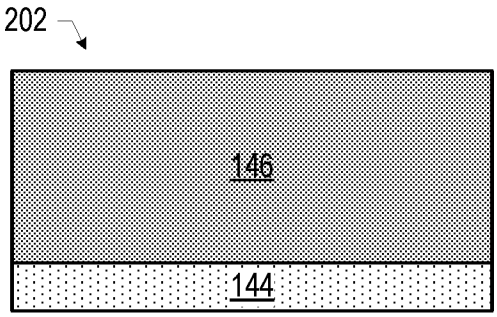

FIG. 5

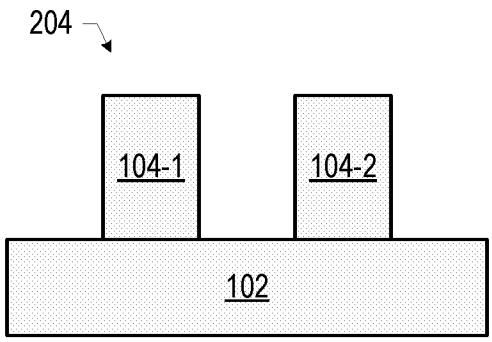

FIG. 6

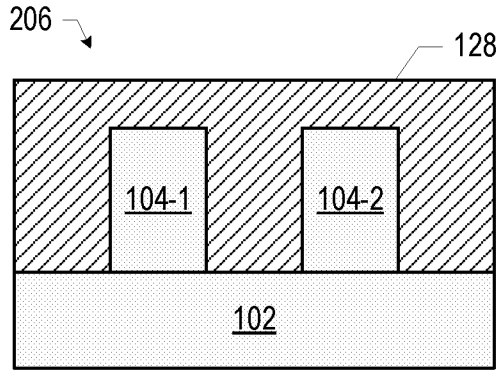

FIG. 7

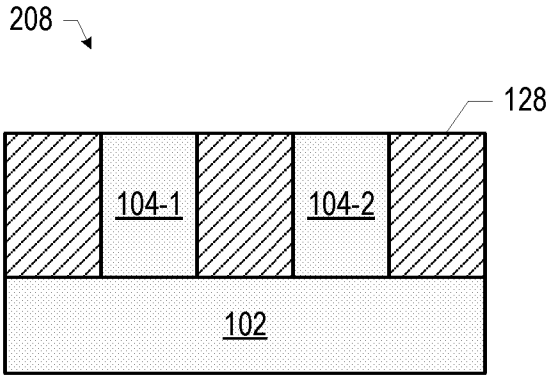

FIG. 8

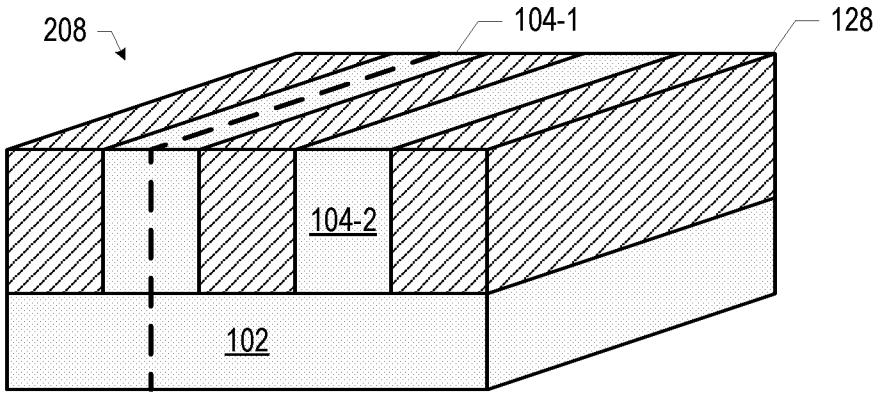

FIG. 9

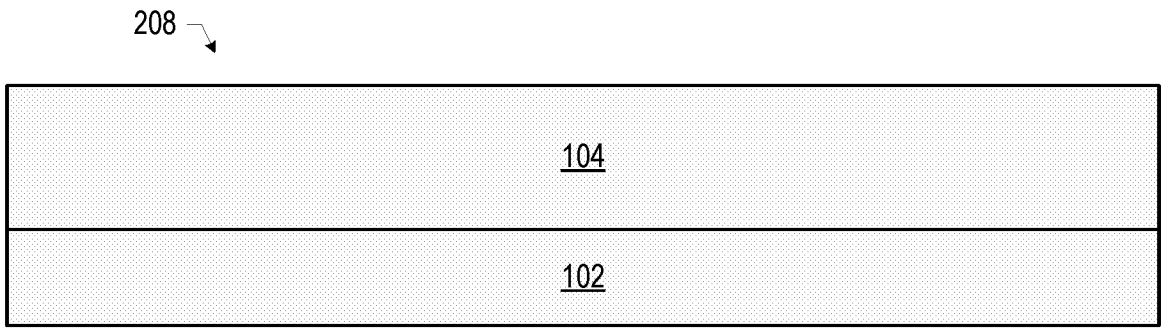

FIG. 10

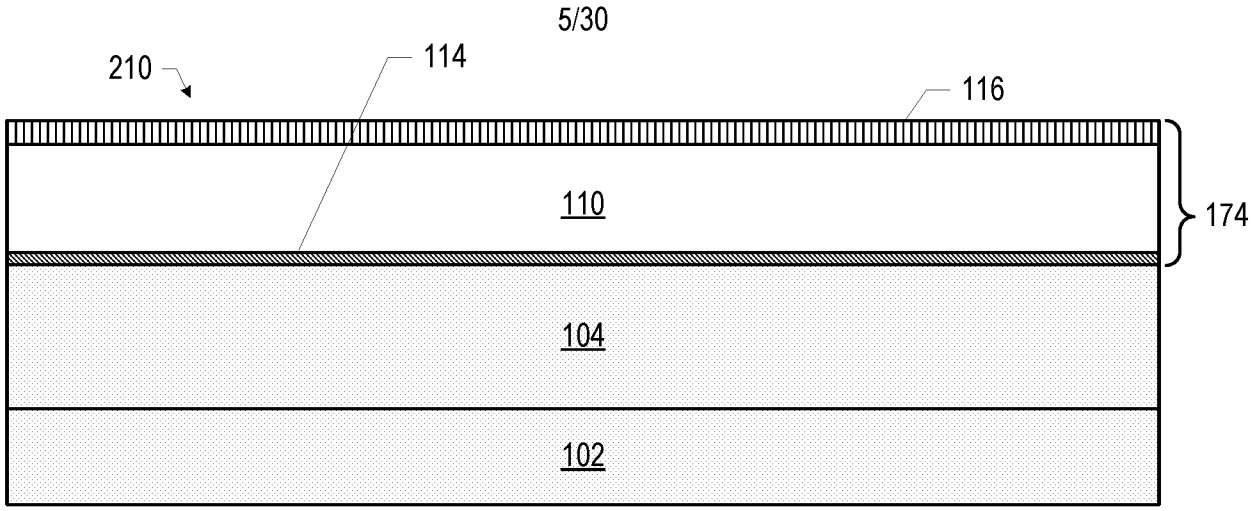

FIG. 11

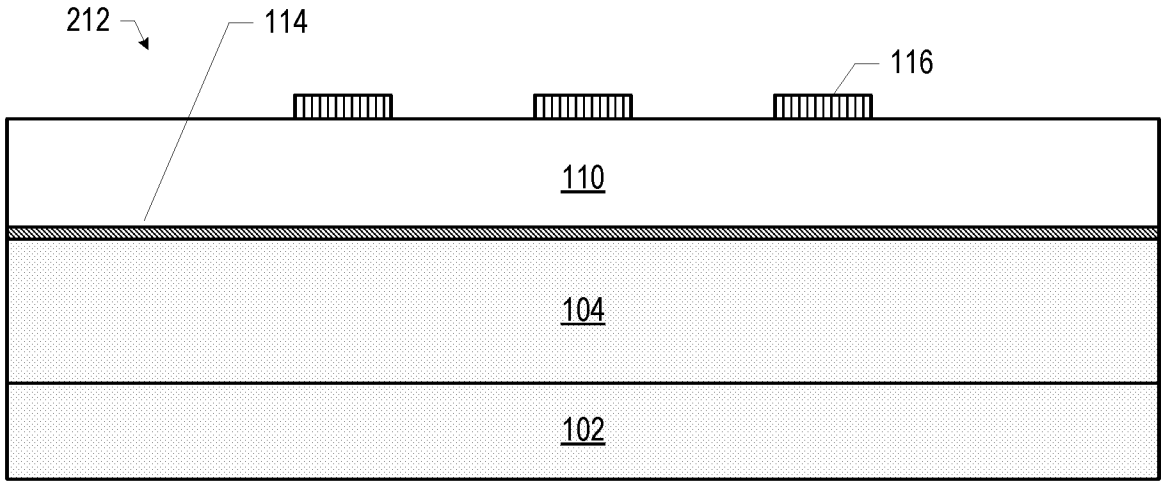

FIG. 12

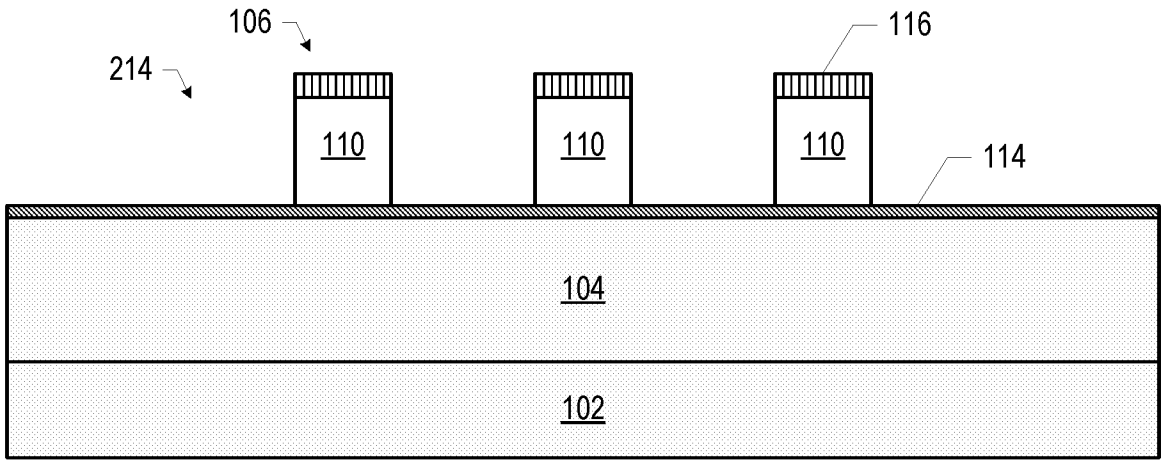

FIG. 13

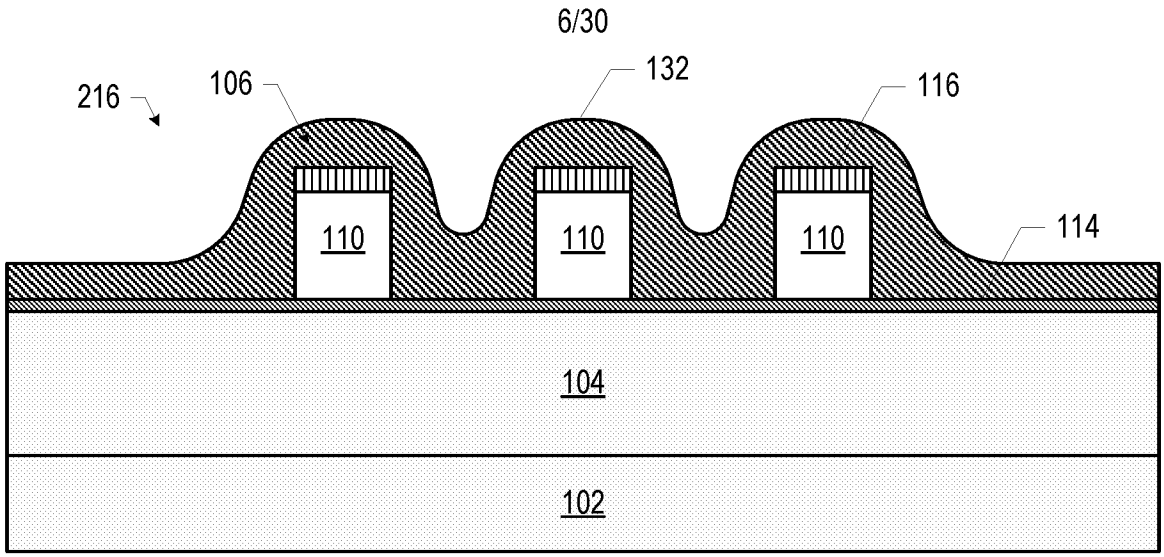

FIG. 14

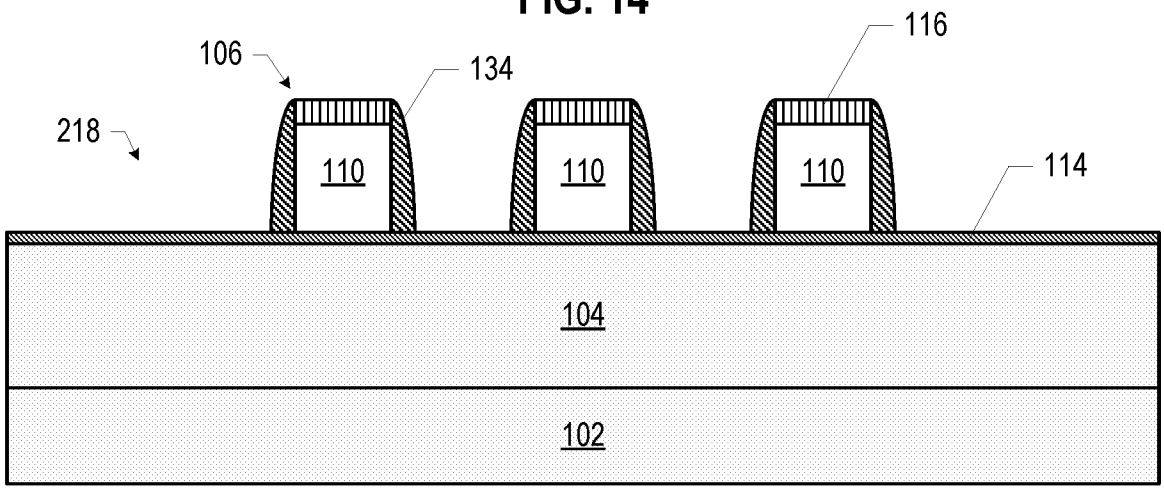

FIG. 15

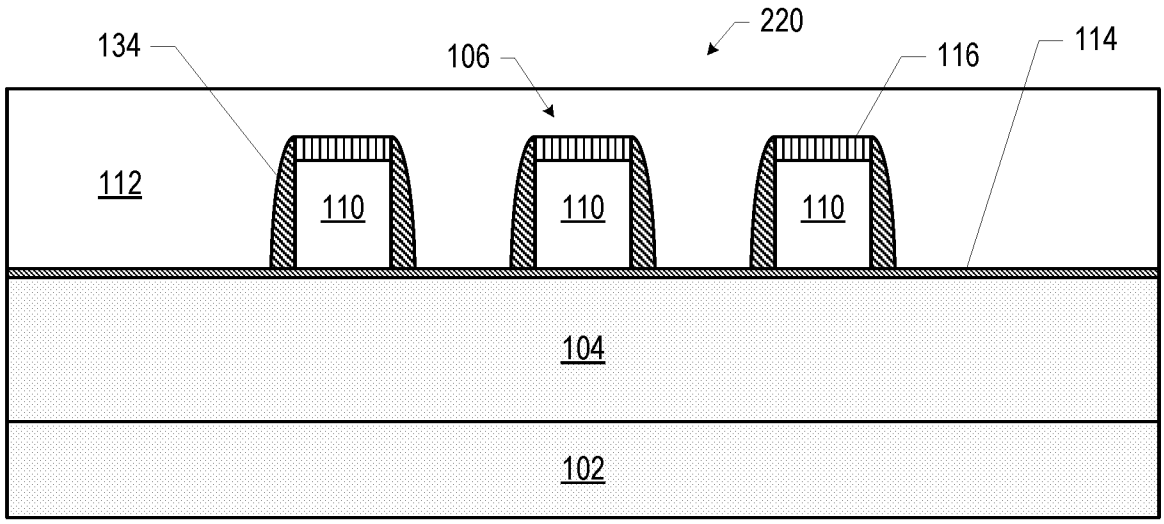

FIG. 16

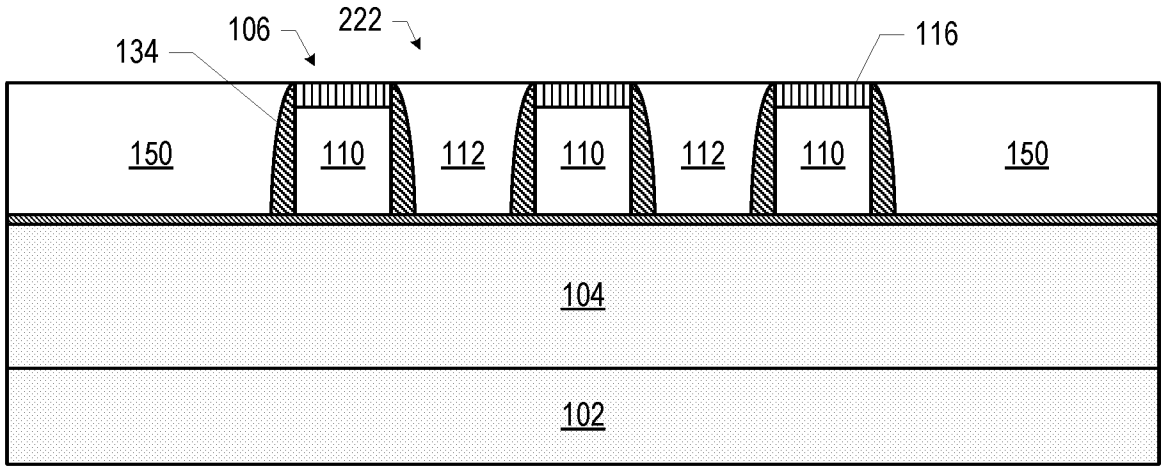

FIG. 17

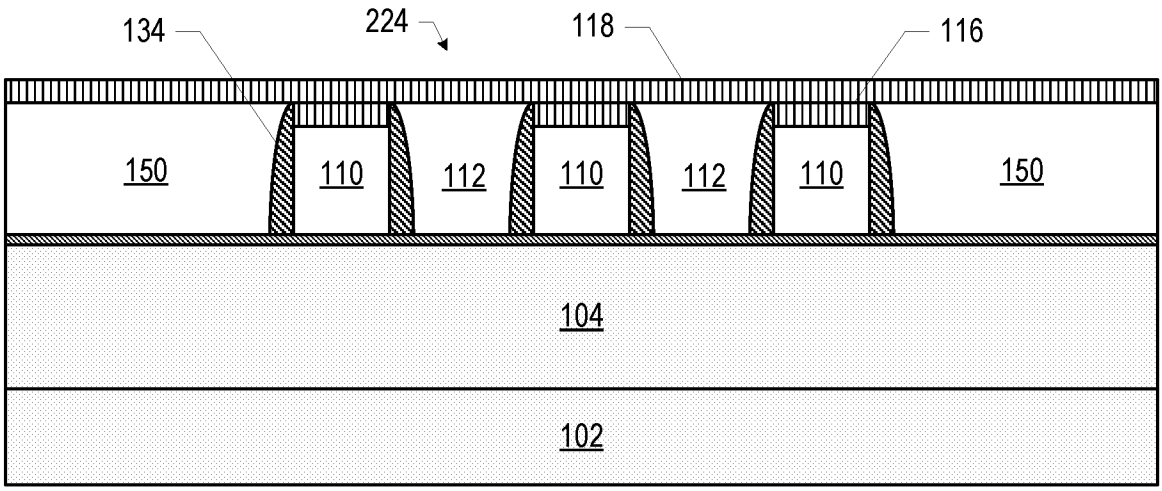

FIG. 18

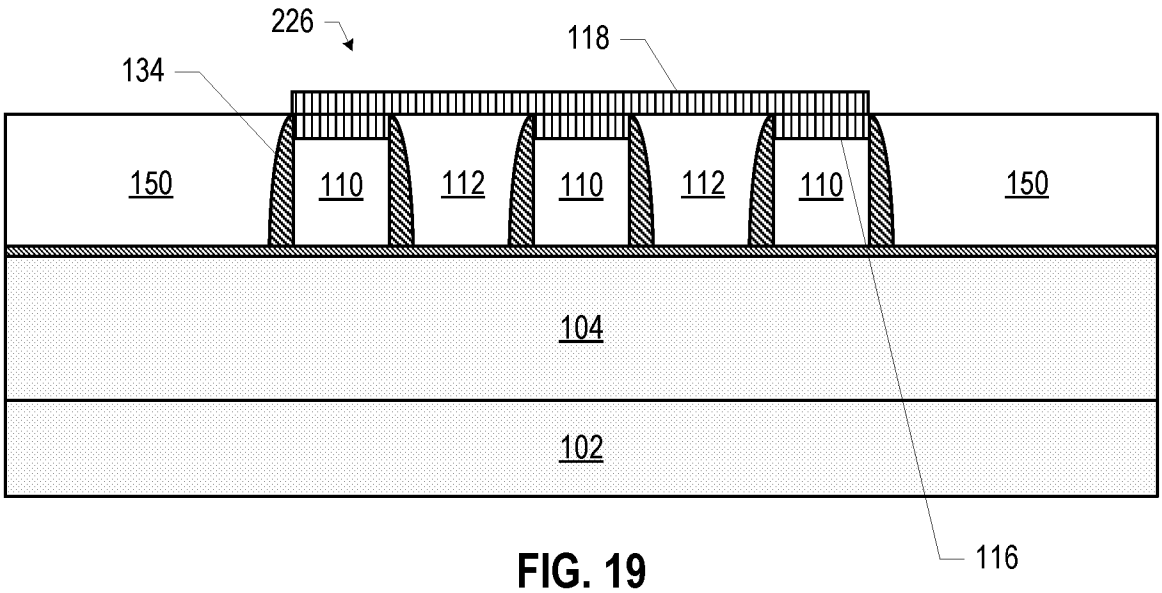

FIG. 19

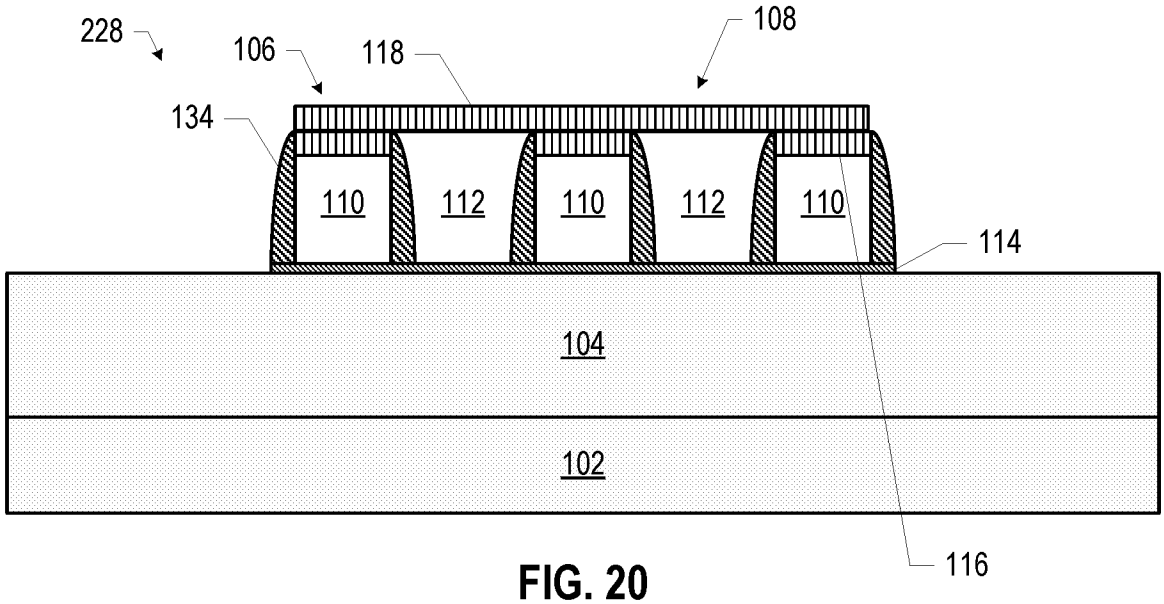
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FIG. 20

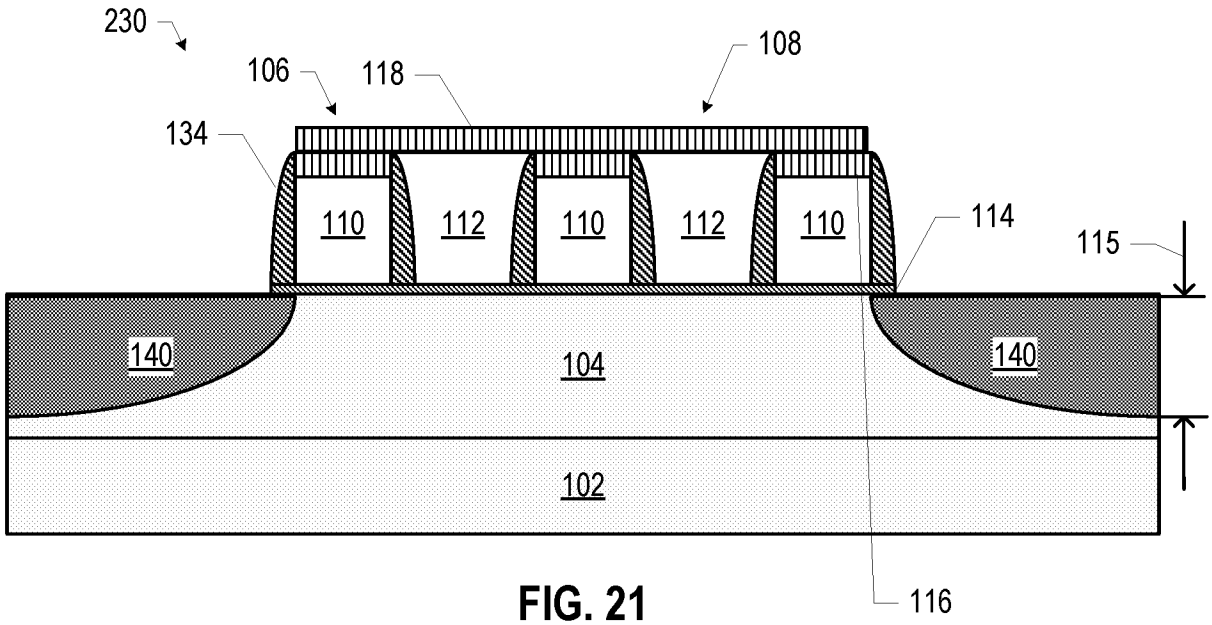
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FIG. 21

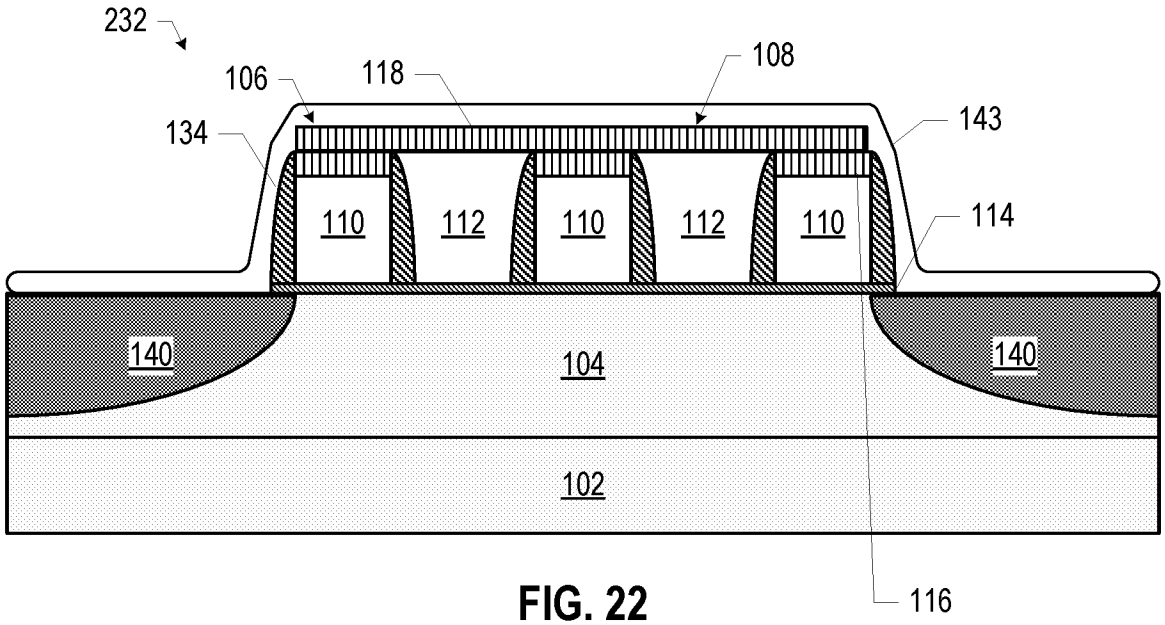
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FIG. 22

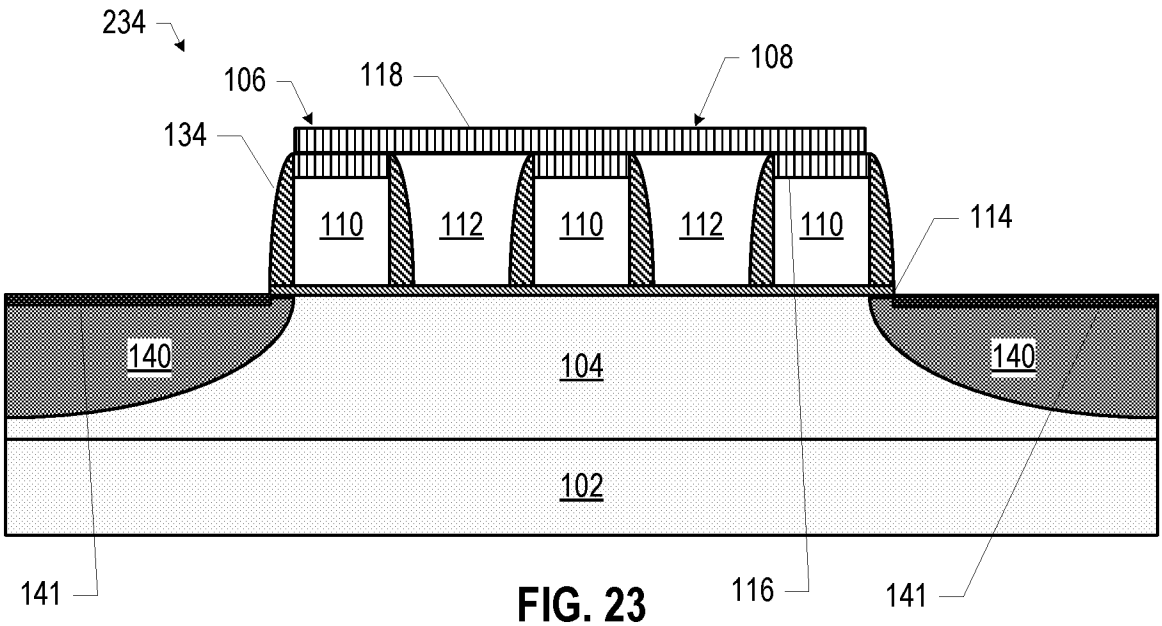
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FIG. 23

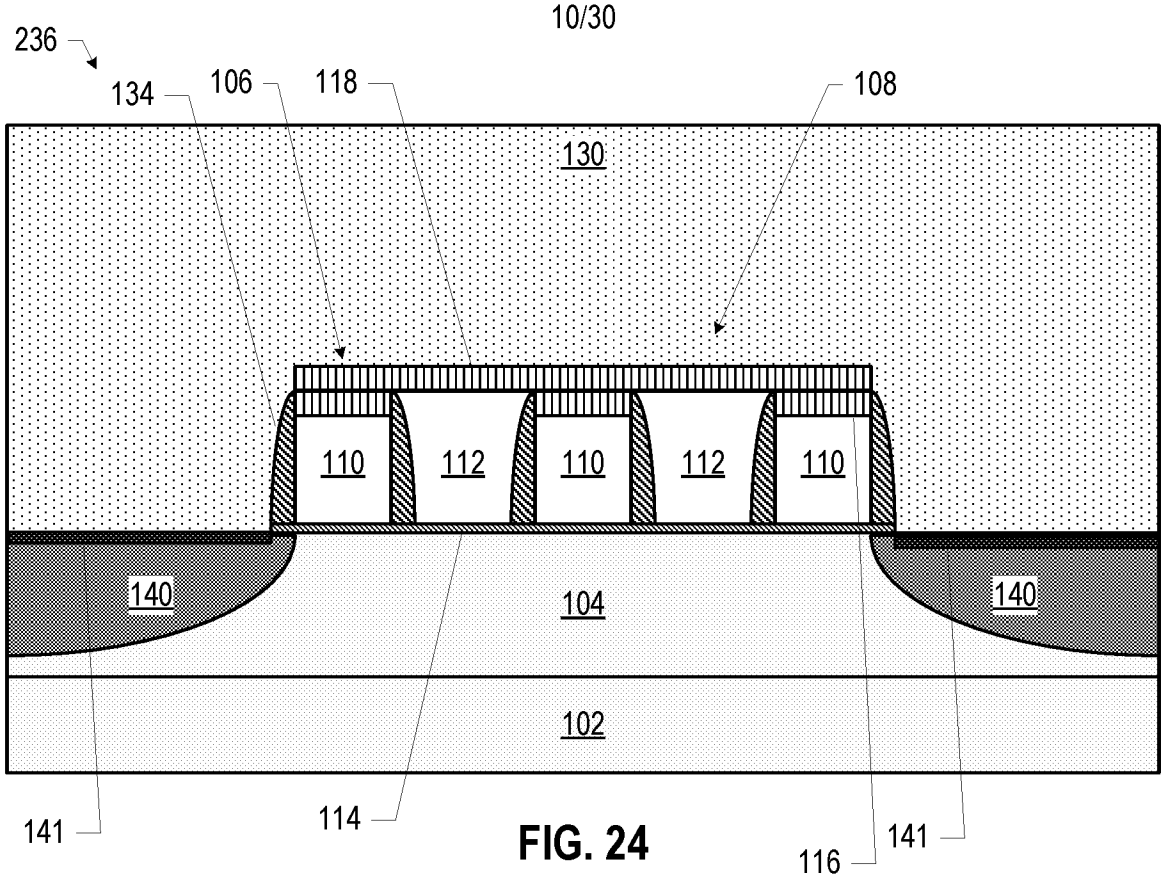
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FIG. 24

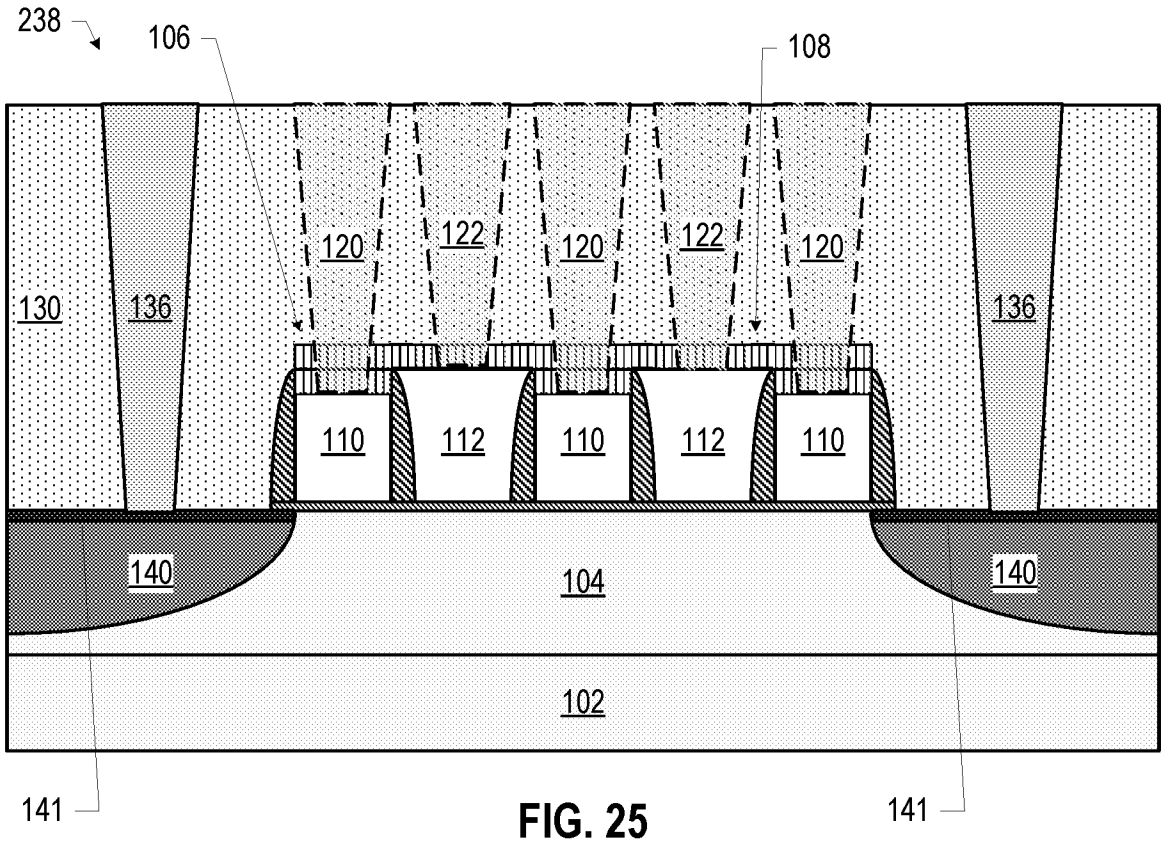
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FIG. 25

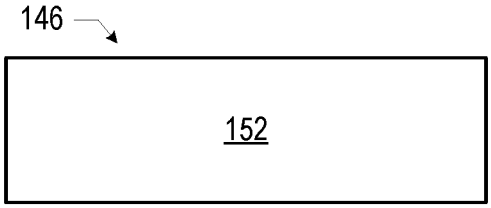

FIG. 26

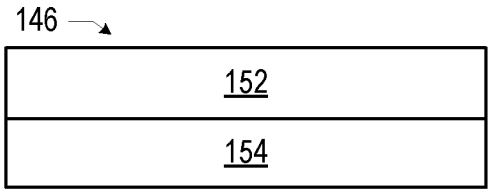

FIG. 27

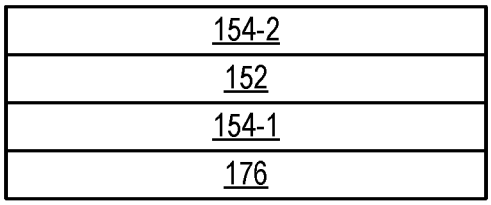

FIG. 28

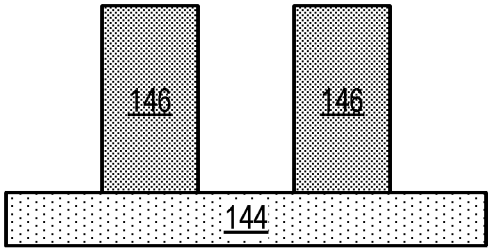

FIG. 29

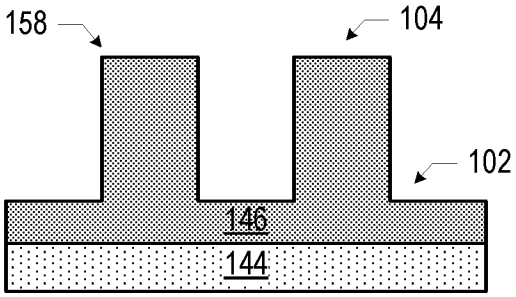

FIG. 30

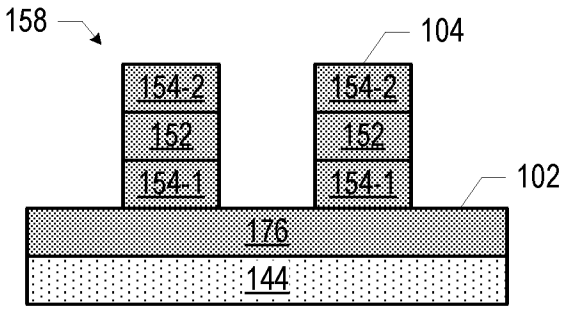

FIG. 31

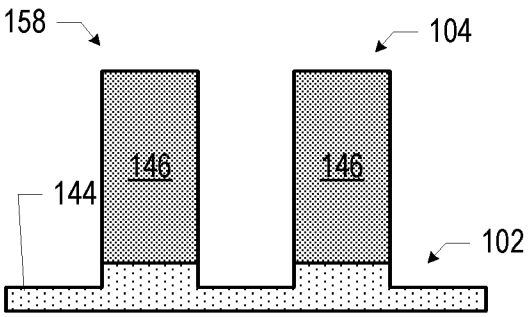

FIG. 32

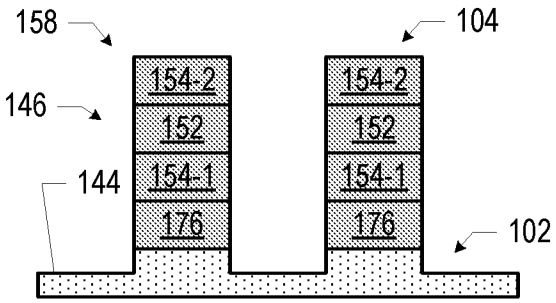

FIG. 33

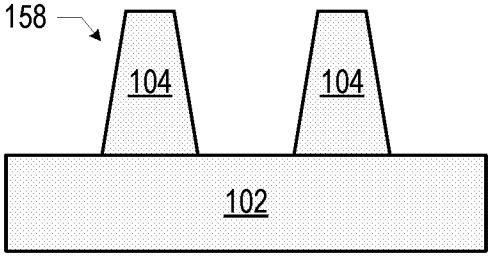

FIG. 34

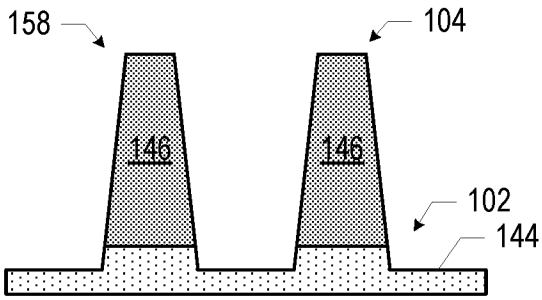

FIG. 35

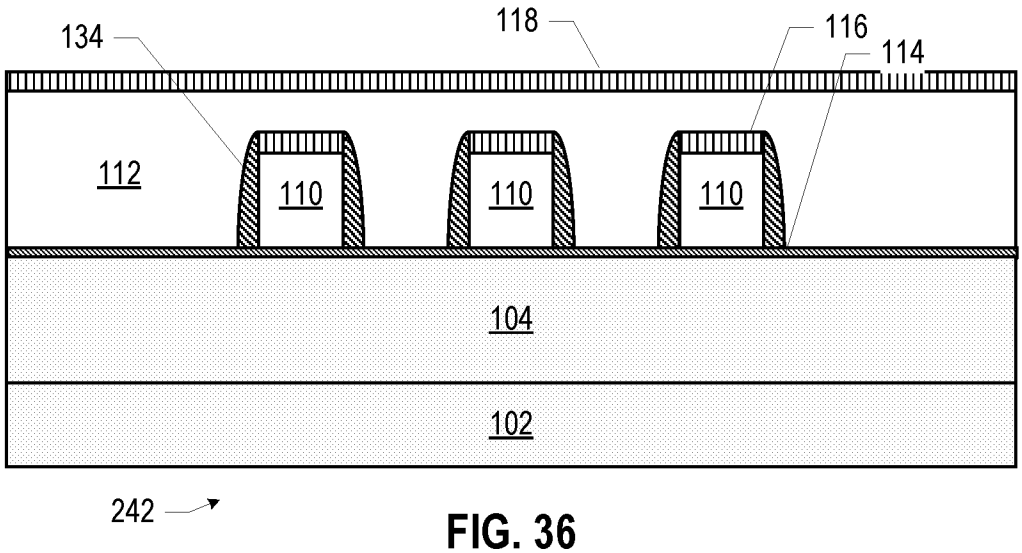

FIG. 36

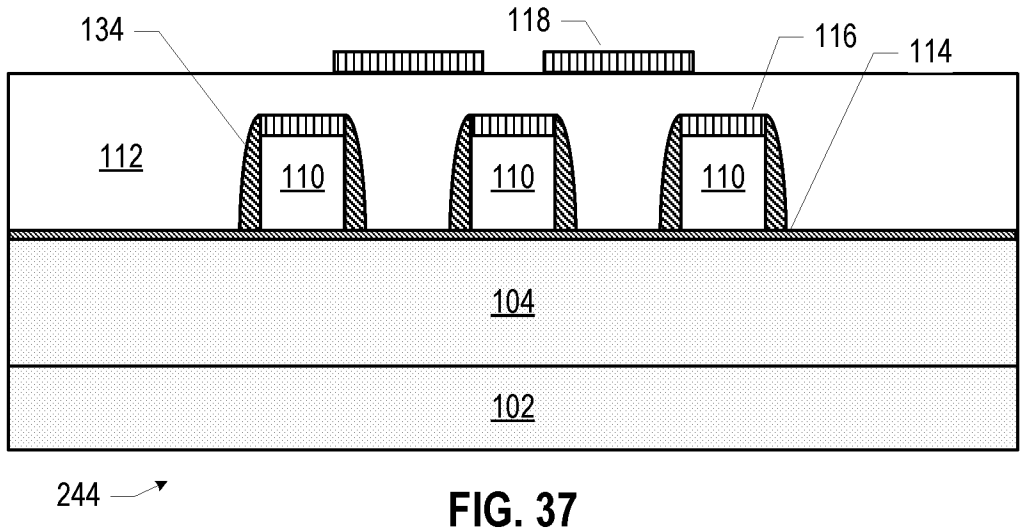

FIG. 37

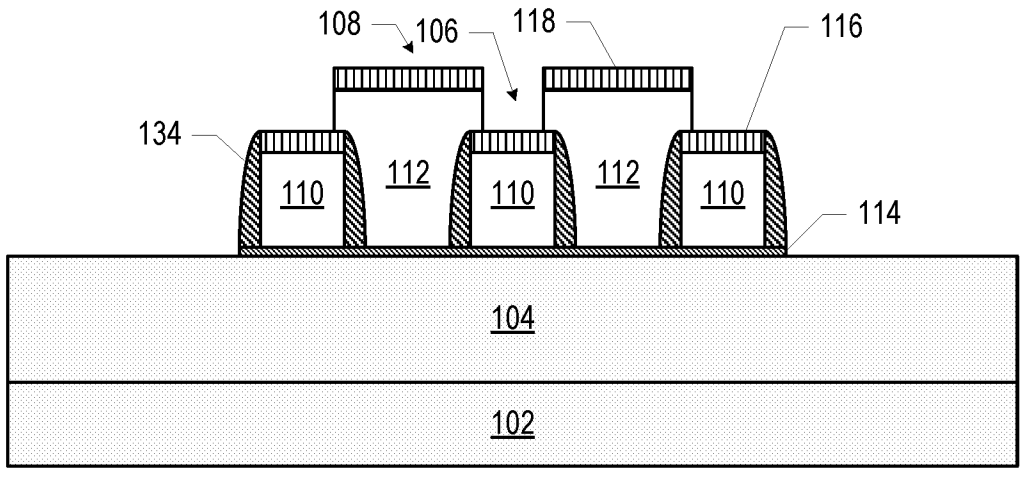

FIG. 38

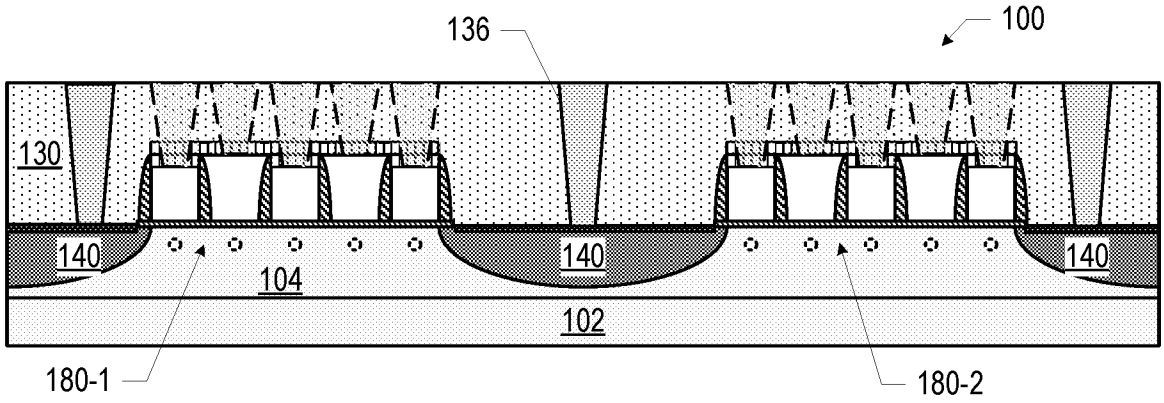

FIG. 39

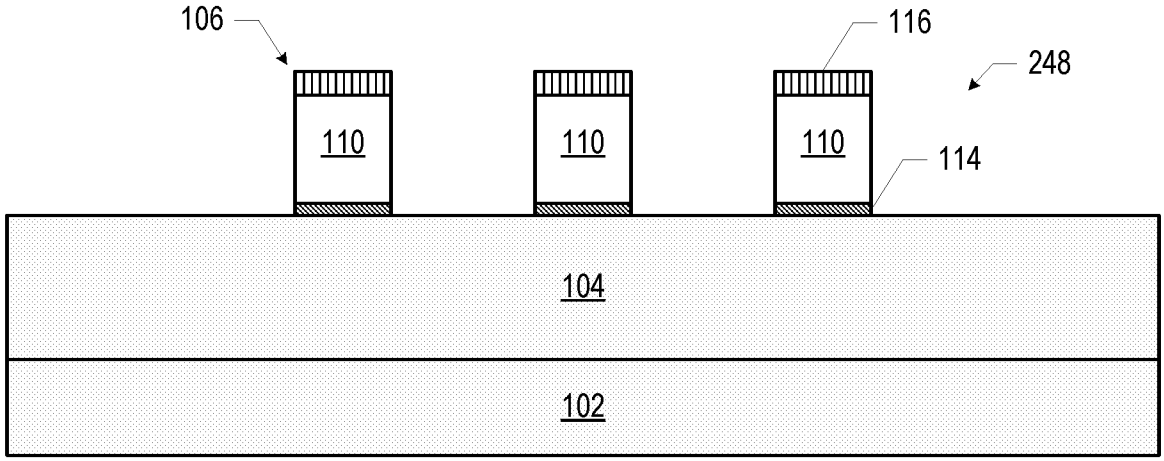

FIG. 40

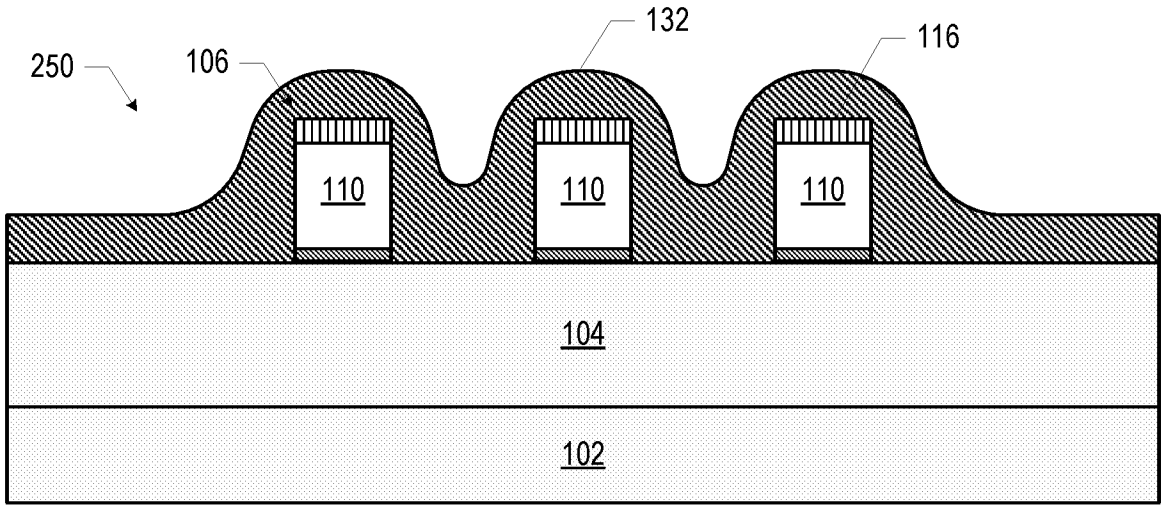

FIG. 41

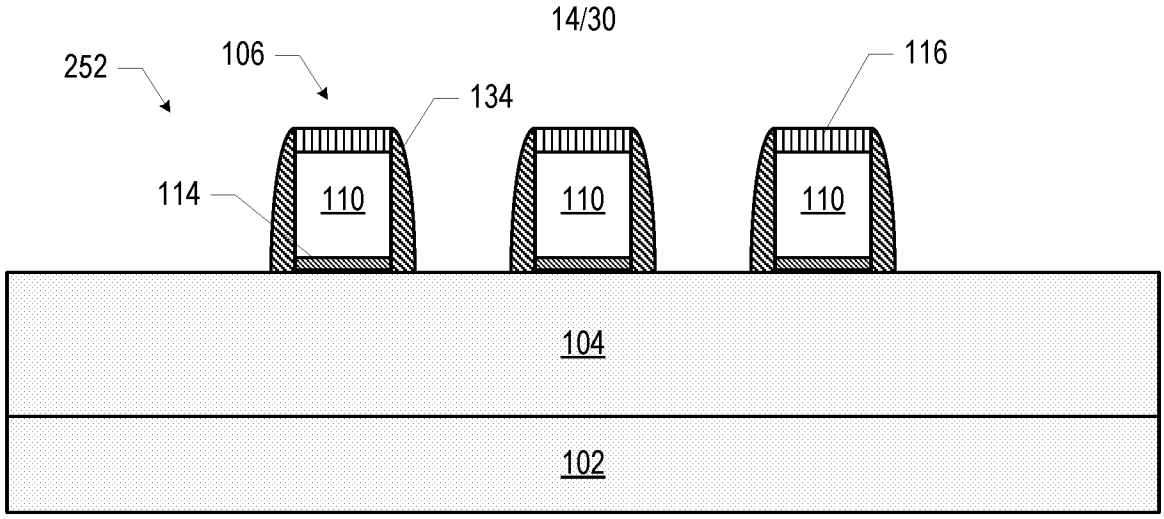

FIG. 42

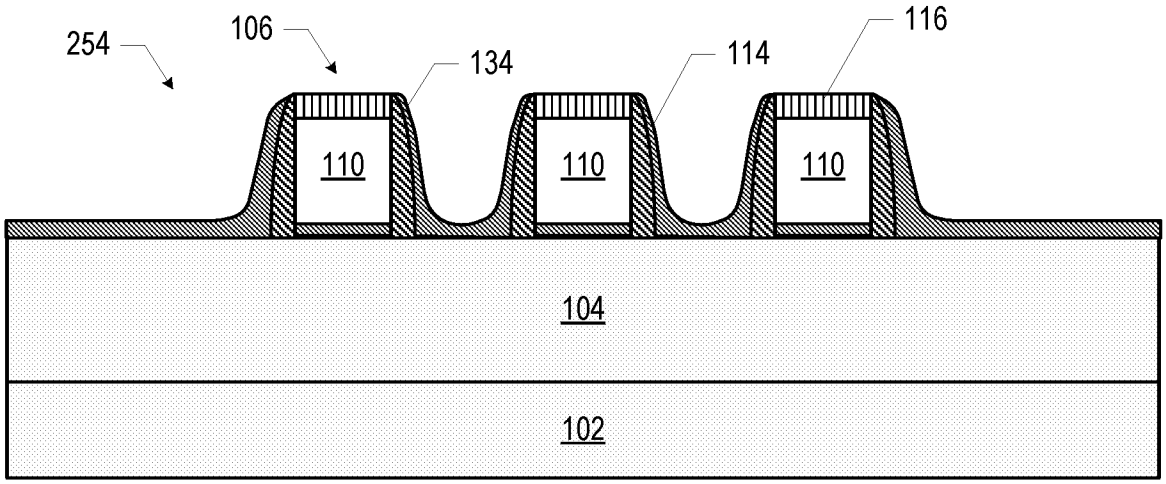

FIG. 43

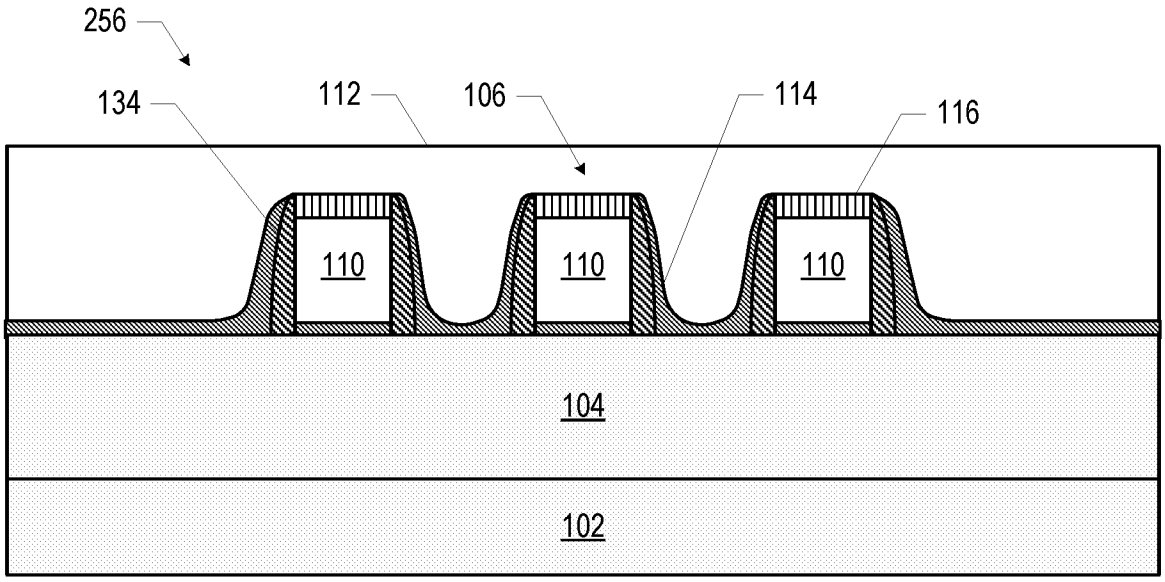

FIG. 44

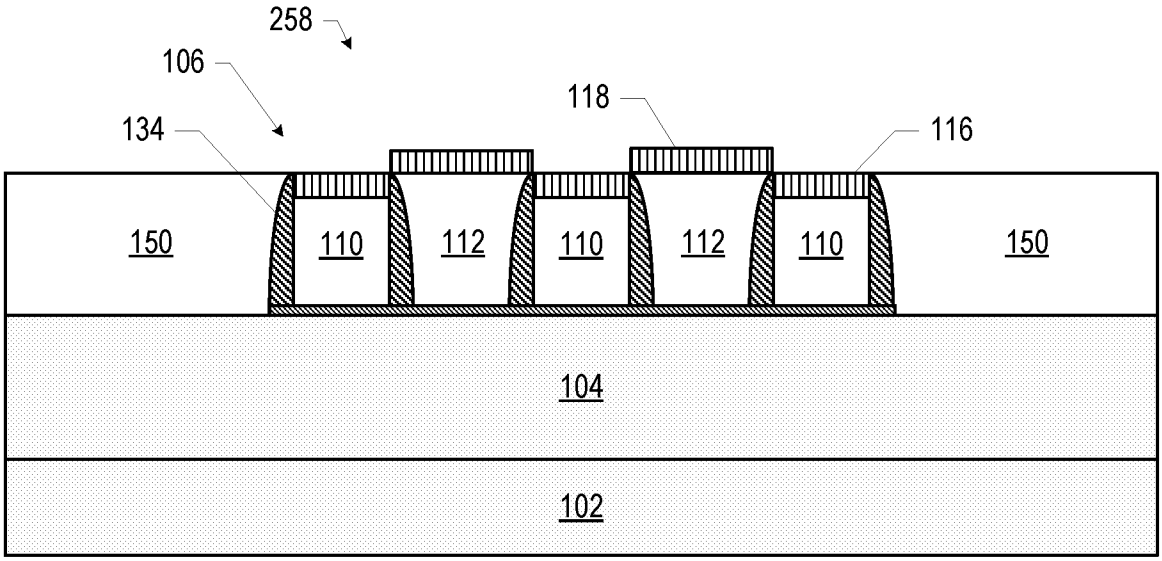

FIG. 45

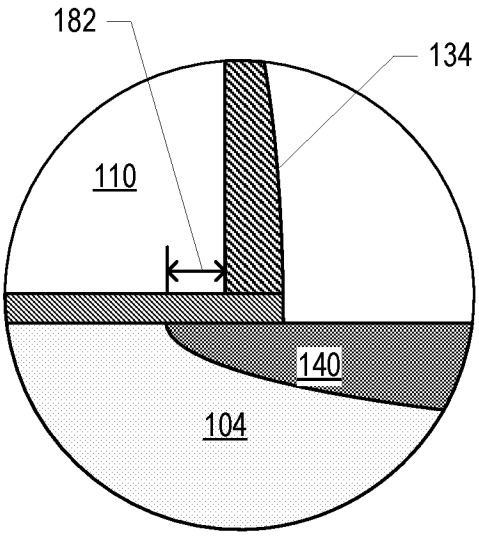

FIG. 46

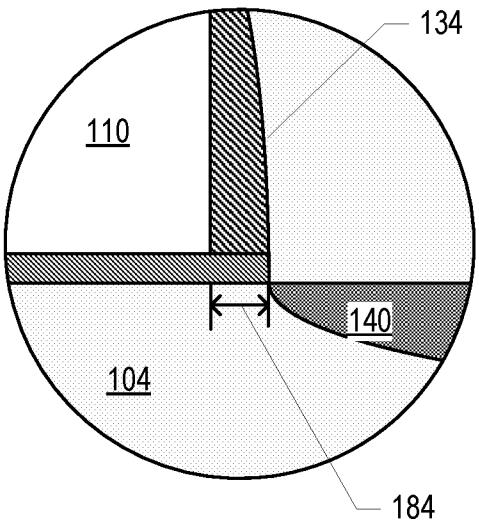

FIG. 47

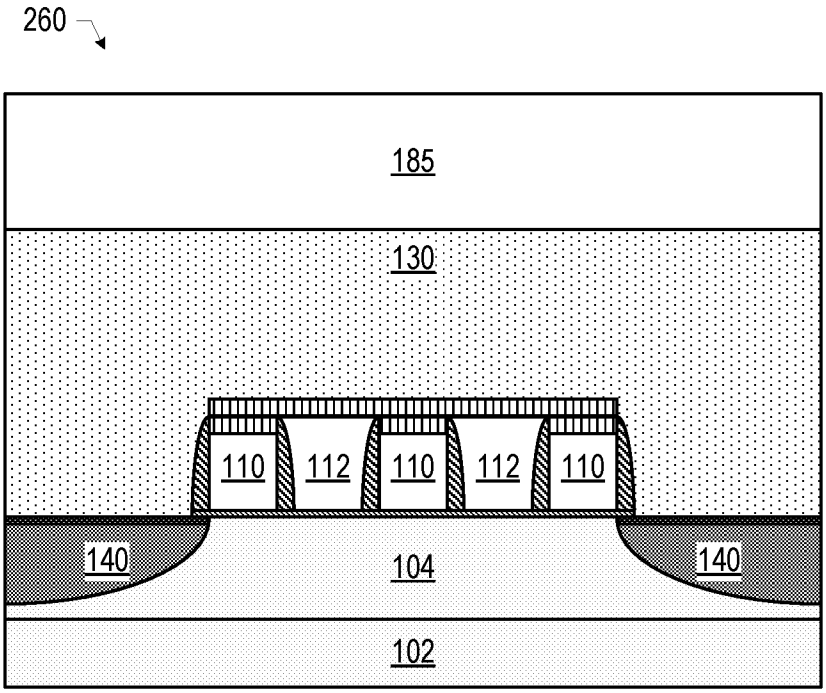
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FIG. 48

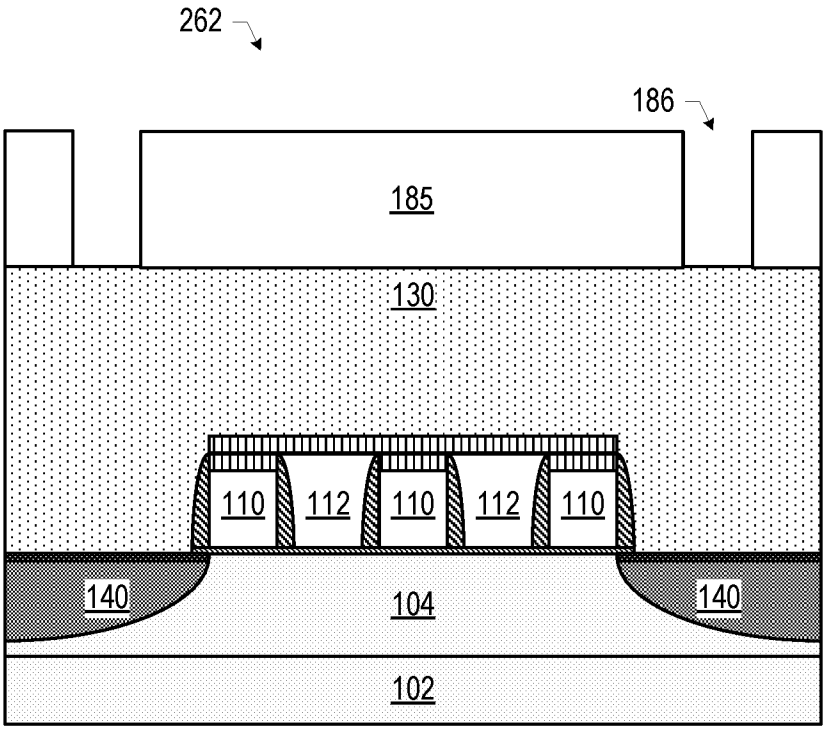
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FIG. 49

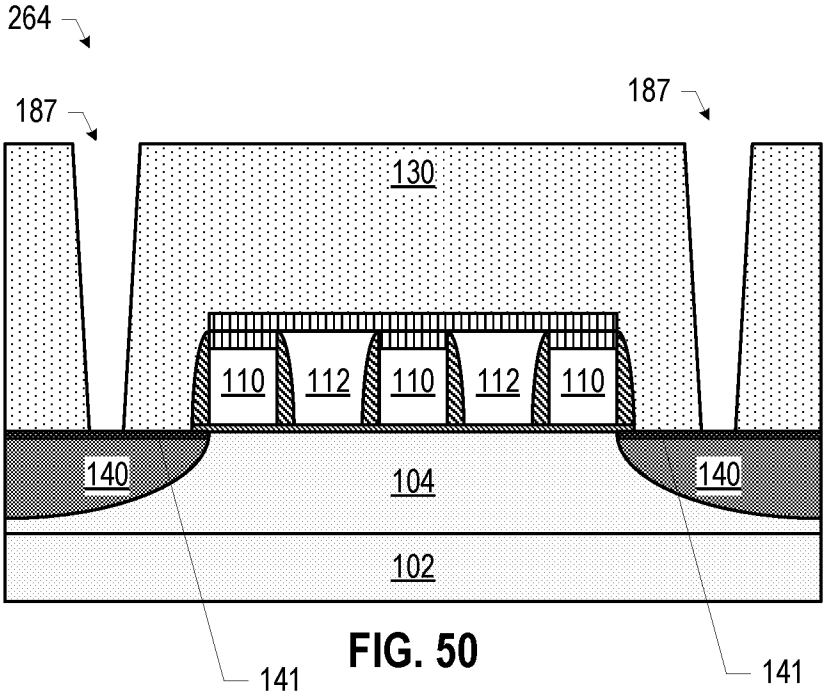
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FIG. 50

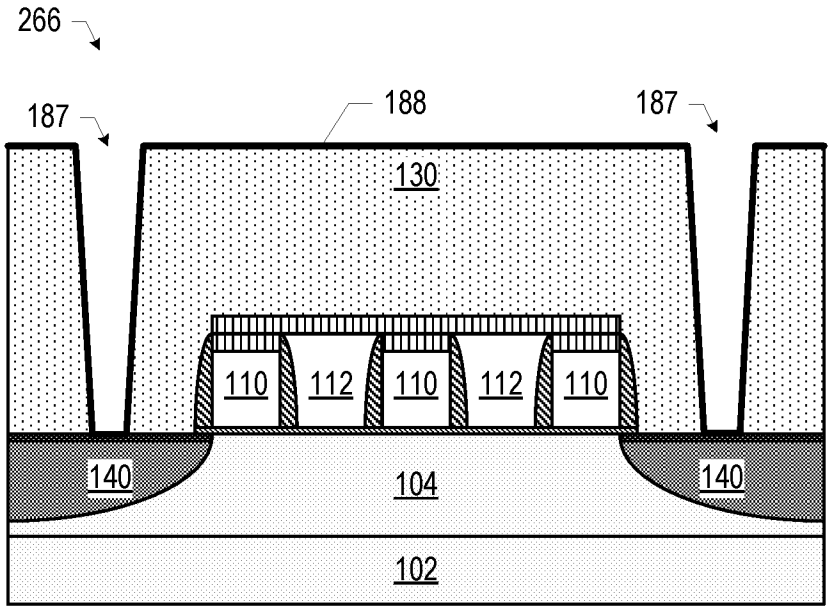
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FIG. 51

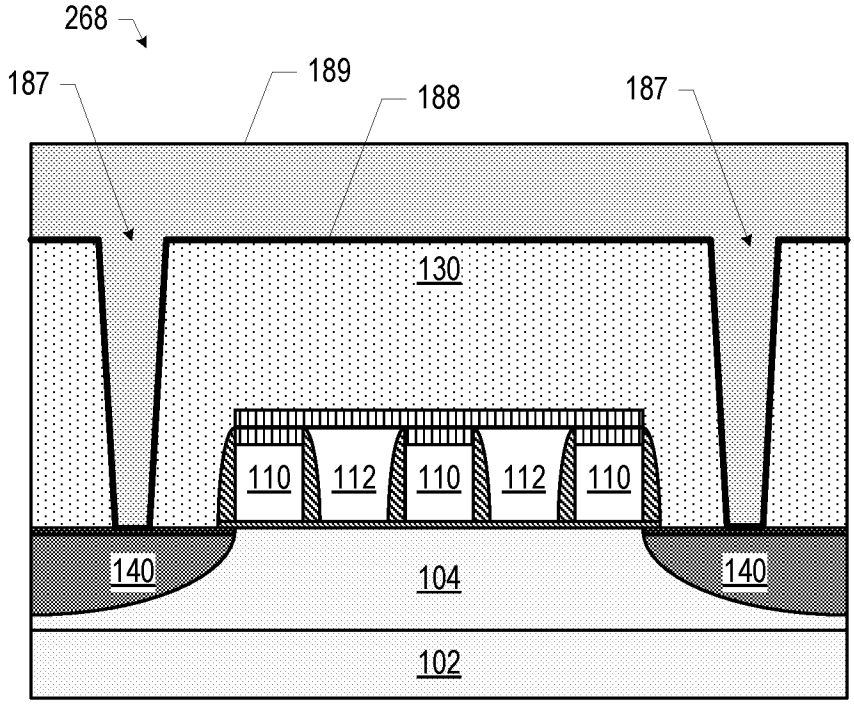
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FIG. 52

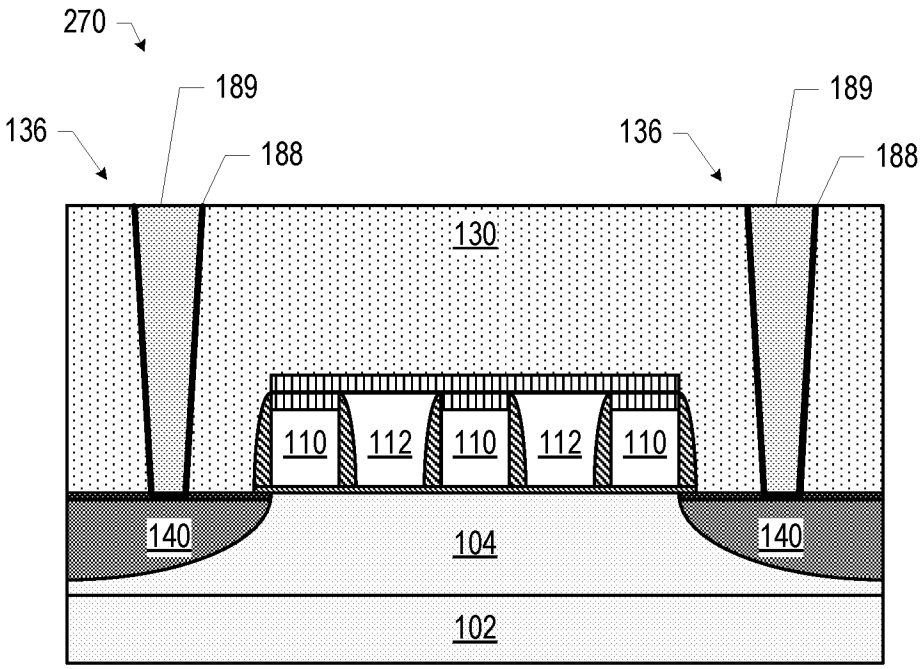
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FIG. 53

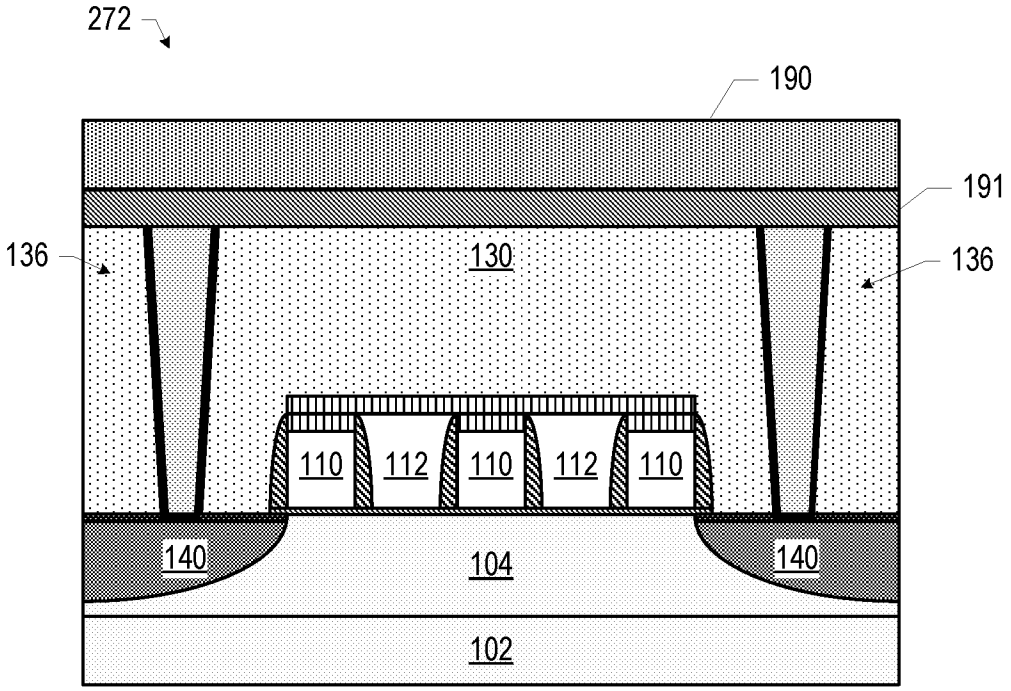
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FIG. 54

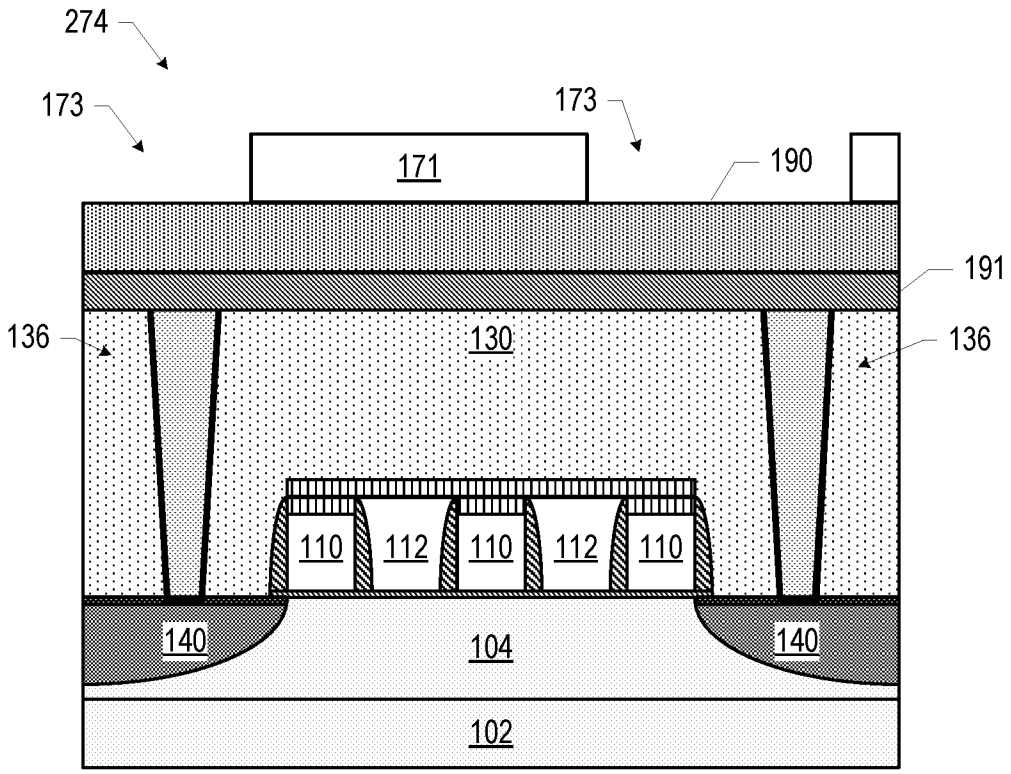
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FIG. 55

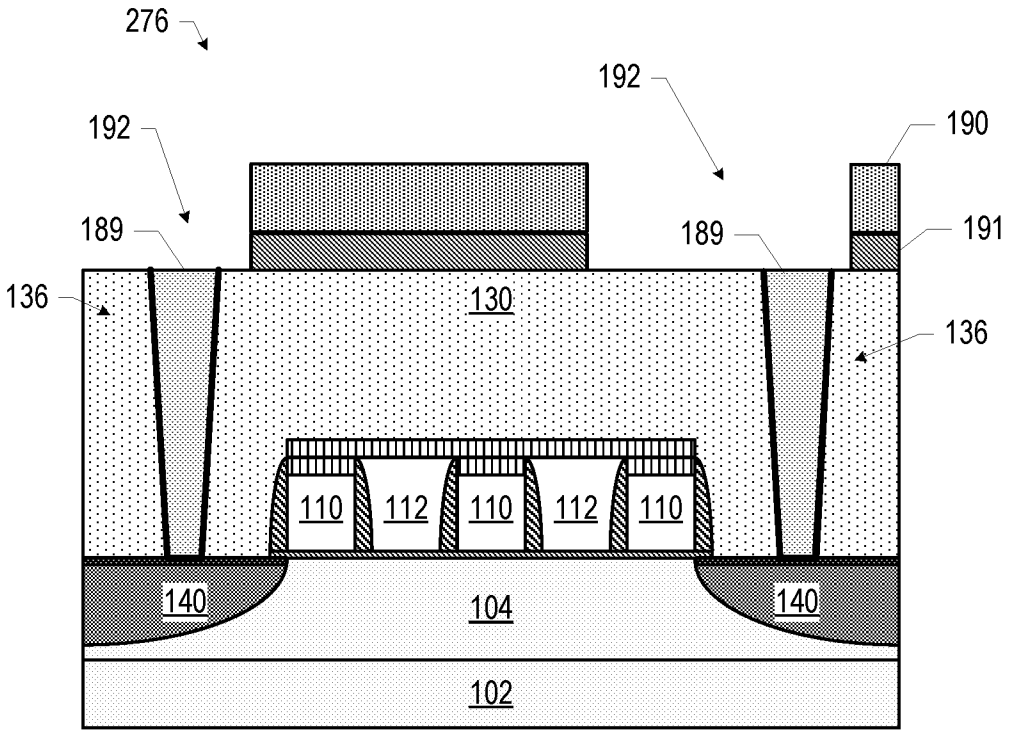
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FIG. 56

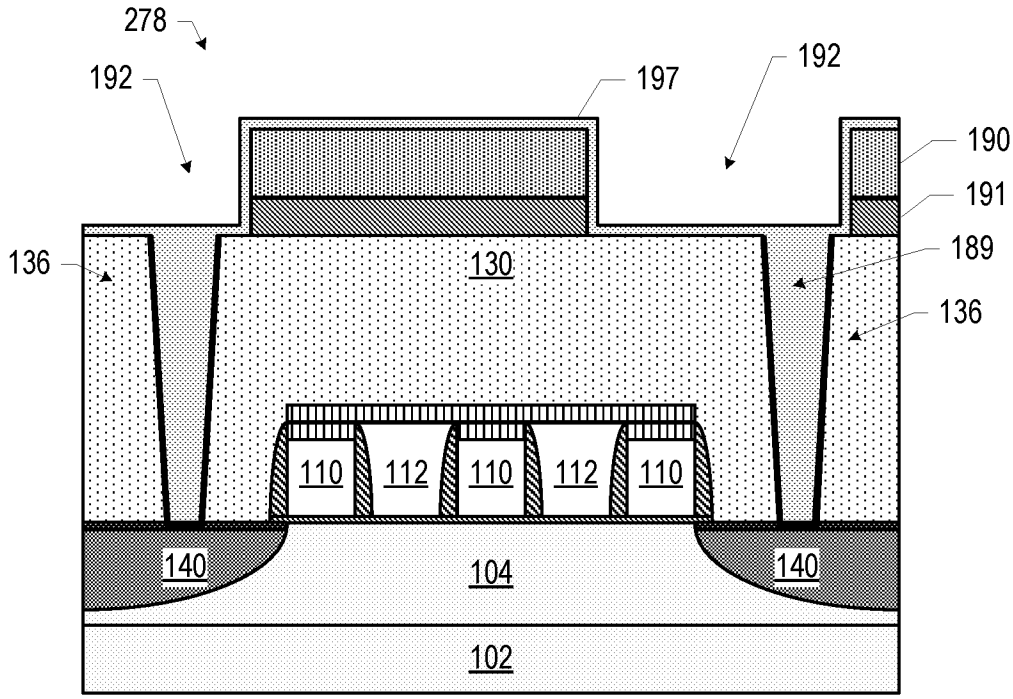
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FIG. 57

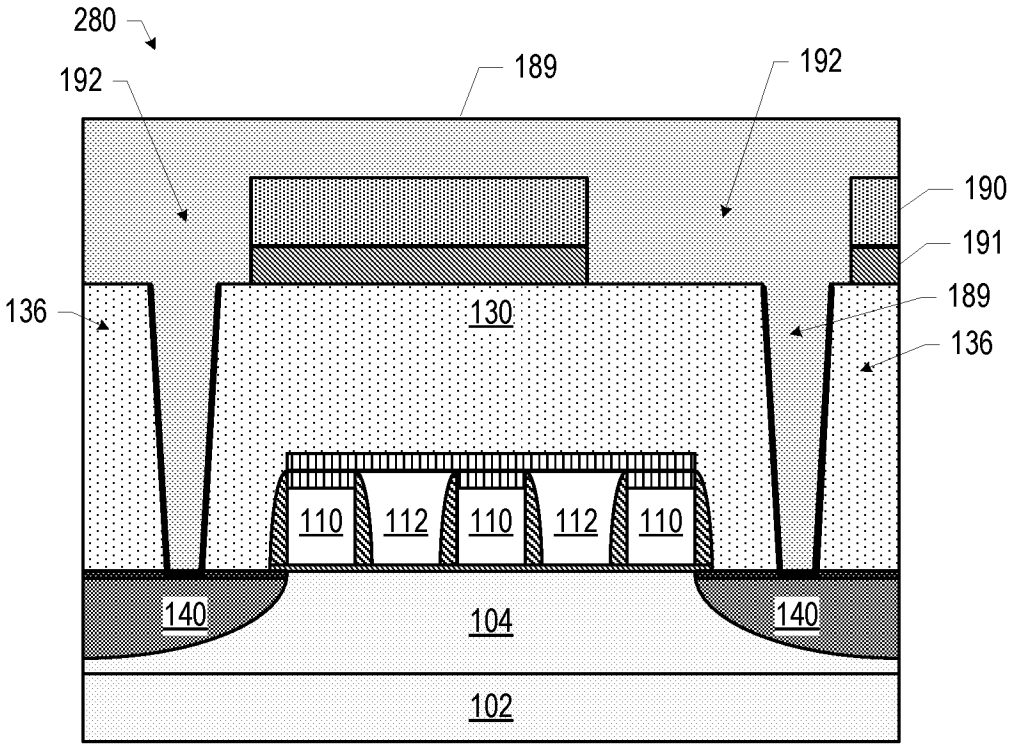
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FIG. 58

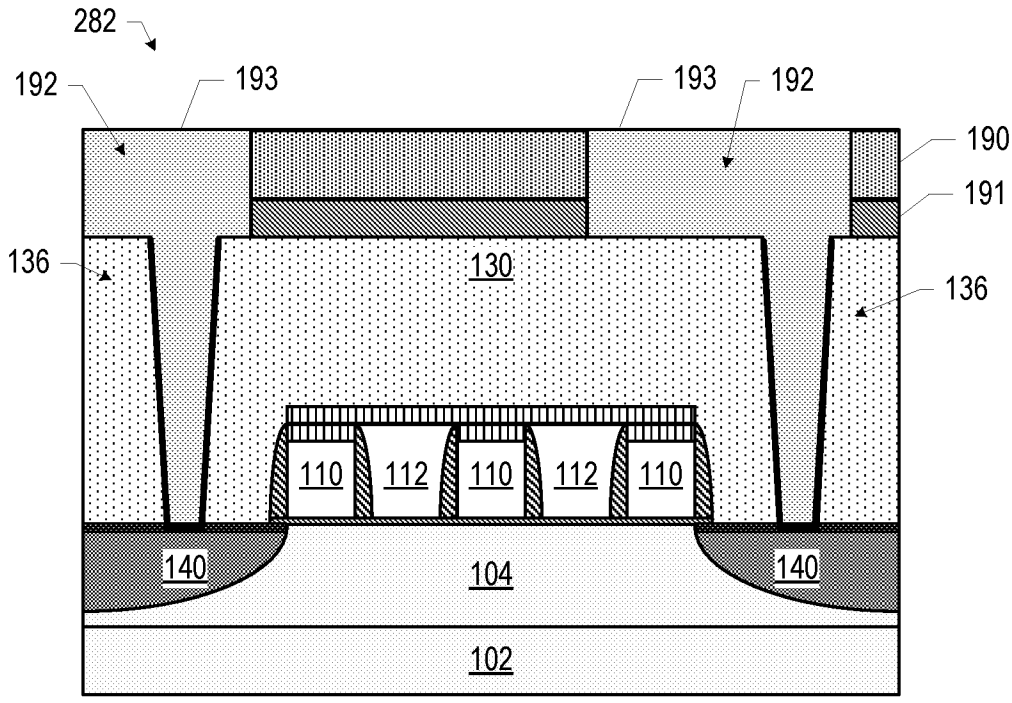
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FIG. 59

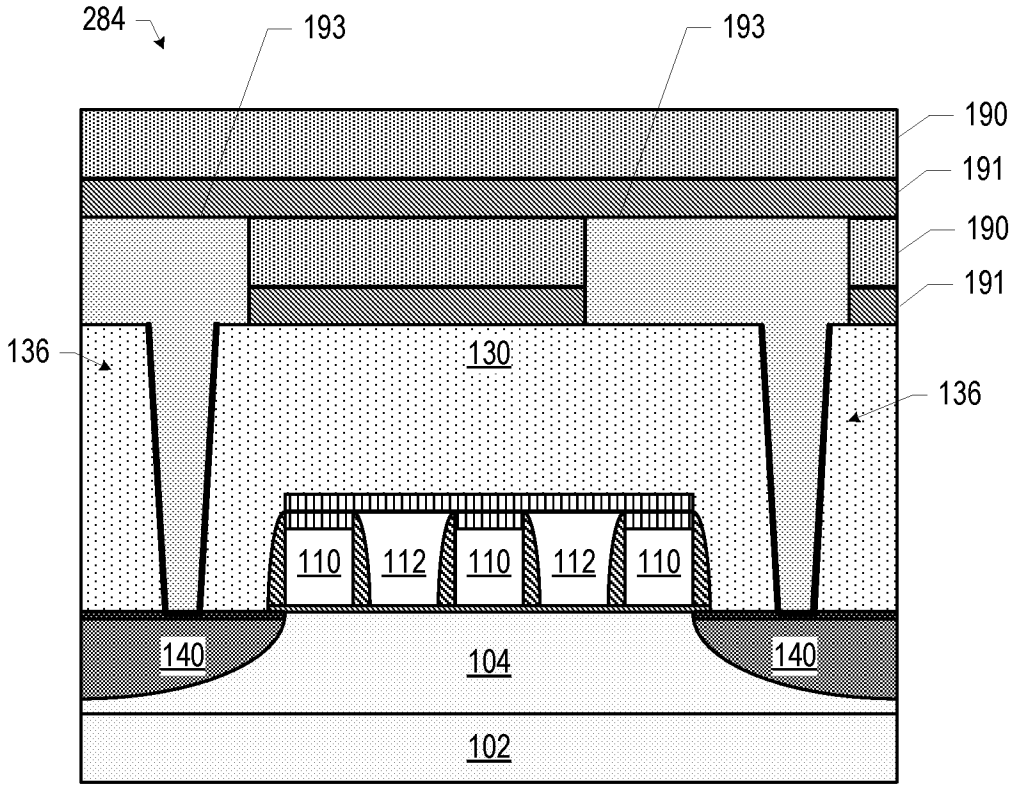
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FIG. 60

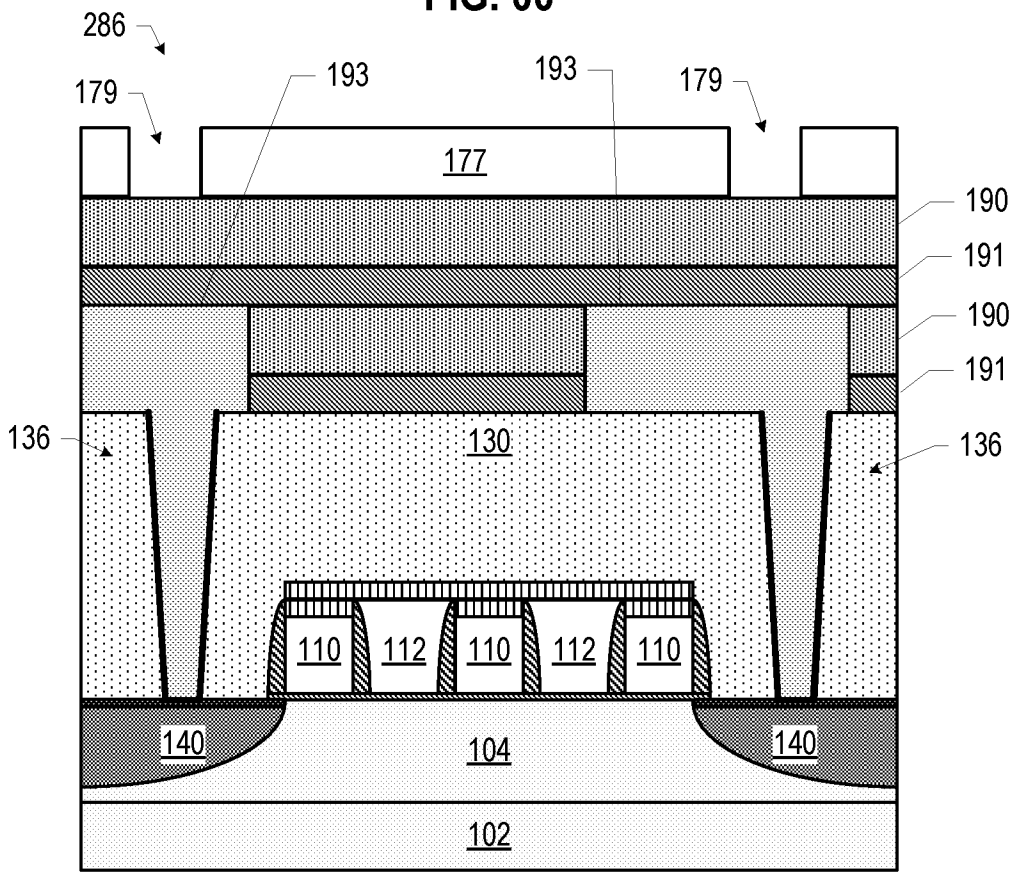
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FIG. 61

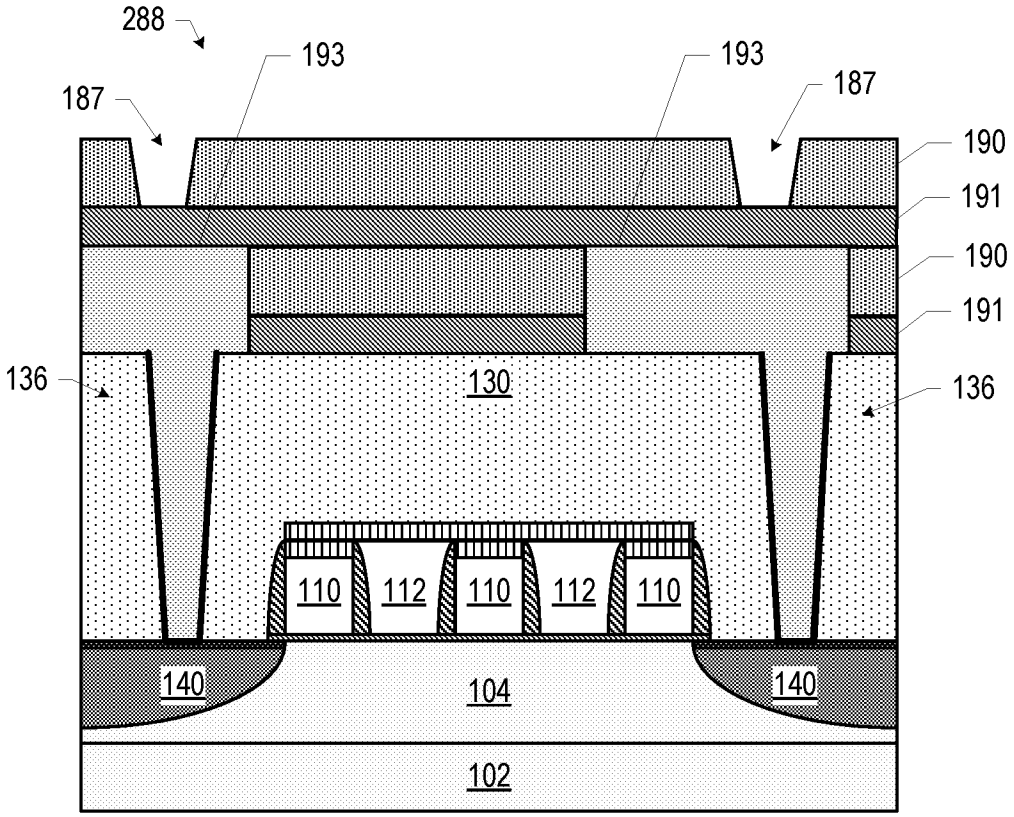
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FIG. 62

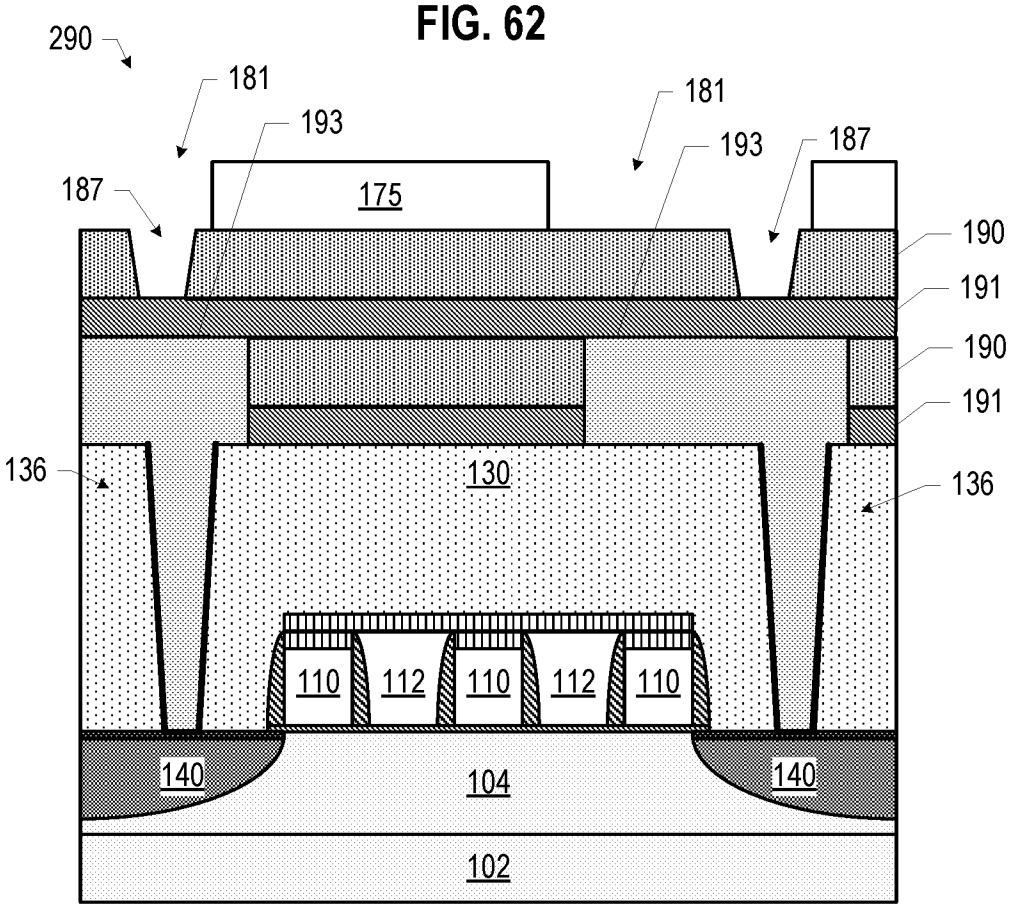
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FIG. 63

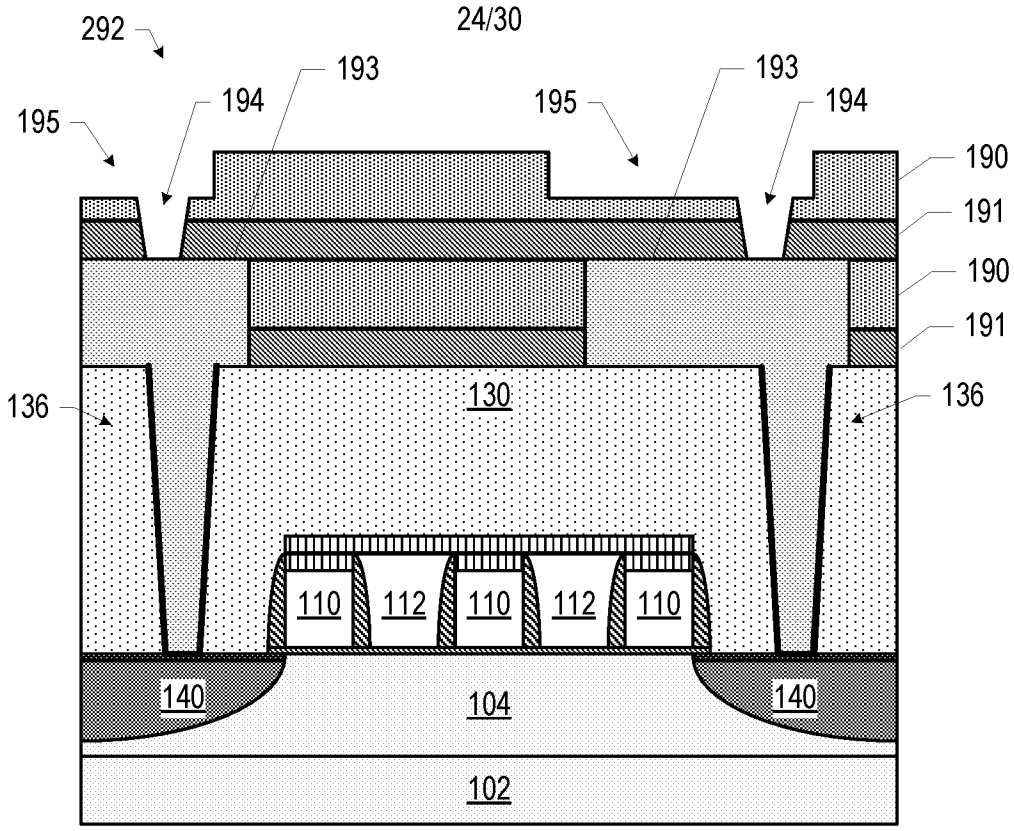
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FIG. 64

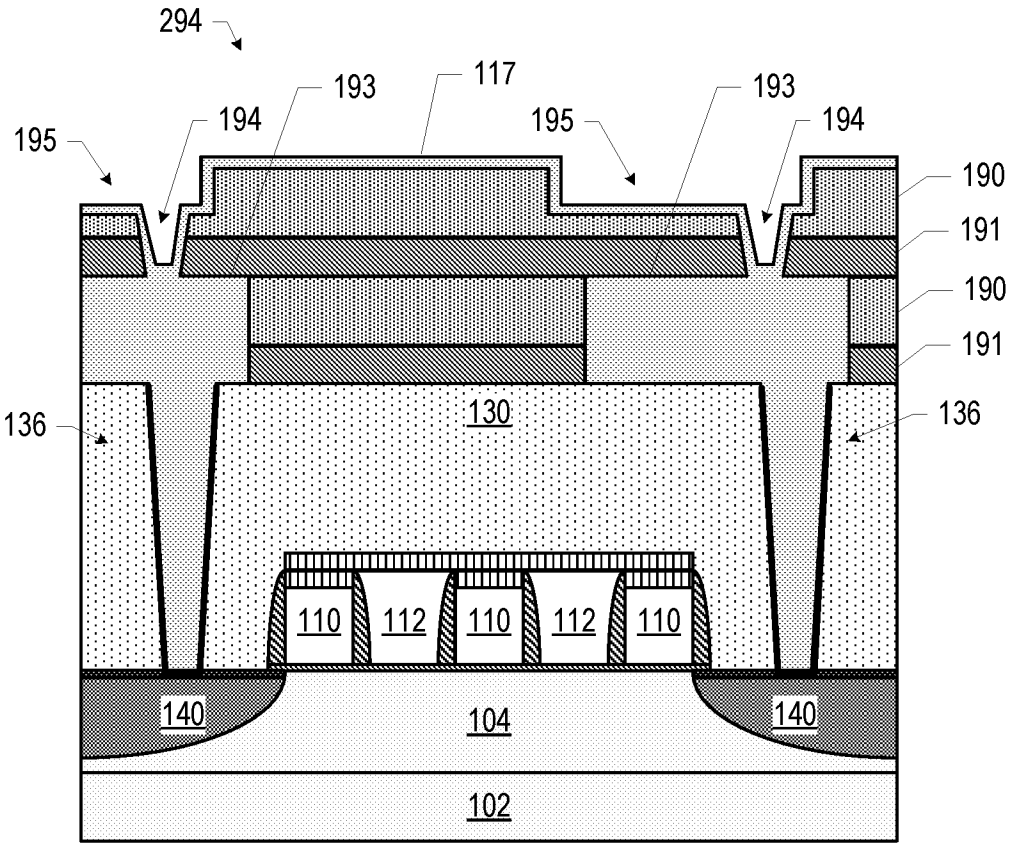
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FIG. 65

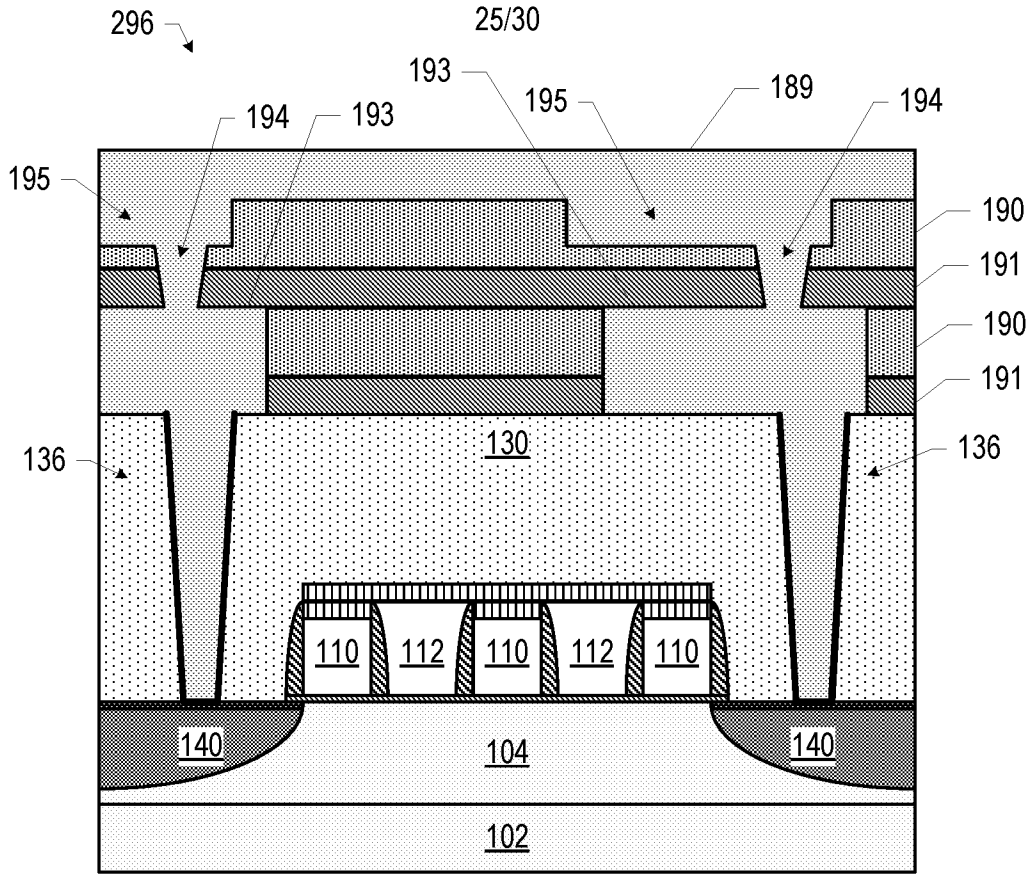
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FIG. 66

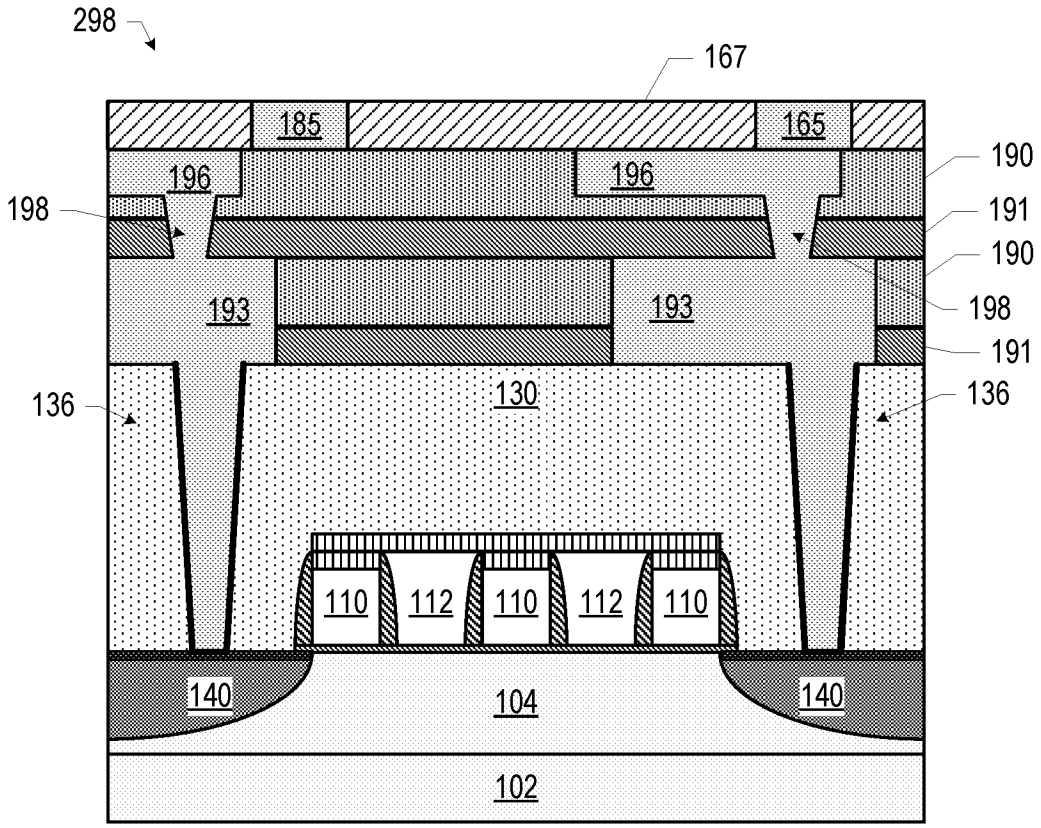
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FIG. 67

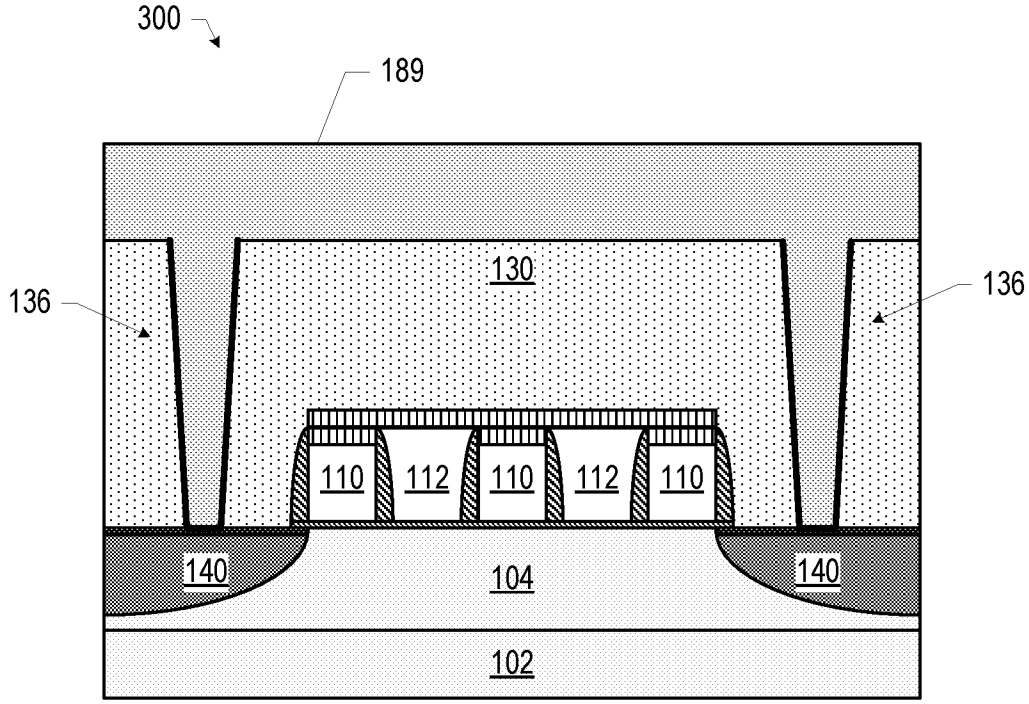
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FIG. 68

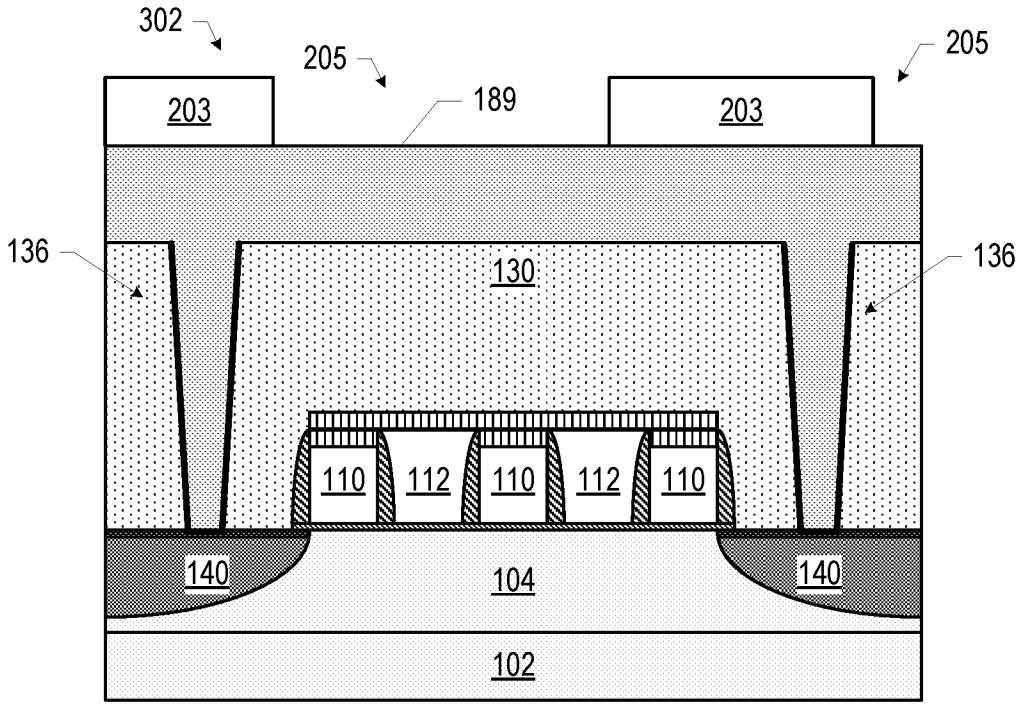
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FIG. 69

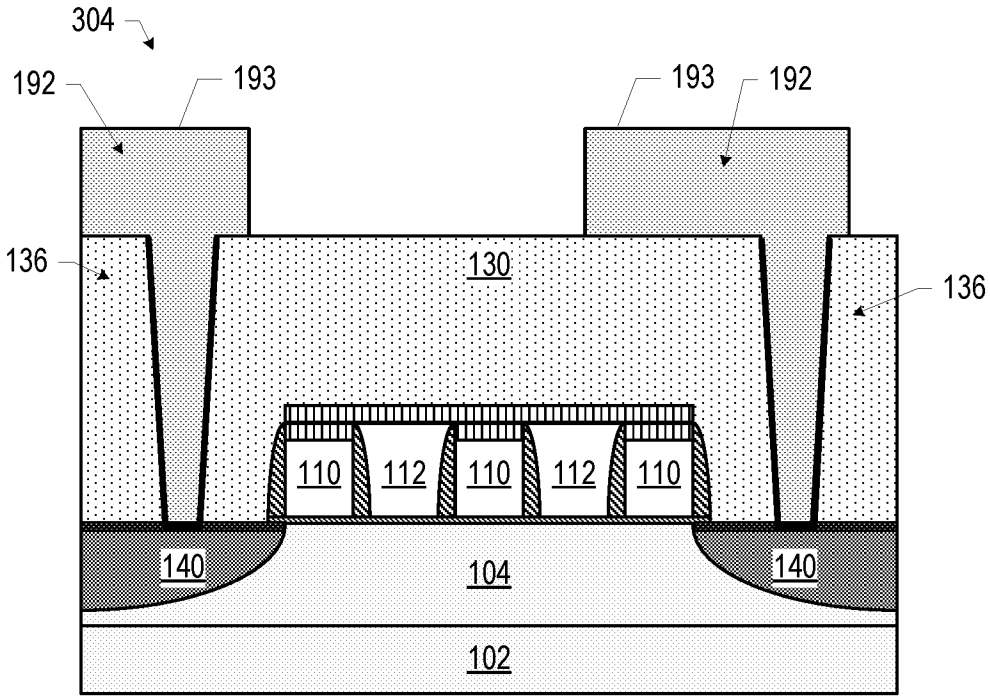
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FIG. 70

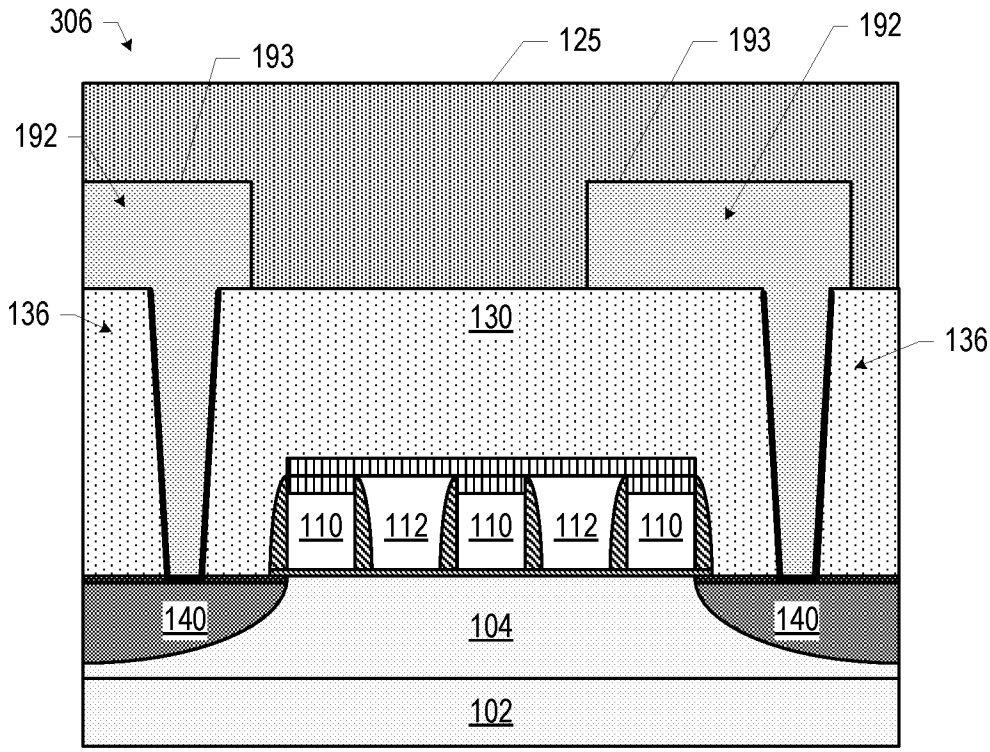
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FIG. 71

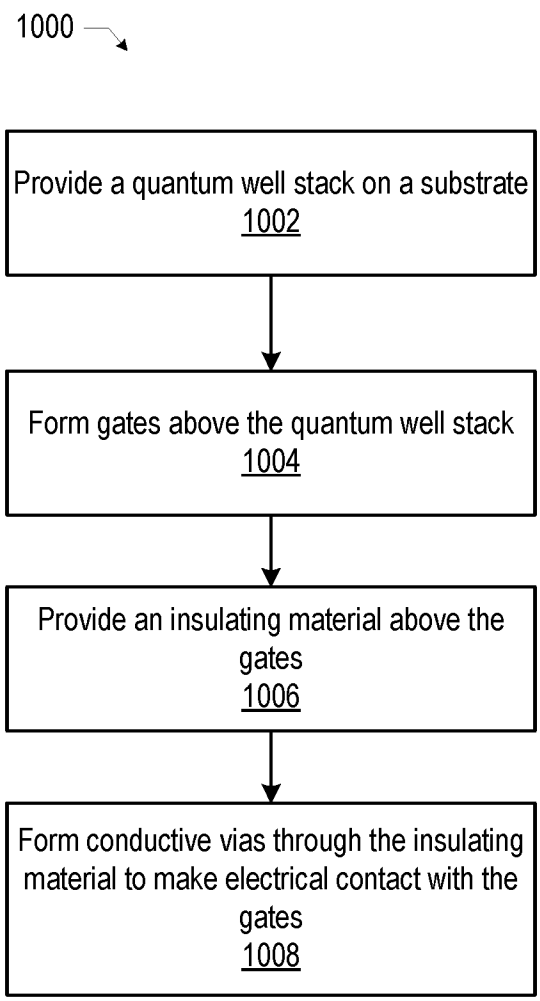
1000
Provide a quantum well stack on a substrate
1002
Form gates above the quantum well stack
1004
Provide an insulating material above the gates
1006
Form conductive vias through the insulating material to make electrical contact with the gates
1008

FIG. 72

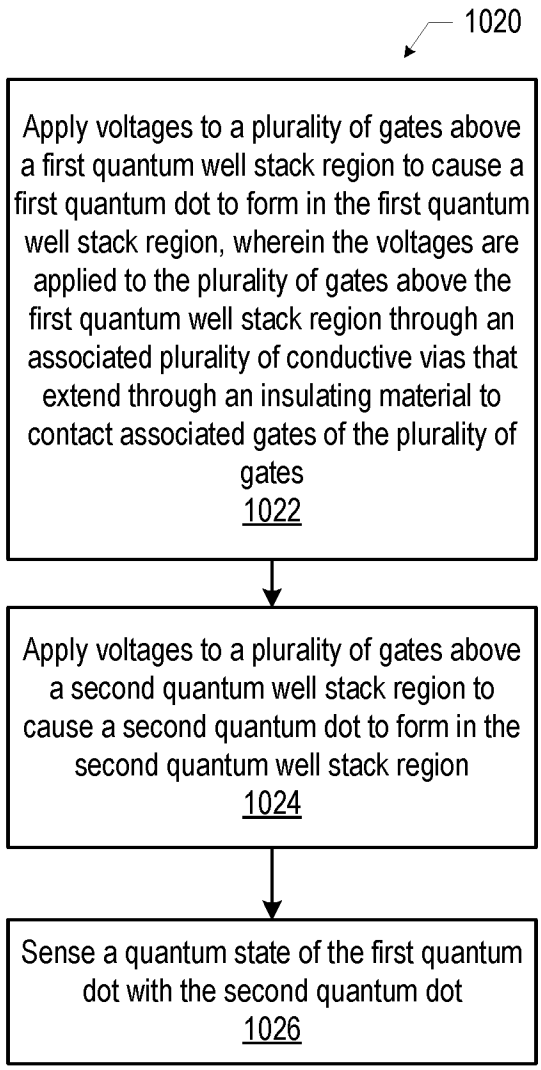
1020
Apply voltages to a plurality of gates above a first quantum well stack region to cause a first quantum dot to form in the first quantum well stack region, wherein the voltages are applied to the plurality of gates above the first quantum well stack region through an associated plurality of conductive vias that extend through an insulating material to contact associated gates of the plurality of gates
1022
Apply voltages to a plurality of gates above a second quantum well stack region to cause a second quantum dot to form in the second quantum well stack region
1024
Sense a quantum state of the first quantum dot with the second quantum dot
1026

FIG. 73

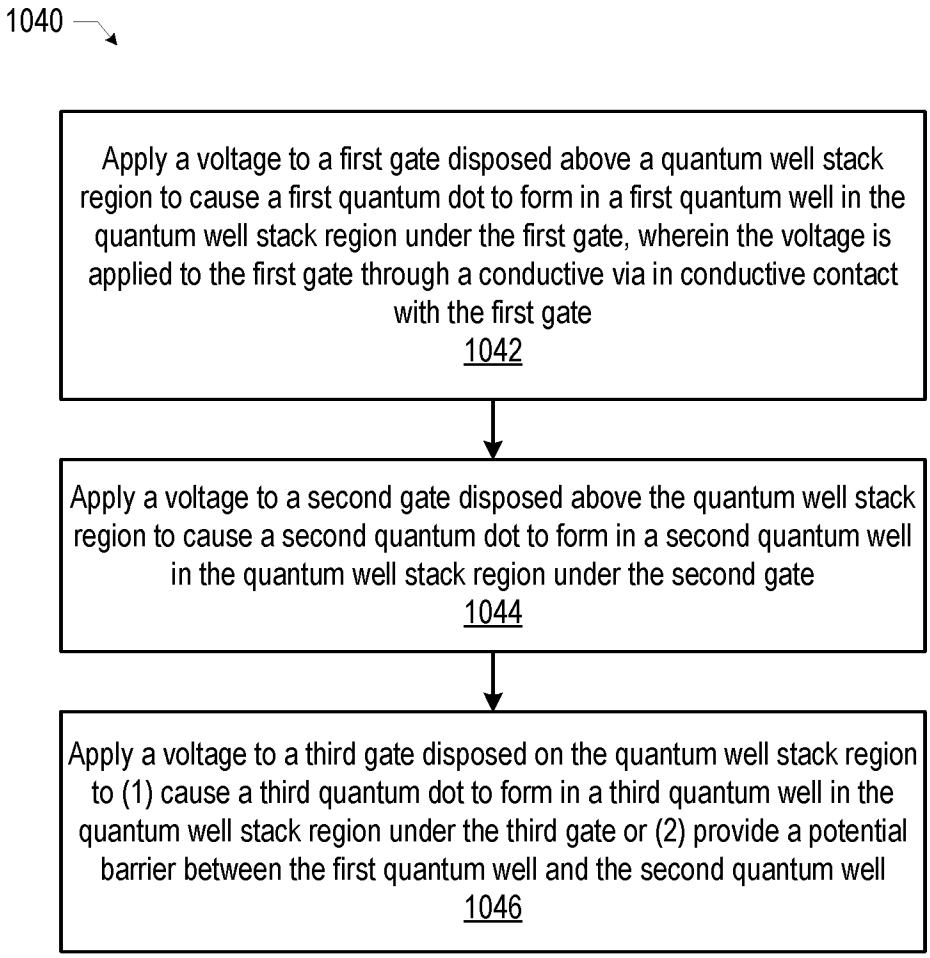
1040
Apply a voltage to a first gate disposed above a quantum well stack region to cause a first quantum dot to form in a first quantum well in the quantum well stack region under the first gate, wherein the voltage is applied to the first gate through a conductive via in conductive contact with the first gate
1042
Apply a voltage to a second gate disposed above the quantum well stack region to cause a second quantum dot to form in a second quantum well in the quantum well stack region under the second gate
1044
Apply a voltage to a third gate disposed on the quantum well stack region to (1) cause a third quantum dot to form in a third quantum well in the quantum well stack region under the third gate or (2) provide a potential barrier between the first quantum well and the second quantum well
1046

FIG. 74

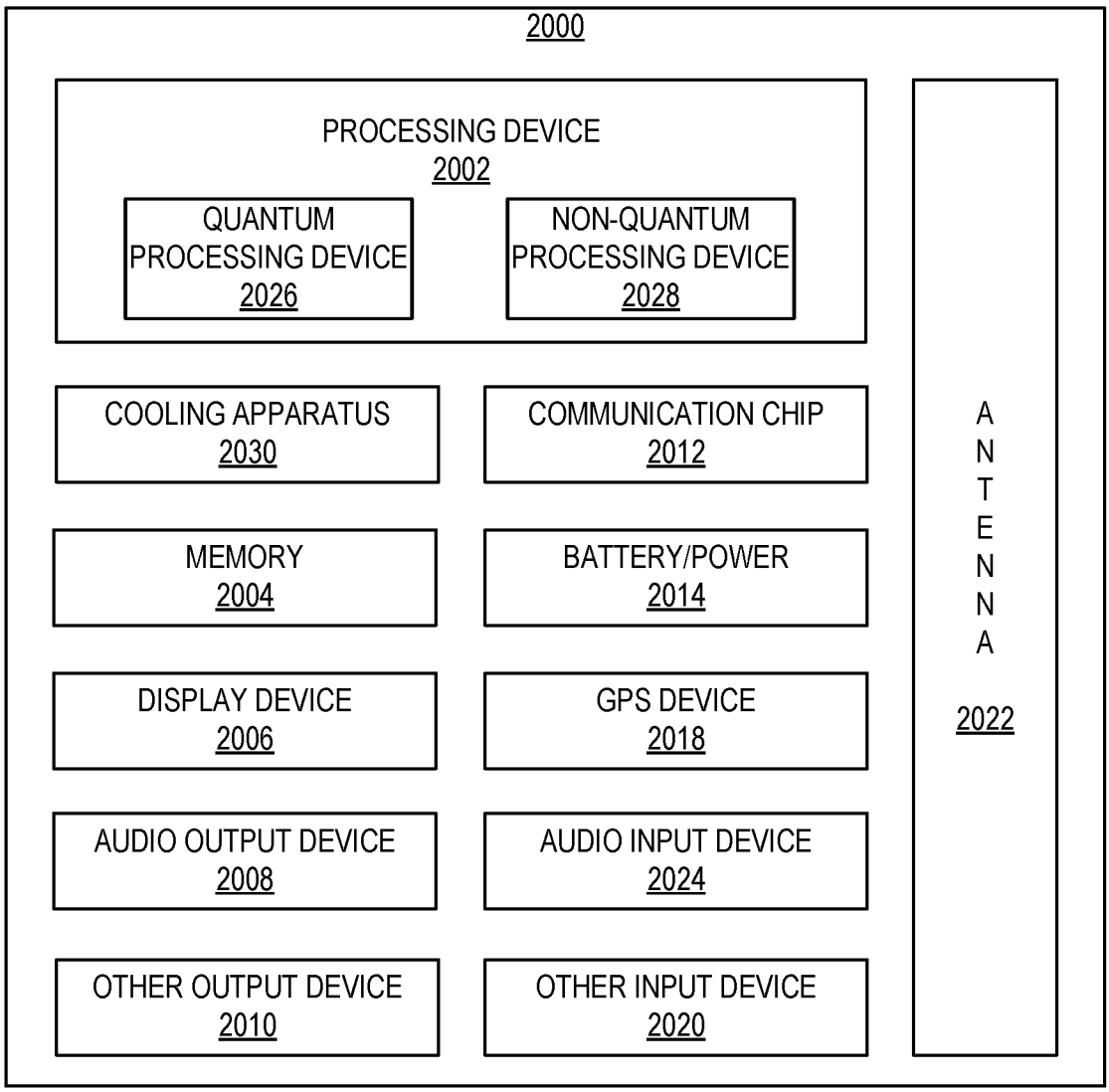
2000
PROCESSING DEVICE
2002
QUANTUM PROCESSING DEVICE
2026
NON-QUANTUM PROCESSING DEVICE
2028
COOLING APPARATUS
2030
COMMUNICATION CHIP
2012
MEMORY
2004
BATTERY/POWER
2014
DISPLAY DEVICE
2006
GPS DEVICE
2018
AUDIO OUTPUT DEVICE
2008
AUDIO INPUT DEVICE
2024
OTHER OUTPUT DEVICE
2010
OTHER INPUT DEVICE
2020
ANTENNA
2022

FIG. 75

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/036325

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/778(2006.01)i, H01L 29/12(2006.01)i, H01L 29/66(2006.01)i, H01L 29/80(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 29/778; H01L 21/71; H01L 21/336; H01L 29/78; H01L 29/772; H01L 29/12; H01L 29/94; H01L 21/338; H01L 31/119; H01L 29/06; H01L 29/68; H01L 29/66; H01L 29/80

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: quantum, well, stack, gate, spacer, buffer, barrier

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012-0280210 A1 (RAVI PILLARISETTY) 08 November 2012 See paragraphs [0011]-[0023] and figures 1-9.	1-5,18-22
Y		6-9
A		10-17,23-25
Y	US 2011-0147712 A1 (MARKO RADOSAVLJEVIC et al.) 23 June 2011 See paragraph [0049] and figure 3.	6
Y	US 2004-0175881 A1 (LEONARD FORBES et al.) 09 September 2004 See paragraphs [0037]-[0039] and figures 1A-1B.	7-8
Y	US 2011-0147711 A1 (RAVI PILLARISETTY et al.) 23 June 2011 See paragraphs [0019]-[0030] and figures 1-4.	9
A	US 2012-0112256 A1 (SHYUE SENG TAN et al.) 10 May 2012 See paragraphs [0033]-[0051] and figures 10-22.	1-25

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
06 March 2017 (06.03.2017)	**06 March 2017 (06.03.2017)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2016/036325

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